LMH6619Q 130 MHz, 1.25 mA RRIO Operational Amplifier

Check for Samples: LMH6619Q

FEATURES

- **V_S = 5V, R_L = 1 kΩ, T_A = 25°C and A_V = +1, unless otherwise specified.**
- **Operating voltage range 2.7V to 11V**
- **Supply current per channel 1.25 mA**
- **Small signal bandwidth 130 MHz**
- **Input offset voltage (limit at 25°C) ±0.75 mV**
- **Slew rate 55 V/µs**
- **Settling time to 0.1% 90 ns**
- **Settling time to 0.01% 120 ns**
- **SFDR (f = 100 kHz, A_V = +1, V_{OUT} = 2 V_{PP}) 100 dBc**
- **0.1 dB bandwidth (A_V = +2) 15 MHz**
- **Low voltage noise 10 nV/√Hz**
- **Rail-to-Rail input and output**
- **AEC-Q100 grade 2 qualified −40°C to +105°C**
- **Manufactured on an automotive grade flow**

APPLICATIONS

- **ADC driver**
- **DAC buffer**
- **Active filters**
- **High speed sensor amplifier**
- **Current sense amplifier**
- **Portable video**
- **STB, TV video amplifier**
- **Automotive**

PRODUCT PREVIEW

DESCRIPTION

The LMH6619Q (dual) is a 130 MHz rail-to-rail input and output amplifier designed for ease of use in a wide range of applications requiring high speed, low supply current, low noise, and the ability to drive complex ADC and video loads. The operating voltage range extends from 2.7V to 11V and the supply current is typically 1.25 mA per channel at 5V. The LMH6619Q is a member of the PowerWise® family and have an exceptional power-to-performance ratio.

The amplifier's voltage feedback design topology provides balanced inputs and high open loop gain for ease of use and accuracy in applications such as active filter design. Offset voltage is typically 0.1 mV and settling time to 0.01% is 120 ns which combined with an 100 dBc SFDR at 100 kHz makes the part suitable for use as an input buffer for popular 8-bit, 10-bit, 12-bit and 14-bit mega-sample ADCs.

The input common mode range extends 200 mV beyond the supply rails. On a single 5V supply with a ground terminated 150Ω load the output swings to within 37 mV of the ground rail, while a mid-rail terminated 1 kΩ load will swing to 77 mV of either rail, providing true single supply operation and maximum signal dynamic range on low power rails. The amplifier output will source and sink 35 mA and drive up to 30 pF loads without the need for external compensation.

The LMH6619Q is offered in the 8-Pin SOIC package.

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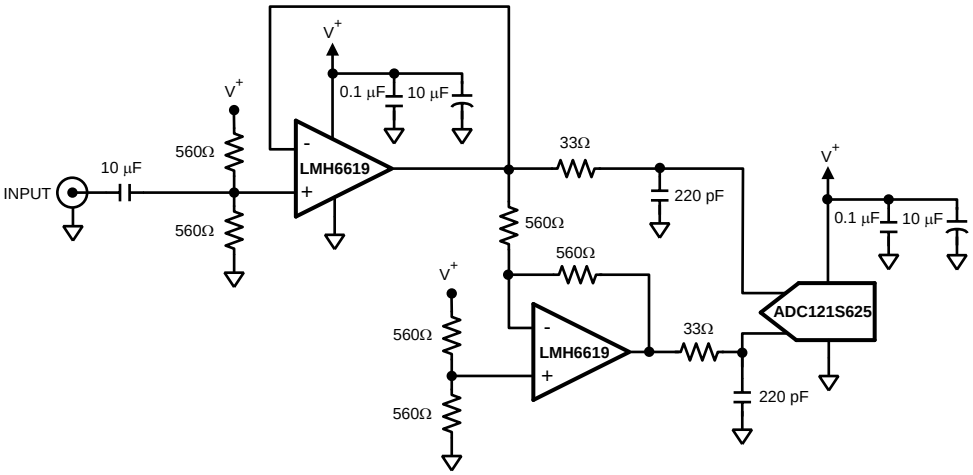
Typical Application

Figure 1. Single to Differential ADC Driver



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

ESD Tolerance (2)	
Human Body Model	
For input pins only	2000V
For all other pins	2000V
Machine Model	200V
Supply Voltage ($V_S = V^+ – V^–$)	12V
Junction Temperature (3)	150°C max
Storage Temperature Range	–65°C to 150°C
Soldering Information:	
See product folder at www.ti.com and www.ti.com/ lit/an/snoa549c /snoa549c.pdf.	

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Operating Ratings (1)

Supply Voltage ($V_S = V^+ – V^–$)	2.7V to 11V
Ambient Temperature Range (2)	−40°C to +105°C
Package Thermal Resistance (θ_{JA})	
8-Pin SOIC	160°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

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+3V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_J = +25°C, V^+ = 3V, V^- = 0V, V_{CM} = V_O = $V^+/2$, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for $A_V \neq +1$, R_L = 1 kΩ || 5 pF. **Boldface** Limits apply at temperature extremes. (1)

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
Frequency Domain Response						
SSBW	–3 dB Bandwidth Small Signal	A_V = 1, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}		120		MHz
		A_V = 2, −1, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}		56		
GBW	Gain Bandwidth	A_V = 10, R_F = 2 kΩ, R_G = 221Ω, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}	55	63		MHz
LSBW	−3 dB Bandwidth Large Signal	A_V = 1, R_L = 1 kΩ, V_{OUT} = 2 V_{PP}		13		MHz
		A_V = 2, R_L = 150Ω, V_{OUT} = 2 V_{PP}		13		
Peak	Peaking	A_V = 1, C_L = 5 pF		1.5		dB
0.1 dBBW	0.1 dB Bandwidth	A_V = 2, V_{OUT} = 0.5 V_{PP} , R_F = R_G = 825Ω		15		MHz
DG	Differential Gain	A_V = +2, 4.43 MHz, 0.6V < V_{OUT} < 2V, R_L = 150Ω to $V^+/2$		0.1		%
DP	Differential Phase	A_V = +2, 4.43 MHz, 0.6V < V_{OUT} < 2V, R_L = 150Ω to $V^+/2$		0.1		deg
Time Domain Response						
t_r/t_f	Rise & Fall Time	2V Step, A_V = 1		36		ns
SR	Slew Rate	2V Step, A_V = 1	36	46		V/µs
$t_{s_0.1}$	0.1% Settling Time	2V Step, A_V = −1		90		ns
$t_{s_0.01}$	0.01% Settling Time	2V Step, A_V = −1		120		
Noise and Distortion Performance						
SFDR	Spurious Free Dynamic Range	f_C = 100 kHz, V_{OUT}= 2 V_{PP}, R_L = 1 kΩ		100		dBc
		f_C = 1 MHz, V_{OUT} = 2 V_{PP}, R_L = 1 kΩ		61		
		f_C = 5 MHz, V_{OUT} = 2 V_{PP}, R_L = 1 kΩ		47		
e_n	Input Voltage Noise Density	f = 100 kHz		10		$nV/\sqrt{Hz}$
i_n	Input Current Noise Density	f = 100 kHz		1		$pA/\sqrt{Hz}$
CT	Crosstalk	f = 5 MHz, V_{IN} = 2 V_{PP}		80		dB
Input, DC Performance						
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V (pnp active) V_{CM} = 2.5V (npn active)		0.1	±0.75 **±1.3**	mV
TCV_{OS}	Input Offset Voltage Temperature Drift	(4)		0.8		µV/°C
I_B	Input Bias Current	V_{CM} = 0.5V (pnp active)		−1.4	**−2.6**	µA
		V_{CM} = 2.5V (npn active)		+1.0	**+1.8**	
I_{OS}	Input Offset Current			0.01	**±0.27**	µA
C_{IN}	Input Capacitance			1.5		pF
R_{IN}	Input Resistance			8		MΩ
CMVR	Common Mode Voltage Range	DC, CMRR ≥ 65 dB	−0.2		3.2	V
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from −0.1V to 1.4V	78	96		dB
		V_{CM} Stepped from 2.0V to 3.1V	81	107		
A_{OL}	Open Loop Voltage Gain	R_L = 1 kΩ to +2.7V or +0.3V	85	98		dB
		R_L = 150Ω to +2.6V or +0.4V	76	82		
Output DC Characteristics						

(1) Boldface limits apply to temperature range of −40°C to 105°C
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(4) Voltage average drift is determined by dividing the change in V_{OS} by temperature change.

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+3V Electrical Characteristics (continued)

Unless otherwise specified, all limits are guaranteed for T_J = +25°C, V^+ = 3V, V^- = 0V, V_{CM} = V_O = $V^+/2$, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for $A_V \neq +1$, R_L = 1 kΩ || 5 pF. **Boldface** Limits apply at temperature extremes. (1)

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
V_{OUT}	Output Voltage Swing High (Voltage from V^+ Supply Rail)	R_L = 1 kΩ to $V^+/2$		50	56 **62**	mV from either rail
		R_L =150Ω to $V^+/2$		160	172 **198**	
	Output Voltage Swing Low (Voltage from V^- Supply Rail)	R_L = 1 kΩ to $V^+/2$		62	68 **76**	
		R_L =150Ω to $V^+/2$		175	189 **222**	
		R_L = 150Ω to V^-		34	44 **48**	
I_{OUT}	Linear Output Current	V_{OUT} = $V^+/2$ (5)	±25	±35		mA
R_{OUT}	Output Resistance	f = 1 MHz		0.17		Ω
Power Supply Performance						
PSRR	Power Supply Rejection Ratio	DC, V_{CM} = 0.5V, V_S = 2.7V to 11V	84	104		dB
I_S	Supply Current (per channel)	R_L = ∞		1.2	1.5 **1.75**	

(5) Do not short circuit the output. Continuous source or sink currents larger than the I_{OUT} typical are not recommended as it may damage the part.

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+5V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_J = +25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+/2, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for A_V ≠ +1, R_L = 1 kΩ || 5 pF. **Boldface** Limits apply at temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
Frequency Domain Response						
SSBW	–3 dB Bandwidth Small Signal	A_V = 1, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}		130		MHz
		A_V = 2, −1, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}		53		
GBW	Gain Bandwidth	A_V = 10, R_F = 2 kΩ, R_G = 221Ω, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}	54	57		MHz
LSBW	−3 dB Bandwidth Large Signal	A_V = 1, R_L = 1 kΩ, V_{OUT} = 2 V_{PP}		15		MHz
		A_V = 2, R_L = 150Ω, V_{OUT} = 2 V_{PP}		15		
Peak	Peaking	A_V = 1, C_L = 5 pF		0.5		dB
0.1 dBBW	0.1 dB Bandwidth	A_V = 2, V_{OUT} = 0.5 V_{PP}, R_F = R_G = 1 kΩ		15		MHz
DG	Differential Gain	A_V = +2, 4.43 MHz, 0.6V < V_{OUT} < 2V, R_L = 150Ω to V^+/2		0.1		%
DP	Differential Phase	A_V = +2, 4.43 MHz, 0.6V < V_{OUT} < 2V, R_L = 150Ω to V^+/2		0.1		deg
Time Domain Response						
t_r/t_f	Rise & Fall Time	2V Step, A_V = 1		30		ns
SR	Slew Rate	2V Step, A_V = 1	44	55		V/µs
$t_{s_0.1}$	0.1% Settling Time	2V Step, A_V = −1		90		ns
$t_{s_0.01}$	0.01% Settling Time	2V Step, A_V = −1		120		
Distortion and Noise Performance						
SFDR	Spurious Free Dynamic Range	f_C = 100 kHz, V_{OUT} = 2 V_{PP}, R_L = 1 kΩ		100		dBc
		f_C = 1 MHz, V_{OUT} = 2 V_{PP}, R_L = 1 kΩ		88		
		f_C = 5 MHz, V_O = 2 V_{PP}, R_L = 1 kΩ		61		
e_n	Input Voltage Noise Density	f = 100 kHz		10		nV/√Hz
i_n	Input Current Noise Density	f = 100 kHz		1		pA/√Hz
CT	Crosstalk	f = 5 MHz, V_{IN} = 2 V_{PP}		80		dB
Input, DC Performance						
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V (pnp active) V_{CM} = 4.5V (npn active)		0.1	±0.75 **±1.3**	mV
TCV_{OS}	Input Offset Voltage Temperature Drift	(3)		0.8		µV/°C
I_B	Input Bias Current	V_{CM} = 0.5V (pnp active)		−1.5	**−2.4**	µA
		V_{CM} = 4.5V (npn active)		+1.0	**+1.9**	
I_{OS}	Input Offset Current			0.01	**±0.26**	µA
C_{IN}	Input Capacitance			1.5		pF
R_{IN}	Input Resistance			8		MΩ
CMVR	Common Mode Voltage Range	DC, CMRR ≥ 65 dB	−0.2		5.2	V
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from −0.1V to 3.4V	81	98		dB
		V_{CM} Stepped from 4.0V to 5.1V	84	108		
A_{OL}	Open Loop Voltage Gain	R_L = 1 kΩ to +4.6V or +0.4V	84	100		dB
		R_L = 150Ω to +4.5V or +0.5V	78	83		
Output DC Characteristics						

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(3) Voltage average drift is determined by dividing the change in V_{OS} by temperature change.

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+5V Electrical Characteristics (continued)

Unless otherwise specified, all limits are guaranteed for T_J = +25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for $A_V \neq +1$, R_L = 1 kΩ || 5 pF. **Boldface** Limits apply at temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
V_{OUT}	Output Voltage Swing High Voltage from V^+ Supply Rail)	R_L = 1 kΩ to $V^+/2$		60	73 **82**	mV from either rail
		R_L = 150Ω to $V^+/2$		230	255 **295**	
	Output Voltage Swing Low Voltage from V^- Supply Rail)	R_L = 1 kΩ to $V^+/2$		77	85 **98**	
		R_L = 150Ω to $V^+/2$		255	275 **326**	
		R_L = 150Ω to V^-		37	48 **50**	
I_{OUT}	Linear Output Current	V_{OUT} = $V^+/2$ (4)	±25	±35		mA
R_{OUT}	Output Resistance	f = 1 MHz		0.17		Ω
Power Supply Performance						
PSRR	Power Supply Rejection Ratio	DC, V_{CM} = 0.5V, V_S = 2.7V to 11V	84	104		dB
I_S	Supply Current (per channel)	R_L = ∞		1.3	1.5 **1.75**	

(4) Do not short circuit the output. Continuous source or sink currents larger than the I_{OUT} typical are not recommended as it may damage the part.

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±5V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_J = +25°C, V^+ = 5V, V^- = −5V, V_{CM} = V_O = 0V, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for A_V ≠ +1, R_L = 1 kΩ || 5 pF. **Boldface** Limits apply at temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
Frequency Domain Response						
SSBW	–3 dB Bandwidth Small Signal	A_V = 1, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}		140		MHz
		A_V = 2, −1, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}		53		
GBW	Gain Bandwidth	A_V = 10, R_F = 2 kΩ, R_G = 221Ω, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}	54	58		MHz
LSBW	−3 dB Bandwidth Large Signal	A_V = 1, R_L = 1 kΩ, V_{OUT} = 2 V_{PP}		16		MHz
		A_V = 2, R_L = 150Ω, V_{OUT} = 2 V_{PP}		15		
Peak	Peaking	A_V = 1, C_L = 5 pF		0.05		dB
0.1 dBBW	0.1 dB Bandwidth	A_V = 2, V_{OUT} = 0.5 V_{PP}, R_F = R_G = 1.21 kΩ		15		MHz
DG	Differential Gain	A_V = +2, 4.43 MHz, 0.6V < V_{OUT} < 2V, R_L = 150Ω to V^+/2		0.1		%
DP	Differential Phase	A_V = +2, 4.43 MHz, 0.6V < V_{OUT} < 2V, R_L = 150Ω to V^+/2		0.1		deg
Time Domain Response						
t_r/t_f	Rise & Fall Time	2V Step, A_V = 1		30		ns
SR	Slew Rate	2V Step, A_V = 1	45	57		V/µs
$t_{s_0.1}$	0.1% Settling Time	2V Step, A_V = −1		90		ns
$t_{s_0.01}$	0.01% Settling Time	2V Step, A_V = −1		120		
Noise and Distortion Performance						
SFDR	Spurious Free Dynamic Range	f_C = 100 kHz, V_{OUT} = 2 V_{PP}, R_L = 1 kΩ		100		dBc
		f_C = 1 MHz, V_{OUT} = 2 V_{PP}, R_L = 1 kΩ		88		
		f_C = 5 MHz, V_{OUT} = 2 V_{PP}, R_L = 1 kΩ		70		
e_n	Input Voltage Noise Density	f = 100 kHz		10		$nV/\sqrt{Hz}$
i_n	Input Current Noise Density	f = 100 kHz		1		$pA/\sqrt{Hz}$
CT	Crosstalk	f = 5 MHz, V_{IN} = 2 V_{PP}		80		dB
Input DC Performance						
V_{OS}	Input Offset Voltage	V_{CM} = −4.5V (pnp active) V_{CM} = 4.5V (npn active)		0.1	±0.75 **±1.3**	mV
TCV_{OS}	Input Offset Voltage Temperature Drift	(3)		0.9		µV/°C
I_B	Input Bias Current	V_{CM} = −4.5V (pnp active)		−1.5	**−2.4**	µA
		V_{CM} = 4.5V (npn active)		+1.0	**+1.9**	
I_{OS}	Input Offset Current			0.01	**±0.26**	µA
C_{IN}	Input Capacitance			1.5		pF
R_{IN}	Input Resistance			8		MΩ
CMVR	Common Mode Voltage Range	DC, CMRR ≥ 65 dB	−5.2		5.2	V
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from −5.1V to 3.4V	84	100		dB
		V_{CM} Stepped from 4.0V to 5.1V	83	108		
A_{OL}	Open Loop Voltage Gain	R_L = 1 kΩ to +4.6V or −4.6V	86	95		dB
		R_L = 150Ω to +4.3V or −4.3V	79	84		
Output DC Characteristics						

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(3) Voltage average drift is determined by dividing the change in V_{OS} by temperature change.

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±5V Electrical Characteristics (continued)

Unless otherwise specified, all limits are guaranteed for T_J = +25°C, V^+ = 5V, V^- = −5V, V_{CM} = V_O = 0V, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for A_V ≠ +1, R_L = 1 kΩ || 5 pF. **Boldface** Limits apply at temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
V_{OUT}	Output Voltage Swing High (Voltage from V^+ Supply Rail)	R_L = 1 kΩ to GND		100	111 **126**	mV from either rail
		R_L = 150Ω to GND		430	457 **526**	
	Output Voltage Swing Low (Voltage from V^- Supply Rail)	R_L = 1 kΩ to GND		115	126 **141**	
		R_L = 150Ω to GND		450	484 **569**	
		R_L = 150Ω to V^-		45	61 **62**	
I_{OUT}	Linear Output Current	V_{OUT} = V^+/2 (4)	±25	±35		mA
R_{OUT}	Output Resistance	f = 1 MHz		0.17		Ω
Power Supply Performance						
PSRR	Power Supply Rejection Ratio	DC, V_{CM} = −4.5V, V_S = 2.7V to 11V	84	104		dB
I_S	Supply Current (per channel)	R_L = ∞		1.45	1.65 **2.0**	

(4) Do not short circuit the output. Continuous source or sink currents larger than the I_{OUT} typical are not recommended as it may damage the part.

Connection Diagram

8-Pin SOIC

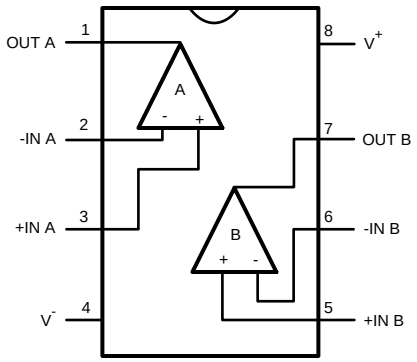

Figure 2. Top View

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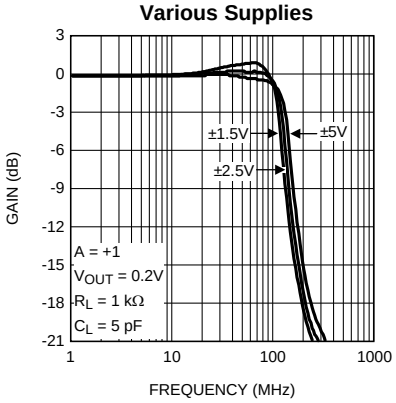
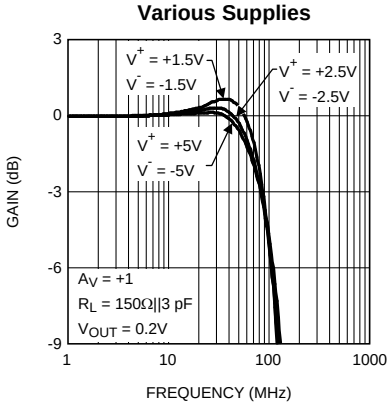
Typical Performance Characteristics

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for $A_V \neq +1$, unless otherwise specified.

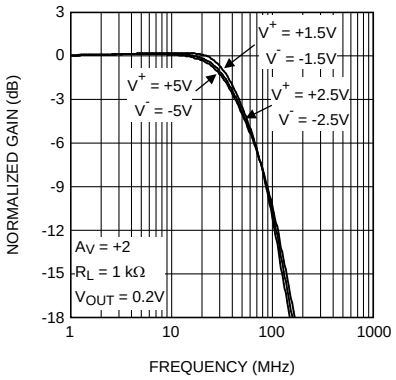
Closed Loop Frequency Response for Various Supplies



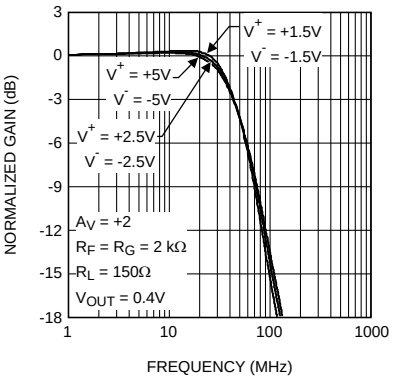
Closed Loop Frequency Response for Various Supplies



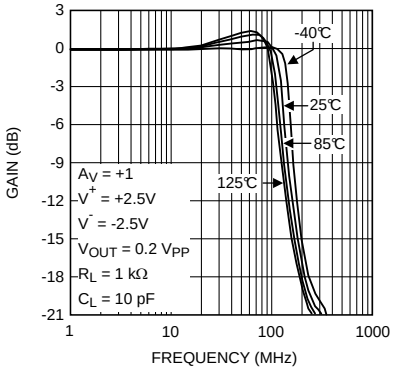
Closed Loop Frequency Response for Various Supplies



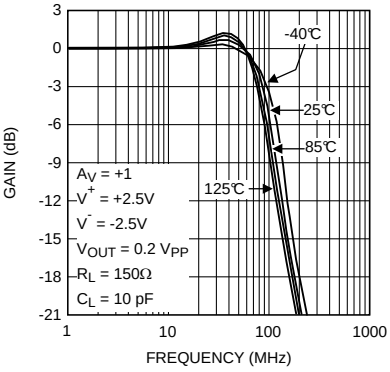
Closed Loop Frequency Response for Various Supplies



Closed Loop Frequency Response for Various Temperatures



Closed Loop Frequency Response for Various Temperatures

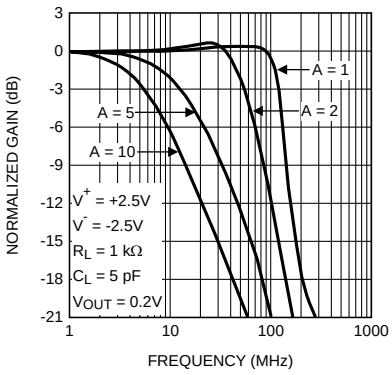


PRODUCT PREVIEW

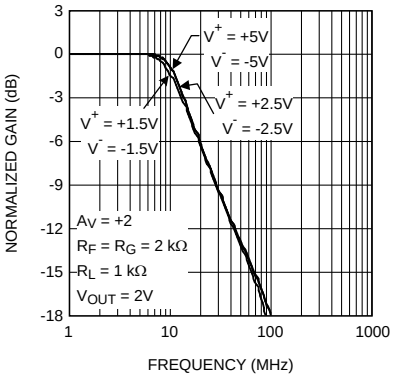
Typical Performance Characteristics (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for $A_V \neq +1$, unless otherwise specified.

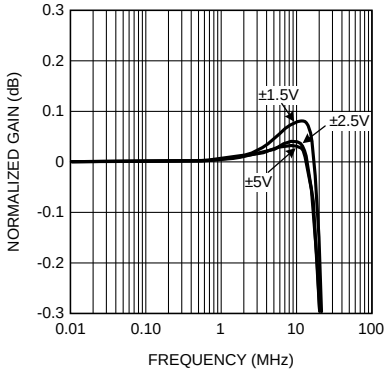
Closed Loop Gain vs. Frequency for Various Gains



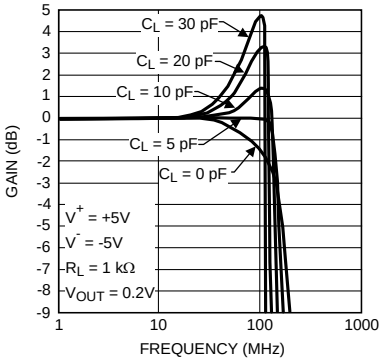
Large Signal Frequency Response



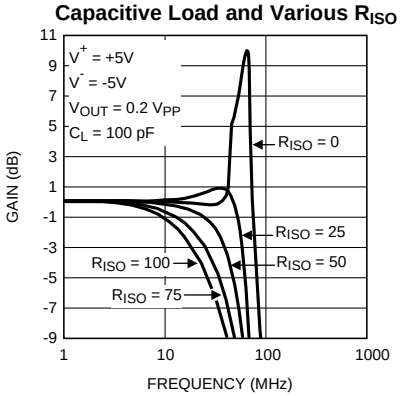
±0.1 dB Gain Flatness for Various Supplies



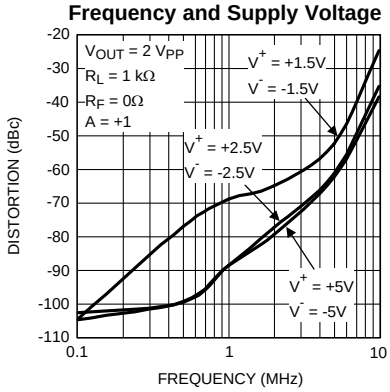
Small Signal Frequency Response with Various Capacitive Load



Small Signal Frequency Response with Capacitive Load and Various R_{ISO}



HD2 vs. Frequency and Supply Voltage



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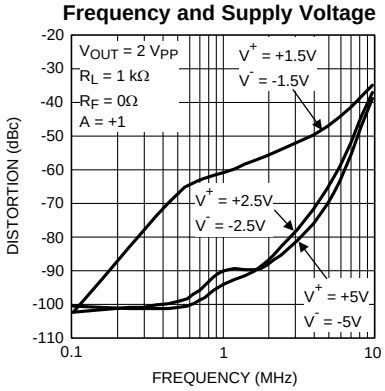
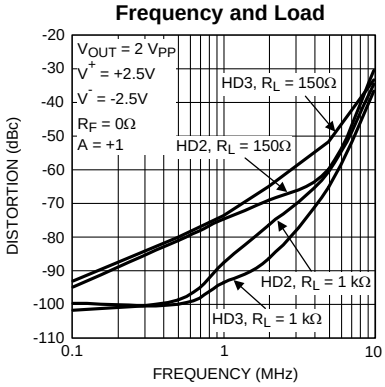
Typical Performance Characteristics (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for $A_V \neq +1$, unless otherwise specified.

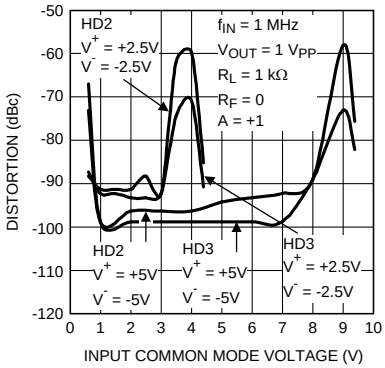
HD3 vs. Frequency and Supply Voltage



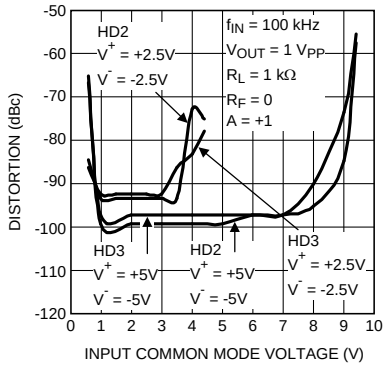
HD2 and HD3 vs. Frequency and Load



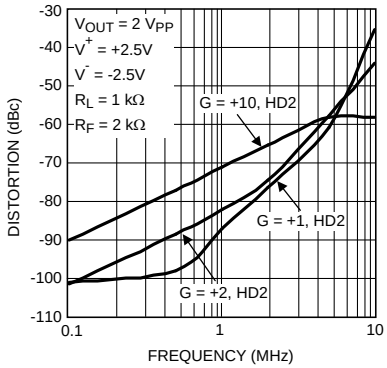
HD2 and HD3 vs. Common Mode Voltage



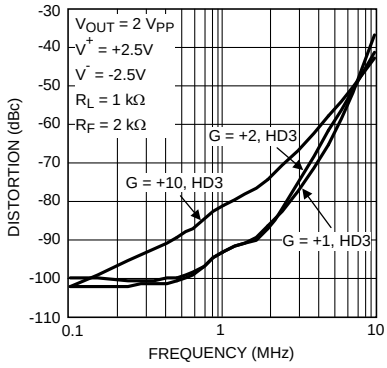
HD2 and HD3 vs. Common Mode Voltage



HD2 vs. Frequency and Gain



HD3 vs. Frequency and Gain

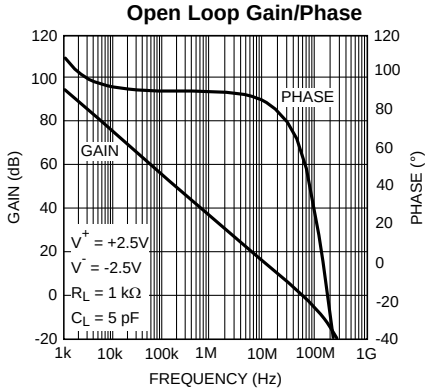


PRODUCT PREVIEW

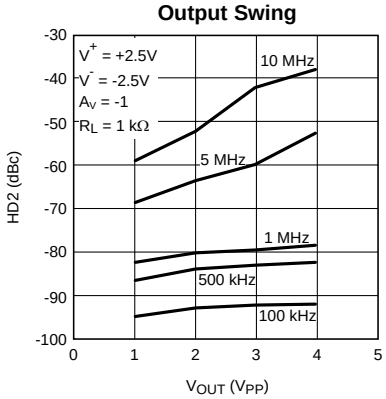
Typical Performance Characteristics (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for A_V ≠ +1, unless otherwise specified.

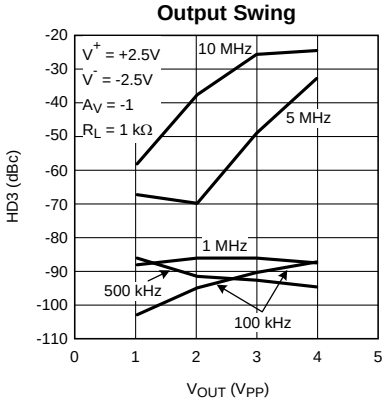
Open Loop Gain/Phase



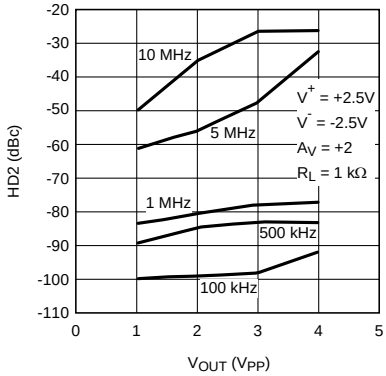
HD2 vs. Output Swing



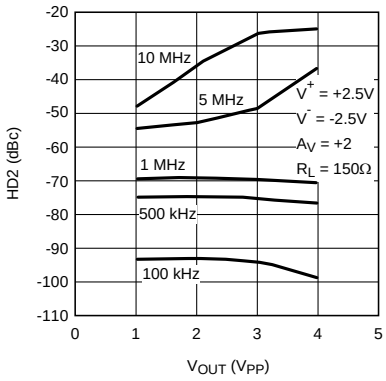
HD3 vs. Output Swing



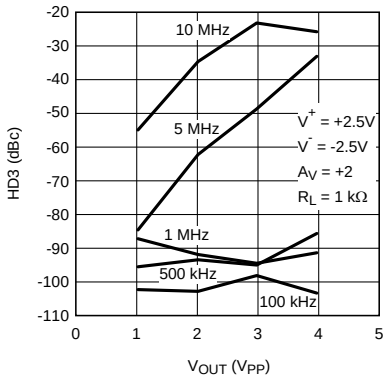
HD2 vs. Output Swing



HD2 vs. Output Swing



HD3 vs. Output Swing



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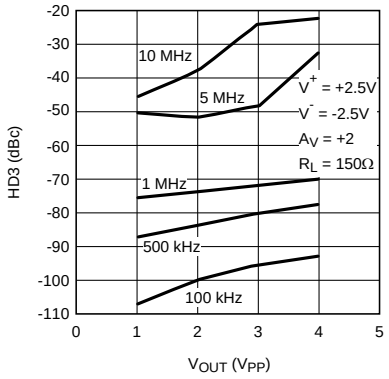
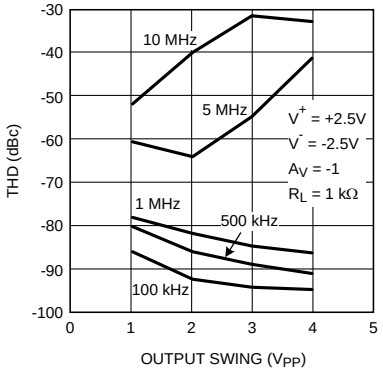
Typical Performance Characteristics (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for $A_V \neq +1$, unless otherwise specified.

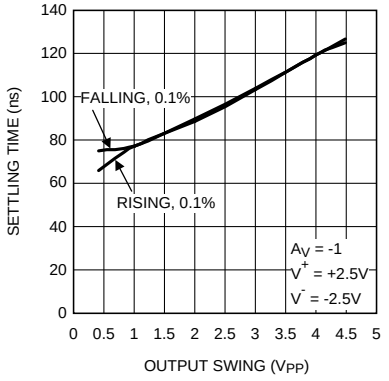
HD3 vs. Output Swing



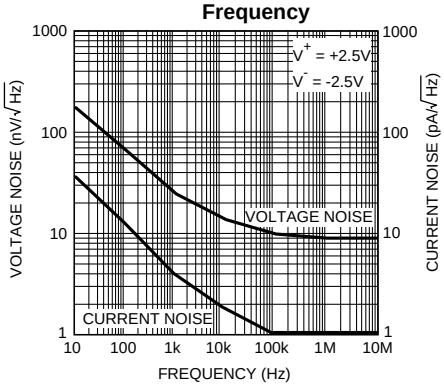
THD vs. Output Swing



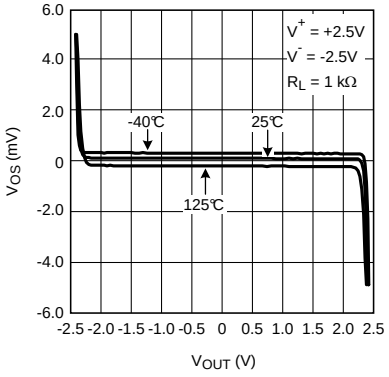
Settling Time vs. Input Step Amplitude (Output Slew and Settle Time)



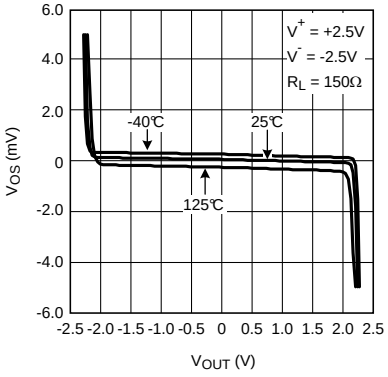
Input Noise vs. Frequency



V_{OS} vs. V_{OUT}



V_{OS} vs. V_{OUT}

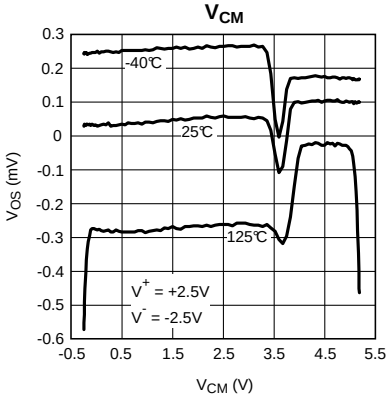


PRODUCT PREVIEW

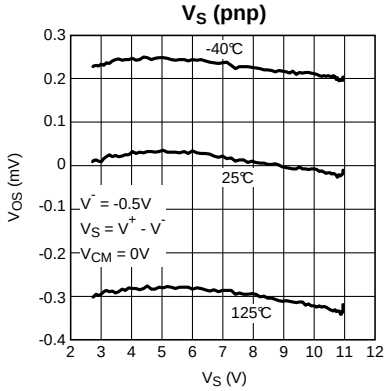
Typical Performance Characteristics (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for A_V ≠ +1, unless otherwise specified.

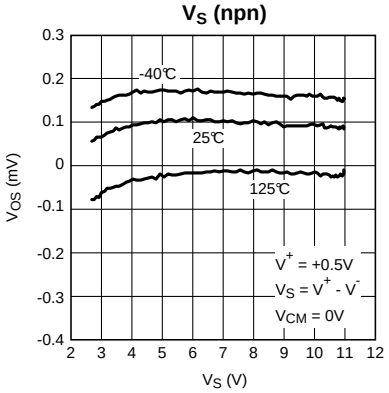
V_{OS} vs. V_{CM}



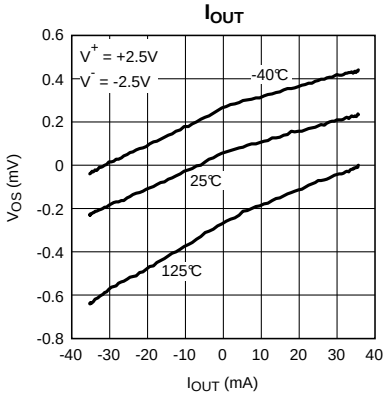
V_{OS} vs. V_S (pnp)



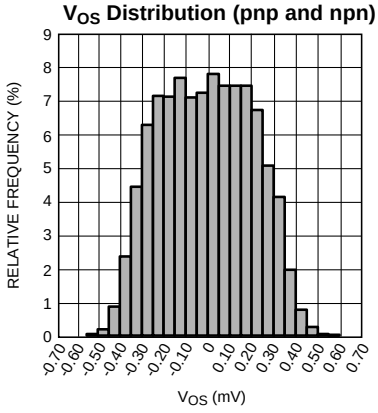
V_{OS} vs. V_S (npn)



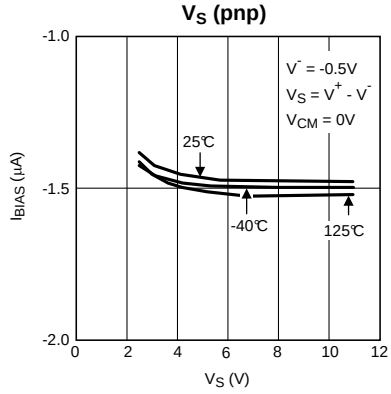
V_{OS} vs. I_{OUT}



V_{OS} Distribution (pnp and npn)



I_B vs. V_S (pnp)



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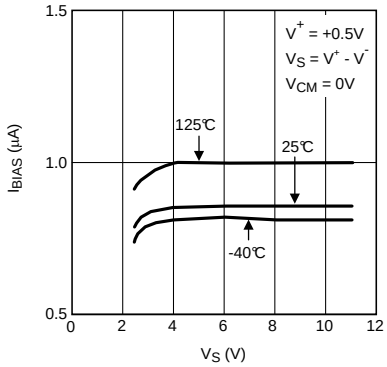
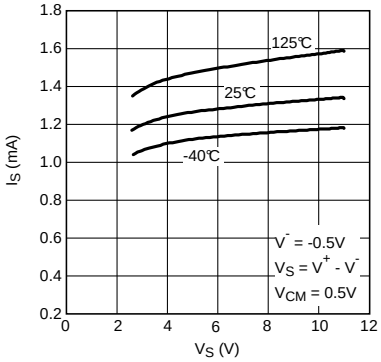
Typical Performance Characteristics (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for $A_V \neq +1$, unless otherwise specified.

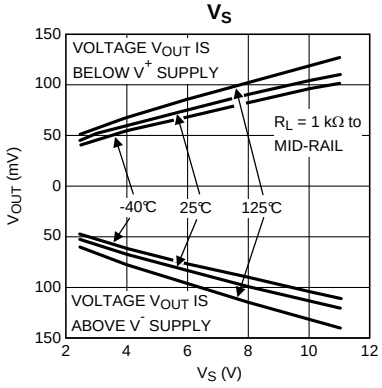
I_B vs. V_S (npn)



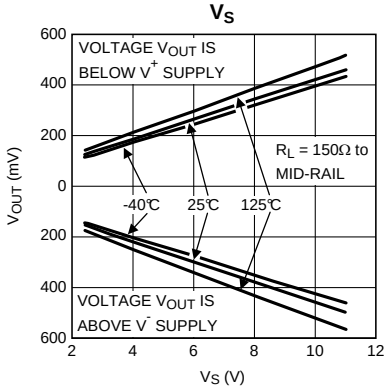
I_S vs. V_S



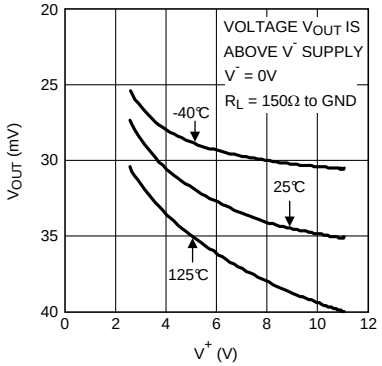
V_{OUT} vs. V_S



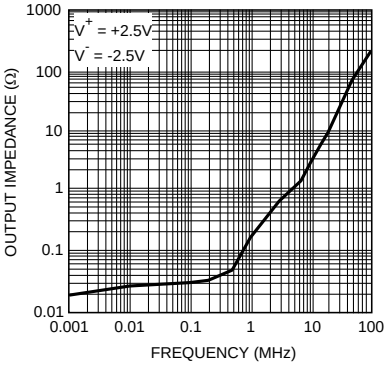
V_{OUT} vs. V_S



V_{OUT} vs. V_S



Closed Loop Output Impedance vs. Frequency A_V = +1

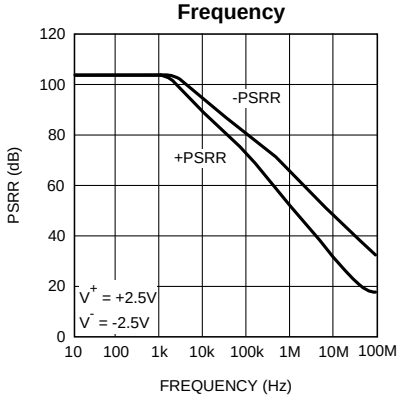


PRODUCT PREVIEW

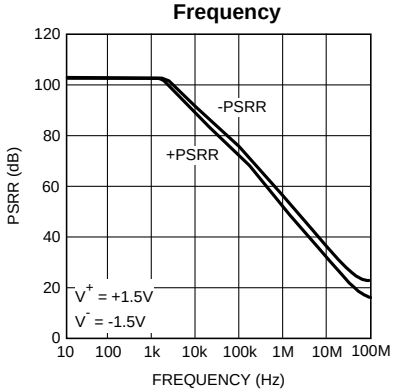
Typical Performance Characteristics (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for A_V ≠ +1, unless otherwise specified.

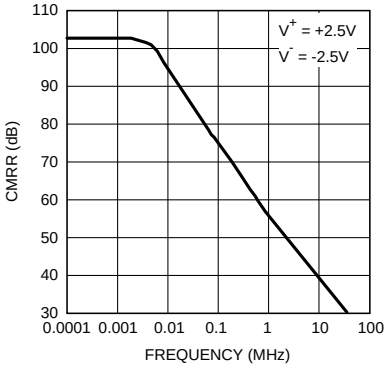
PSRR vs. Frequency



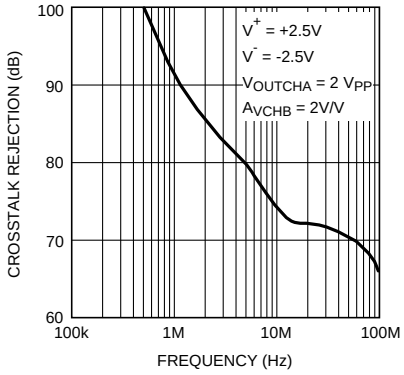
PSRR vs. Frequency



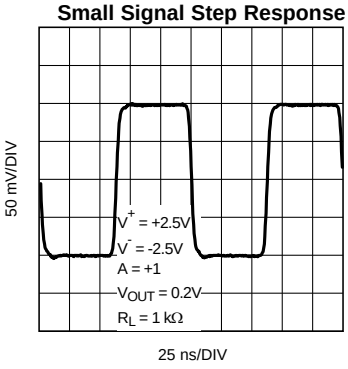
CMRR vs. Frequency



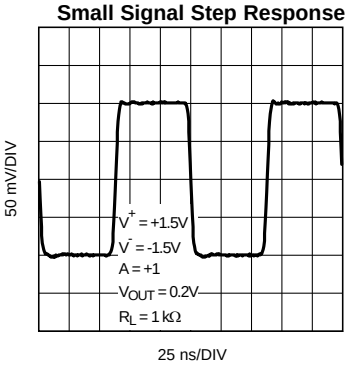
Crosstalk Rejection vs. Frequency (Output to Output)



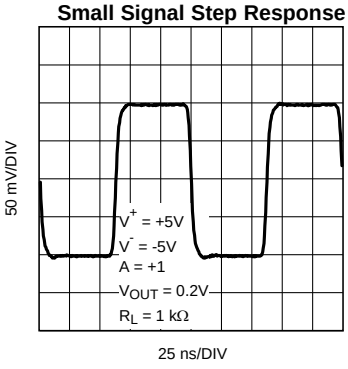
Small Signal Step Response



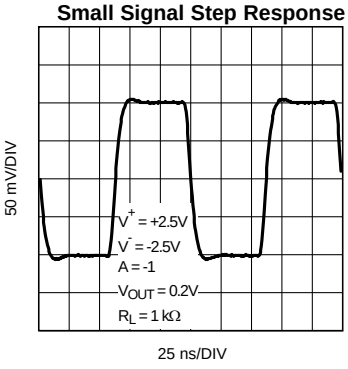
Small Signal Step Response



Small Signal Step Response



Small Signal Step Response



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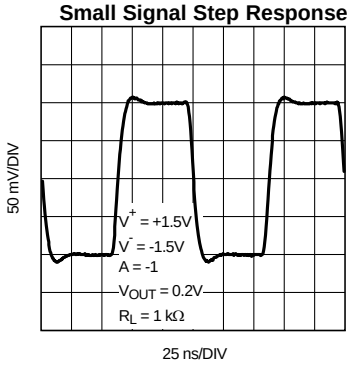
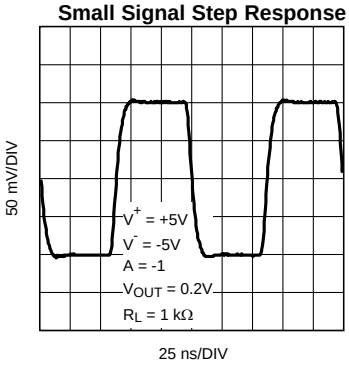
Typical Performance Characteristics (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 2 kΩ for $A_V \neq +1$, unless otherwise specified.

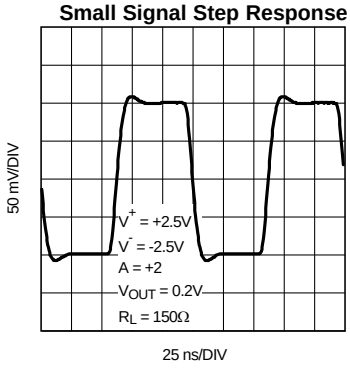
Small Signal Step Response



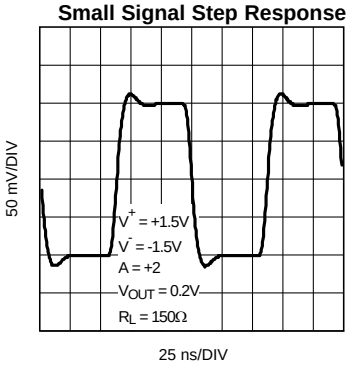
Small Signal Step Response



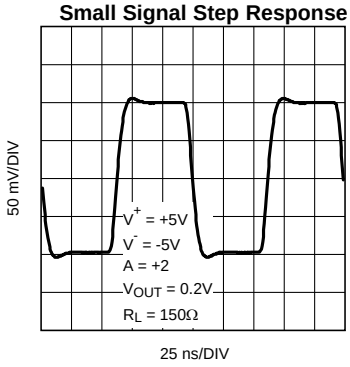
Small Signal Step Response



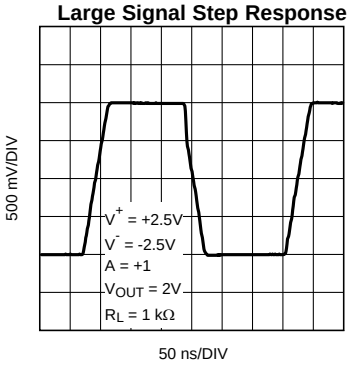
Small Signal Step Response



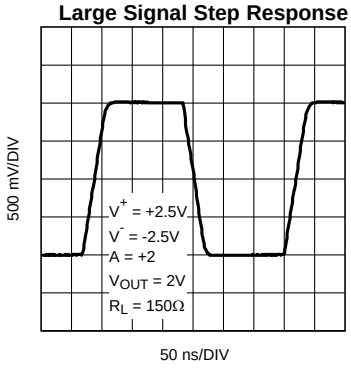
Small Signal Step Response



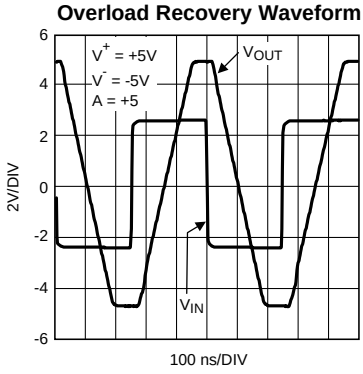
Large Signal Step Response



Large Signal Step Response



Overload Recovery Waveform



Application Information

The LMH6619Q is based on National Semiconductor's proprietary VIP10 dielectrically isolated bipolar process. This device family architecture features the following:

- Complimentary bipolar devices with exceptionally high f_t (~8 GHz) even under low supply voltage (2.7V) and

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low bias current.

- Common emitter push-push output stage. This architecture allows the output to reach within millivolts of either supply rail.
- Consistent performance from any supply voltage $_{(2.7V - 11V)}$ with little variation with supply voltage for the most important specifications (e.g. BW, SR, I_{OUT}.)
- Significant power saving compared to competitive devices on the market with similar performance.

With 3V supplies and a common mode input voltage range that extends beyond either supply rail, the LMH6619Q is well suited to many low voltage/low power applications. Even with 3V supplies, the −3 dB BW (at A_V = +1) is typically 120 MHz.

The LMH6619Q is designed to avoid output phase reversal. With input over-drive, the output is kept near the supply rail (or as close to it as mandated by the closed loop gain setting and the input voltage). Figure 3 shows the input and output voltage when the input voltage significantly exceeds the supply voltages.

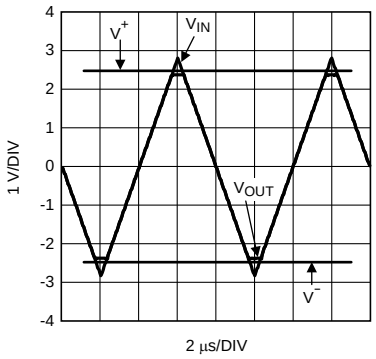

Figure 3. Input and Output Shown with CMVR Exceeded

SINGLE TO DIFFERENTIAL ADC DRIVER

Figure 4 shows the LMH6619Q used to drive a differential ADC with a single-ended input. The ADC121S625 is a fully differential 12-bit ADC. Table 1 shows the performance data of the LMH6619Q and the ADC121S625.

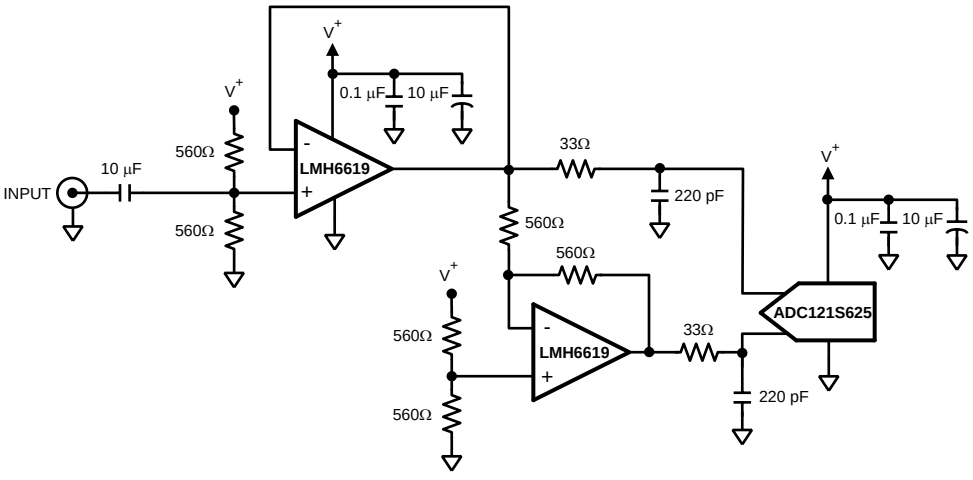

Figure 4. LMH6619Q Driving an ADC121S625

Table 1. Performance Data for the Single to Differential ADC Driver

Parameter	Measured Value
Signal Frequency	10 kHz
Signal Amplitude	2.5V

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Table 1. Performance Data for the Single to Differential ADC Driver (continued)

Parameter	Measured Value
SINAD	67.9 dB
SNR	68.29 dB
THD	−78.6 dB
SFDR	75.0 dB
ENOB	11.0 bits

DIFFERENTIAL ADC DRIVER

Its low noise and wide bandwidth make the LMH6619Q an excellent choice for driving a 12-bit ADC. Figure 5 shows the LMH6619Q driving an ADC121S705. The ADC121S705 is a fully differential 12-bit ADC.The LMH6619Q is set up in a 2nd order multiple-feedback configuration with a gain of −1. The −3 dB point is at 500 kHz and the −0.01 dB point is at 100 kHz. The 22Ω resistor and 390 pF capacitor form an antialiasing filter for the ADC121S705. The capacitor also stores and delivers charge to the switched capacitor input of the ADC. The capacitive load on the LMH6619Q created by the 390 pF capacitor is decreased by the 22Ω resistor. Table 2 shows the performance data.

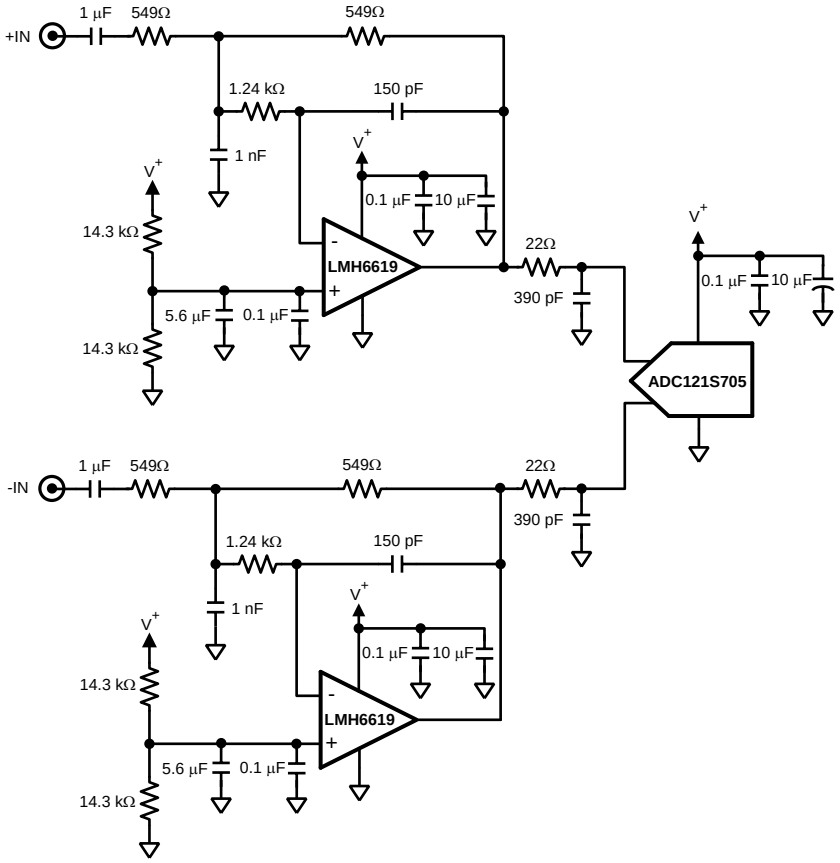

Figure 5. LMH6619Q Driving an ADC121S705

Table 2. Performance Data for the Differential ADC Driver

Parameter	Measured Value
Signal Frequency	100 kHz
SINAD	71.5 dB
SNR	71.87 dB
THD	−82.4 dB

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Table 2. Performance Data for the Differential ADC Driver (continued)

Parameter	Measured Value
SFDR	90.97 dB
ENOB	11.6 bits

DC LEVEL SHIFTING

Often a signal must be both amplified and level shifted while using a single supply for the op amp. The circuit in Figure 6 can do both of these tasks. The procedure for specifying the resistor values is as follows.

1. Determine the input voltage.
2. Calculate the input voltage midpoint, $V_{INMID} = V_{INMIN} + (V_{INMAX} – V_{INMIN})/2$.
3. Determine the output voltage needed.
4. Calculate the output voltage midpoint, $V_{OUTMID} = V_{OUTMIN} + (V_{OUTMAX} – V_{OUTMIN})/2$.
5. Calculate the gain needed, gain = $(V_{OUTMAX} – V_{OUTMIN})/(V_{INMAX} – V_{INMIN})$
6. Calculate the amount the voltage needs to be shifted from input to output, $\Delta V_{OUT} = V_{OUTMID} – \text{gain} \times V_{INMID}$.
7. Set the supply voltage to be used.
8. Calculate the noise gain, noise gain = gain + $\Delta V_{OUT}/V_S$.
9. Set R_F.
10. Calculate R_1, $R_1 = R_F/\text{gain}$.
11. Calculate R_2, $R_2 = R_F/(\text{noise gain-gain})$.
12. Calculate R_G, $R_G = R_F/(\text{noise gain} – 1)$.

Check that both the V_{IN} and V_{OUT} are within the voltage ranges of the LMH6619Q.

The following example is for a V_{IN} of 0V to 1V with a V_{OUT} of 2V to 4V.

1. V_{IN} = 0V to 1V
2. V_{INMID} = 0V + (1V – 0V)/2 = 0.5V
3. V_{OUT} = 2V to 4V
4. V_{OUTMID} = 2V + (4V – 2V)/2 = 3V
5. Gain = (4V – 2V)/(1V – 0V) = 2
6. ΔV_{OUT} = 3V – 2 x 0.5V = 2
7. For the example the supply voltage will be +5V.
8. Noise gain = 2 + 2/5V = 2.4
9. R_F = 2 kΩ
10. R_1 = 2 kΩ/2 = 1 kΩ
11. R_2 = 2 kΩ/(2.4-2) = 5 kΩ
12. R_G = 2 kΩ/(2.4 – 1) = 1.43 kΩ

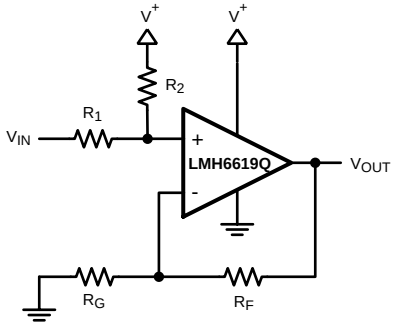

Figure 6. DC Level Shifting

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4th ORDER MULTIPLE FEEDBACK LOW-PASS FILTER

Figure 7 shows the LMH6619Q used as the amplifier in a multiple feedback low pass filter. This filter is set up to have a gain of +1 and a −3 dB point of 1 MHz. Values can be determined by using the WEBENCH® Active Filter Designer found at amplifiers.national.com.

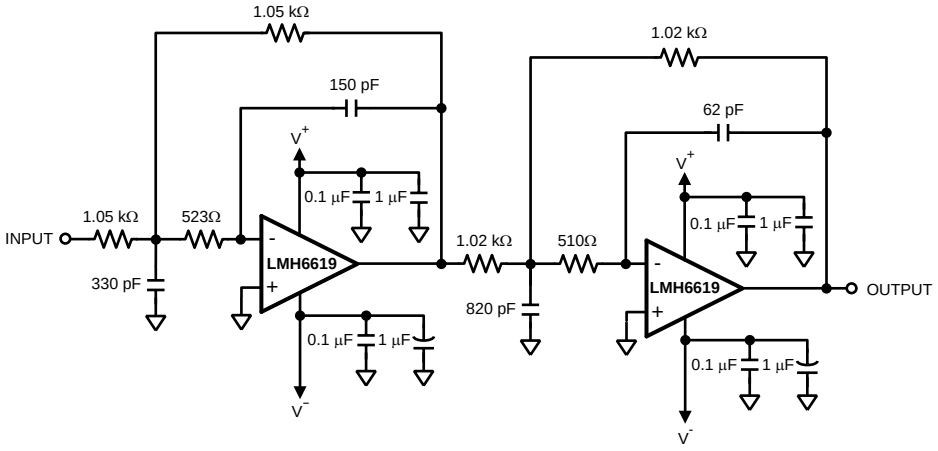

Figure 7. 4th Order Multiple Feedback Low-Pass Filter

CURRENT SENSE AMPLIFIER

With it's rail-to-rail input and output capability, low V_{OS}, and low I_B the LMH6619Q is an ideal choice for a current sense amplifier application. Figure 8 shows the schematic of the LMH6619Q set up in a low-side sense configuration which provides a conversion gain of 2V/A. Voltage error due to V_{OS} can be calculated to be V_{OS} x (1 + R_F/R_G) or 0.6 mV x 21 = 12.6 mV. Voltage error due to I_O is I_O x R_F or 0.26 µA x 1 kΩ = 0.26 mV. Hence total voltage error is 12.6 mV + 0.26 mV or 12.86 mV which translates into a current error of 12.86 mV/(2 V/A) = 6.43 mA.

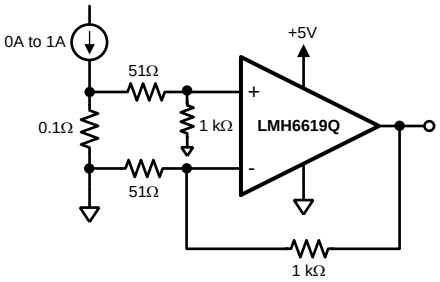

Figure 8. Current Sense Amplifier

TRANSIMPEDANCE AMPLIFIER

By definition, a photodiode produces either a current or voltage output from exposure to a light source. A Transimpedance Amplifier (TIA) is utilized to convert this low-level current to a usable voltage signal. The TIA often will need to be compensated to insure proper operation.

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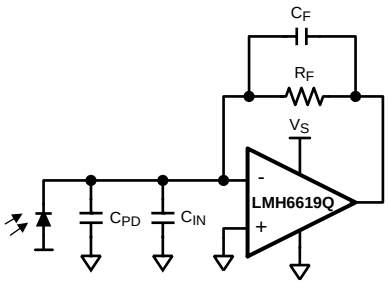

Figure 9. Photodiode Modeled with Capacitance Elements

Figure 9 shows the LMH6619Q modeled with photodiode and the internal op amp capacitances. The LMH6619Q allows circuit operation of a low intensity light due to its low input bias current by using larger values of gain (R_F). The total capacitance (C_T) on the inverting terminal of the op amp includes the photodiode capacitance (C_{PD}) and the input capacitance of the op amp (C_{IN}). This total capacitance (C_T) plays an important role in the stability of the circuit. The noise gain of this circuit determines the stability and is defined by:

$$NG = \frac{1 + sR_F (C_T + C_F)}{1 + sC_F R_F} \quad (1)$$

$$\text{Where, } f_Z \cong \frac{1}{2\pi R_F C_T} \text{ and } f_P = \frac{1}{2\pi R_F C_F} \quad (2)$$

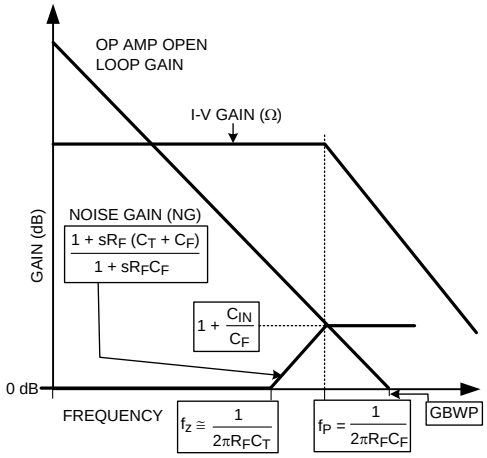

Figure 10. Bode Plot of Noise Gain Intersecting with Op Amp Open-Loop Gain

Figure 10 shows the bode plot of the noise gain intersecting the op amp open loop gain. With larger values of gain, C_T and R_F create a zero in the transfer function. At higher frequencies the circuit can become unstable due to excess phase shift around the loop.

A pole at f_P in the noise gain function is created by placing a feedback capacitor (C_F) across R_F. The noise gain slope is flattened by choosing an appropriate value of C_F for optimum performance.

Theoretical expressions for calculating the optimum value of C_F and the expected −3 dB bandwidth are:

$$C_F = \sqrt{\frac{C_T}{2\pi R_F (GBWP)}} \quad (3)$$

$$f_{-3\,dB} = \sqrt{\frac{GBWP}{2\pi R_F C_T}} \quad (4)$$

Equation 4 indicates that the −3 dB bandwidth of the TIA is inversely proportional to the feedback resistor. Therefore, if the bandwidth is important then the best approach would be to have a moderate transimpedance gain stage followed by a broadband voltage gain stage.

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Table 3 shows the measurement results of the LMH6619Q with different photodiodes having various capacitances (C_{PD}) and a feedback resistance (R_F) of 1 kΩ.

Table 3. TIA (Figure 1) Compensation and Performance Results

C_{PD} (pF)	C_T (pF)	$C_{F\ CAL}$ (pF)	$C_{F\ USED}$ (pF)	$f_{-3\ dB\ CAL}$ (MHz)	$f_{-3\ dB\ MEAS}$ (MHz)	Peaking (dB)
22	24	7.7	5.6	23.7	20	0.9
47	49	10.9	10	16.6	15.2	0.8
100	102	15.8	15	11.5	10.8	0.9
222	224	23.4	18	7.81	8	2.9

Figure 11 shows the frequency response for the various photodiodes in Table 3.

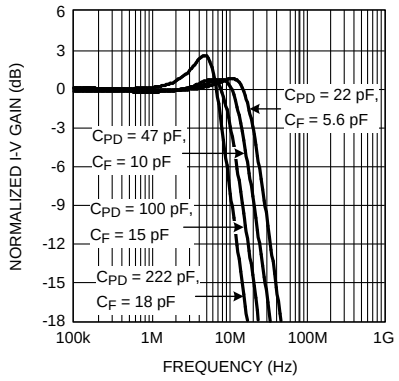

Figure 11. Frequency Response for Various Photodiode and Feedback Capacitors

When analyzing the noise at the output of the TIA, it is important to note that the various noise sources (i.e. op amp noise voltage, feedback resistor thermal noise, input noise current, photodiode noise current) do not all operate over the same frequency band. Therefore, when the noise at the output is calculated, this should be taken into account. The op amp noise voltage will be gained up in the region between the noise gain's zero and pole (f_Z and f_P in Figure 10). The higher the values of R_F and C_T, the sooner the noise gain peaking starts and therefore its contribution to the total output noise will be larger. It is obvious to note that it is advantageous to minimize C_{IN} by proper choice of op amp or by applying a reverse bias across the diode at the expense of excess dark current and noise.

DIFFERENTIAL CABLE DRIVER FOR NTSC VIDEO

The LMH6619Q can be used to drive an NTSC video signal on a twisted-pair cable. Figure 12 shows the schematic of a differential cable driver for NTSC video. This circuit can be used to transmit the signal from a camera over a twisted pair to a monitor or display located a distance. C_1 and C_2 are used to AC couple the video signal into the LMH6619Q. The two amplifiers of the LMH6619Q are set to a gain of 2 to compensate for the 75Ω back termination resistors on the outputs. The LMH6619Q is set to a gain of 1. Because of the DC bias the output of the LMH6619Q is AC coupled. Most monitors and displays will accept AC coupled inputs.

PRODUCT PREVIEW

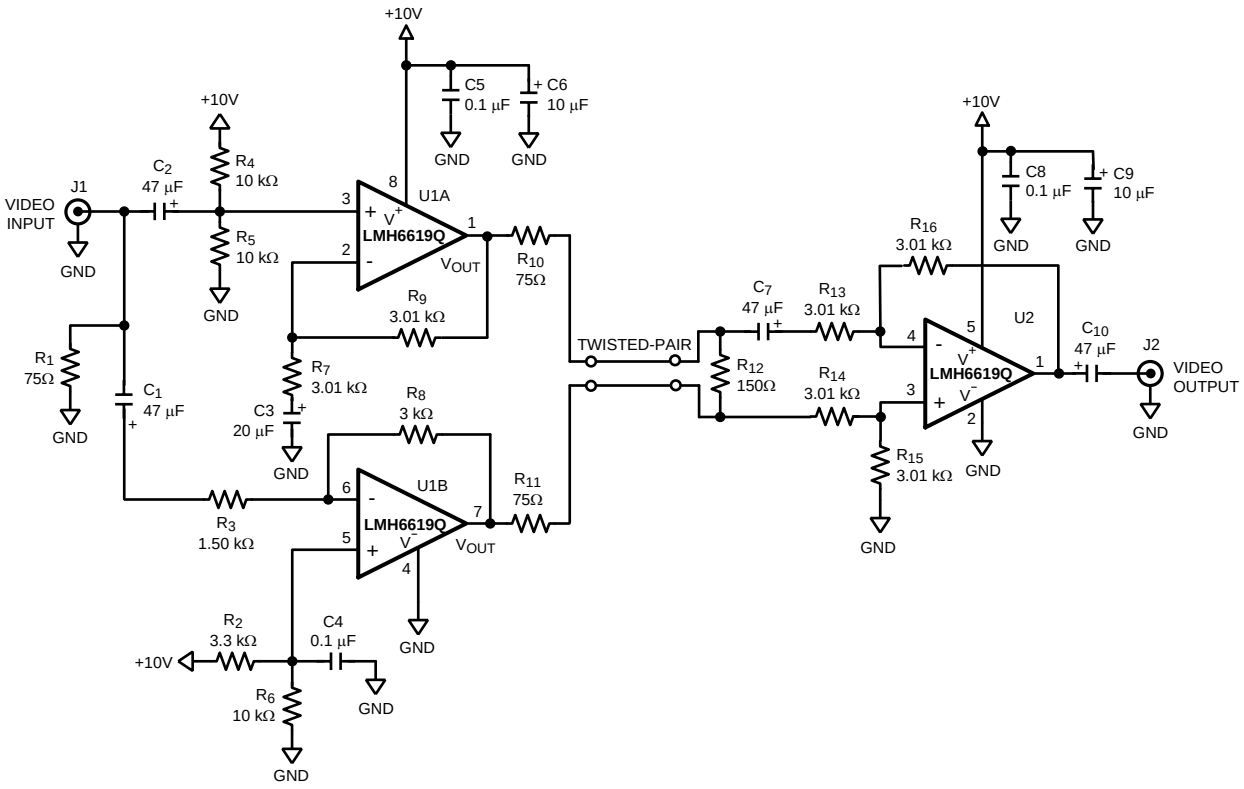

Figure 12. Differential Cable Driver

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6619QMAK/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 105	LMH66 19QMA	Samples
LMH6619QMAKE/NOPB	ACTIVE	SOIC	D	8	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 105	LMH66 19QMA	Samples
LMH6619QMAKX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 105	LMH66 19QMA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMH6619-Q1 :

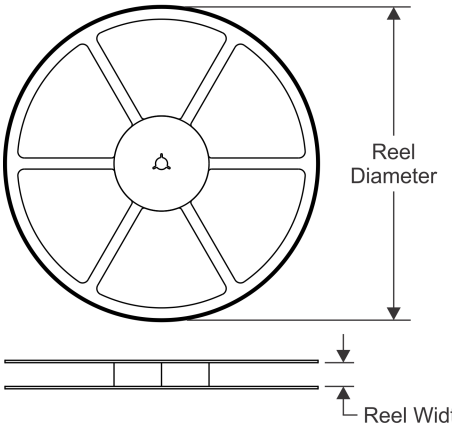
- Catalog: LMH6619

NOTE: Qualified Version Definitions:

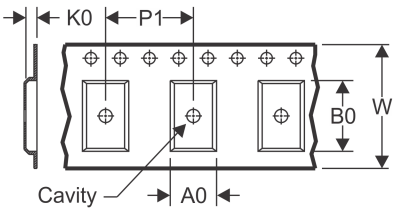
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

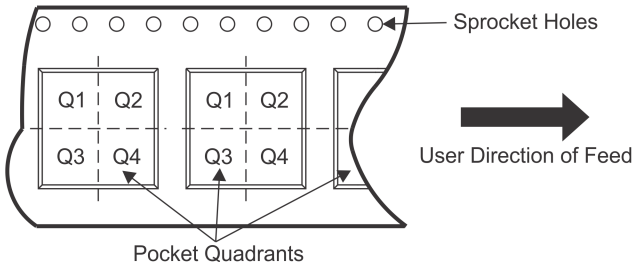


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

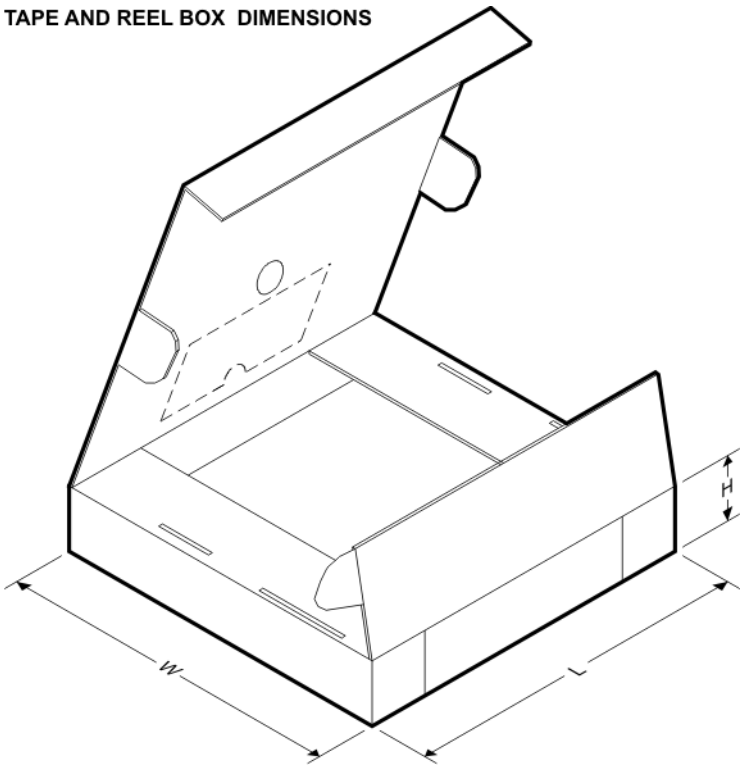
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

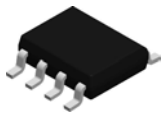
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6619QMAKE/NOPB	SOIC	D	8	250	178.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6619QMAKX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6619QMAKE/NOPB	SOIC	D	8	250	210.0	185.0	35.0
LMH6619QMAKX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

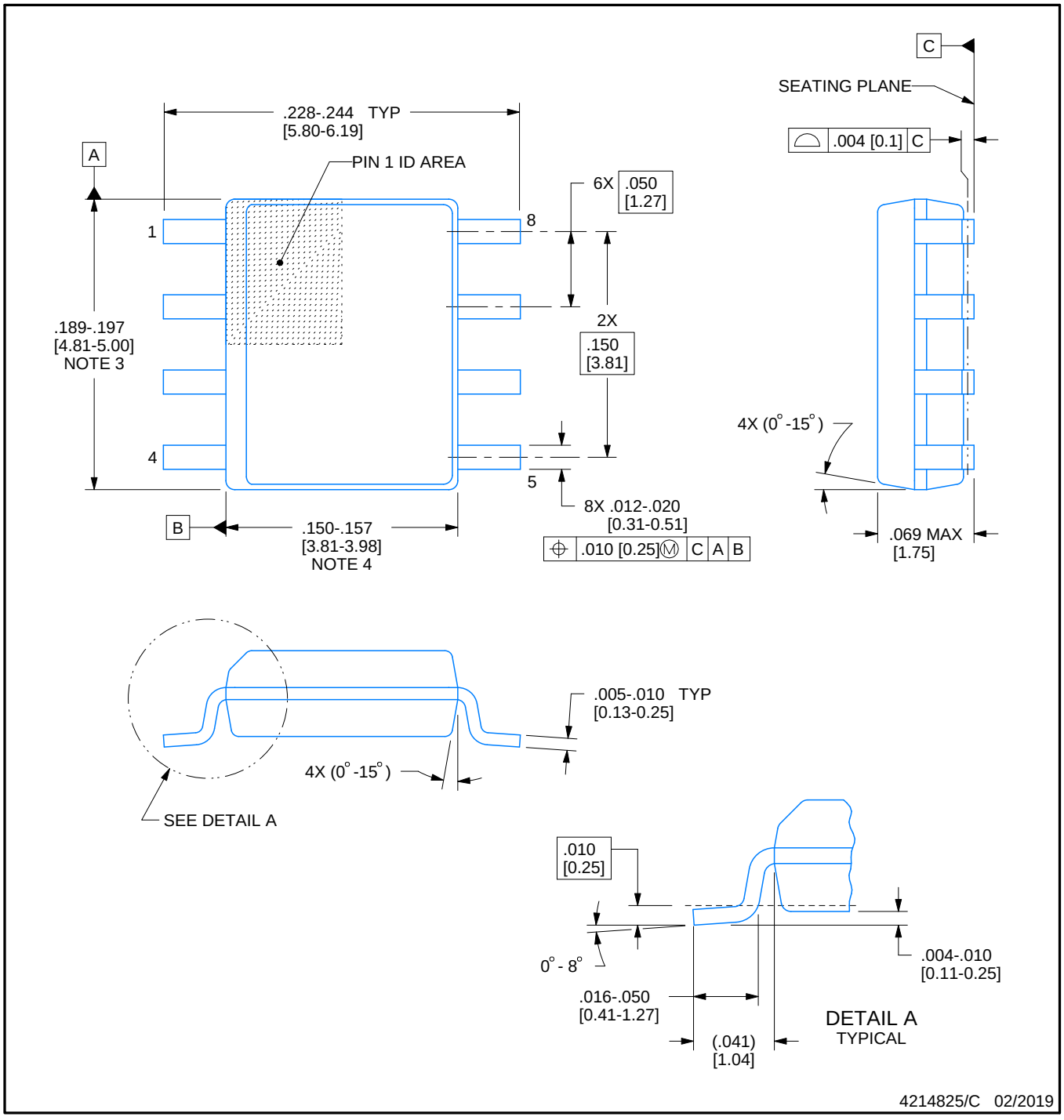


PACKAGE OUTLINE

D0008A

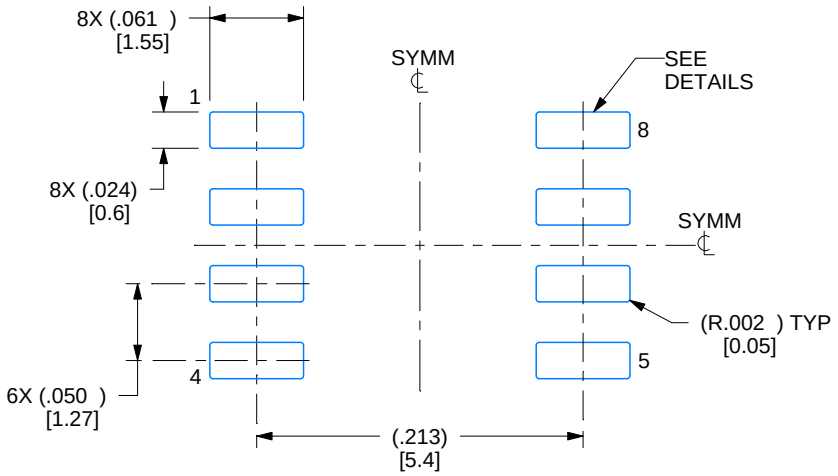
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

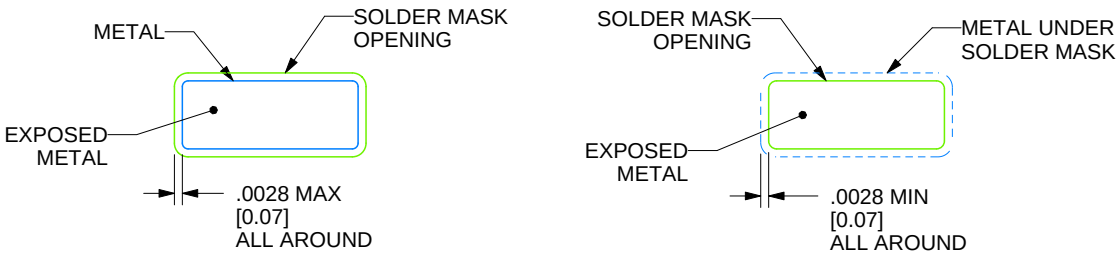


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

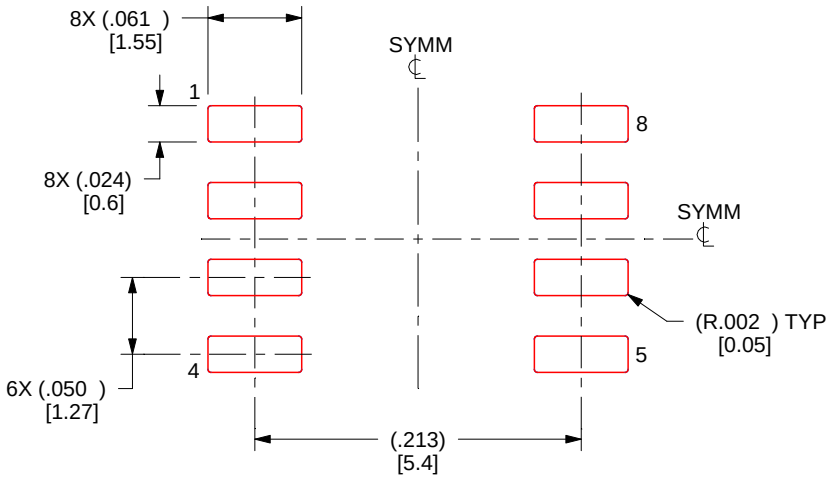
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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