Tsi721 PCIe2 to S-RIO2 Protocol Conversion Bridge

IDT
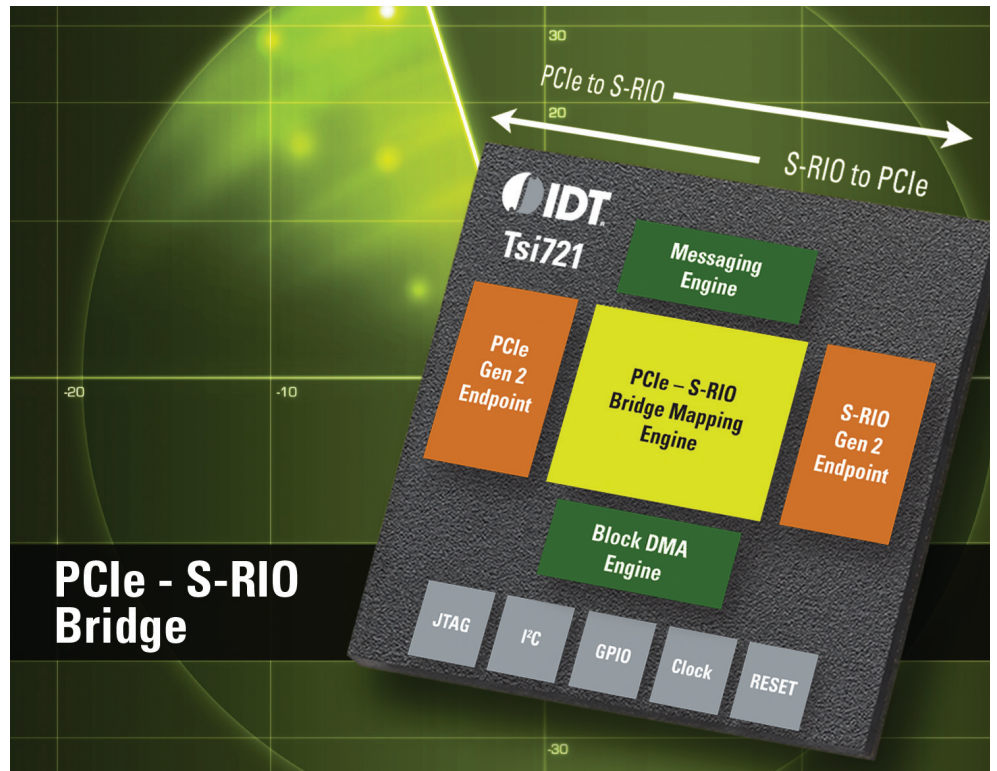**Integrated Device Technology**

FEATURES
- x4 PCIe V2.1 to x4 S-RIO V2.1
- Single port: x4, x2 or x1 support
- 1.25, 2.5, 3.125 and 5 Gbaud support
- 8 DMA and Messaging channels/engines each capable of supporting full 20 Gbaud I/O
- 8Kbyte packet buffering per DMA and Messaging Channel
- 20 Gaud line rate performance for 64 byte or larger packets, max TLP payload 256 bytes, max block DMA 64 Mbyte
- PCI Express non-transparent bridging for transaction mapping
- Lane reversal
- Automatic Polarity inversion for PCI Express
- Typical power 2W
- Reach Support: 60 cm over 2 connectors
- 100, 125, 156.25 MHz S-RIO and PCIe Endpoint compatible clocking options
- JTAG 1149.1 and 1149.6
- 13x13 mm FCBGA
- Industrial and Commercial options

BENEFITS
- Use RapidIO's peer to peer networking performance with PCIe enabled microprocessors and Network Processors
- Design Heterogeneous systems with RapidIO and PCI Express
- Execute large block data transfers without processor involvement for real time signal processing tasks
- No in house NRE required to develop bridging solutions with FPGA or ASIC
- Save on FPGA development, board space and power with Tsi721 solution
- Superior cost and form factor to Ethernet and Infiniband NICs
- Use a mix of RapidIO and PCIe based payload processing cards in the same chassis
- Map Block DMA transfers to RapidIO messages with dedicated DMA engine per messaging channel, ideal in highly data intensive signal processing applications
- Superior and deterministic performance and latency in embedded peer to peer networks compared to Ethernet and Infiniband solutions
- Provides Server Network Interface Controller Functionality

TARGET APPLICATIONS
- Defense & Aerospace: Radar, sonar and navigations systems
- Server and High Performance Computing
- Medical Imaging: CT Scanners, MRIs
- Video: Teleconferencing and Head End
- Wireless: Design Baseband Cards with PCIe enabled MAC/Control processor with S-RIO DSPs, S-RIO FPGA and S-RIO backplane

IDT is the industry's leading supplier of RapidIO® and PCI Express® Interconnect solutions, providing a broad portfolio of switches, bridges, IP and development platforms for defense, aerospace, video, imaging and wireless markets. The Tsi721 is IDT's solution for hardware based PCIe Gen 2 to RapidIO Gen 2 protocol conversion in a bridging device
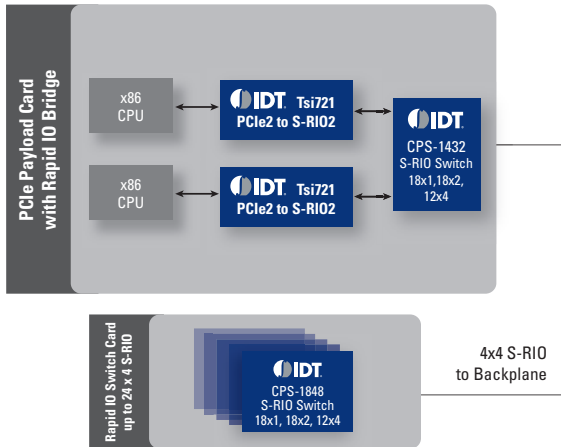
Tsi721 Device Overview

The Tsi721 converts from PCIe to RapidIO and vice versa and provides full line rate bridging at 20 Gbaud. Using the Tsi721 designers can develop heterogeneous systems that leverage the peer to peer networking performance of RapidIO while at the same time using multiprocessor clus¬ters that may only be PCIe enabled. Using the Tsi721, applications that require large amounts of data transferred efficiently without processor involvement can be executed using the full line rate block DMA+Messaging engines of the Tsi721.
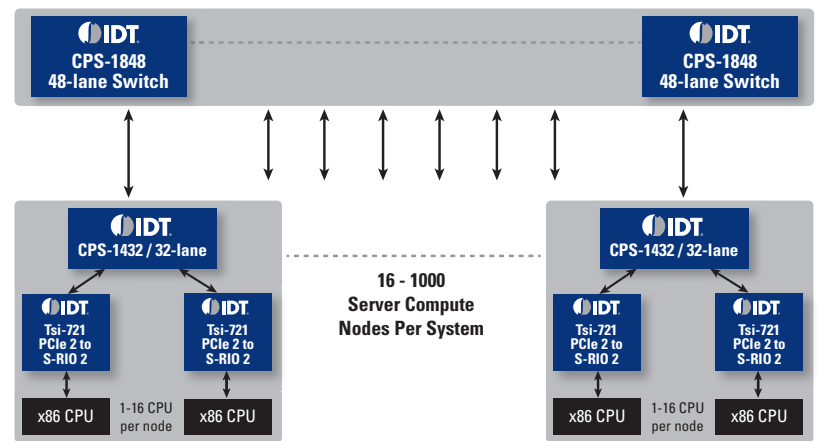
Protocol Conversion and Bridging Functionality

Key to the Tsi721 is the hardware bridging functionality that converts and maps PCIe transactions to RapidIO. The Tsi721 supports PCIe non transparent bridging for transaction mapping. The Tsi721 has both RapidIO and PCIe endpoints embedded in the bridge. With respect to bridging large data transfers, each of the DMA/Messaging channels can buffer up to 8K byte PCIe block DMA trans¬fers on the PCIe side and messages totaling 32 256 byte packets on the RapidIO side. This is all achieved in a significantly smaller form factor when compared to alternative implementations in FPGAs or Ethernet/Inifinband NIC devices.

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POWER MANAGEMENT | ANALOG & RF | **INTERFACE & CONNECTIVITY** | CLOCKS & TIMING | MEMORY & LOGIC | TOUCH & USER INTERFACE | VIDEO & DISPLAY | AUDIO
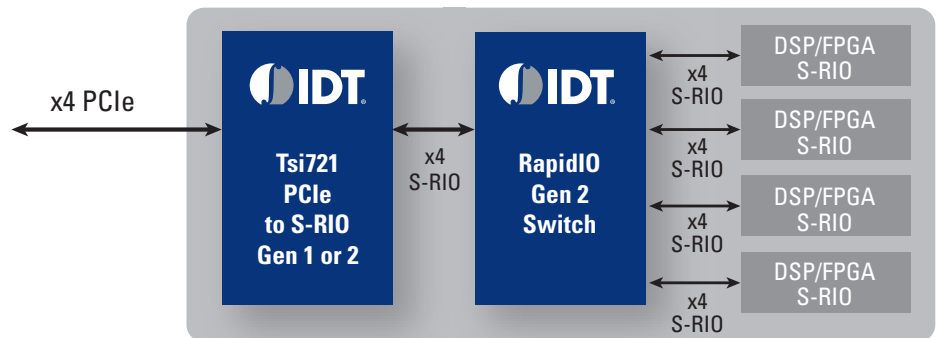
Defense/Aerospace Application

Server

PCI EXPRESS FEATURES

- Max-Packet-Size 128Byte or256Byte
- Max Read Request Size 4KByte
- Up to 32 simultaneous transactions
- 12K input, output buffers
- Store and forward from PCIe to RapidIO
- Support for End-to-End CRC (ECRC)
- Support for MSI-X with 70 vectors
- Support for legacy INTx/MSI
- Support for 32b and 64b addressing
- Support for Internal Error Reporting (IER) and Advanced Error Reporting (AER)
- PCIe spec compliant power management
- Boot from PCIe enabled processor or EEPROM

SERIAL RAPIDIO FEATURES

- Line rate performance with 64Byte and larger S-RIO packets with up to 256 outstanding transactions
- 8KB S-RIO ingress buffer (256x32 byte)
- Support for 34b, 50b, 66b addressing
- Support for 8b, 16b S-RIO Transport ids
- Support for 8 levels of priority using 4 S-RIO standard priorities plus CRF bit
- S-RIO messaging (type11) implemented with 4KB max message
- Store and Forward RapidIO to PCIe
- Support for following SRIO transaction types:
  - NRead, SWrite, NWrite, NWrite_R
  - Port Write
  - Doorbell
  - Maintenance Read, Maintenance Write
  - Message
- Access to all Tsi721 registers via SRIO maintenance transactions
- Hot Insertion/Extraction Support

Imaging/Video Application

Wireless Application

PB_TSI721_REVD0711

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