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#### Data Sheet

#### October 2013

#### N-Channel UltraFET Power MOSFET 55 V, 35 A, 34 mΩ

These N-Channel power MOSFETs are manufactured using the innovative UltraFET process. This advanced process technology achieves the lowest possible onresistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and batteryoperated products.

Formerly developmental type TA75321.

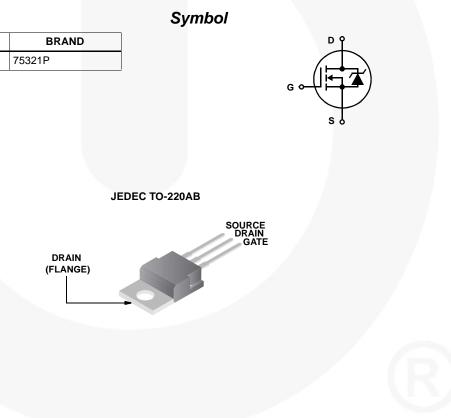
#### **Ordering Information**

Packaging

PART NUMBER	PACKAGE	BRAND
HUF75321P3	TO-220AB	75321P

#### Features

- 35A, 55V
- Simulation Models
  - Temperature Compensated PSPICE® and SABER™ Models
  - Thermal Impedance SPICE and SABER Models Available on the WEB at: www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"



Product reliability information can be found at http://www.fairchildsemi.com/products/discrete/reliability/index.html For severe environments, see our Automotive HUFA series.

All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

#### Absolute Maximum Ratings $T_C = 25^{\circ}C$ , Unless Otherwise Specified

		UNITS
Drain to Source Voltage (Note 1) V <sub>DSS</sub>	55	V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1)V <sub>DGR</sub>	55	V
Gate to Source Voltage	±20	V
Drain Current		
Continuous (Figure 2)	35	А
Pulsed Drain Current	Figure 4	
Pulsed Avalanche Rating E <sub>AS</sub>	Figures 6, 14, 15	
Power Dissipation P <sub>D</sub>	93	W
Derate Above 25 <sup>o</sup> C	0.625	W/ <sup>o</sup> C
Operating and Storage Temperature	-55 to 175	°C
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10sTL	300	oC
Package Body for 10s, See Techbrief 334	260	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE:

1.  $T_J = 25^{\circ}C$  to  $150^{\circ}C$ .

#### **Electrical Specifications** $T_C = 25^{\circ}C$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST	CONDITIONS	MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS	L.				1		1
Drain to Source Breakdown Voltage	BV <sub>DSS</sub>	$I_{D} = 250 \mu A, V_{GS} =$	0V (Figure 11)	55	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS}$ = 50V, $V_{GS}$ =	0V	-	-	1	μΑ
		$V_{DS}$ = 45V, $V_{GS}$ =	0V, T <sub>C</sub> = 150 <sup>o</sup> C	-	-	250	μΑ
Gate to Source Leakage Current	I <sub>GSS</sub>	$V_{GS} = \pm 20V$		-	-	±100	nA
ON STATE SPECIFICATIONS	<u>.</u>						
Gate to Source Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D = 25$	50μA (Figure 10)	2	-	4	V
Drain to Source On Resistance	r <sub>DS(ON)</sub>	I <sub>D</sub> = 35A, V <sub>GS</sub> = 10	V (Figure 9)	-	0.028	0.034	Ω
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	$R_{ extsf{ heta}JC}$	(Figure 3)		-	-	1.6	°C/W
Thermal Resistance Junction to Ambient	$R_{\thetaJA}$	TO-220		-	-	62	°C/W
SWITCHING SPECIFICATIONS (V <sub>GS</sub> = 10)	/)					1	
Turn-On Time	<sup>t</sup> ON	$V_{DD} = 30V, I_D \cong 35A, \\ R_L = 0.86\Omega, V_{GS} = 10V, \\ R_{GS} = 25\Omega$		-	-	100	ns
Turn-On Delay Time	t <sub>d(ON)</sub>			-	11	-	ns
Rise Time	t <sub>r</sub>			-	55	-	ns
Turn-Off Delay Time	<sup>t</sup> d(OFF)			-	47	-	ns
Fall Time	t <sub>f</sub>			-	66	•	ns
Turn-Off Time	tOFF			-	-	170	ns
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q <sub>g(TOT)</sub>	$V_{GS} = 0V$ to 20V	$V_{DD} = 30V,$	-	36	44	nC
Gate Charge at 10V	Q <sub>g(10)</sub>	$V_{GS} = 0V$ to 10V	<sup>−</sup> I <sub>D</sub> ≅ 35A, R <sub>I</sub> = 0.86Ω	-	21	26	nC
Threshold Gate Charge	Q <sub>g(TH)</sub>	$V_{GS} = 0V$ to 2V	$I_{g(REF)} = 1.0 \text{mA}$	-	1.3	1.6	nC
Gate to Source Gate Charge	Q <sub>gs</sub>		(Figure 13)	-	3	-	nC
Reverse Transfer Capacitance	Q <sub>gd</sub>			-	9	-	nC

### **Electrical Specifications** $T_{C} = 25^{\circ}C$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CAPACITANCE SPECIFICATIONS						
Input Capacitance	C <sub>ISS</sub>	$V_{DS} = 25V, V_{GS} = 0V,$	-	680	-	pF
Output Capacitance	C <sub>OSS</sub>	f = 1MHz (Figure 12)	-	270	-	pF
Reverse Transfer Capacitance	C <sub>RSS</sub>		-	60	-	pF

#### Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	ТҮР	MAX	UNITS
Source to Drain Diode Voltage	V <sub>SD</sub>	I <sub>SD</sub> = 35A	-	-	1.25	V
Reverse Recovery Time	t <sub>rr</sub>	$I_{SD} = 35A$ , $dI_{SD}/dt = 100A/\mu s$	-	-	59	ns
Reverse Recovered Charge	Q <sub>RR</sub>	$I_{SD} = 35A$ , $dI_{SD}/dt = 100A/\mu s$	-	-	82	nC

## Typical Performance Curves

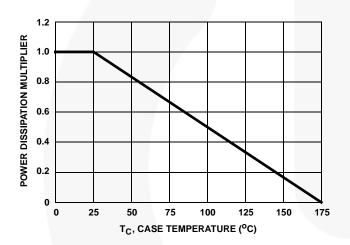


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

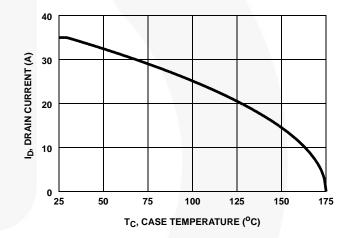


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

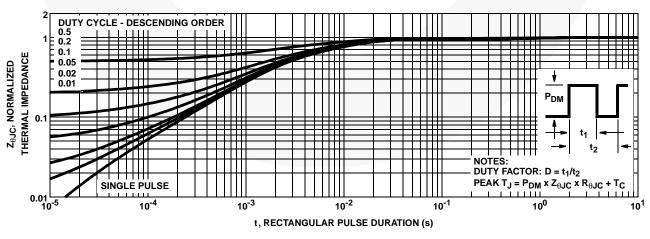
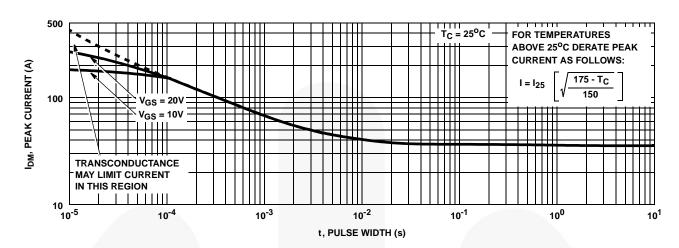


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE







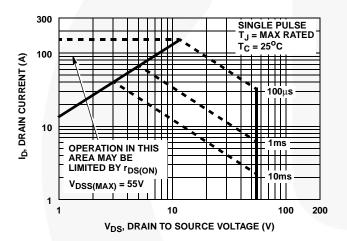


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA

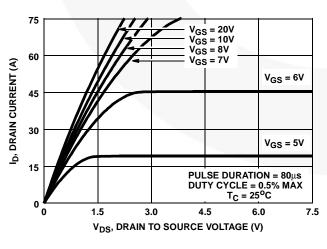
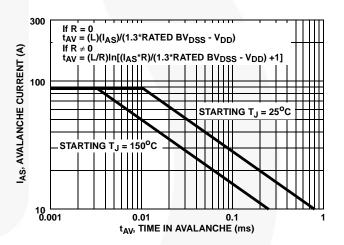
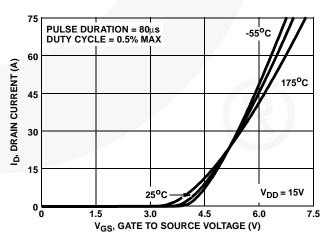


FIGURE 7. SATURATION CHARACTERISTICS

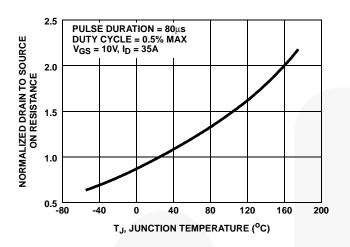


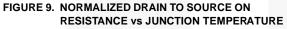
NOTE: Refer to Fairchild Application Notes AN9321 and AN9322. FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

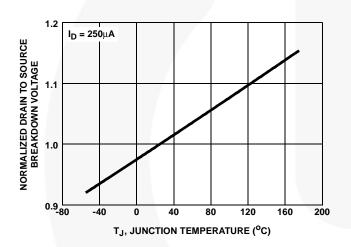


#### FIGURE 8. TRANSFER CHARACTERISTICS

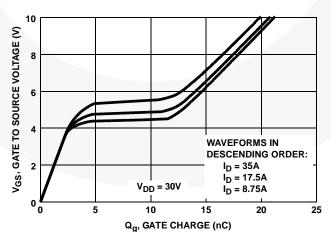
#### Typical Performance Curves (Continued)













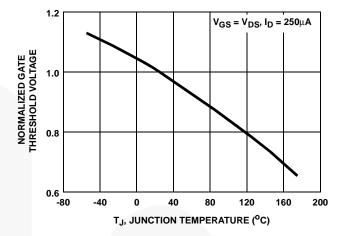
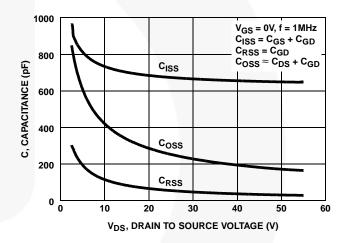


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE



#### FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

#### Test Circuits and Waveforms

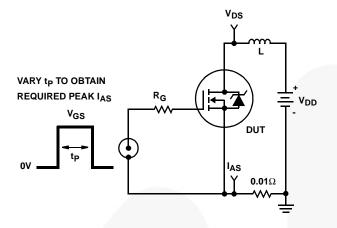


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

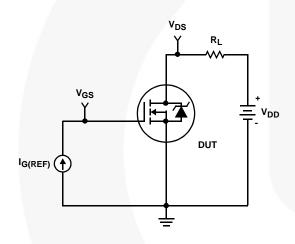


FIGURE 16. GATE CHARGE TEST CIRCUIT

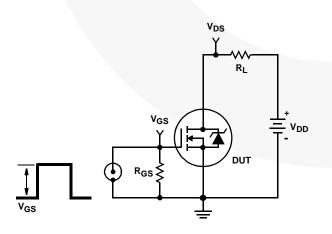


FIGURE 18. SWITCHING TIME TEST CIRCUIT

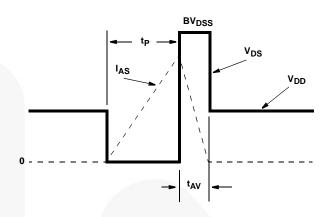
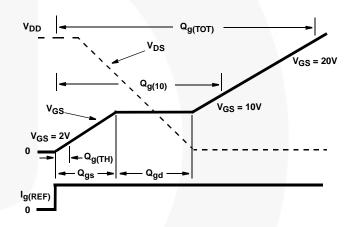


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS





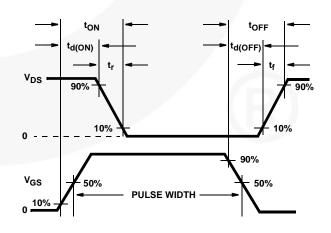
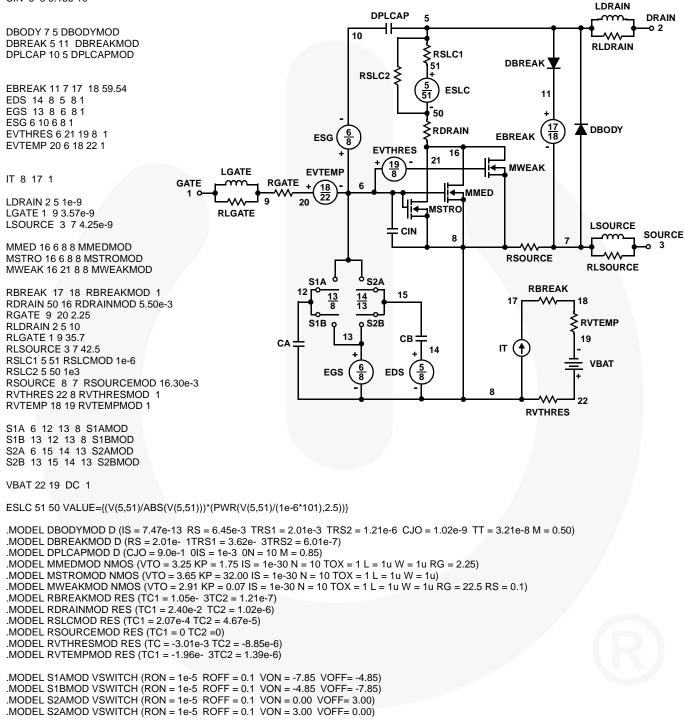


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

#### **PSPICE Electrical Model**

.SUBCKT HUF75321P 2 1 3 ; rev 4/29/98

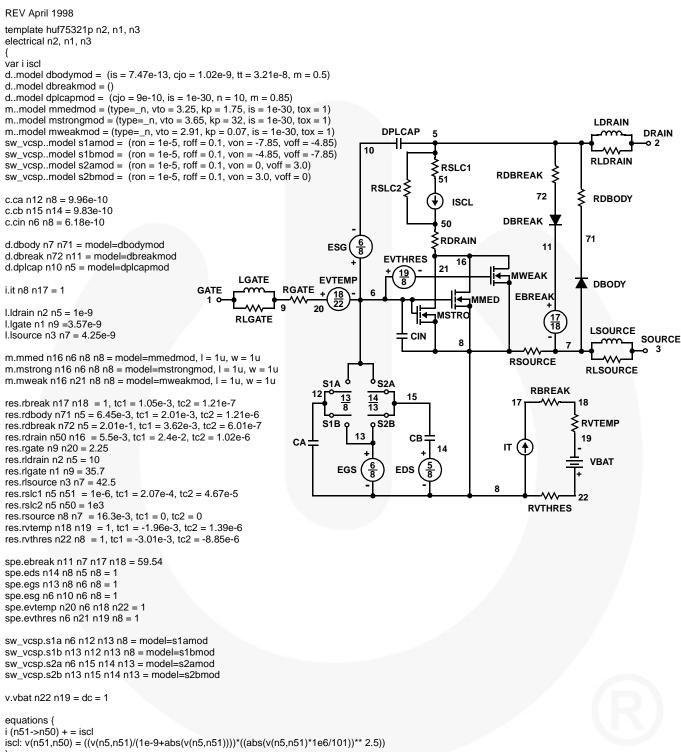
CA 12 8 9.96e-10 CB 15 14 9.83e-10 CIN 6 8 6.18e-10



#### .ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

#### SABER Electrical Model



#### SPICE Thermal Model

REV 24 February 1999

#### HUF75321P

CTHERM1 th 6 2.7e-3 CTHERM2 6 5 3.7e-3 CTHERM3 5 4 1.2e-2 CTHERM4 4 3 3.8e-3 CTHERM5 3 2 1.4e-2 CTHERM6 2 tl 10.55

RTHERM1 th 6 1.10e-2 RTHERM2 6 5 2.72e-2 RTHERM3 5 4 7.67e-2 RTHERM4 4 3 4.30e-1 RTHERM5 3 2 6.49e-1 RTHERM6 2 tl 8.61e-2

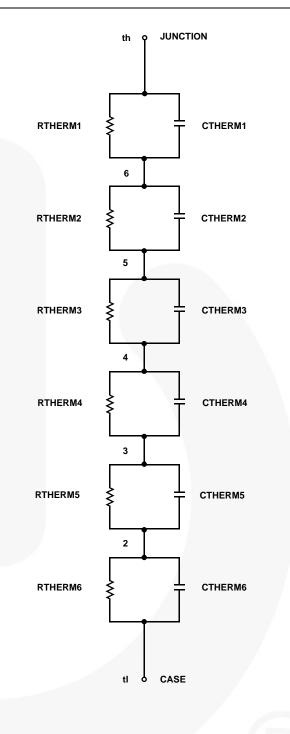
#### SABER Thermal Model

SABER thermal model HUF75321P

template thermal\_model th tl thermal\_c th, tl

ctherm.ctherm1 th 6 = 2.7e-3ctherm.ctherm2 6 5 = 3.7e-3ctherm.ctherm3 5 4 = 1.2e-2ctherm.ctherm4 4 3 = 3.8-3ctherm.ctherm5 3 2 = 1.4e-2ctherm.ctherm6 2 tl = 10.55

rtherm.rtherm1 th 6 = 1.10e-3rtherm.rtherm2 6 5 = 2.72e-2rtherm.rtherm3 5 4 = 7.67e-2rtherm.rtherm4 4 3 = 4.30e-1rtherm.rtherm5 3 2 = 6.49e-1rtherm.rtherm6 2 tl = 8.61e-2





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