MC74HC393A

Dual 4-Stage Binary Ripple Counter

High−Performance Silicon−Gate CMOS

The MC74HC393A is identical in pinout to the LS393. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

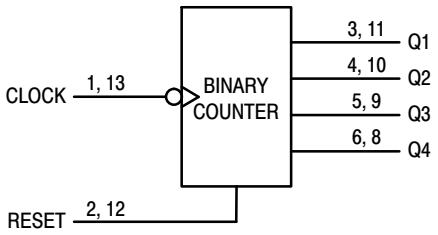
This device consists of two independent 4−bit binary ripple counters with parallel outputs from each counter stage. A ÷ 256 counter can be obtained by cascading the two binary counters.

Internal flip−flops are triggered by high−to−low transitions of the clock input. Reset for the counters is asynchronous and active−high. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the HC393A.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 236 FETs or 59 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

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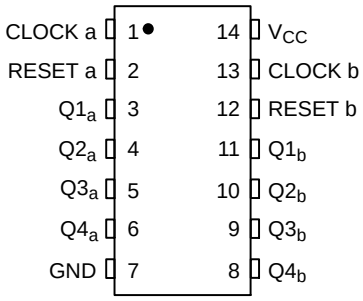
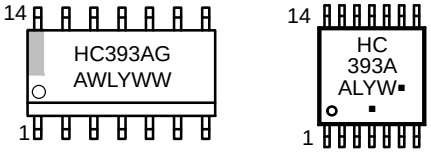
SOIC−14 NB
D SUFFIX
CASE 751A

TSSOP−14
DT SUFFIX
CASE 948G

PIN ASSIGNMENT



MARKING DIAGRAMS



SOIC−14 NB **TSSOP−14**

A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Inputs		
Clock	**Reset**	**Outputs**
X	H	L
H	L	No Change
L	L	No Change
↗	L	No Change
↘	L	Advance to Next State

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds SOIC or TSSOP Package	 260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: –7 mW/°C from 65° to 125°C
TSSOP Package: −6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		–55	+125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0 V	0	1000	ns
		V_{CC} = 3.0 V	0	600	
	(Figure 1)	V_{CC} = 4.5 V	0	500	
		V_{CC} = 6.0 V	0	400	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High−Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low−Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.80	0.5 0.9 1.35 1.80	0.5 0.9 1.35 1.80	V
V_{OH}	Minimum High−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND) (continued)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤ 85°C	≤ 125°C	
V_{OL}	Maximum Low−Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 2.4$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μA	6.0	4	40	160	μA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	2.0 3.0 4.5 6.0	10 15 30 50	9 14 28 45	8 12 25 40	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q1 (Figures 1 and 3)	2.0 3.0 4.5 6.0	70 40 24 20	80 45 30 26	90 50 36 31	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q2 (Figures 1 and 3)	2.0 3.0 4.5 6.0	100 56 34 20	105 70 45 38	180 100 55 48	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q3 (Figures 1 and 3)	2.0 3.0 4.5 6.0	130 80 44 37	150 105 55 47	180 130 70 58	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q4 (Figures 1 and 3)	2.0 3.0 4.5 6.0	160 110 52 44	250 185 65 55	300 210 82 65	ns
t_{PHL}	Maximum Propagation Delay, Reset to any Q (Figures 2 and 3)	2.0 3.0 4.5 6.0	80 48 30 26	95 65 38 33	110 75 50 43	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance	–	10	10	10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Counter)*	35	pF

* Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			−55 to 25°C	≤ 85°C	≤ 125°C	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 3.0 4.5 6.0	25 15 10 9	30 20 13 11	40 30 15 13	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 15	110 36 22 19	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 15	110 36 22 19	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

PIN DESCRIPTIONS

INPUTS

Clock (Pins 1, 13)

Clock input. The internal flip−flops are toggled and the counter state advances on high−to−low transitions of the clock input.

OUTPUTS

Q1, Q2, Q3, Q4 (Pins 3, 4, 5, 6, 8, 9, 10, 11)

Parallel binary outputs Q4 is the most significant bit.

CONTROL INPUTS

Reset (Pins 2, 12)

Active−high, asynchronous reset. A separate reset is provided for each counter. A high at the Reset input prevents counting and forces all four outputs low.

SWITCHING WAVEFORMS

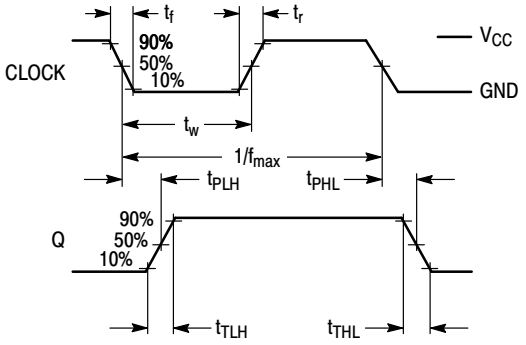


Figure 1.

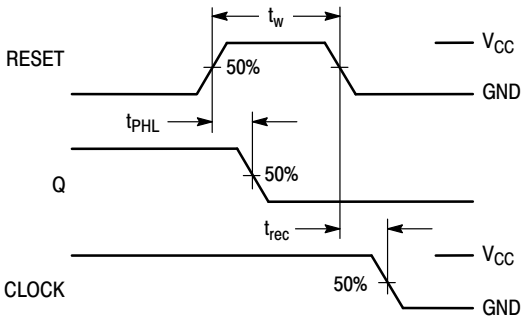
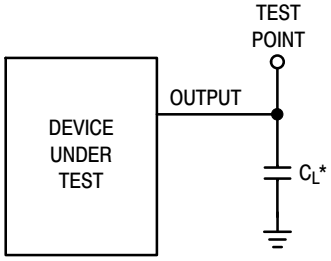


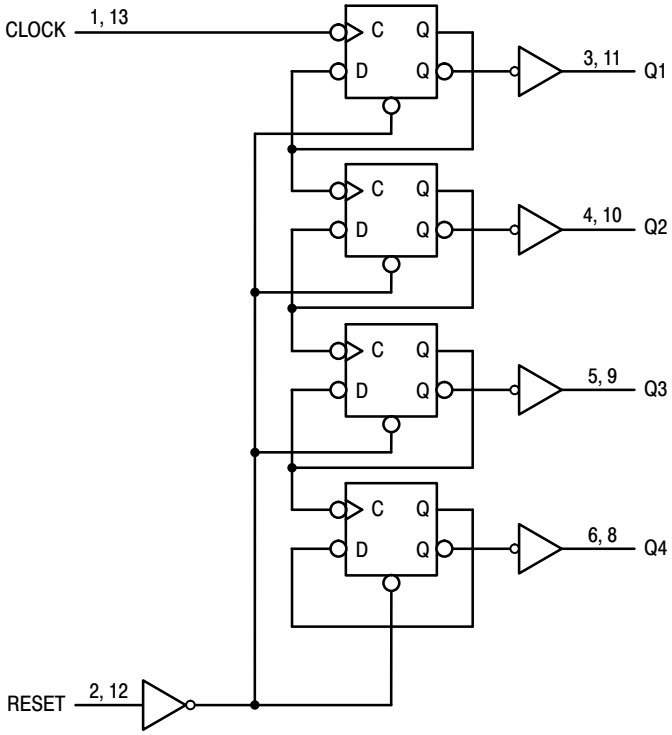
Figure 2.



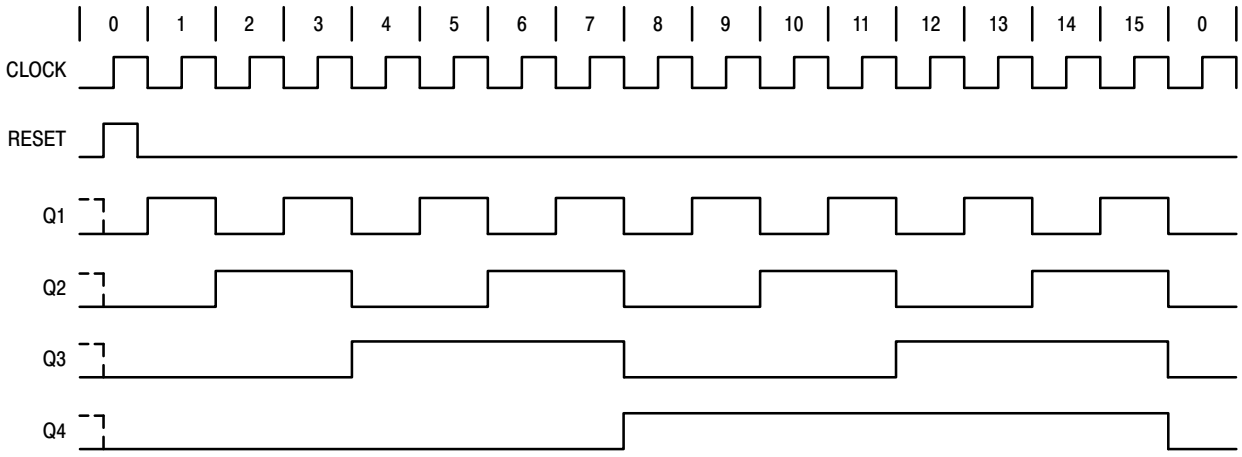
*Includes all probe and jig capacitance

Figure 3. Test Circuit

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM



COUNT SEQUENCE

Count	Outputs			
	Q4	Q3	Q2	Q1
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

ORDERING INFORMATION

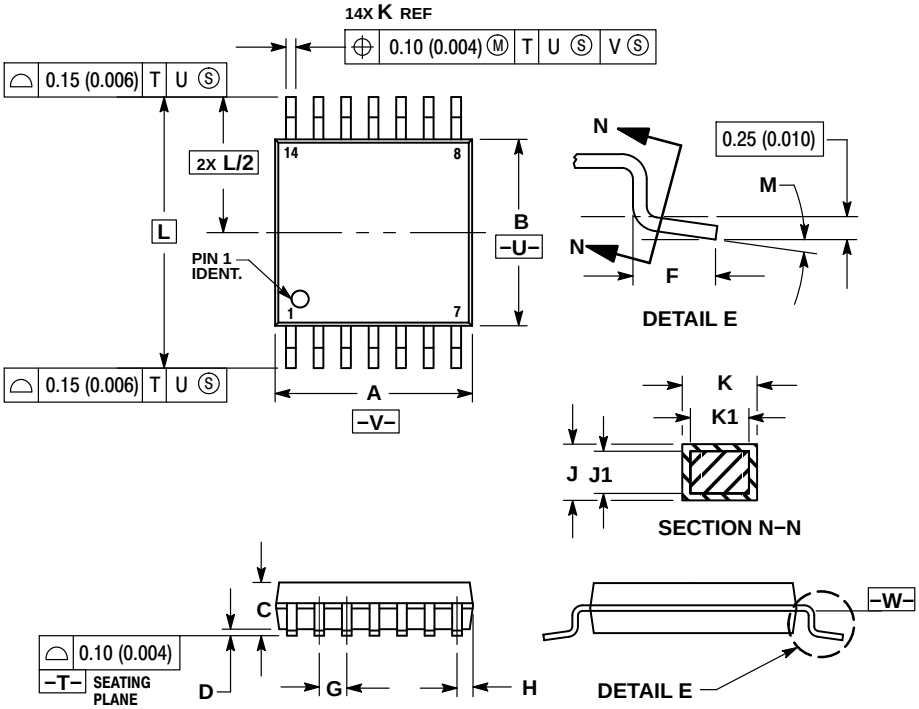
Device	Package	Shipping†
MC74HC393ADG	SOIC−14 NB (Pb−Free)	55 Units / Rail
MC74HC393ADR2G	SOIC−14 NB (Pb−Free)	2500 / Tape & Reel
NLV74HC393ADR2G*	SOIC−14 NB (Pb−Free)	2500 / Tape & Reel
MC74HC393ADTR2G	TSSOP−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

PACKAGE DIMENSIONS

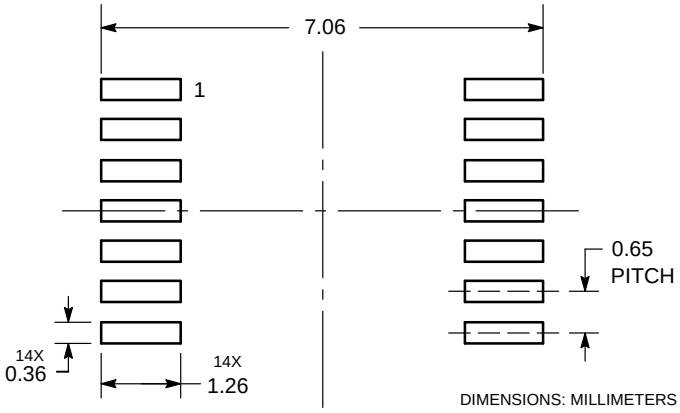
TSSOP−14
DT SUFFIX
CASE 948G
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

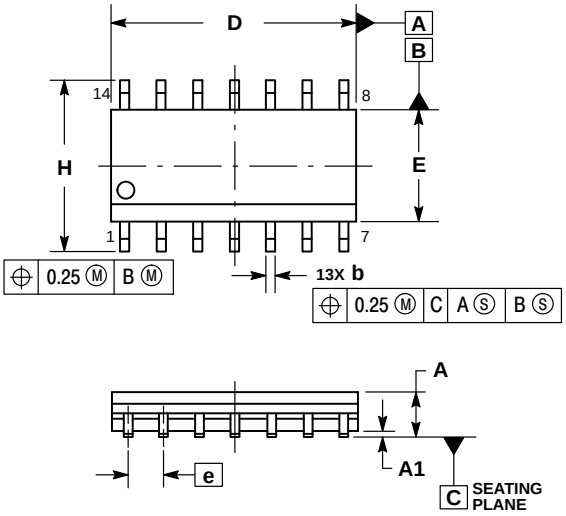
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

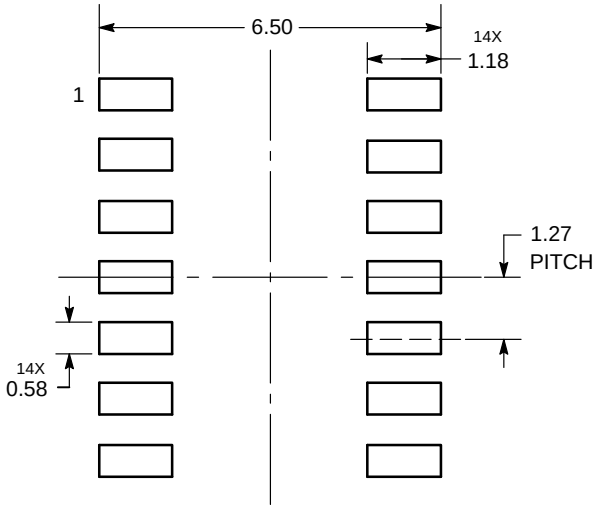
SOIC−14 NB
CASE 751A−03
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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Europe, Middle East and Africa Technical Support:
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