

LV77D Series 3.3 V LVDS Clock Oscillators

June 2019

Lead Free



- Pletronics' LV77D Series is a quartz crystal controlled precision square wave generator with an LVDS output.
- The package is designed for high density surface mount designs.
- Low cost mass produced oscillator.
- Tape and Reel or cut tape packaging is available.
- 5 x 7 mm LCC Ceramic Package
- Enable/Disable Function on pad 1
- Disable function includes low standby power mode
- Low Jitter
- 80 MHz ~ 325 MHz

**Pletronics Inc. certifies this device is in accordance with the
RoHS 6/6 (2011/65/EC) and WEEE (2002/96/EC) directives.**

Pletronics Inc. guarantees the device does not contain the following:

Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's

Weight of the Device: 0.16 grams

Moisture Sensitivity Level: 1 As defined in J-STD-020D.1

Second Level Interconnect code: e4

Absolute Maximum Ratings:

Parameter	Unit
V _{CC} Supply Voltage	-0.5V to +5.0V
V _i Input Voltage	-0.5V to V _{CC} + 0.5V
V _o Output Voltage	-0.5V to V _{CC} + 0.5V

Thermal Characteristics

The maximum die or junction temperature is 155°C

The thermal resistance junction to board is 30 to 50°C/Watt depending on the solder pads, ground plane and construction of the PCB.

Part Number:

LV77	45	D	E	V	-125.0M	-XX
------	----	---	---	---	---------	-----

Part Marking:

							Packaging code or blank T250 = 250 per Tape and Reel T500 = 500 per Tape and Reel T1K = 1000 per Tape and Reel	PLE LV77 FF.FFF M • YMDXX
							Frequency in MHz	or
							Supply Voltage V_{cc} V = 3.3V ± 10%	LV7XYWWXX FF.FFF M • PLE XXX
							Optional Enhanced OTR Blank = Temp. range -10 to +70°C C = Temp. range -20 to +70°C E = Temp. range -40 to +85°C	
							Series Model	
							Frequency Stability 45 = ± 50 ppm 44 = ± 25 ppm 20 = ± 20 ppm	
							Series Model	

Marking Legend:

PLE = Pletronics

FF.FFF M = Frequency in MHz

YYWW or YWW or YMD = Date of Manufacture (year and week, or year-month-day)

All other marking is internal factory codes

Specifications such as frequency stability, supply voltage and operating temperature range, etc. are not identified from the marking. External packaging labels and packing list will correctly identify the ordered Pletronics part number.

Codes for Date Code YMD

Code	6	7	8	9	0	Code	A	B	C	D	E	F	G	H	J	K	L	M
Year	2016	2017	2018	2019	2020	Month	JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC

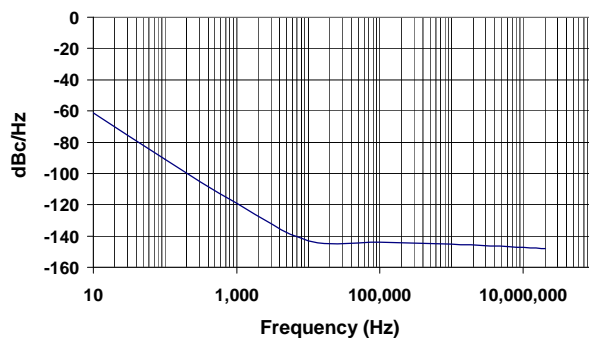
Code	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	G
Day	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Code	H	J	K	L	M	N	P	R	T	U	V	W	X	Y	Z	
Day	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	

Electrical Specification for 3.30V $\pm 10\%$ over the specified temperature range and the frequency range of 80 to 325 MHz

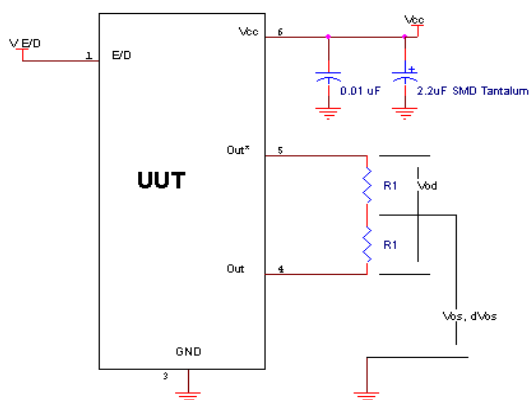
Item	Min	Max	Unit	Condition	
Frequency Accuracy “45”	-50	+50	ppm	For all supply voltages, load changes, aging for 1 year, shock, vibration and temperatures	
“44”	-25	+25			
“20”	-20	+20			
Output Waveform	LVDS				
Output High Level	--	1.60	Volts	-	See load circuit R1 = 50 ohms
Output Low Level	0.90	--	Volts	-	
Differential Output (V _{OD})	250	450	mVolts	-	
Output Offset Voltage (V _{OS})	1.125	1.375	Volts	≥ 80 MHz	
	1.125	1.500	Volts	< 80 MHz	
Differential Output Error (dV _{OS})	--	50	mVolts	-	
Output Symmetry	45	55	%	Referenced to 50% of amplitude or crossing point	
Output T _{RISE} and T _{FALL}	300	700	pS	≥ 80 MHz	Vth is 20% and 80% of waveform
	400	900	pS	< 80 MHz	
Jitter	-	0.6	pS RMS	Measured from 12KHz to 20MHz from Fnominal	
	-	2.8		Measured from 10Hz to 1MHz from Fnominal	
Vcc Supply Current	-	66	mA	≥ 80 MHz	Includes current of properly terminated device
	-	45	mA	< 80 MHz	
Enable/Disable Internal Pull-up	50	-	Kohm	To Vcc (equivalent resistance)	
V disable	-	0.8	Volts	Referenced to Ground	
V enable	2.0	-	Volts	Referenced to Ground	
Output leakage V _{OUT} = V _{CC}	-10	+10	uA	Pad 1 low, device disabled	
V _{OUT} = 0V	-10	+10	uA		
Enable time	-	2	mS	Time for output to reach a logic state	
Disable time	-	200	nS	Time for output to reach a high Z state	
Start up time	-	5	mS	≥ 80 MHz	Measured from the time Vcc = 3.0V
	-	3	mS	< 80 MHz	
Operating Temperature Range	-10	+70	°C	Standard Temperature Range	
	-20	+70	°C	Extended Temperature Range “C” Option	
	-40	+85	°C	Extended Temperature Range “E” Option	
Storage Temperature Range	-55	+125	°C		
Standby Current I _{CC}	-	30	uA	≥ 80 MHz	Pad 1 low, device disabled
	-	1.5	mA	< 80 MHz	

Specifications with Pad 1 E/D open circuit

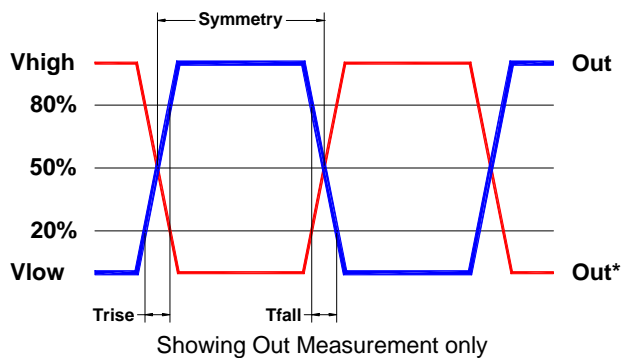
Typical Phase-Noise Response



Load Circuit



Test Waveform



Reliability: Environmental Compliance

Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002, Condition B
Vibration	MIL-STD-883 Method 2007, Condition A
Solderability	MIL-STD-883 Method 2003
Thermal Shock	MIL-STD-883 Method 1011, Condition A

ESD Rating

Model	Minimum Voltage	Conditions
Human Body Model	1500	MIL-STD-883 Method 3115
Charged Device Model	1000	JESD 22-C101

Package Labeling

Label is 1" x 2.6" (25.4mm x 66.7mm)

Font is Courier New

Bar code is 39-Full ASCII

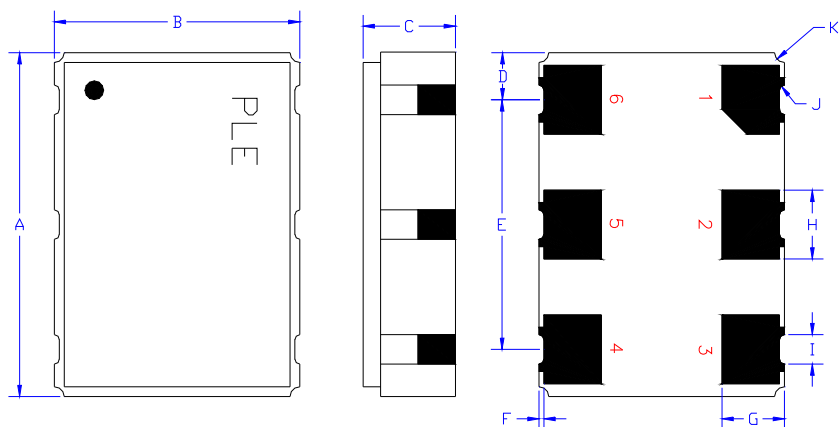
Label is 1" x 2.6" (25.4mm x 66.7mm)

Font is Arial

P/N:		
	LV7745DV-100.0M	
Customer P/N:		
	12345678	
Qty:		D/C 
	1000	75501

RoHS Compliant
2nd Lvl Interconnect
Category=e4
Max Safe Temp=260C for 10s 2X Max

Mechanical:



	Inches	mm
A	0.276 ±0.006	7.00 ±0.15
B	0.197 ±0.006	5.00 ±0.15
C	0.067 max	1.70 max
D ¹	0.038	0.96
E ¹	0.200	5.08
F ¹	0.004	0.10
G ¹	0.050	1.27
H ¹	0.055	1.40
I ¹	0.024	0.60
J ¹	0.004R	0.10R
K ¹	0.008R	0.20R

Contacts (pads):

Gold 11.8 to 39.4µinches (0.3 to 1.0µm)
over

Nickel 50 to 350 µinches (1.27 to 8.89 µm)

¹ Typical dimensions

Not to Scale

Pad	Function	Note
1	Output Enable/Disable	When this pad is not connected the oscillator shall operate. When this pad is <0.30 volts, the output will be inhibited (high impedance state.) Recommend connecting this pad to V _{CC} if the oscillator is to be always on.
2	No connect	There is no internal connection to this pad
3	Ground (GND)	
4	Output	The outputs must be terminated, 100 ohms between the outputs is the ideal termination.
5	Output*	
6	Supply Voltage (V _{CC})	Recommend connecting appropriate power supply bypass capacitors as close as possible.



Layout and application information

Recommend connecting Pad 1 and Pad 2 together to permit the design to accept Enable/Disable on both input pads

For Optimum Jitter Performance, Pletronics recommends:

- a ground plane under the device
- no large transient signals (both current and voltage) should be routed under the device
- do not layout near a large magnetic field such as a high frequency switching power supply
- do not place near piezoelectric buzzers or mechanical fans.

7

IMPORTANT NOTICE

Pletronics Incorporated (PLE) reserves the right to make corrections, improvements, modifications and other changes to this product at anytime. PLE reserves the right to discontinue any product or service without notice. Customers are responsible for obtaining the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to PLE's terms and conditions of sale supplied at the time of order acknowledgment.

PLE warrants performance of this product to the specifications applicable at the time of sale in accordance with PLE's limited warranty. Testing and other quality control techniques are used to the extent PLE deems necessary to support this warranty. Except where mandated by specific contractual documents, testing of all parameters of each product is not necessarily performed.

PLE assumes no liability for application assistance or customer product design. Customers are responsible for their products and applications using PLE components. To minimize the risks associated with the customer products and applications, customers should provide adequate design and operating safeguards.

PLE products are not designed, intended, authorized or warranted to be suitable for use in life support applications, weapons, weapon systems or space applications, devices or systems or other critical applications that may involve potential risks of death, personal injury or severe property or environmental damage. Inclusion of PLE products in such applications is understood to be fully at the risk of the customer. Use of PLE products in such applications requires the written approval of an appropriate PLE officer. Questions concerning potential risk applications should be directed to PLE.

PLE does not warrant or represent that any license, either express or implied, is granted under any PLE patent right, copyright, artwork or other intellectual property right relating to any combination, machine or process which PLE product or services are used. Information published by PLE regarding third-party products or services does not constitute a license from PLE to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from PLE under the patents or other intellectual property of PLE.

Reproduction of information in PLE data sheets or web site is permissible only if the reproduction is without alteration and is accompanied by associated warranties, conditions, limitations and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. PLE is not responsible or liable for such altered documents.

Resale of PLE products or services with statements different from or beyond the parameters stated by PLE for that product or service voids all express and implied warranties for the associated PLE product or service and is an unfair or deceptive business practice. PLE is not responsible for any such statements.

Contacting Pletronics Inc.

Pletronics Inc.
19013 36th Ave. West
Lynnwood, WA 98036-5761 USA

Tel: 425-776-1880
Fax: 425-776-2760
E-mail: ple-sales@pletronics.com
URL: www.pletronics.com

Copyright © 2018 Pletronics Inc.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Pletronics:

[LV7744DEV-100.0M](#) [LV7744DEV-106.25M](#) [LV7744DEV-125.0M](#) [LV7744DEV-156.25M](#) [LV7744DEV-25.0M](#)
[LV7744DEV-40.0M](#) [LV7744DEV-50.0M](#) [LV7744DEV-62.50M](#) [LV7744DEV-75.0M](#) [LV7745DEV-100.000M](#)
[LV7745DEV-156.250M](#) [LV7745DEV-212.50M](#) [LV7745DEV-125.0M](#) [LV7744DV-125.0M](#) [LV7745DV-100.0M](#)
[LV7745DEV-156.25M](#) [LV7744DV-100.0M](#) [LV7720DEV-125.0MT250](#) [LV7720DEV-125.0M-T250](#) [LV7745DEV-155.520M](#) [LV7745DEV-106.25M](#)