

- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

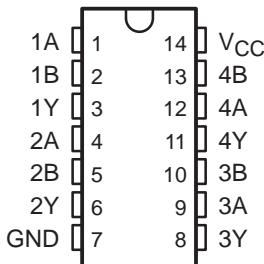
These devices contain four independent 2-input positive-OR gates. They perform the Boolean functions $Y = A \bullet B$ or $Y = A + B$ in positive logic.

The SN54ALS32 and SN54AS32 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS32 and SN74AS32 are characterized for operation from 0°C to 70°C .

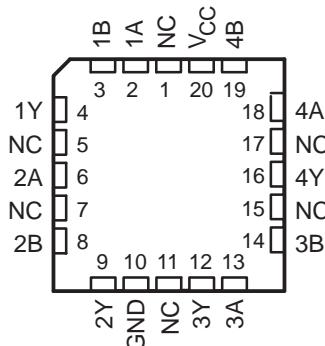
FUNCTION TABLE
(each gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | X | H |
| X | H | H |
| L | L | L |

SN54ALS32, SN54AS32 . . . J PACKAGE
SN74ALS32, SN74AS32 . . . D OR N PACKAGE
(TOP VIEW)

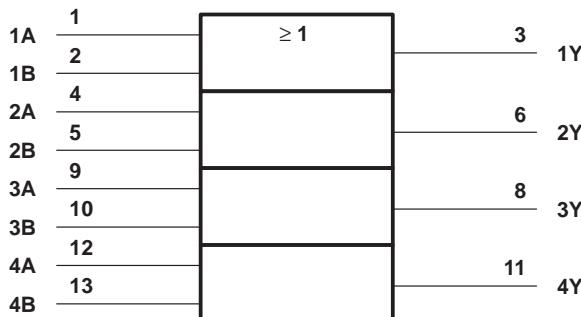


SN54ALS32, SN54AS32 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

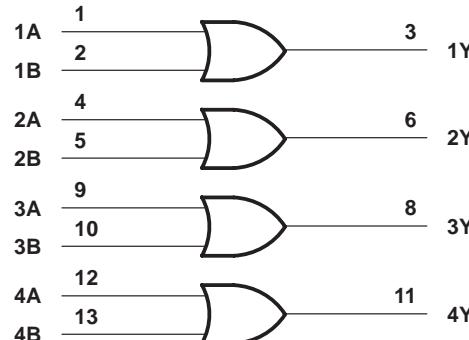
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



SN54ALS32, SN54AS32, SN74ALS32, SN74AS32 QUADRUPLE 2-INPUT POSITIVE-OR GATES

SDAS113B – APRIL 1982 – REVISED DECEMBER 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I | 7 V |
| Operating free-air temperature range, T_A : | |
| SN54ALS32 | -55°C to 125°C |
| SN74ALS32 | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| | | SN54ALS32 | | | SN74ALS32 | | | UNIT |
|-----------------|--------------------------------|-----------|-----|------|-----------|-----|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V _{IH} | High-level input voltage | | 2 | | | 2 | | V |
| V _{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I _{OH} | High-level output current | | | -0.4 | | | -0.4 | mA |
| I _{OL} | Low-level output current | | | 4 | | | 8 | mA |
| T _A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SN54ALS32 | | | SN74ALS32 | | | UNIT |
|------------------|---|------------------------|------|------|---------------------|------|------|------|
| | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| V _{IK} | V _{CC} = 4.5 V, I _I = -18 mA | | | -1.5 | | | -1.5 | V |
| V _{OH} | V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA | V _{CC} - 2 | | | V _{CC} - 2 | | | V |
| V _{OL} | V _{CC} = 4.5 V | I _{OL} = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 |
| | | I _{OL} = 8 mA | | | | | 0.35 | 0.5 |
| I _I | V _{CC} = 5.5 V, V _I = 7 V | | | 0.1 | | | 0.1 | mA |
| I _{IH} | V _{CC} = 5.5 V, V _I = 2.7 V | | | 20 | | | 20 | µA |
| I _{IL} | V _{CC} = 5.5 V, V _I = 0.4 V | | | -0.1 | | | -0.1 | mA |
| I _O § | V _{CC} = 5.5 V, V _O = 2.25 V | -20 | -112 | | -30 | -112 | | mA |
| I _{CCH} | V _{CC} = 5.5 V, V _I = 4.5 V | | | 1.9 | 4 | | 1.9 | 4 |
| I _{CCL} | V _{CC} = 5.5 V, V _I = 0 | | | 2.6 | 4.9 | | 2.6 | 4.9 |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

⁸ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1).

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX [¶] | | | | UNIT | |
|------------------|-----------------|----------------|---|-----|-----------|-----|------|--|
| | | | SN54ALS32 | | SN74ALS32 | | | |
| | | | MIN | MAX | MIN | MAX | | |
| t _{PLH} | A or B | Y | 3 | 18 | 3 | 14 | ns | |
| t _{PHL} | | | 3 | 16 | 3 | 12 | | |

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| | | SN54AS32 | | | SN74AS32 | | | UNIT |
|-----------------|--------------------------------|----------|-----|-----|----------|-----|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V _{IH} | High-level input voltage | | 2 | | | 2 | | V |
| V _{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I _{OH} | High-level output current | | | -2 | | | -2 | mA |
| I _{OL} | Low-level output current | | | 20 | | | 20 | mA |
| T _A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SN54AS32 | | | SN74AS32 | | | UNIT |
|-----------|--|--------------|------|------|--------------|------|------|---------------|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V_{IK} | $V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$ | | | -1.2 | | | -1.2 | V |
| V_{OH} | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -2 \text{ mA}$ | $V_{CC} - 2$ | | | $V_{CC} - 2$ | | | V |
| V_{OL} | $V_{CC} = 4.5 \text{ V}$, $I_{OL} = 20 \text{ mA}$ | | 0.35 | 0.5 | | 0.35 | 0.5 | V |
| I_I | $V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$ | | | 0.1 | | | 0.1 | mA |
| I_{IH} | $V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$ | | | 20 | | | 20 | μA |
| I_{IL} | $V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$ | | | -0.5 | | | -0.5 | mA |
| $I_O\$$ | $V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$ | -30 | -112 | | -30 | -112 | | mA |
| I_{CCH} | $V_{CC} = 5.5 \text{ V}$, $V_I = 4.5 \text{ V}$ | | 7.3 | 12 | | 7.3 | 12 | mA |
| I_{CCL} | $V_{CC} = 5.5 \text{ V}$, $V_I = 0$ | | 16.5 | 26.6 | | 16.5 | 26.6 | mA |

[‡]All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

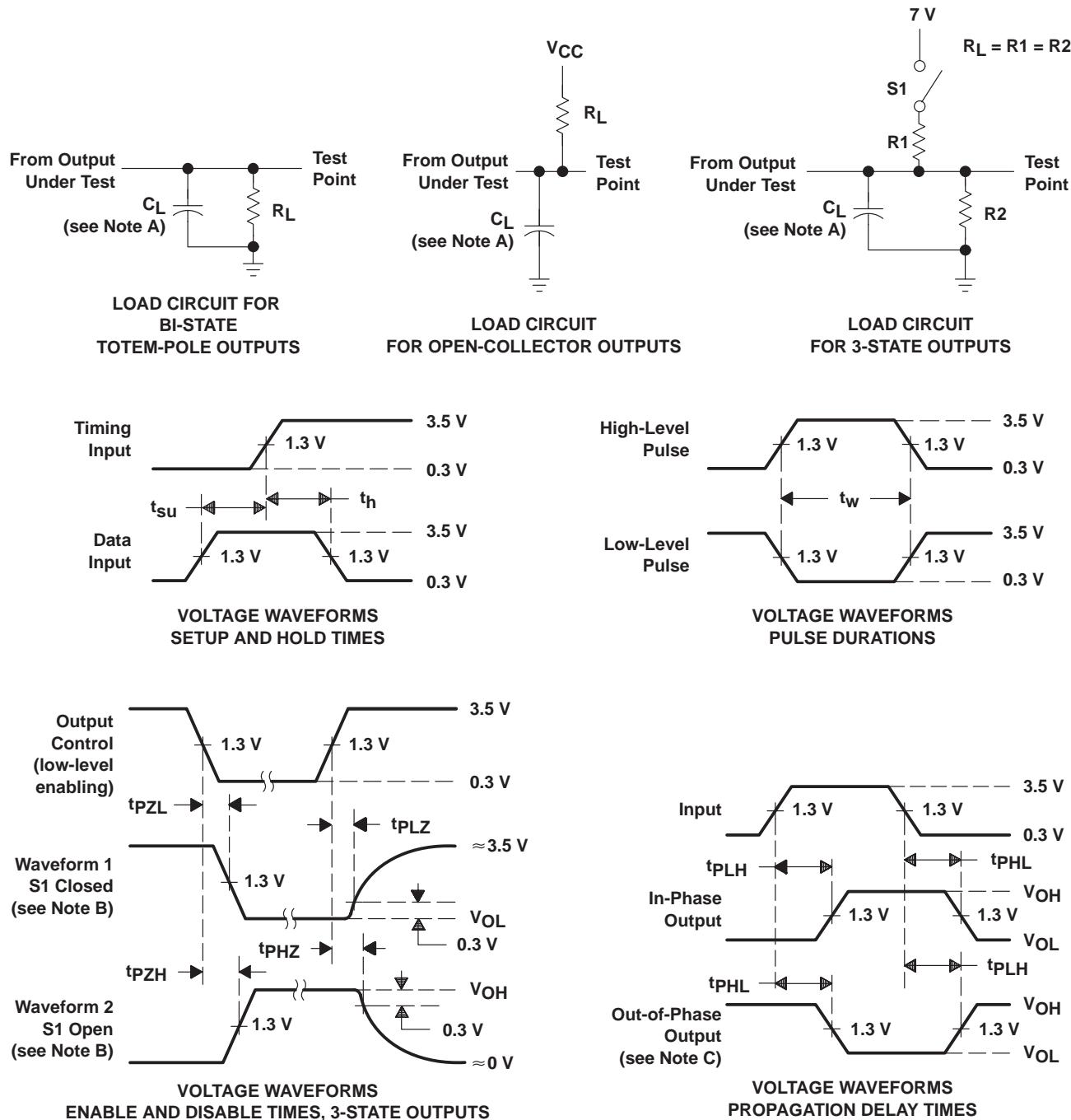
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 500\text{ }\Omega$, $T_A = \text{MIN to MAX}^{\dagger}$ | | | | UNIT | |
|-----------|-----------------|----------------|---|-----|-----|-----|------|--|
| | | | SN54AS32 | | | | | |
| | | | MIN | MAX | MIN | MAX | | |
| | | | 1 | 7.5 | 1 | 5.8 | | |
| t_{PLH} | A or B | Y | 1 | 6.5 | 1 | 5.8 | ns | |
| t_{PHL} | | | 1 | 6.5 | 1 | 5.8 | | |

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54ALS32, SN54AS32, SN74ALS32, SN74AS32 QUADRUPLE 2-INPUT POSITIVE-OR GATES

SDAS113B – APRIL 1982 – REVISED DECEMBER 1994

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|--------------------------------------|----------------------|--------------|------------------------------------|---|
| 5962-86836012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-86836012A SNJ54ALS 32FK | Samples |
| 5962-8683601DA | ACTIVE | CFP | W | 14 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8683601DA SNJ54ALS32W | Samples |
| 5962-9756001Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9756001Q2A SNJ54AS 32FK | Samples |
| 5962-9756001QCA | ACTIVE | CDIP | J | 14 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9756001QC A SNJ54AS32J | Samples |
| JM38510/37501B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 37501B2A | Samples |
| JM38510/37501BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 37501BCA | Samples |
| M38510/37501B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 37501B2A | Samples |
| M38510/37501BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 37501BCA | Samples |
| SN54ALS32J | ACTIVE | CDIP | J | 14 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | SN54ALS32J | Samples |
| SN54AS32J | ACTIVE | CDIP | J | 14 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | SN54AS32J | Samples |
| SN74ALS32D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS32 | Samples |
| SN74ALS32DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS32 | Samples |
| SN74ALS32DRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS32 | Samples |
| SN74ALS32N | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS32N | Samples |
| SN74ALS32NE4 | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS32N | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------------|--------------------------------------|----------------------|--------------|--|-------------------------|
| SN74ALS32NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS32 | Samples |
| SN74ALS32NSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS32 | Samples |
| SN74AS32D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS32 | Samples |
| SN74AS32DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS32 | Samples |
| SN74AS32N | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74AS32N | Samples |
| SN74AS32NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74AS32 | Samples |
| SNJ54ALS32FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 86836012A SNJ54ALS 32FK | Samples |
| SNJ54ALS32J | ACTIVE | CDIP | J | 14 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54ALS32J | Samples |
| SNJ54ALS32W | ACTIVE | CFP | W | 14 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8683601DA SNJ54ALS32W | Samples |
| SNJ54AS32FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 9756001Q2A SNJ54AS 32FK | Samples |
| SNJ54AS32J | ACTIVE | CDIP | J | 14 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9756001QC A SNJ54AS32J | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ALS32, SN54AS32, SN74ALS32, SN74AS32 :

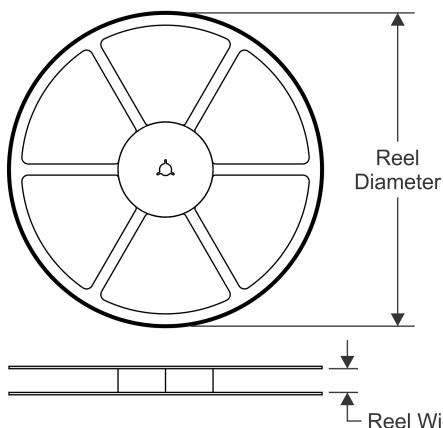
- Catalog: [SN74ALS32](#), [SN74AS32](#)
- Military: [SN54ALS32](#), [SN54AS32](#)

NOTE: Qualified Version Definitions:

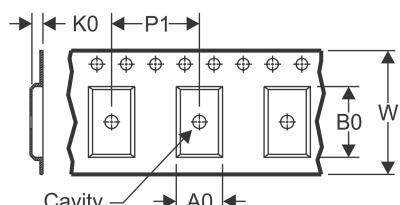
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

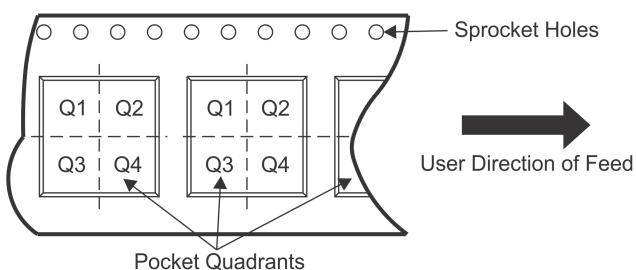


TAPE DIMENSIONS



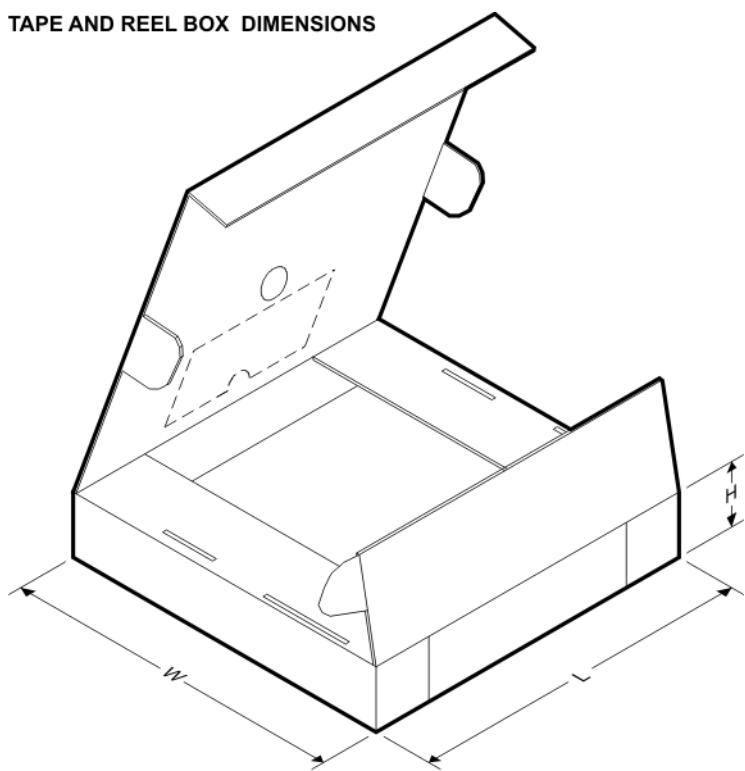
| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| All dimensions are nominal | | | | | | | | | | | | | |
|----------------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|--|
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant | |
| SN74ALS32DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 | |
| SN74ALS32NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 | |
| SN74AS32DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 | |
| SN74AS32NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 | |

TAPE AND REEL BOX DIMENSIONS


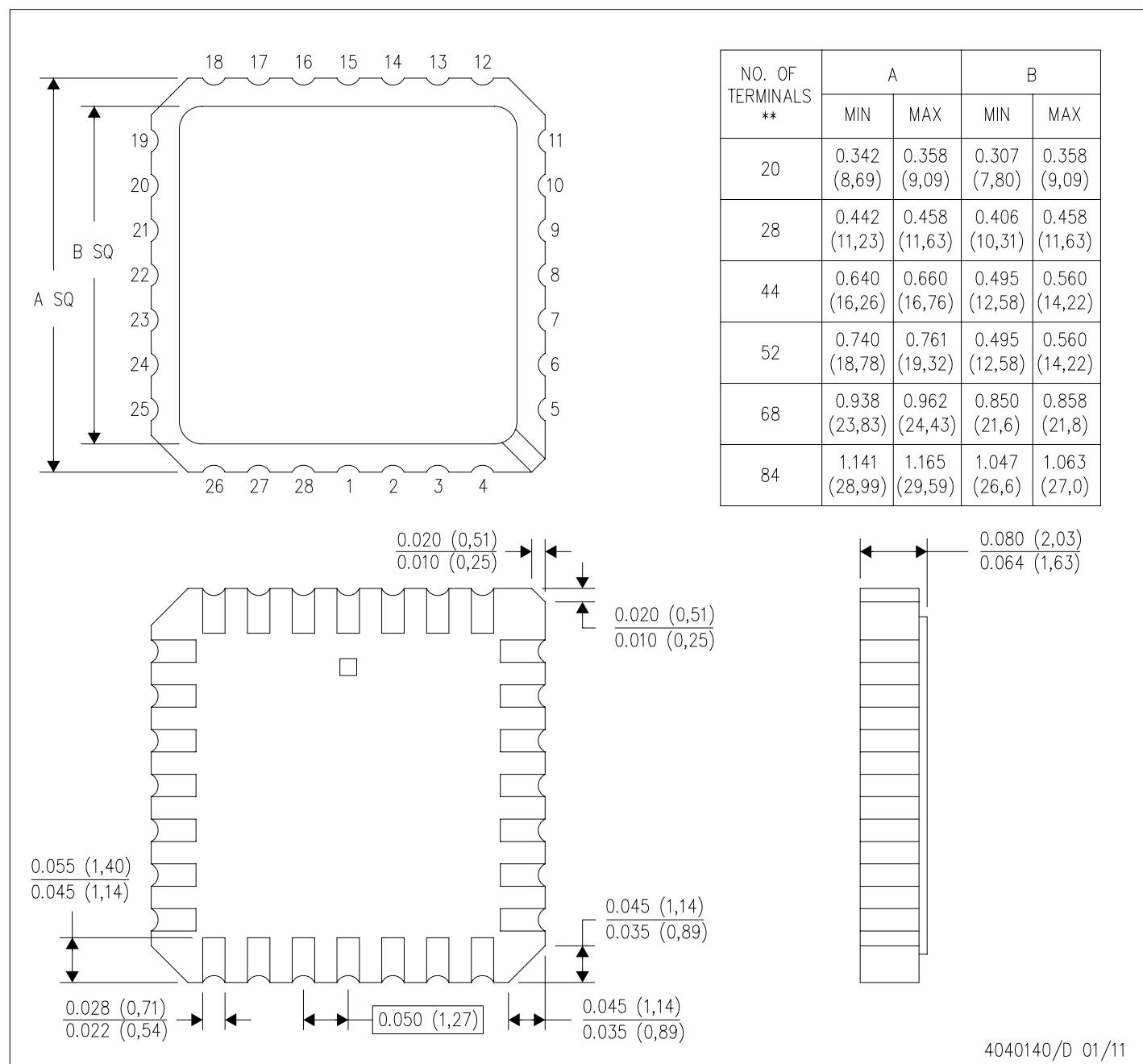
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALS32DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74ALS32NSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74AS32DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74AS32NSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. Falls within JEDEC MS-004

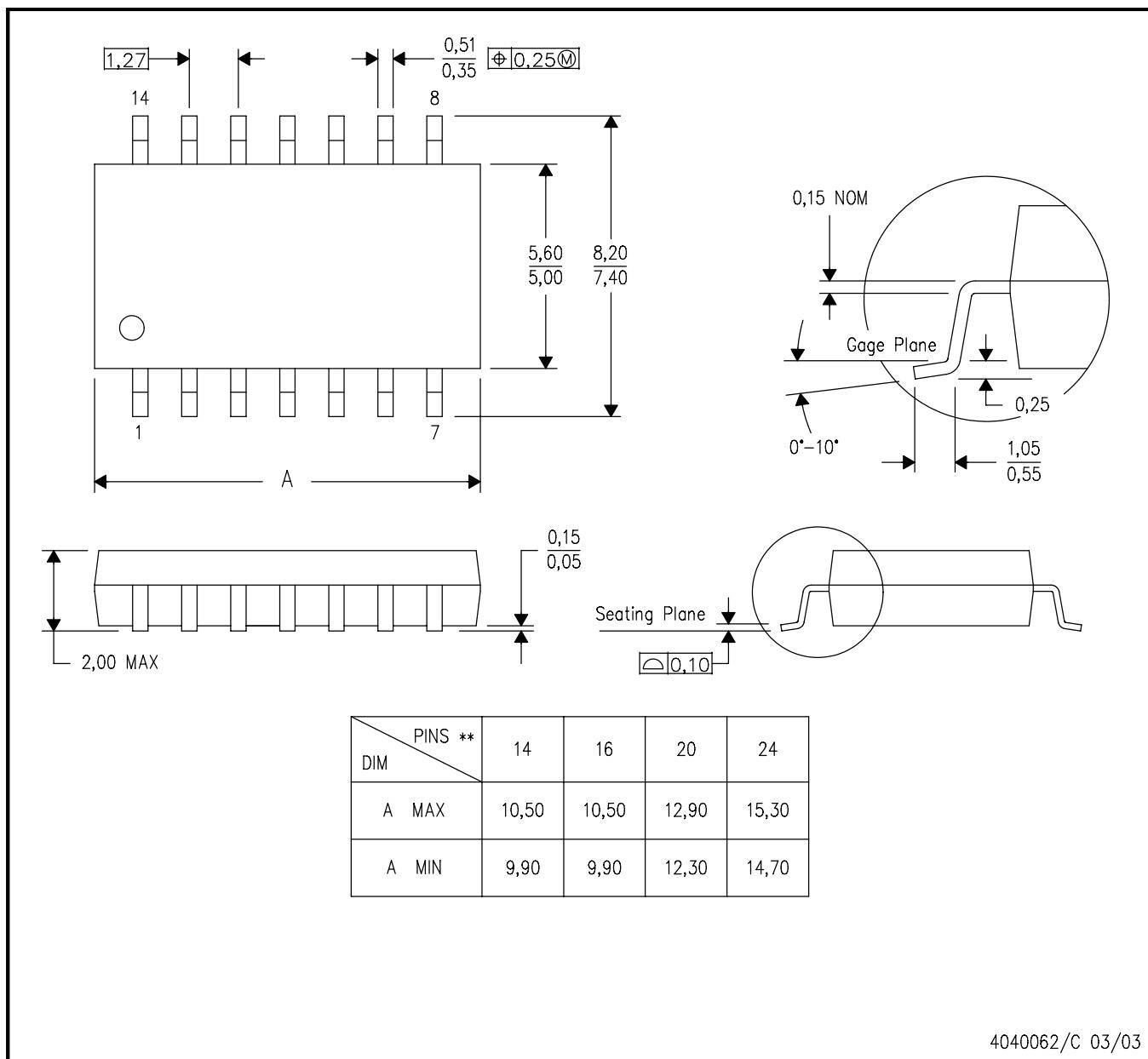
4040140/D 01/11

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

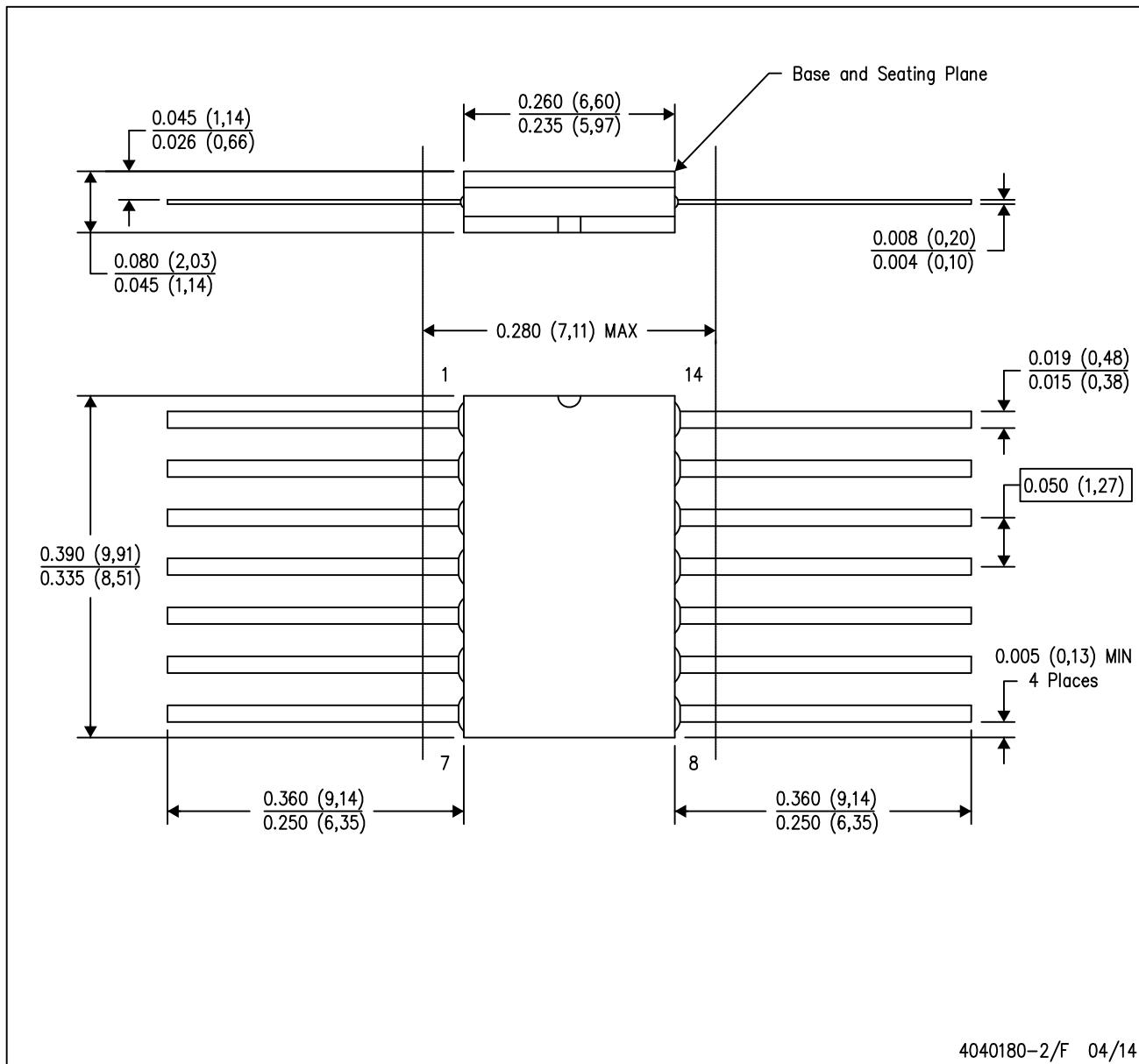


4040062/C 03/03

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



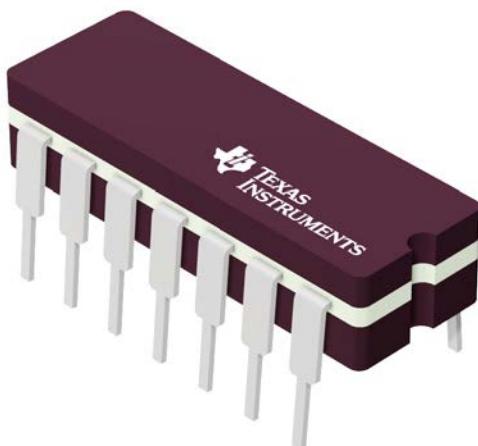
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL-STD 1835 GDFP1-F14

GENERIC PACKAGE VIEW

J 14

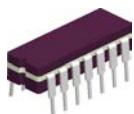
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

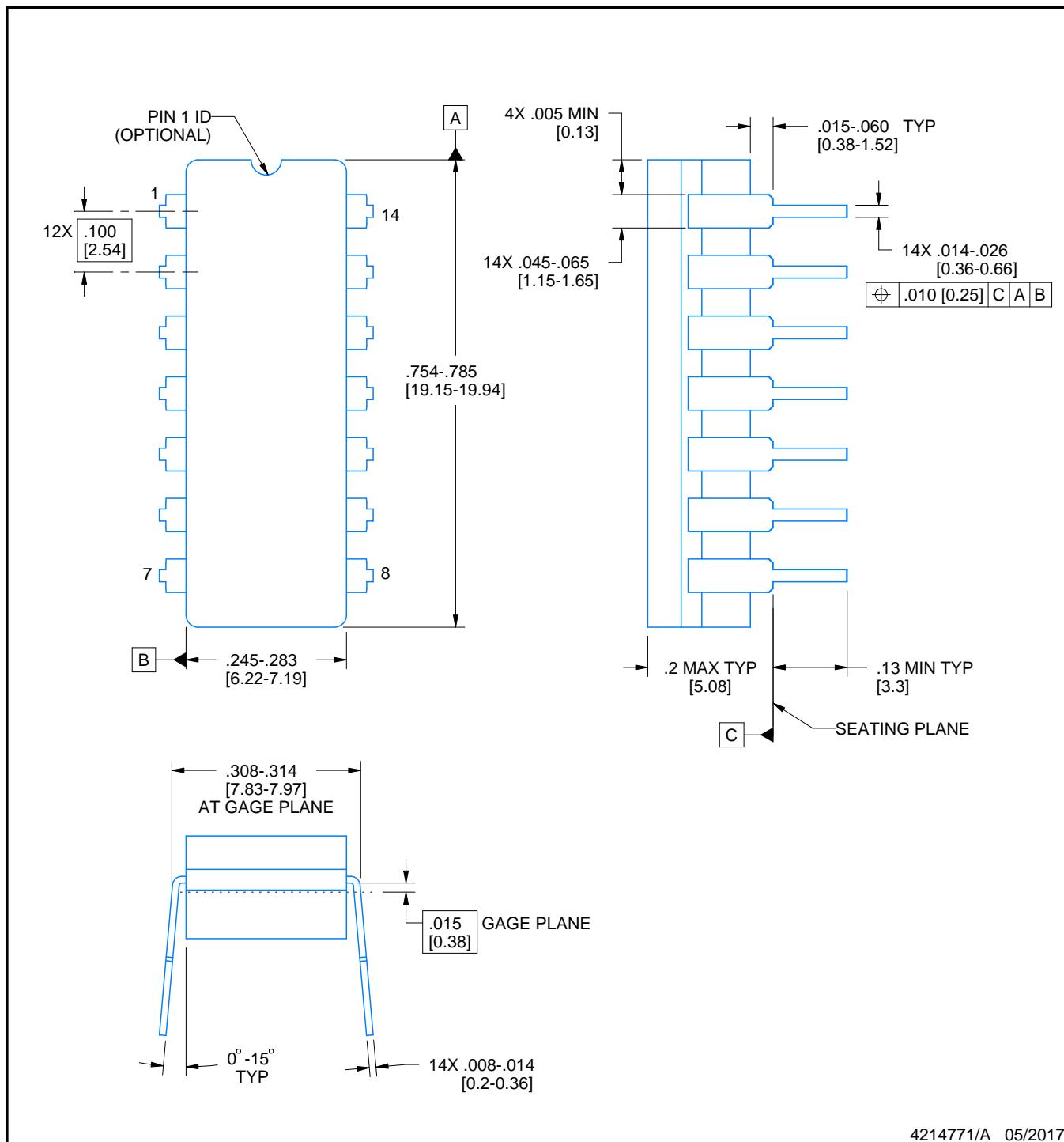


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

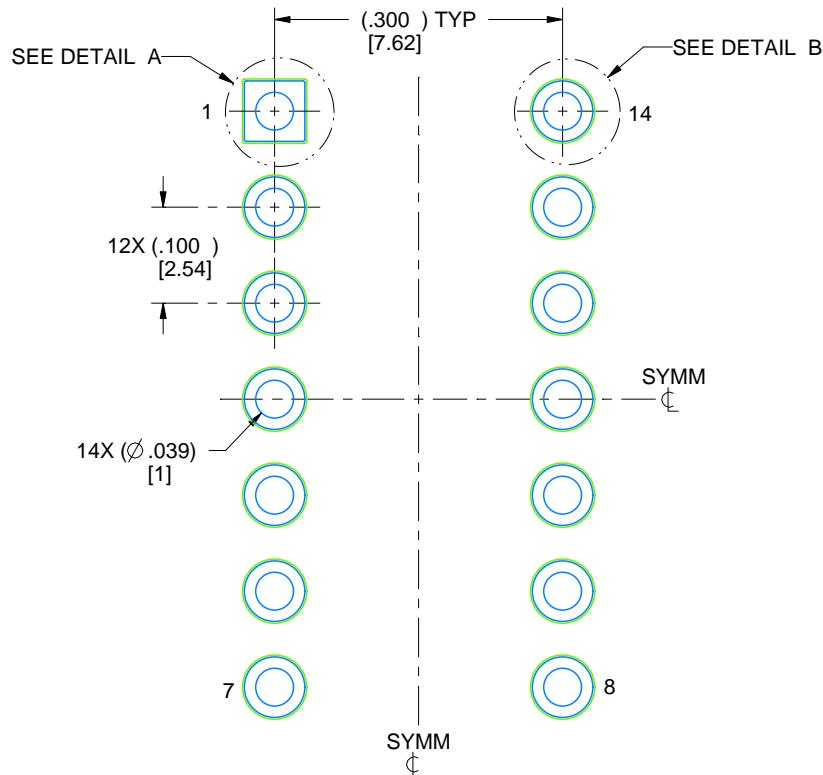
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

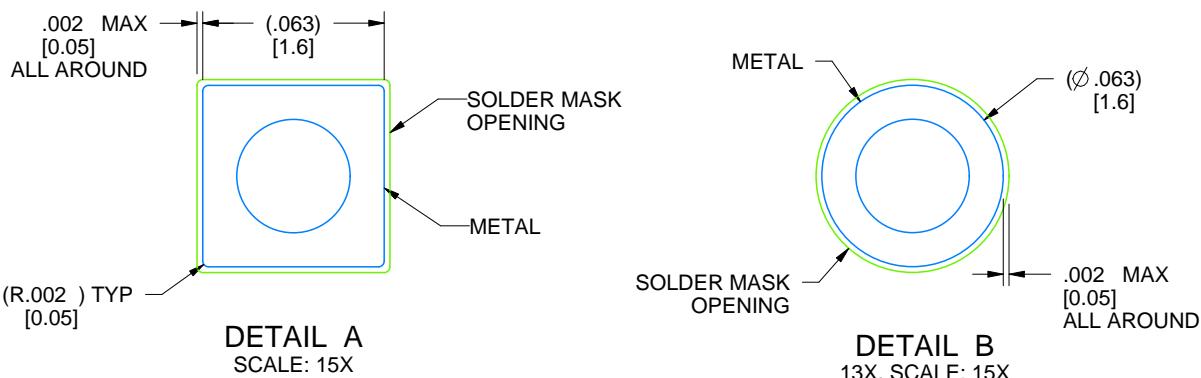
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



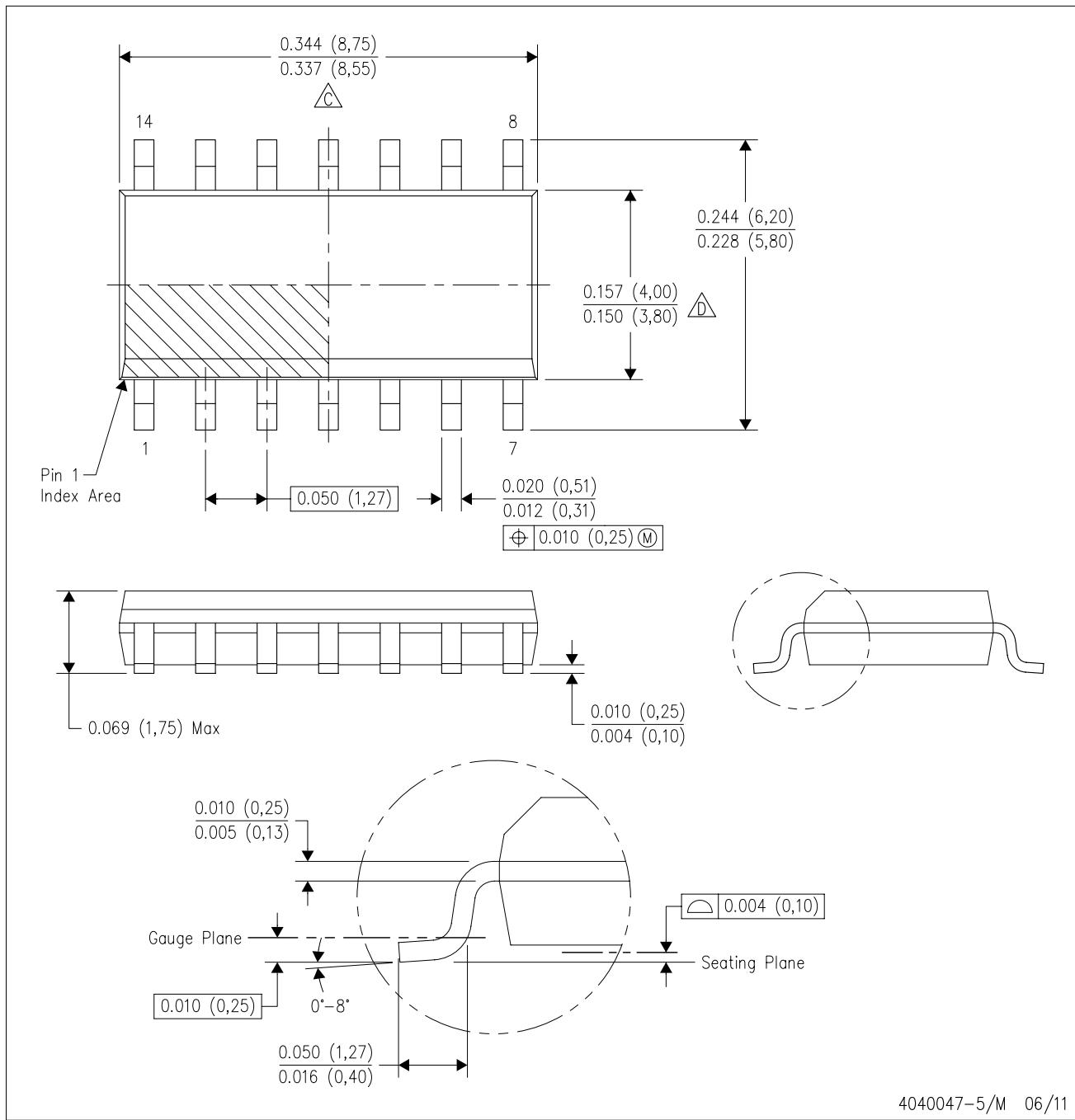
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

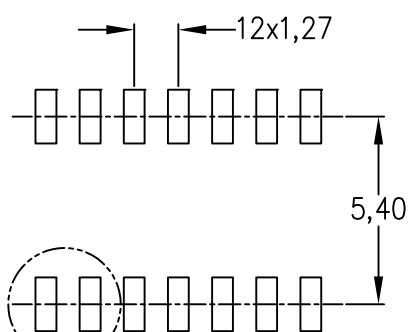
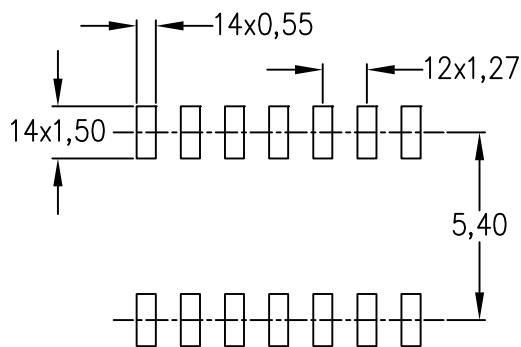
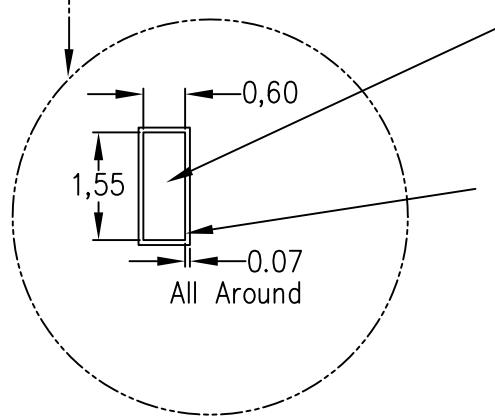
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

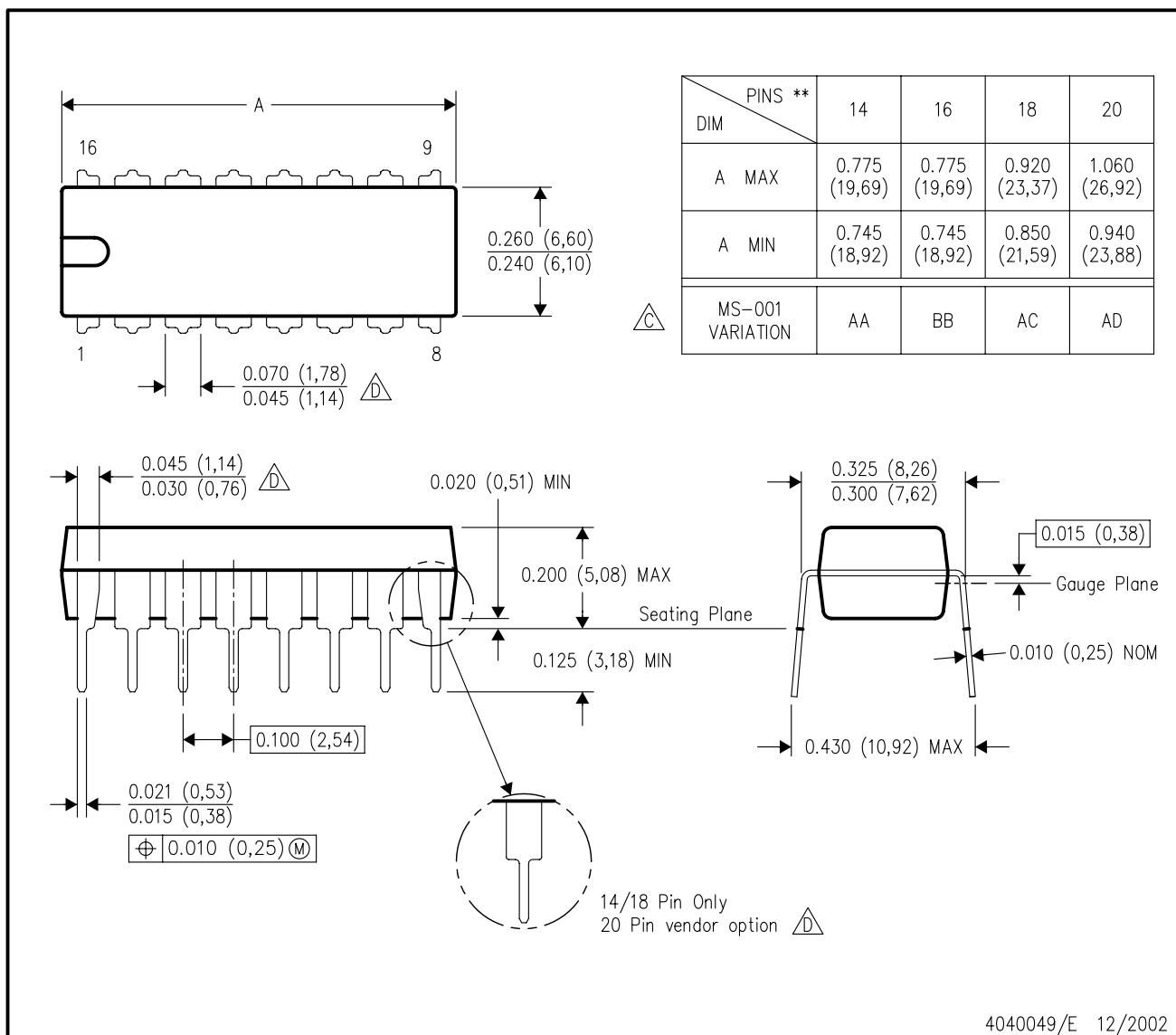
4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



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