CY39C604

PSR LED Driver IC for LED Lighting

Description

CY39C604 is a Primary Side Regulation (PSR) LED driver IC for LED lighting. Using the information of the primary peak current and the transformer-energy-zero time, it is able to deliver a well regulated current to the secondary side without using an opto-coupler in an isolated flyback topology. Operating in critical conduction mode, a smaller transformer is required. In addition, CY39C604 has a built-in dimmable circuit and can constitute the lighting system for PWM dimming.

It is most suitable for the general lighting applications, for example replacement of commercial and residential incandescent lamps.

Features

- PSR topology in an isolated flyback circuit
- High power factor (>0.9 : Not dimming) in Single Conversion
- High efficiency (>85% : Not dimming) and low EMI by detecting transformer zero energy
- PWM Dimmable LED lighting
- Highly reliable protection functions
  - Under voltage lock out (UVLO)
  - Over voltage protection (OVP)
  - Over current protection (OCP)
  - Short circuit protection (SCP)
  - Over temperature protection (OTP)
- Switching frequency setting : 30 kHz to 133 kHz
- Input voltage range VDD : 9V to 20V
- Input voltage for LED lighting applications : $AC110V_{RMS}$, $AC230V_{RMS}$
- Output power range for LED lighting applications : 5W to 50W
- Small Package : SOP-8 (3.9 mm × 5.05 mm × 1.75 mm[Max])

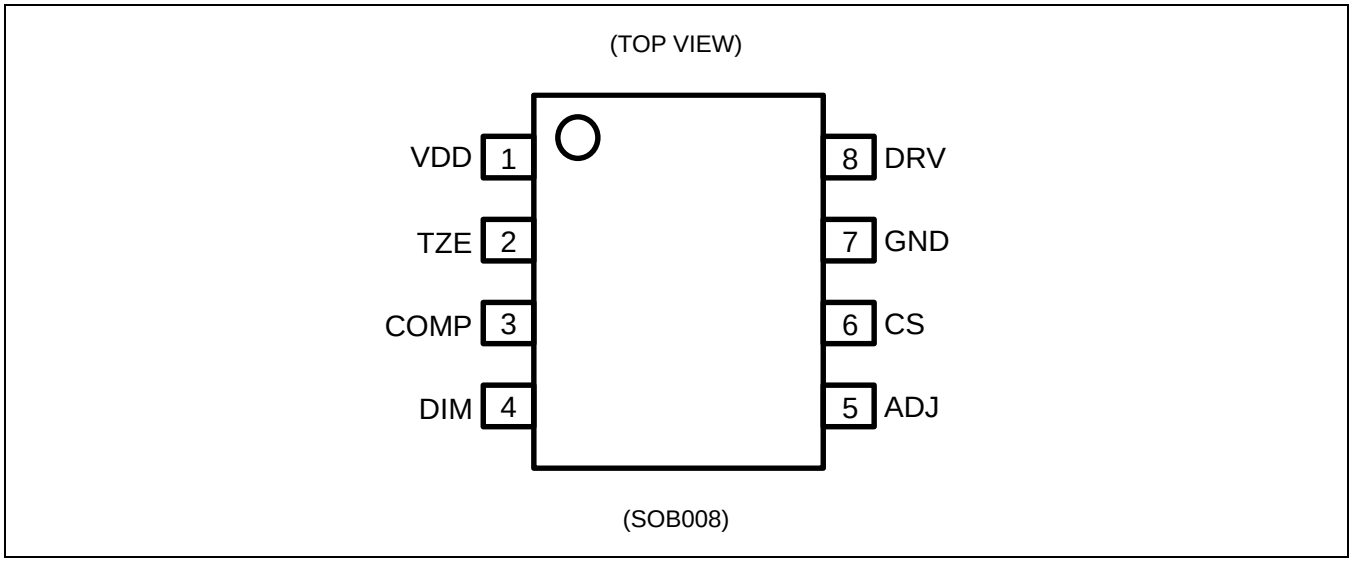
Applications

- LED lighting
- PWM dimmable LED lighting

Contents

1. Pin Assignment

Figure 1. Pin Assignment



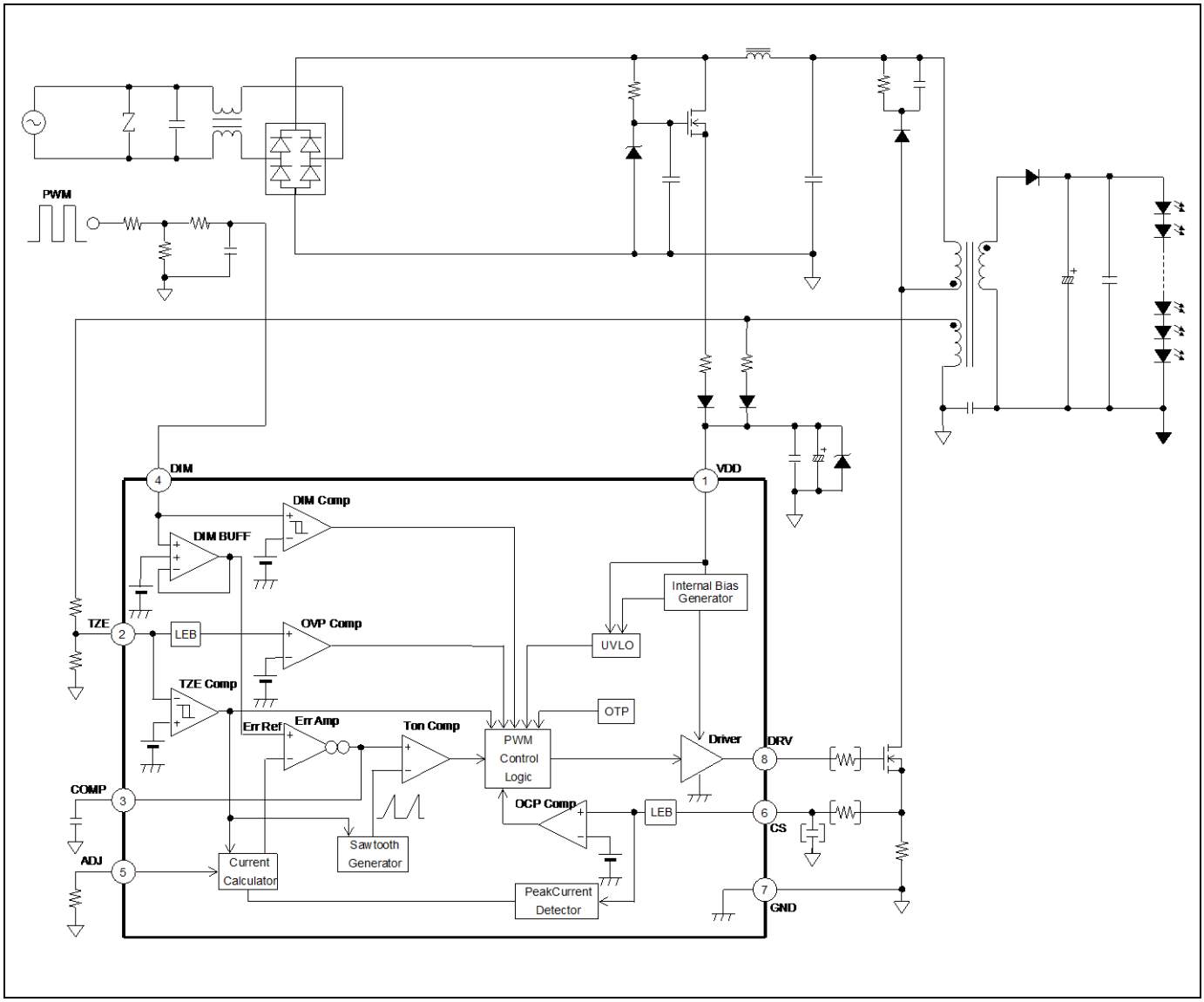
2. Pin Descriptions

Table 1. Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	VDD	-	Power supply pin.
2	TZE	I	Transformer Zero Energy detecting pin.
3	COMP	O	External Capacitor connection pin for the compensation.
4	DIM	I	Dimming control pin.
5	ADJ	O	Pin for adjusting the switch-on timing.
6	CS	I	Pin for detecting peak current of transformer primary winding.
7	GND	-	Ground pin.
8	DRV	O	External MOSFET gate connection pin.

3. Block Diagram

Figure 2. Block Diagram (Isolated Flyback Application)



4. Absolute Maximum Ratings

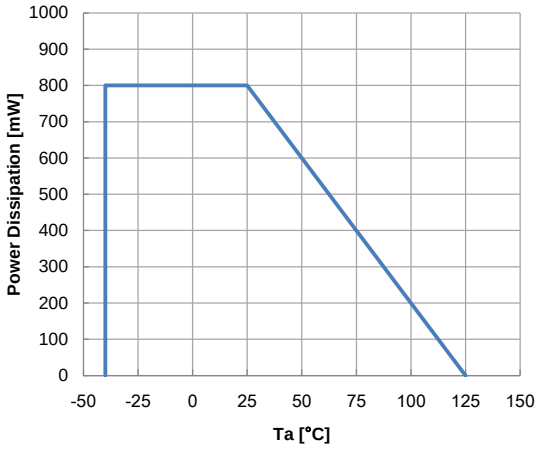
Table 2. Absolute Maximum Rating

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power Supply Voltage	V_{VDD}	VDD pin	-0.3	+25	V
Input Voltage	V_{CS}	CS pin	-0.3	+6.0	V
	V_{TZE}	TZE pin	-0.3	+6.0	V
	V_{DIM}	DIM pin	-0.3	+6.0	V
Output Voltage	V_{DRV}	DRV pin	-0.3	+25	V
Output Current	I_{ADJ}	ADJ pin	-1	-	mA
	I_{DRV}	DRV pin DC level	-50	+50	mA
Power Dissipation	P_D	Ta ≤ +25°C	-	800 (*1)	mW
Storage temperature	T_{STG}	-	-55	+125	°C
ESD Voltage 1	V_{ESDH}	Human Body Model	-2000	+2000	V
ESD Voltage 2	V_{ESDC}	Charged Device Model	-1000	+1000	V

*1: The value when using two layers PCB.

Reference: θja (wind speed 0m/s): 125°C/W

Figure 3. Power Dissipation



WARNING:

1. Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

5. Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
VDD pin Input Voltage	VDD	VDD pin	9	-	20	V
DIM pin Input Voltage	V_{DIM}	DIM pin After UVLO release	0	-	5	V
DIM pin Input Current	I_{DIM}	DIM pin Before UVLO release	0	-	2.5	µA
TZE pin Resistance	R_{TZE}	TZE pin	50	-	200	kΩ
ADJ pin Resistance	R_{ADJ}	ADJ pin	9.3	-	185.5	kΩ
COMP pin Capacitance	C_{COMP}	COMP pin	-	4.7	-	µF
VDD pin Capacitance	C_{BP}	Set between VDD pin and GND pin	-	100	-	µF
Operating Junction Temperature	Tj	-	-40	-	+125	°C

WARNING:

1. The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.
2. Any use of semiconductor devices will be under their recommended operating condition.
3. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
4. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

6. Electrical Characteristics

Table 4. Electrical Characteristics

(Ta = +25°C, V_{VDD} = 12V)

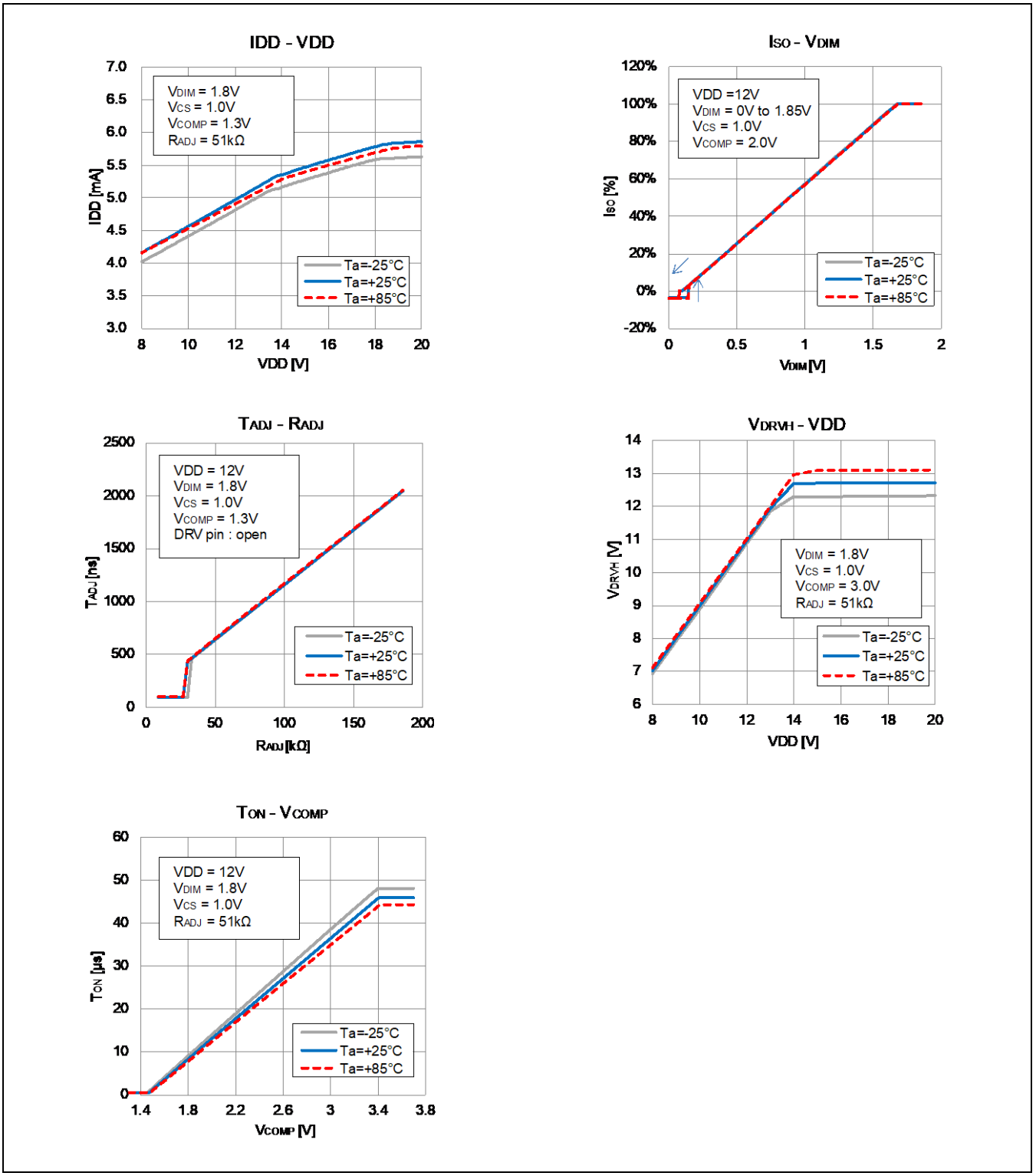
Parameter		Symbol	Pin	Condition	Value			Unit
					Min	Typ	Max	
UVLO	UVLO Turn-on threshold voltage	V_{TH}	VDD	-	12.25	13	13.75	V
	UVLO Turn-off threshold voltage	V_{TL}	VDD	-	7.55	7.9	8.5	V
	Startup current	I_{START}	VDD	V_{VDD} = 7V	-	65	160	µA
TRANSFORMER ZERO ENERGY DETECTION	Zero energy threshold voltage	V_{TZETL}	TZE	TZE = "H" to "L"	-	20	-	mV
	Zero energy threshold voltage	V_{TZETH}	TZE	TZE = "L" to "H"	0.6	0.7	0.8	V
	TZE clamp voltage	$V_{TZECLAMP}$	TZE	I_{TZE} = -10 µA	-200	-160	-100	mV
	OVP threshold voltage	V_{TZEOVP}	TZE	-	4.15	4.3	4.45	V
	OVP blanking time	$t_{OVPBLANK}$	TZE	-	0.6	1	1.7	µs
	TZE input current	I_{TZE}	TZE	V_{TZE} = 5V	-1	-	+1	µA
COMPENSATION	Source current	I_{SO}	COMP	V_{COMP} = 2V, V_{CS} = 0V V_{DIM} = 1.85V	-	-27	-	µA
	Trans conductance	gm	COMP	V_{COMP} = 2.5V, V_{CS} = 1V	-	96	-	µA/V
ADJUSTMENT	ADJ voltage	V_{ADJ}	ADJ	-	1.81	1.85	1.89	V
	ADJ source current	I_{ADJ}	ADJ	V_{ADJ} = 0V	-650	-450	-250	µA
	ADJ time	T_{ADJ}	TZE DRV	T_{ADJ} (R_{ADJ} = 51 kΩ) - T_{ADJ} (R_{ADJ} = 9.1 kΩ)	490	550	610	ns
	Minimum switching period	T_{SW}	TZE DRV	-	6.75	7.5	8.25	µs
CURRENT SENSE	OCP threshold voltage	V_{OCPTH}	CS	-	1.9	2	2.1	V
	OCP delay time	t_{OCPDLY}	CS	-	-	400	500	ns
	CS input current	I_{CS}	CS	V_{CS} = 5V	-1	-	+1	µA

(Ta = +25°C, V_{VDD} = 12V)

Parameter		Symbol	Pin	Condition	Value			Unit
					Min	Typ	Max	
DRV	DRV high voltage	V_{DRVH}	DRV	VDD = 18V, I_{DRV} = -30 mA	7.6	9.4	-	V
	DRV low voltage	V_{DRVL}	DRV	VDD = 18V, I_{DRV} = 30 mA	-	130	260	mV
	Rise time	t_{RISE}	DRV	VDD = 18V, CLOAD = 1 nF	-	94	-	ns
	Fall time	t_{FALL}	DRV	VDD = 18V, CLOAD = 1 nF	-	16	-	ns
	Minimum on time	t_{ONMIN}	DRV	TZE trigger	300	500	700	ns
	Maximum on time	t_{ONMAX}	DRV	-	27	44	60	µs
	Minimum off time	t_{OFFMIN}	DRV	-	1	1.5	1.93	µs
	Maximum off time	t_{OFFMAX}	DRV	TZE = GND	270	320	370	µs
OTP	OTP threshold	T_{OTP}	-	Tj, temperature rising	-	150	-	°C
	OTP hysteresis	T_{OTPHYS}	-	Tj, temperature falling, degrees below T_{OTP}	-	25	-	°C
DIMMING	DIM input current	I_{DIM}	DIM	V_{DIM} = 5V	-0.1	-	+0.1	µA
	DIMCMP threshold voltage	$V_{DIMCMPVTH}$	DIM	-	135	150	165	mV
	DIMCMP hysteresis	$V_{DIMCMPHYS}$	DIM	-	-	70	-	mV
POWER SUPPLY CURRENT	Power supply current	$I_{VDD(STATIC)}$	VDD	V_{VDD} = 20V, V_{TZE} = 1V	-	3	3.6	mA
		$I_{VDD(OPERATING)}$	VDD	V_{VDD} = 20V, Qg = 20 nC, f_{SW} = 133 kHz	-	5.6	-	mA

7. Standard Characteristics

Figure 4. Standard Characteristics



8. Function Explanations

8.1 LED Current Control by PSR (Primary Side Regulation)

CY39C604 regulates the average LED current (I_{LED}) by feeding back the information based on Primary Winding peak current (I_{P_PEAK}) and Secondary Winding energy discharge time (T_{DIS}) and switching period (T_{SW}). Figure 5 shows the operating waveform in steady state. I_P is Primary Winding current and I_S is Secondary Winding current. I_{LED} as an average current of the Secondary Winding is described by the following equation.

$$I_{LED} = \frac{1}{2} \times I_{S\_PEAK} \times \frac{T_{DIS}}{T_{SW}}$$

Using I_{P_PEAK} and the transformer Secondary to Primary turns ratio (N_P/N_S), Secondary Winding peak current (I_{S_PEAK}) is described by the following equation.

$$I_{S\_PEAK} = \frac{N_P}{N_S} \times I_{P\_PEAK}$$

Therefore,

$$I_{LED} = \frac{1}{2} \times \frac{N_P}{N_S} \times I_{P\_PEAK} \times \frac{T_{DIS}}{T_{SW}}$$

CY39C604 detects T_{DIS} by monitoring the TZE pin and I_{P_PEAK} by monitoring the CS pin and then controls I_{LED}. An internal Err Amp sinks gm current proportional to I_{P_PEAK} from the COMP pin during T_{DIS} period. In steady state, since the average of the gm current is equal to internal reference current (I_{SO}), the voltage on the COMP pin (V_{COMP}) is nearly constant.

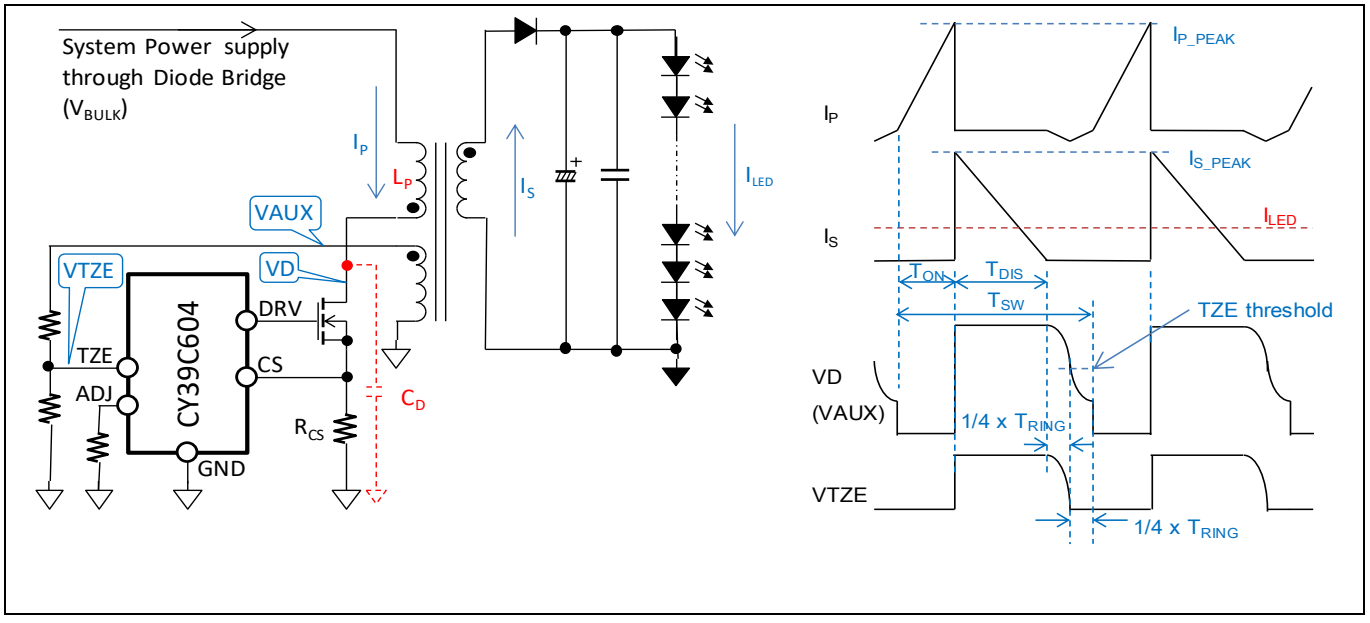
$$I_{P\_PEAK} \times R_{CS} \times gm \times T_{DIS} = I_{SO} \times T_{SW}$$

In above equation, gm is transconductance of the Err Amp and R_{CS} is a sense resistance.

Eventually, I_{LED} can be calculated by the following equation.

$$I_{LED} = \frac{1}{2} \times \frac{N_P}{N_S} \times \frac{I_{SO}}{gm} \times \frac{1}{R_{CS}}$$

Figure 5. LED Current Control Waveform



8.2 PFC (Power Factor Correction) Function

Switching on time (T_{ON}) is generated by comparing V_{COMP} with an internal sawtooth waveform (refer to Figure 2). Since V_{COMP} is slow varying with connecting an external capacitor (C_{COMP}) from the COMP pin to the GND pin, T_{ON} is nearly constant within an AC line cycle. In this state, I_{P_PEAK} is nearly proportional to the AC Line voltage (V_{BULK}). It can bring the phase differences between the input voltage and the input current close to zero, so that high Power Factor can be achieved.

8.3 Dimming Function

CY39C604 has the built-in dimmable circuit to control I_{LED} by changing a reference of Err Amp based on the input voltage level on the DIM pin (V_{DIM}), and realizes dimming. Figure 6 shows I_{LED} dimming ratio based on V_{DIM}.

Figure 7 shows the input circuit to the DIM pin for PWM dimming. PWM signal is divided and filtered into an analog voltage with RC network. It is possible to configurate PWM dimmable system by inputting the voltage to the DIM pin.

Figure 6. Dimming Curve

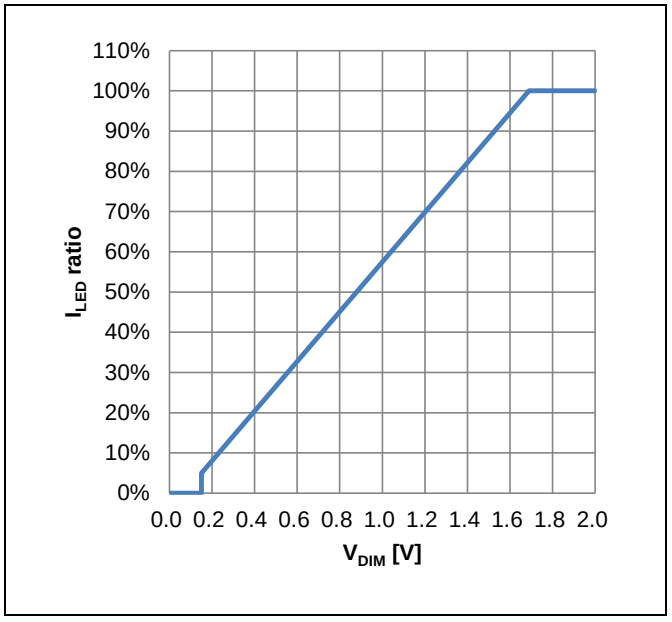
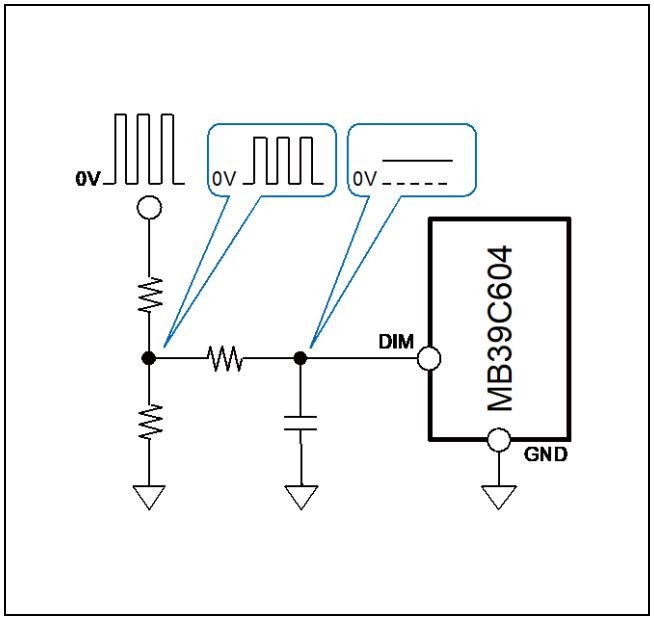


Figure 7. DIM Pin Input Circuit



8.4 Power-On Sequence

When the AC line voltage is supplied, V_{BULK} is powered from the AC line through a diode bridge, and the VDD pin is charged from V_{BULK} through an external source-follower BiasMOS.(Figure 8 red path)

When the VDD pin is charged up and the voltage on the VDD pin (V_{VDD}) rises above the UVLO threshold voltage, an internal Bias circuit starts operating, and CY39C604 starts the dimming control. After the UVLO is released, this device enables switching and is operating in a forced switching mode (T_{ON} = 1.5 µs, T_{OFF} = 78 µs to 320 µs). When the voltage on the TZE pin reaches the Zero energy threshold voltage (V_{TZETH} = 0.7V), CY39C604 enters normal operation mode. After the switching begins, the VDD pin is also charged from Auxiliary Winding through an external diode (DBIAS).(Figure 8 blue path)

Around zero cross points of the AC line voltage V_{VDD} is not supplied from V_{BULK} or Auxiliary Winding. It is necessary to set an appropriate capacitor of the VDD pin in order to keep V_{VDD} above the UVLO threshold voltage in this period. An external diode (D1) between BiasMOS and the VDD pin is used to prevent discharge from the VDD pin to V_{BULK} at the zero cross points.

Figure 8. VDD Supply Path at Power-On

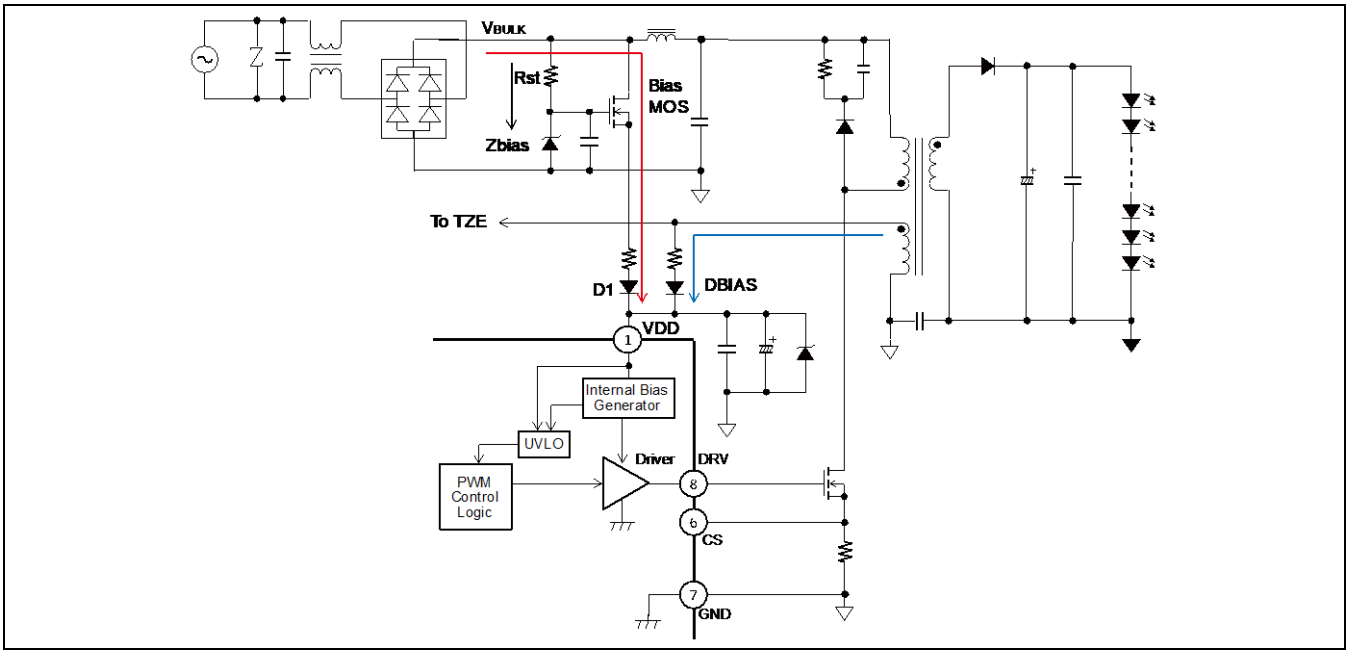
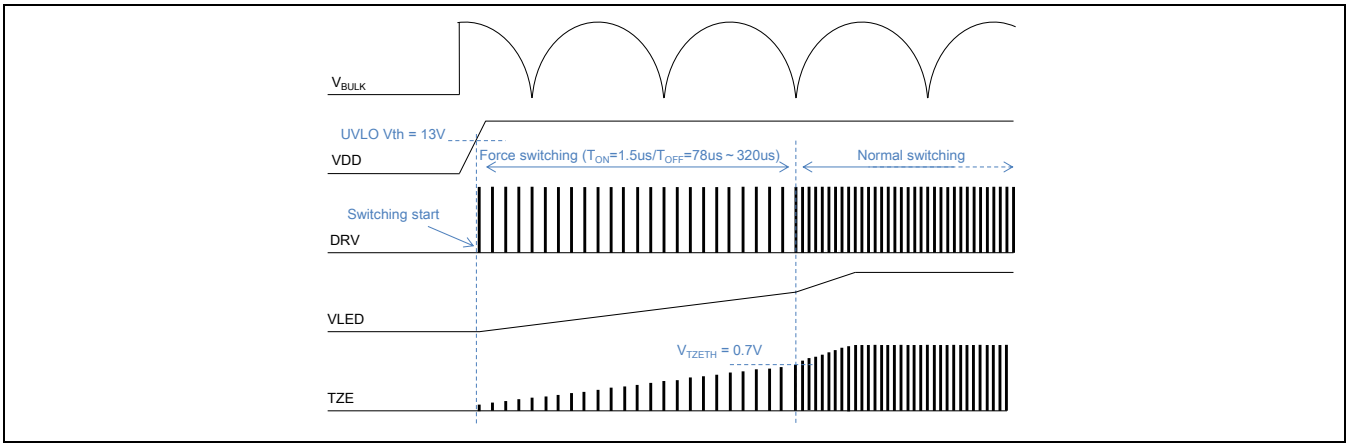


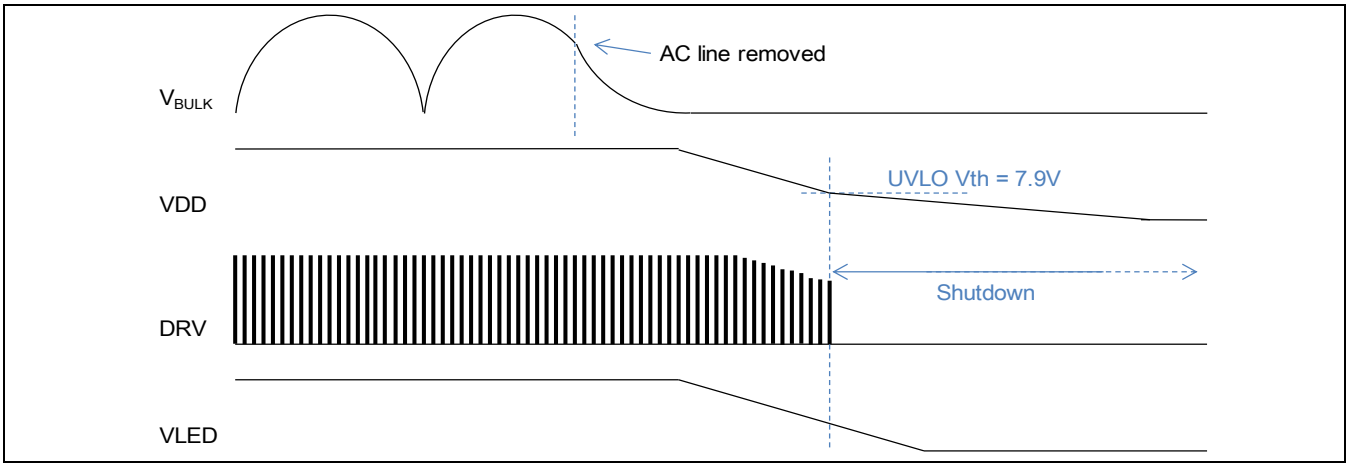
Figure 9. Power-On Waveform



8.5 Power-Off Sequence

After the AC line voltage is removed, V_{BULK} is discharged by switching operation. Since any Secondary Winding current does not flow, I_{LED} is supplied only from output capacitors and decreases gradually. V_{VDD} also decreases because there is no current supply from both Auxiliary Winding and V_{BULK}. When V_{VDD} falls below the UVLO threshold voltage, CY39C604 shuts down.

Figure 10. Power-Off Waveform



8.6 I_{P_PEAK} Detection Function

CY39C604 detects Primary Winding peak current (I_{P_PEAK}) of Transformer. I_{LED} is set by connecting a sense resistance (Rcs) between the CS pin and the GND pin. Maximum I_{P_PEAK} ($I_{P\_PEAKMAX}$) limited by Over Current Protection (OCP) can also be set with the resistance.

Using the Secondary to Primary turns ratio (N_P/N_S) and I_{LED}, R_{CS} is set as the following equation (refer to 8.1)

$$R_{CS} = \frac{N_P}{N_S} \times \frac{0.14}{I_{LED}}$$

In addition, using the OCP threshold voltage (V_{OCPTH}) and R_{CS}, $I_{P\_PEAKMAX}$ is calculated with the following equation.

$$I_{P\_PEAKMAX} = \frac{V_{OCPTH}}{R_{CS}}$$

8.7 Zero Voltage Switching Function

CY39C604 has built-in zero voltage switching function to minimize switching loss of the external switching MOSFET. This device detects a zero crossing point through a resistor divider connected from the TZE pin to Auxiliary Winding. A zero energy detection circuit detects a negative crossing point of the voltage on the TZE pin to Zero energy threshold voltage (V_{TZETL}). On-timing of switching MOSFET is decided with waiting an adjustment time (t_{ADJ}) after the negative crossing occurs.

t_{ADJ} is set by connecting an external resistance (R_{ADJ}) between the ADJ pin and the GND pin. Using Primary Winding inductance (L_P) and the parasitic drain capacitor of switching MOSFET (C_D), t_{ADJ} is calculated with the following equation.

$$t_{ADJ} = \frac{\pi\sqrt{L_P \times C_D}}{2}$$

Using t_{ADJ}, R_{ADJ} is set as the following equation.

$$R_{ADJ}\ [k\Omega] = 0.0927 \times t_{ADJ}\ [ns]$$

8.8 Protection Functions

Under Voltage Lockout Protection (UVLO)

The under voltage lockout protection (UVLO) prevents IC from a malfunction in the transient state during V_{VDD} startup and a malfunction caused by a momentary drop of V_{VDD}, and protects the system from destruction/deterioration. An UVLO comparator detects the voltage decrease below the UVLO threshold voltage on the VDD pin, and then the DRV pin is turned to “L” and the switching stops. CY39C604 automatically returns to normal operation mode when V_{VDD} increases above the UVLO threshold voltage.

Over Voltage Protection (OVP)

The over voltage protection (OVP) protects Secondary side components from an excessive voltage stress. If the LED is disconnected, the output voltage of Secondary Winding rises up. The output overvoltage can be detected by monitoring the TZE pin. During Secondary Winding energy discharge time, V_{TZE} is proportional to V_{AUX} and the voltage of Secondary Winding (refer to 8.1). When V_{TZE} rises higher than the OVP threshold voltage for 3 continues switching cycles, the DRV pin is turned to “L”, and the switching stops (latch off). When V_{VDD} drops below the UVLO threshold voltage, the latch is removed.

Over Current Protection (OCP)

The over current protection (OCP) prevents inductor or transformer from saturation. The drain current of the external switching MOSFET is limited by OCP. When the voltage on the CS pin reaches the OCP threshold voltage, the DRV pin is turned to “L” and the switching cycle ends. After zero crossing is detected on the TZE pin again, the DRV pin is turned to “H” and the next switching cycle begins.

Short Circuit Protection (SCP)

The short circuit protection (SCP) protects the transformer and the Secondary side diode from an excessive current stress. When the short circuit between LED terminals occurs, the output voltage decreases. If the voltage on the TZE pin falls below SCP threshold voltage, V_{COMP} is discharged and fixed at 1.5V and then the switching enters a low frequency mode.(T_{ON} = 1.5 µs /T_{OFF} = 78 µs to 320 µs)

Over Temperature Protection (OTP)

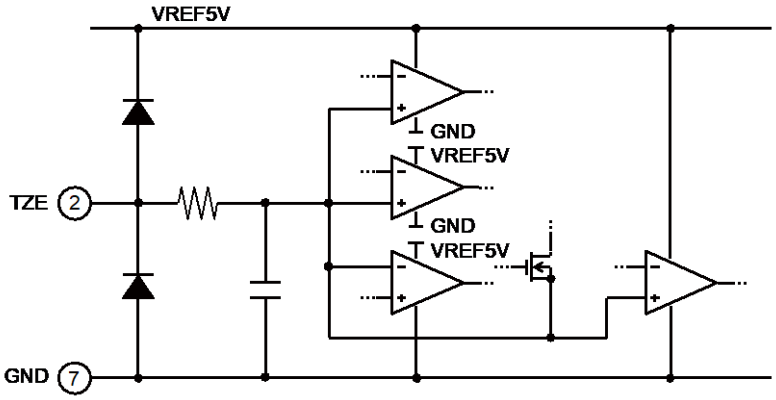
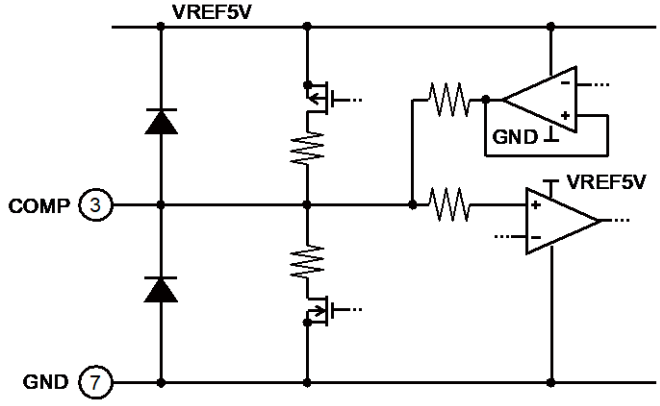
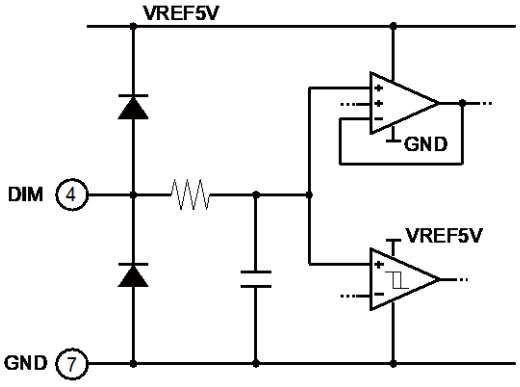
The over temperature protection (OTP) protects IC from thermal destruction. When the junction temperature reaches +150°C, the DRV pin is turned to “L”, and the switching stops. It automatically returns to normal operation mode if the junction temperature falls back below +125°C.

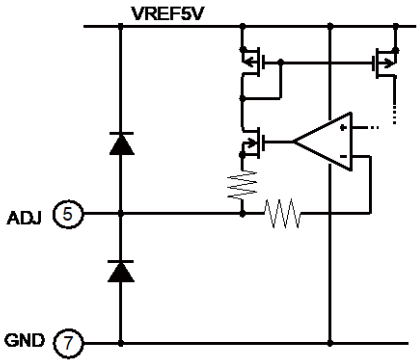
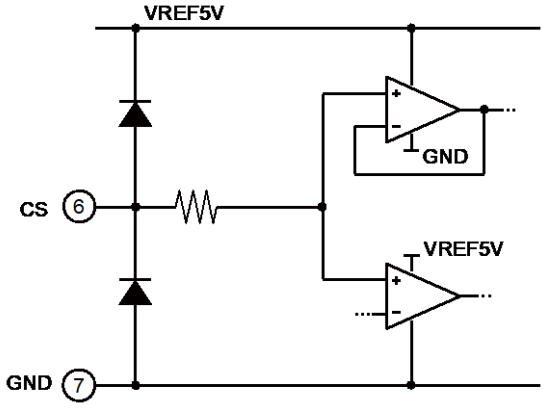
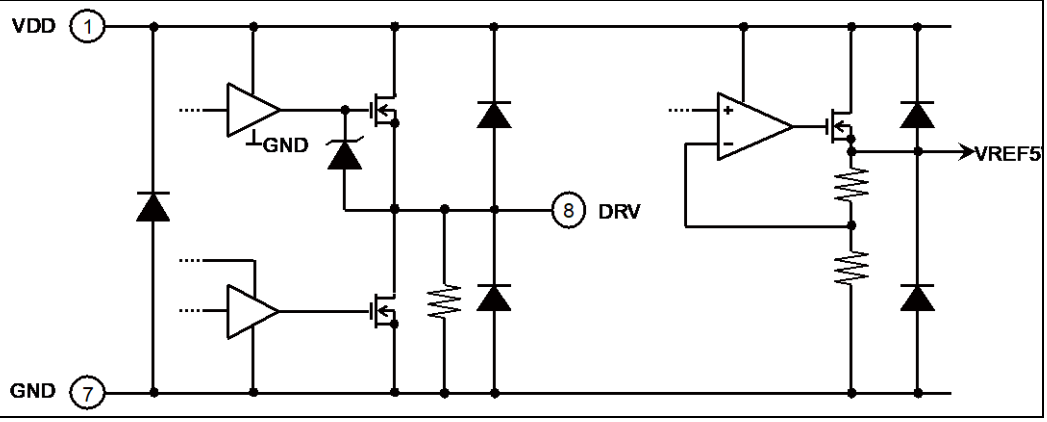
Table 5. Protection Functions Table

Function	PIN Operation			Detection Condition	Return Condition	Remarks
	DRV	COMP	ADJ			
Normal Operation	Active	Active	Active	-	-	-
Under Voltage Lockout Protection (UVLO)	L	L	L	VDD < 7.9V	VDD > 13V	Auto Restart
Over Voltage Protection (OVP)	L	1.5V fixed	Active	TZE > 4.3V	VDD < 7.9V → VDD > 13V	Latch off
Over Current Protection (OCP)	L	Active	Active	CS > 2V	Cycle by cycle	Auto Restart
Short Circuit Protection (SCP)	Active	1.5V fixed	Active	TZE (peak) < 0.7V	TZE (peak) > 0.7V	Auto Restart
Over Temperature Protection (OTP)	L	1.5V fixed	Active	Tj > +150°C	Tj < +125°C	Auto Restart

9. I/O Pin Equivalent Circuit Diagram

Figure 11. I/O Pin Equivalent Circuit Diagram

Pin No.	Pin Name	Equivalent Circuit Diagram
2	TZE	
3	COMP	
4	DIM	

Pin No.	Pin Name	Equivalent Circuit Diagram
5	ADJ	
6	CS	
8	DRV	

10. Application Examples

10.1 50W Isolated and PWM Dimming Application

Input: AC85V$_{RMS}$ to 265V$_{RMS}$, Output: 1.5A/27V to 36V

Figure 12. 50W EVB Schematic

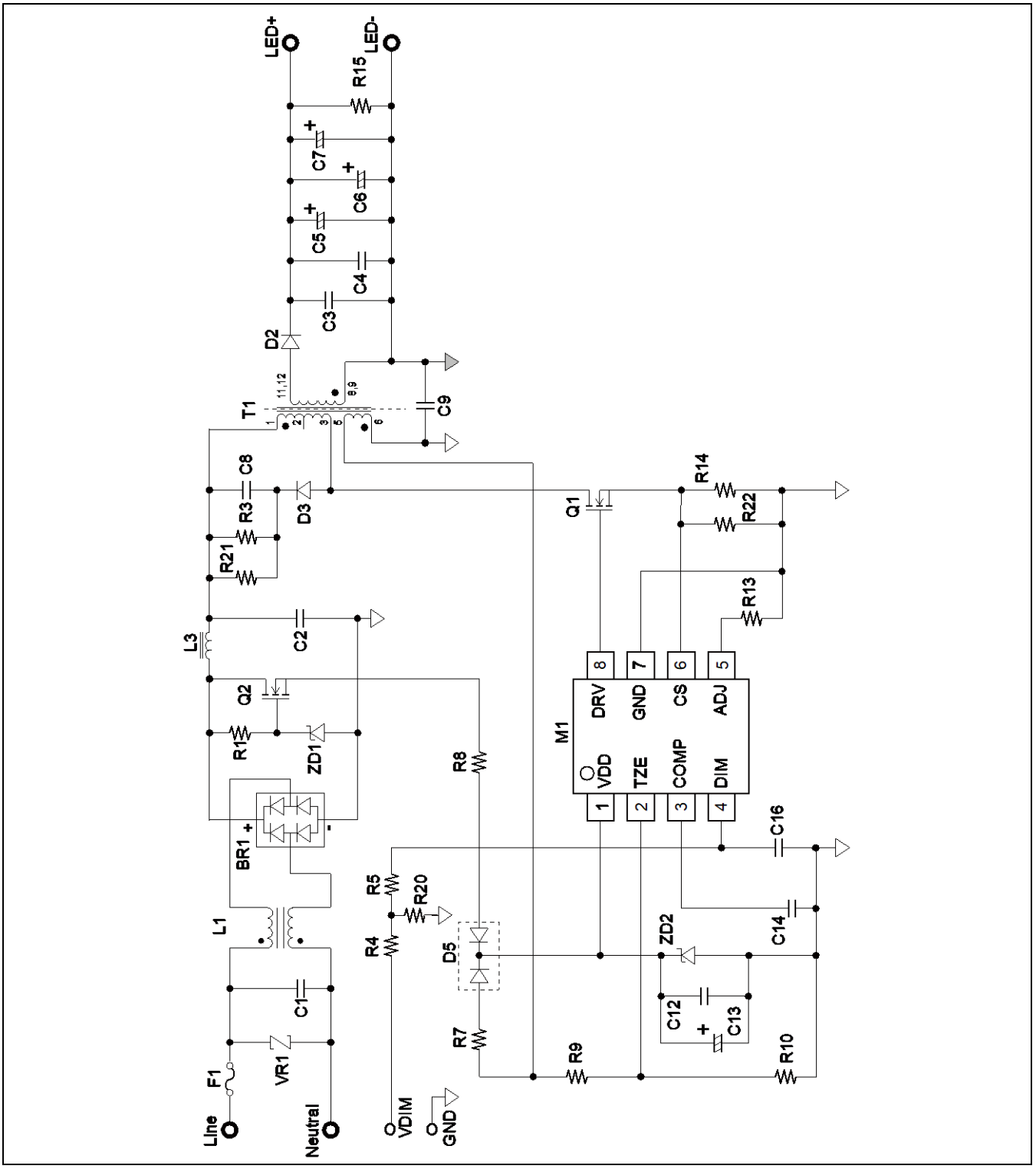
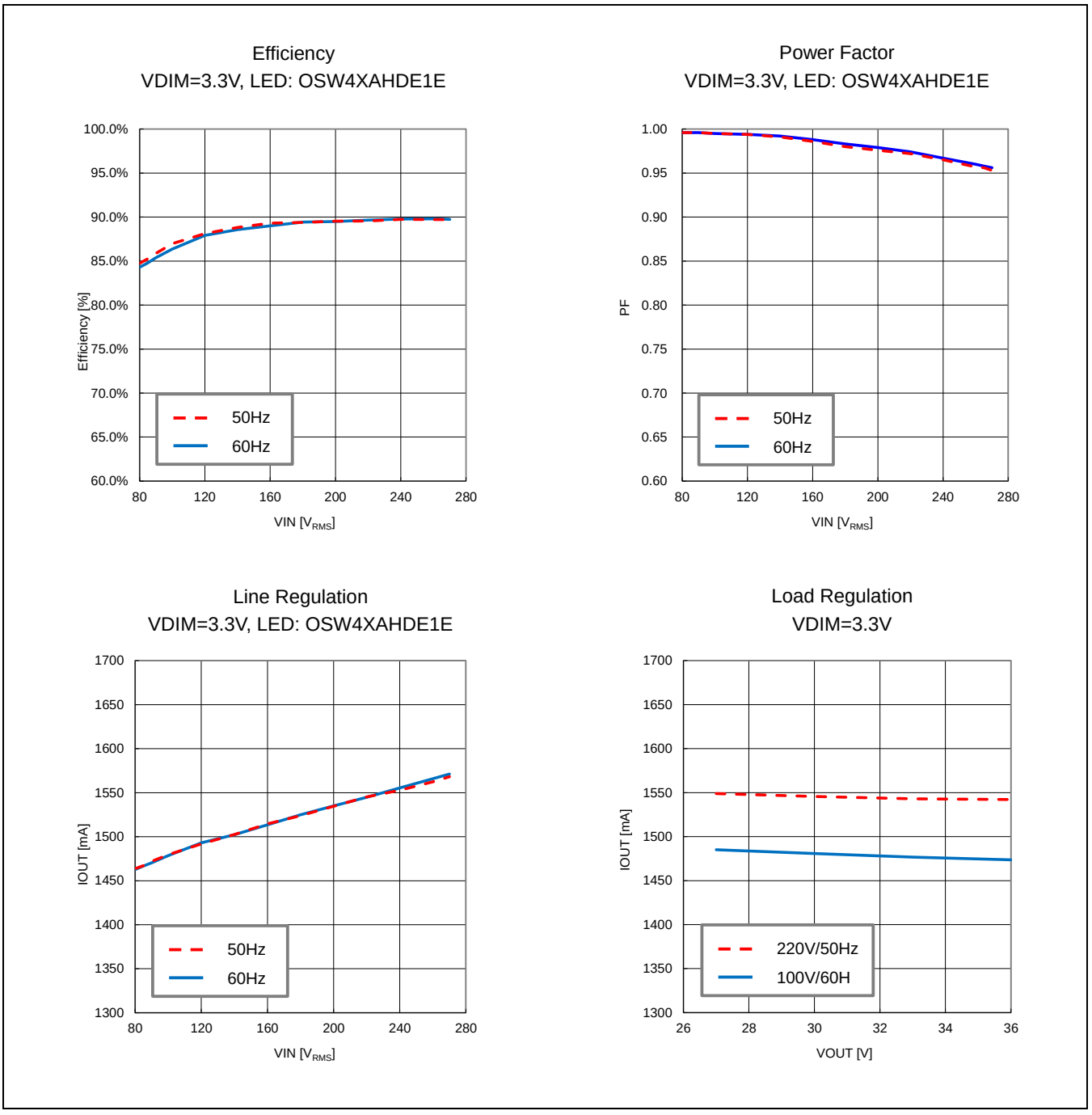


Table 6. 50W BOM List

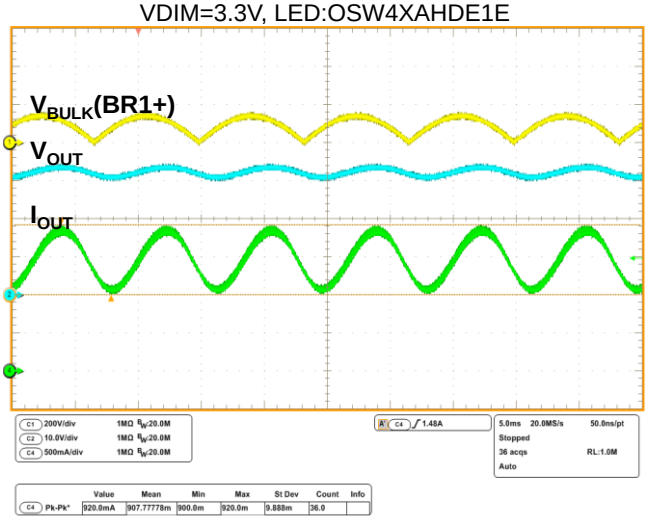
No.	Component	Description	Part No.	Vendor
1	M1	Driver IC for LED Lighting, SO-8	CY39C604	Cypress
2	Q1	MOSFET, N-channel, 800V, 5.5A, TO-220F	FQPF8N80C	Fairchild
3	Q2	MOSFET, N-channel, 600V, 2.8A, TO-251	FQU5N60C	Fairchild
4	BR1	Bridge rectifier, 3A, 600V, GBU-4L	GBU4J	Fairchild
5	D2	Diode, ultra fast rectifier, 10A, 200V, TO-220F	FFPF10UP20S	Fairchild
6	D3	Diode, fast rectifier, 1A, 800V, DO-41	UF4006	Fairchild
7	D5	Diode, 200 mA, 200V, SOT-23	MMBD1404	Fairchild
8	ZD1	Diode, Zener, 20V, 500 mW, SOD-123	MMSZ20T1G	ON Semiconductor
9	ZD2	Diode, Zener, 18V, 500 mW, SOD-123	MMSZ18T1G	ON Semiconductor
10	T1	Transformer, 200 µH, Np/Ns = 3.5/1 Np/Na = 7/1	PQ-2625	-
11	L1	Common mode choke, 47.0 mH	LF2429NP-T473	Sumida
12	L3	Inductor, 1.0 mH, 0.65A, 0.9Ω, ϕ12.5 × 16.0	RCH1216BNP-102K	Sumida
13	C1	Capacitor, X2, 305VAC, 0.1 µF	B32921C3104M	EPCOS
14	C2	Capacitor, polyester film, 220 nF, 400V, 18.5 × 5.9	ECQ-E4224KF	Panasonic
15	C3,C4	Capacitor, ceramic, 10 µF, 50V, X7S, 1210	C3225X7S1H106K250AB	TDK
16	C5,C6,C7	Capacitor, aluminum electrolytic, 470 µF 50V, ϕ10.0 × 20	EKMG500ELL471MJ20S	NIPPON-CHEMI-CON
17	C8	Capacitor, ceramic, 33 nF, 250V, 1206	C3216X7R2E333K160AA	TDK
18	C9	Capacitor, ceramic, 2.2 nF, X1/Y1 radial	DE1E3KX222M	muRata
19	C12,C16	Capacitor, ceramic, 0.1 µF, 25V, 0603	-	-
20	C13	Capacitor, aluminum, 47 µF, 25V	-	-
21	C14	Capacitor, ceramic, 4.7 µF, 16V, 0805	-	-
22	R1	Resistor, chip, 1.00 MΩ, 1/4W, 1206	-	-
23	R3,R21	Resistor, 100 kΩ, 2W	-	-
24	R4	Resistor, chip, 68 kΩ, 1/10W, 0603	-	-
25	R5	Resistor, chip, 1.0 MΩ, 1/10W, 0603	-	-
26	R7	Resistor, chip, 10Ω, 1/8W, 0805	-	-
27	R8	Resistor, chip, 22Ω, 1/10W, 0603	-	-
28	R9	Resistor, chip, 91 kΩ, 1/10W, 0603	-	-
29	R10	Resistor, chip, 24 kΩ, 1/10W, 0603	-	-
30	R13	Resistor, chip, 27 kΩ, 1/10W, 0603	-	-
31	R14,R22	Resistor, chip, 0.68Ω, 1/4W, 1206	-	-
32	R15	Resistor, chip, 30 kΩ, 1/10W, 0603	-	-
33	R20	Resistor, chip, 100 kΩ, 1/10W, 0603	-	-
34	VR1	Varistor, 275VAC, 7 mm DISK	ERZ-V07D431	Panasonic
35	F1	Fuse, 2A, 300VAC	3691200000	Littelfuse

Fairchild	:	Fairchild Semiconductor International, Inc.
On Semiconductor	:	ON Semiconductor
Sumida	:	SUMIDA CORPORATION
EPCOS	:	EPCOS AG
Panasonic	:	Panasonic Corporation
TDK	:	TDK Corporation
NIPPON-CHEMI-CON	:	Nippon Chemi-Con Corporation
muRata	:	Murata Manufacturing Co., Ltd.
Littelfuse	:	Littelfuse, Inc.

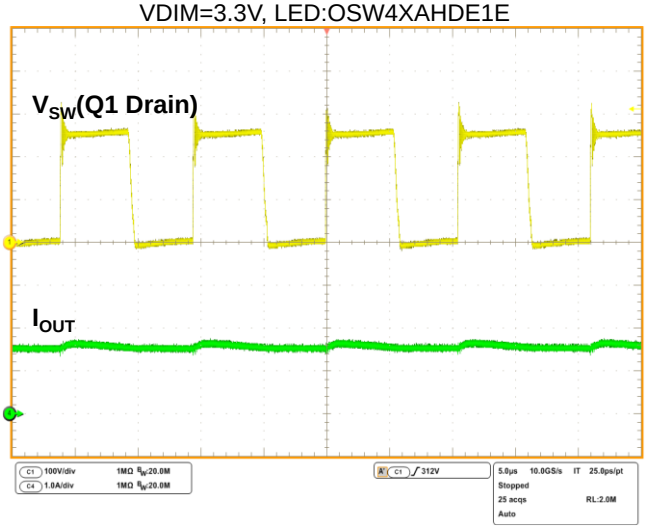
Figure 13. 50W Reference Data



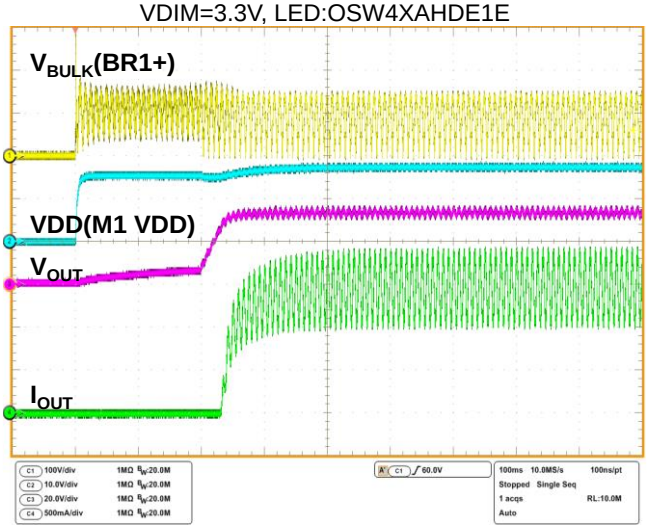
Output Ripple Waveform
V_{IN}=100V_{RMS} / 60Hz
VDIM=3.3V, LED:OSW4XAHDE1E



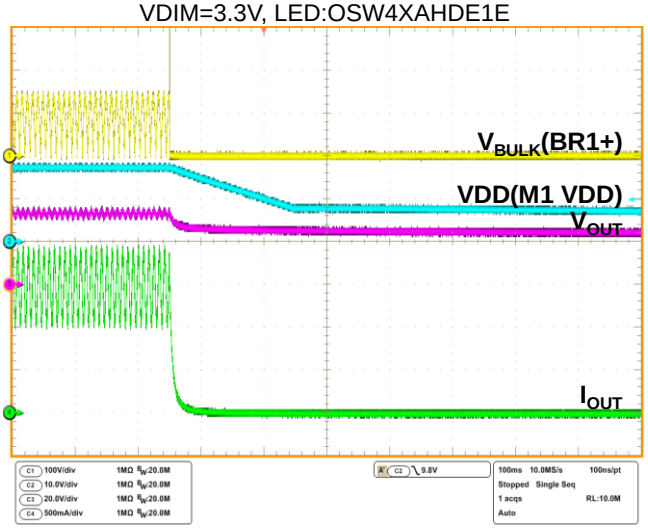
Switching Waveform
V_{IN}=100V_{RMS} / 60Hz
VDIM=3.3V, LED:OSW4XAHDE1E



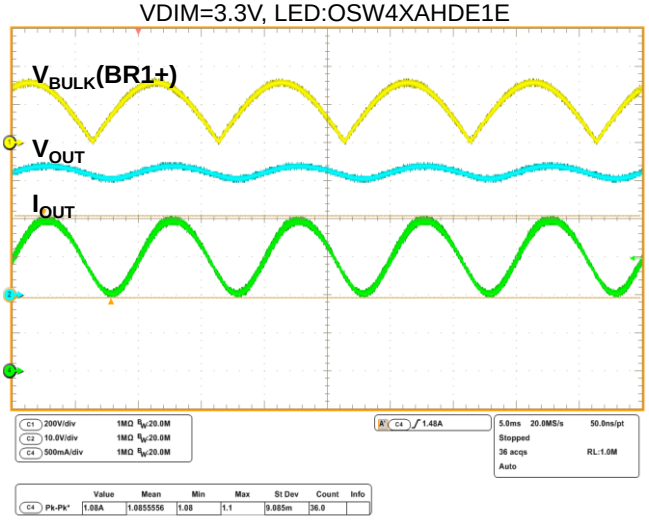
Turn-On Waveform
V_{IN}=100V_{RMS} / 60Hz
VDIM=3.3V, LED:OSW4XAHDE1E



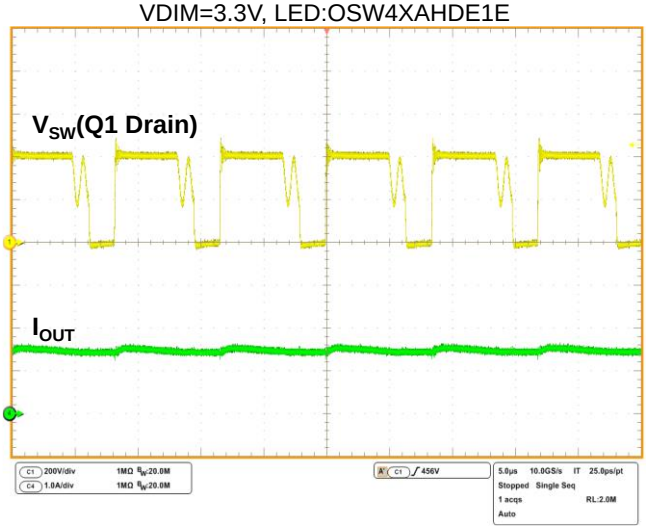
Turn-Off Waveform
V_{IN}=100V_{RMS} / 60Hz
VDIM=3.3V, LED:OSW4XAHDE1E



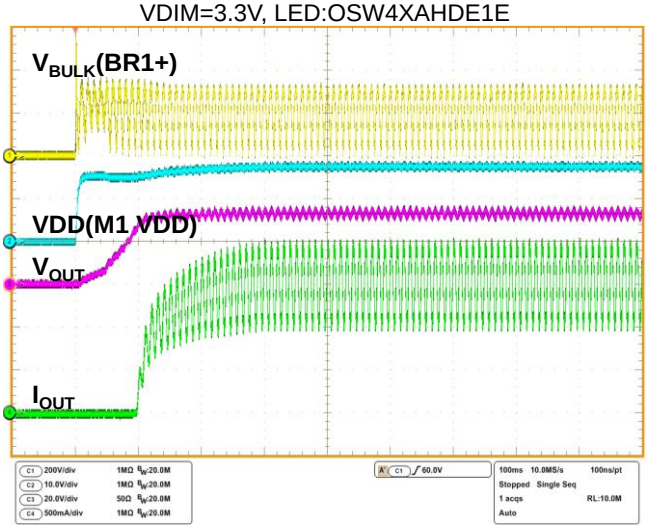
Output Ripple Waveform
V_{IN}=220V_{RMS} / 50Hz
VDIM=3.3V, LED:OSW4XAHDE1E



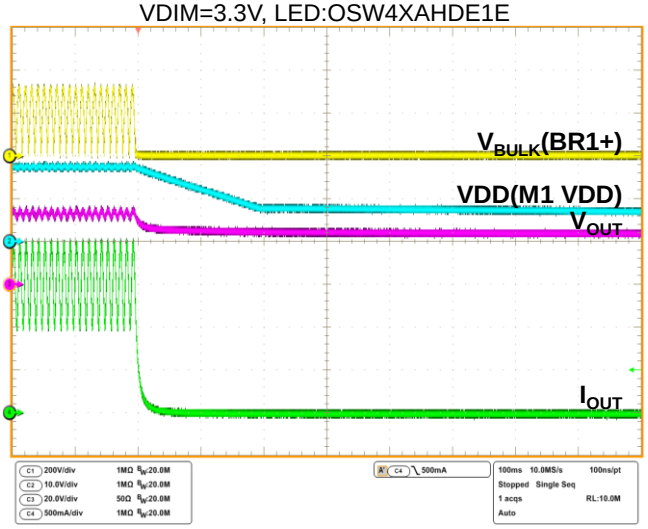
Switching Waveform
V_{IN}=220V_{RMS} / 50Hz
VDIM=3.3V, LED:OSW4XAHDE1E



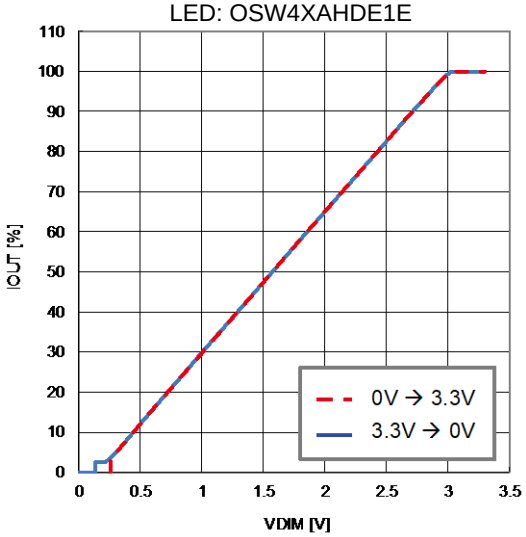
Turn-On Waveform
V_{IN}=220V_{RMS} / 50Hz
VDIM=3.3V, LED:OSW4XAHDE1E



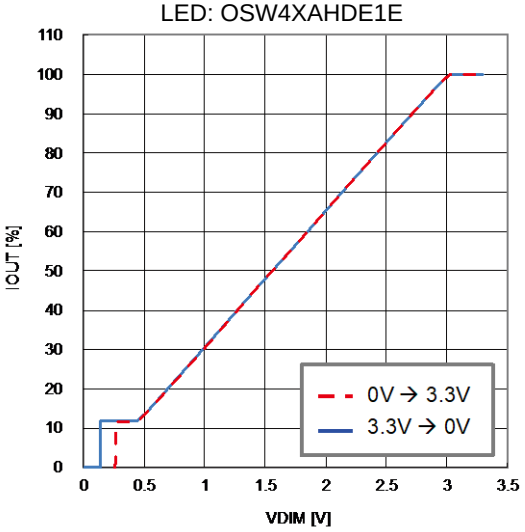
Turn-Off Waveform
V_{IN}=220V_{RMS} / 50Hz
VDIM=3.3V, LED:OSW4XAHDE1E



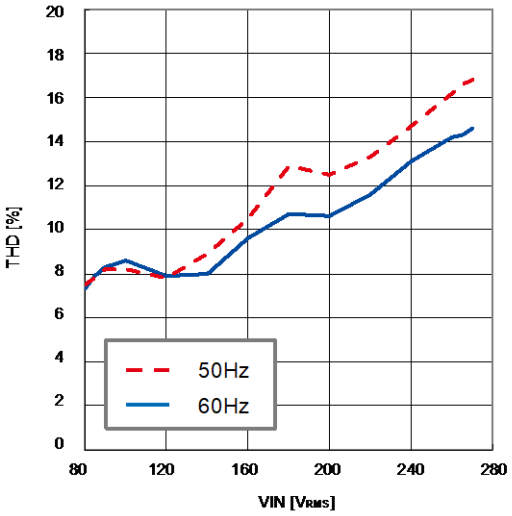
Dimming Curve
V_{IN}=100V_{RMS} / 60Hz
LED: OSW4XAHDE1E



Dimming Curve
V_{IN}=220V_{RMS} / 50Hz
LED: OSW4XAHDE1E



Total Harmonic Distortion (THD)
VDIM=3.3V, LED: OSW4XAHDE1E



10.2 5W Non-Isolated and Non-Dimming Application

Input: AC85V$_{RMS}$ to 145V$_{RMS}$, Output: 70mA/67V to 82V

Figure 14. 5W EVB Schematic

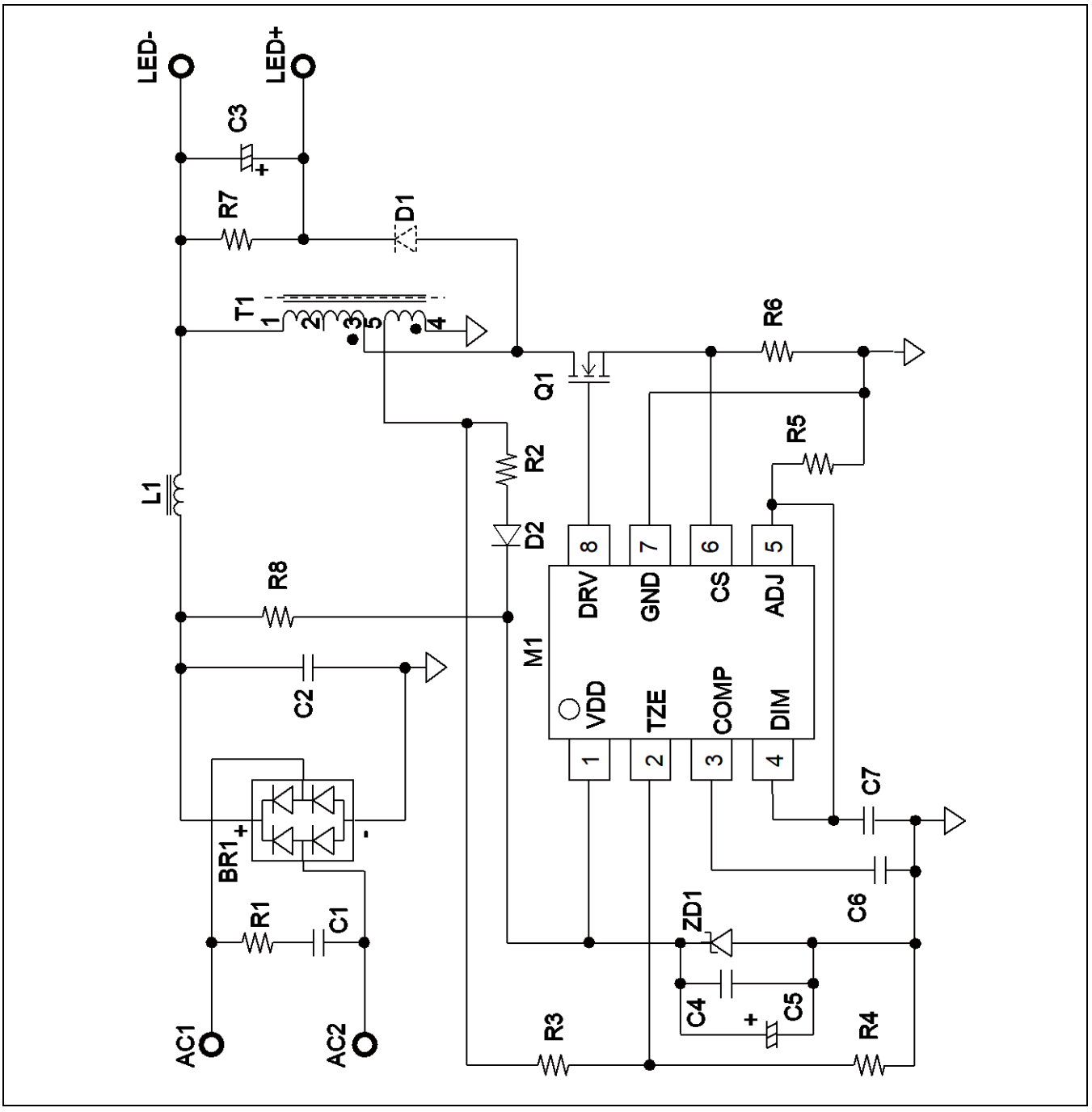
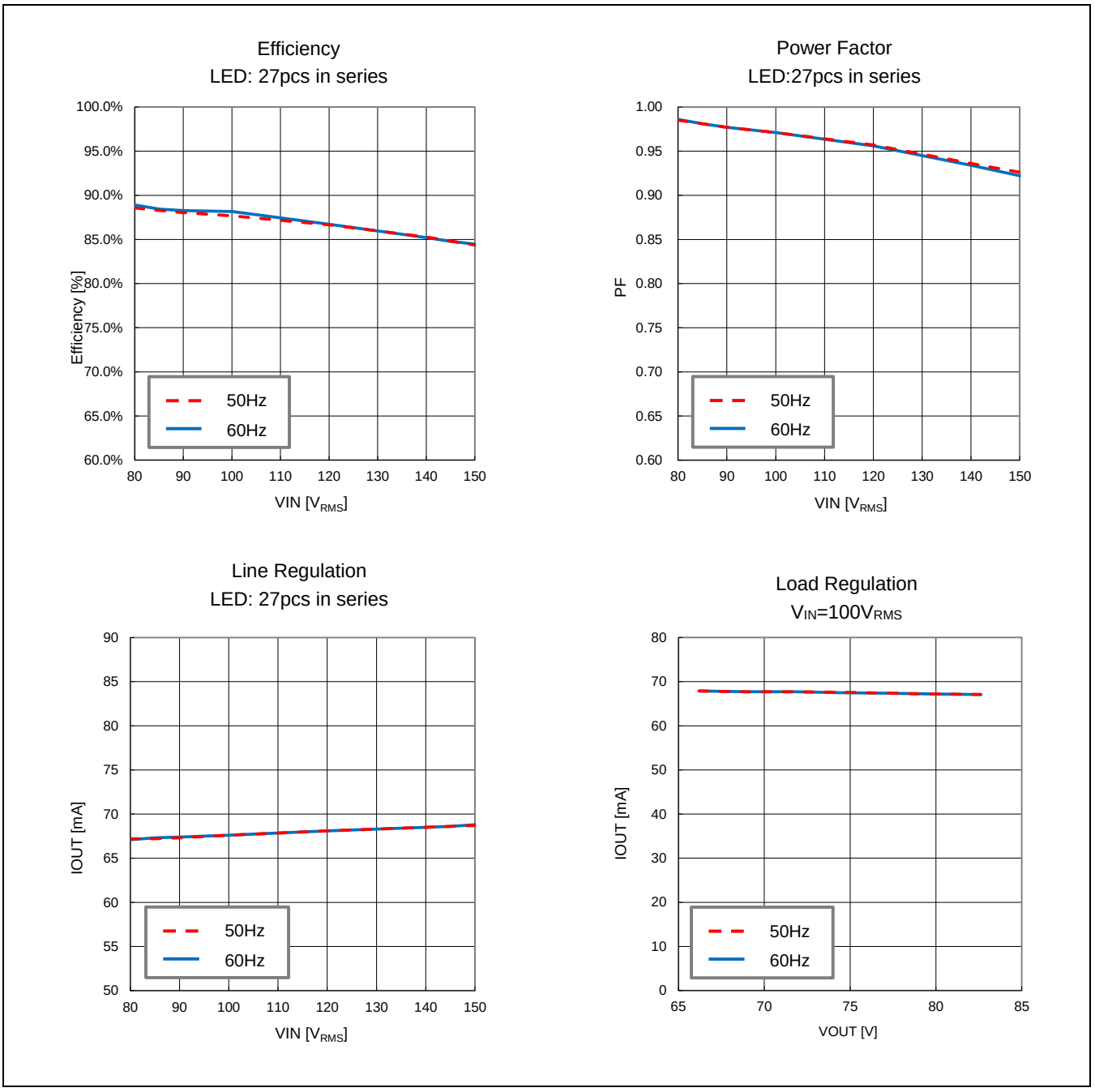


Table 7. 5W BOM List

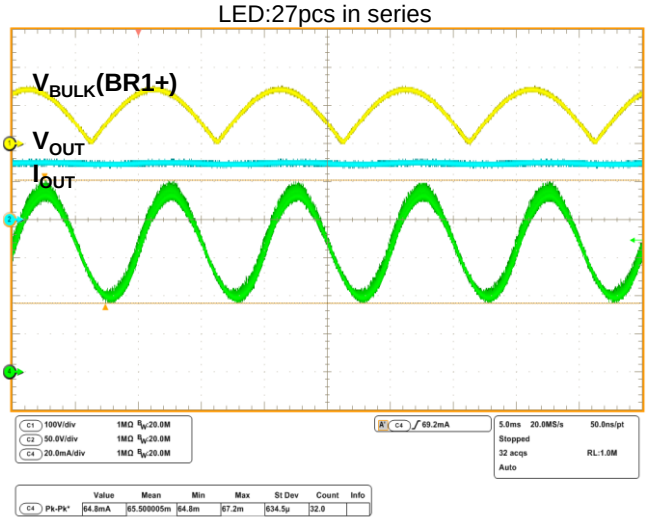
No.	Component	Description	Part No.	Vendor
1	M1	Driver IC for LED Lighting, SO-8	CY39C604	Cypress
2	Q1	MOSFET, N-channel, 600V, 2.8A, TO-251	FQU5N60C	Fairchild
3	BR1	Bridge rectifier, 1A, 600V, Micro-DIP	MDB6S	Fairchild
4	D1	Diode, ultra fast rectifier, 1A, 600V, SMA	ES1J	Fairchild
5	D2	Diode, 200 mA, 200V, SOT-23	MMBD1404	Fairchild
6	ZD1	Diode, Zener, 18V, 500 mW, SOD-123	MMSZ18T1G	ON Semiconductor
7	T1	Transformer, Lp = 430 µH, Np/Na = 5.33/1	EE808	-
8	L1	Inductor 470 µH 0.31A ϕ7.2 mm × 10.5 mm	22R474C	muRata
9	C1	Capacitor, polyester film, 100 nF, 630V, 18.5 × 6.3	ECQ-E6104KF	Panasonic
10	C2	Capacitor, polyester film, 100 nF, 250V, 7.9 × 5.9	ECQE2104KB	Panasonic
11	C3	Capacitor, aluminum electrolytic, 100 µF 100V, ϕ10.0 × 20	EKMG101ELL101MJ20S	NIPPON-CHEMI-CON
12	C4	Capacitor, ceramic, 0.1 µF, 25V, 0603	-	-
13	C5	Capacitor, aluminum, 47 µF, 25V	-	-
14	C6	Capacitor, ceramic, 4.7 µF, 16V, 0805	-	-
15	C7	Capacitor, ceramic, 0.1 µF, 25V, 0603	-	-
16	R1	Resistor, 510Ω, 1/2W	-	-
17	R2	Resistor, chip, 10Ω, 1/8W, 0805	-	-
18	R3	Resistor, chip, 110 kΩ, 1/10W, 0603	-	-
19	R4	Resistor, chip, 30 kΩ, 1/10W, 0603	-	-
20	R5	Resistor, chip, 22 kΩ, 1/10W, 0603	-	-
21	R6	Resistor, 2Ω, 1W	-	-
22	R7	Resistor, chip, 100 kΩ, 1/10W, 0603	-	-
23	R8	Resistor, 47 kΩ, 2W	-	-

Fairchild : Fairchild Semiconductor International, Inc.
On Semiconductor : ON Semiconductor
Panasonic : Panasonic Corporation
NIPPON-CHEMI-CON : Nippon Chemi-Con Corporation
muRata : Murata Manufacturing Co., Ltd.

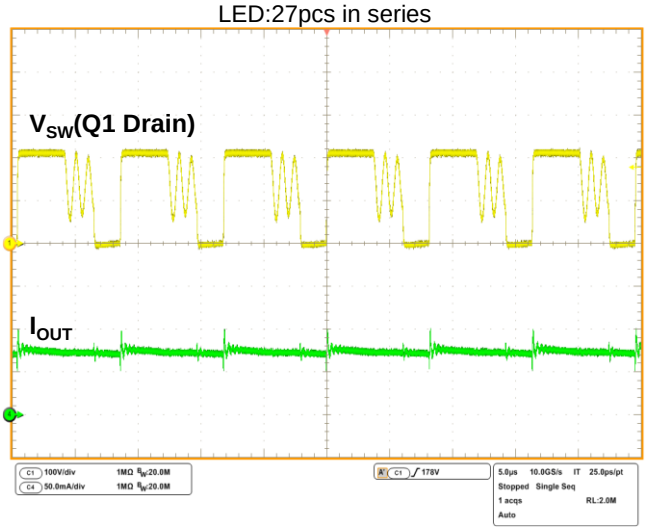
Figure 15. 5W Reference Data



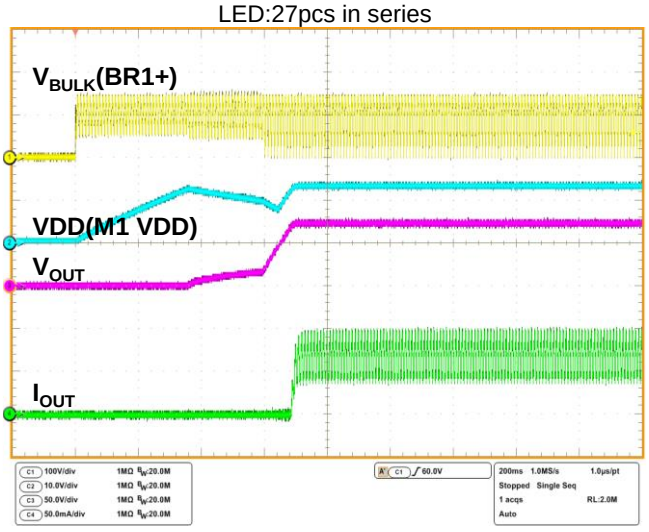
Output Ripple Waveform
V_{IN}=100V_{RMS} / 50Hz
LED:27pcs in series



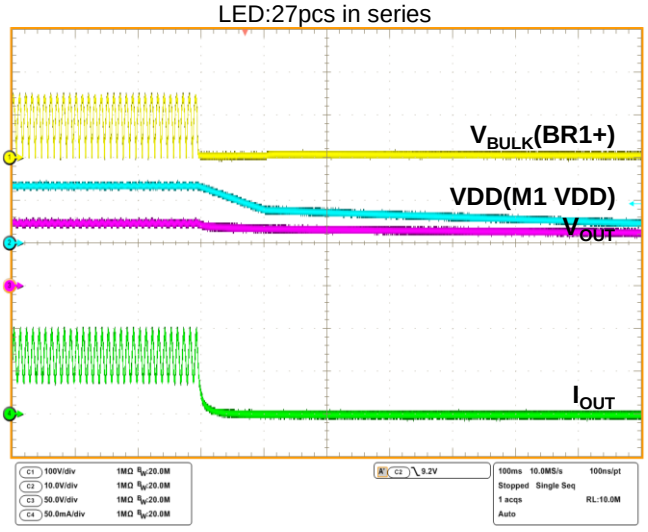
Switching Waveform
V_{IN}=100V_{RMS} / 50Hz
LED:27pcs in series



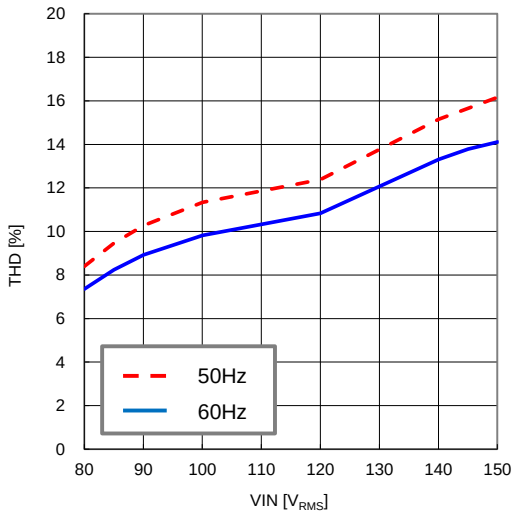
Turn-On Waveform
V_{IN}=100V_{RMS} / 50Hz
LED:27pcs in series



Turn-Off Waveform
V_{IN}=100V_{RMS} / 50Hz
LED:27pcs in series



Total Harmonic Distortion (THD)
LED: 27pcs in series



11. Usage Precautions

Do not configure the IC over the maximum ratings.
If the IC is used over the maximum ratings, the LSI may be permanently damaged.

It is preferable for the device to normally operate within the recommended usage conditions. Usage outside of these conditions can have an adverse effect on the reliability of the LSI.

Use the device within the recommended operating conditions.
The recommended values guarantee the normal LSI operation under the recommended operating conditions.

The electrical ratings are guaranteed when the device is used within the recommended operating conditions and under the conditions stated for each item.

Printed circuit board ground lines should be set up with consideration for common impedance.

Take appropriate measures against static electricity.

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ in serial between body and ground.

Do not apply negative voltages.
The use of negative voltages below - 0.3 V may make the parasitic transistor activated to the LSI, and can cause malfunctions.

12. RoHS Compliance Information

This product has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE).

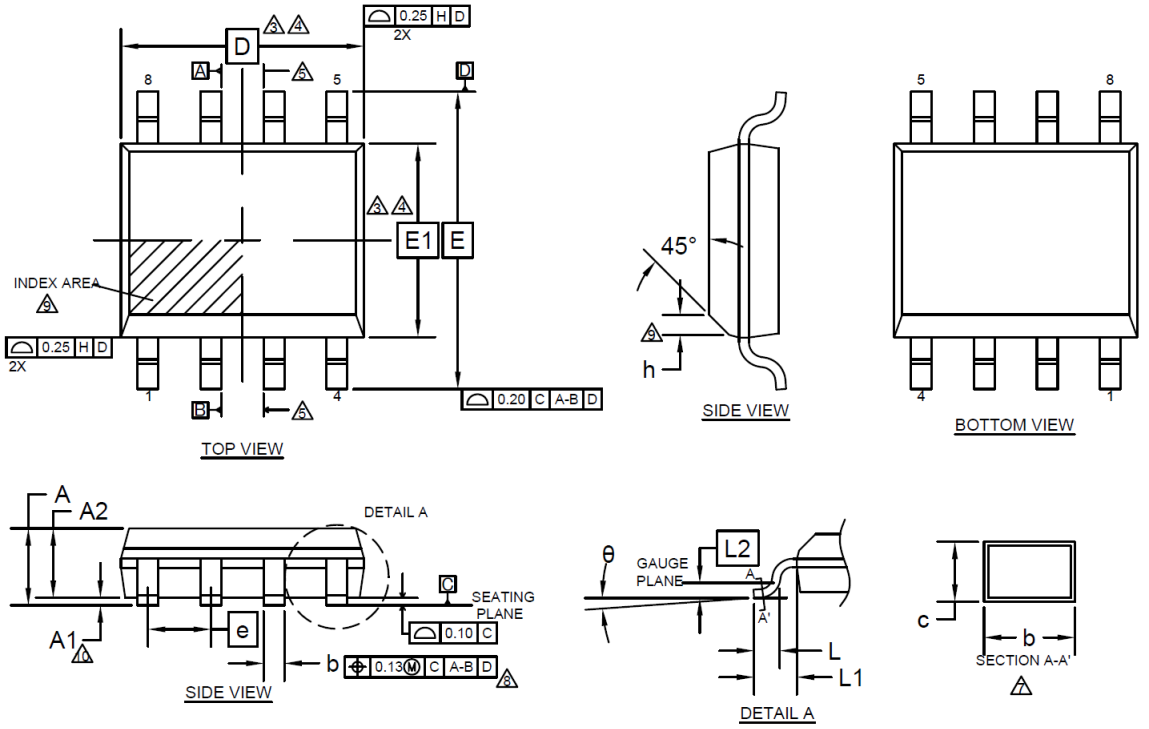
13. Ordering Information

Table 8. Ordering Information

Part Number	Package	Shipping Form
CY39C604PNF-G-JNEFE1	8-pin plastic SOP (SOB008)	Emboss
CY39C604PNF-G-JNE1		Tube

14. Package Dimensions

Package Code: SOB008



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.75
A1	0.05	—	0.25
A2	1.30	1.40	1.50
D	5.05 BSC.		
E	6.00 BSC.		
E1	3.90 BSC		
θ	0°	—	8°
c	0.15	—	0.25
b	0.36	0.44	0.52
L	0.45	0.60	0.75
L 1	1.05 REF		
L 2	0.25 BSC		
e	1.27 BSC.		
h	0.40 BSC.		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A & B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. LF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
10. "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
11. JEDEC SPECIFICATION NO. REF : N/A

002-15856 Rev. **

15. Major Changes

Spansion Publication Number: MB39C604_DS405-00016

Page	Section	Descriptions
Revision 1.0		
-	-	Initial release
Revision 2.0		
16	11. Function Explanations 11.7 Zero Voltage Switching Function	Corrected the R_{ADJ} formula
32	15. Ordering Information	Added Shipping in Table 15-1
-	-	Rewrote entire document for improving the ease of understanding (the original intentions are remained unchanged).
Revision 2.0		
8	7. Absolute Maximum Ratings	Removed ESD Voltage (Machine Model) from Table 7-1
-	Labeling Sample	Removed section of Labeling Sample
34	17. Recommended mounting condition [JEDEC Level3] Lead Free	Changed Recommended Condition from three conditions to one condition “JEDEC LEVEL3”

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: CY39C604 PSR LED Driver IC for LED Lighting
Document Number: 002-08441

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	HSAT	02/20/2015	Migrated to Cypress and assigned document number 002-08441. No change to document contents or format.
*A	5141647	HSAT	02/22/2016	Updated to Cypress format.
*B	5740103	HIXT	05/22/2017	Updated Pin Assignment: Change the package name from FPT-8P-M02 to SOB008 Added RoHS Compliance Information Updated Ordering Information: Change the package name from FPT-8P-M02 to SOB008 Deleted “Marking Format” Deleted “Recommended Mounting Condition [JEDEC Level3] Lead Free” Updated Package Dimensions: Updated to Cypress format
*C	6059028	YOST	02/05/2018	Updated the Sales information and legal. Completing Sunset Review.
*D	6437385	ATTS	01/21/2019	Changed part number to CY39C604

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