LP2982 50-mA Micropower Ultra-Low-Dropout LDO in SOT-23 Package

1 Features

- 2.1-V to 16-V Input Voltage
- Ultra-Low-Dropout Voltage
- Ensured 50-mA Output Current
- Typical Dropout Voltage 180 mV at 80 mA
- Requires Minimum External Components
- < 1 μA Quiescent Current When Shut Down
- Low Ground Pin Current at All Loads
- Output Voltage Accuracy 1% (A Grade)
- High Peak Current Capability (150 mA Typical)
- Wide Supply Voltage Range (16 V Maximum)
- Low Z_{OUT} 0.3 Ω Typical (10 Hz to 1 MHz)
- Overtemperature and Overcurrent Protection
- −40°C to +125°C Junction Temperature Range

2 Applications

- Cellular Phones
- Palmtop and Laptop Computers
- Personal Digital Assistants (PDA)
- Camcorders, Personal Stereos, Cameras

3 Description

The LP2982 is a 50-mA, fixed-output voltage LDO designed to provide ultra-low dropout and lower noise in battery-powered applications.

Using an optimized vertically integrated PNP (VIP) process, the LP2982 delivers unequaled performance in all specifications critical to battery-powered designs:

Dropout Voltage: Typically 120 mV at 50 mA load, and 7 mV at 1 mA load.

Ground Pin Current: Typically 375 μA at 50 mA load, and 80 μA at 1 mA load.

Sleep Mode: Less than 1-μA quiescent current when ON/$\overline{\text{OFF}}$ pin is pulled low.

Precision Output: 1% tolerance output voltages available (A grade).

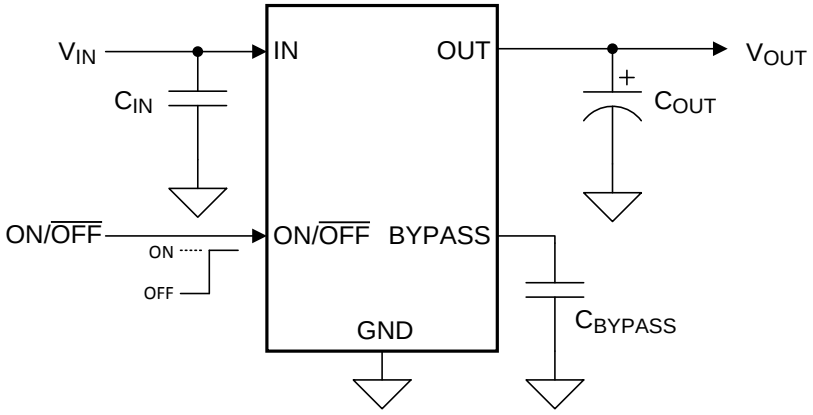
Low Noise: By adding an external bypass capacitor, output noise can be reduced to 30 μV (typical).

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP2982	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (April 2013) to Revision K — **Page**

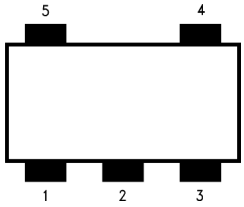
- Deleted TM symbol from VIP - no longer trademarked; changed word in title from "Regulator" to "LDO" ... 1
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed update typical application drawing and change pin names from Vin, Vout to IN and OUT; remove last paragraph of *Description* beginning "Four output voltage versions..." ... 1
- Deleted Lead temperature row from *Abs Max*; this information is in the POA; remove "(survival)" and "(operating)" from rows in *Abs Max* table ... 4
- Added "ON/$\overline{\text{OFF}}$ input voltage" to *ROC* table ... 4
- Changed $V_{IN} – V_O$ to "V_{DO}" ... 5

Changes from Revision I (April 2013) to Revision J — **Page**

- Changed layout of National Semiconductor Data Sheet to TI format ... 18

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Descriptions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1	IN	Input	Input voltage
2	GND	—	Common ground (device substrate)
3	ON/OFF	Input	Logic high enable input
4	BYPASS	Input/Output	Bypass capacitor for low noise operation
5	OUT	Output	Regulated output voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Operating junction temperature	−40	125	°C
Power dissipation(3)	Internally limited		
Input supply voltage	−0.3	16	V
Shutdown input voltage	−0.3	16	V
Output voltage(4)	−0.3	9	V
I_{OUT}	Short-circuit protected		
Input-output voltage(5)	−0.3	16	V
Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace-specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using $P_{(MAX)} = (T_{J(MAX)} – T_A) / R_{\theta JA}$. The value of $R_{\theta JA}$ for the SOT-23 package is 169°C/W. Exceeding the maximum allowable power dissipation causes excessive die temperature, and the regulator will go into thermal shutdown.
(4) If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2982 output must be diode-clamped to ground.
(5) The output PNP structure contains a diode between the IN and OUT pins that is normally reverse-biased. Reversing the polarity from V_{IN} to V_{OUT} turns on this diode (see *Reverse Current Path*).

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Pins 1, 2 and 5	±2000	V
			Pins 3 and 4	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating junction temperature	−40	125	°C
Input supply voltage	2.1	16	V
ON/$\overline{\text{OFF}}$ input voltage	0	16	V

6.4 Thermal Information

THERMAL METRIC[1]		LP2982 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance, High-K[2]	175.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	121.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal resistance value $R_{\theta JA}$ is based on the EIA/JEDEC High-K printed circuit board defined by: JESD51-7 - *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.

6.5 Electrical Characteristics

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, I_L = 1 mA, C_{OUT} = 1 µF, $V_{ON/\overline{OFF}}$ = 2 V.

PARAMETER		TEST CONDITIONS	LP2982AI-XX[1]			LP2982I-XX[1]			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ΔV_O	Output voltage tolerance	I_L = 1 mA	−1		1	−1.5		1.5	%V_{NOM}
		1 mA < I_L < 50 mA	−1.5		1.5	−2		2	
		1 mA < I_L < 50 mA –40°C ≤ T_J ≤ 125°C	−2		2	−3.5		3.5	
$\Delta V_O/\Delta V_{IN}$	Output voltage line regulation	$V_{O(NOM)}$ + 1 V ≤ V_{IN} ≤ 16 V		0.007	0.014		0.007	0.014	%/V
		$V_{O(NOM)}$ + 1 V ≤ V_{IN} ≤ 16 V –40°C ≤ T_J ≤ 125°C			0.032			0.032	
V_{DO}	Dropout voltage[2]	I_L = 0 mA		1	3		1	3	mV
		I_L = 0 mA, –40°C ≤ T_J ≤ 125°C			5			5	
		I_L = 1 mA		7	10		7	10	
		I_L = 1 mA, –40°C ≤ T_J ≤ 125°C			15			15	
		I_L = 10 mA		40	60		40	60	
		I_L = 10 mA, –40°C ≤ T_J ≤ 125°C			90			90	
		I_L = 50 mA		120	150		120	150	
		I_L = 50 mA, –40°C ≤ T_J ≤ 125°C			225			225	
		I_L = 80 mA		180	225		180	225	
		I_L = 80 mA, –40°C ≤ T_J ≤ 125°C			325			325	
I_{GND}	Ground pin current	I_L = 0 mA		65	95		65	95	µA
		I_L = 0 mA, –40°C ≤ T_J ≤ 125°C			125			125	
		I_L = 1 mA		80	110		80	110	
		I_L = 1 mA, –40°C ≤ T_J ≤ 125°C			170			170	
		I_L = 10 mA		140	220		140	220	
		I_L = 10 mA, –40°C ≤ T_J ≤ 125°C			460			460	
		I_L = 50 mA		375	600		375	600	
		I_L = 50 mA, –40°C ≤ T_J ≤ 125°C			1200			1200	
		I_L = 80 mA		525	750		525	750	
		I_L = 80 mA, –40°C ≤ T_J ≤ 125°C			1400			1400	
		$V_{ON/\overline{OFF}}$ < 0.3 V		0.01	0.8		0.01	0.8	
		$V_{ON/\overline{OFF}}$ < 0.15 V –40°C ≤ T_J ≤ 125°C		0.1	2		0.1	2	

(1) Temperature range are ensured through correlation using statistical quality control (SQC) methods. The limits are used to calculate average outgoing quality level (AOQL).
(2) Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1-V differential.

Electrical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, I_L = 1 mA, C_{OUT} = 1 µF, $V_{ON/\overline{OFF}}$ = 2 V.

PARAMETER		TEST CONDITIONS	LP2982AI-XX(1)			LP2982I-XX(1)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input voltage(3)	High = O/P ON		1.4			1.4		V
		High = O/P ON –40°C ≤ T_J ≤ 125°C	1.6			1.6			
		Low = O/P OFF	0.55			0.55			
		Low = O/P OFF –40°C ≤ T_J ≤ 125°C			0.15			0.15	
$I_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input current	$V_{ON/\overline{OFF}}$ = 0 V		0.01			0.01		µA
		$V_{ON/\overline{OFF}}$ = 0 V –40°C ≤ T_J ≤ 125°C			–2			–2	
		$V_{ON/\overline{OFF}}$ = 5 V		5			5		
		$V_{ON/\overline{OFF}}$ = 5 V –40°C ≤ T_J ≤ 125°C			15			15	
$I_{O(PK)}$	Peak output current	V_{OUT} ≥ $V_{O(NOM)}$ − 5%	150	100			100		mA
e_n	Output noise voltage (RMS)	BW = 300 Hz to 50 kHz C_{OUT} = 10 µF		30			30		µV
$\Delta V_O/\Delta V_{IN}$	Ripple rejection	f = 1 kHz, C_{OUT} = 10 µF		45			45		dB
$I_{O(MAX)}$	Short-circuit current	R_L = 0 Ω (steady state)(4)		150			150		mA

(3) The ON/$\overline{OFF}$ inputs must be properly driven to prevent misoperation. For details, see *Operation With ON/$\overline{OFF}$ Control*.
(4) See related curve(s) in *Typical Characteristics* section.

6.6 Typical Characteristics

Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

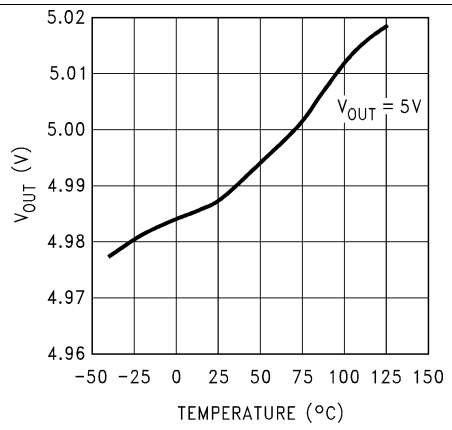


Figure 1. Output Voltage vs Temperature

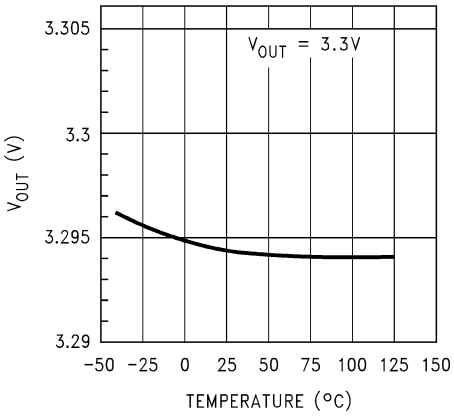


Figure 2. Output Voltage vs Temperature

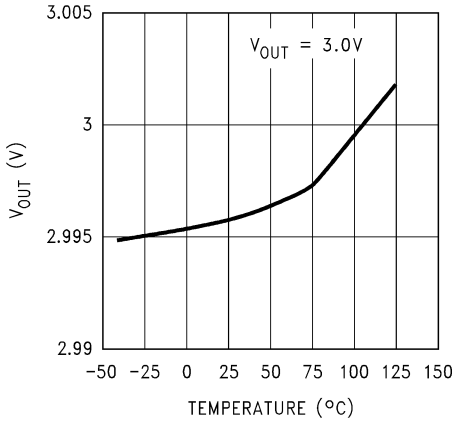


Figure 3. Output Voltage vs Temparature

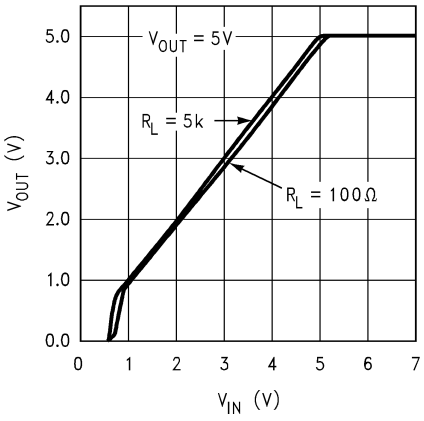


Figure 4. Dropout Characteristics

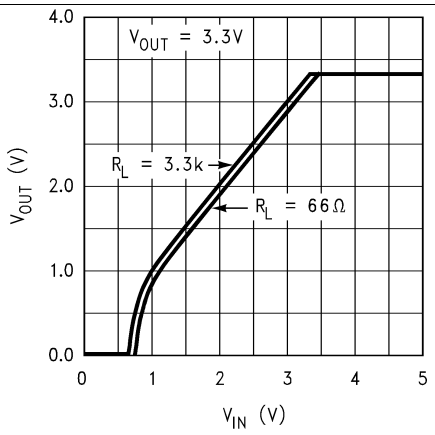


Figure 5. Dropout Characteristics

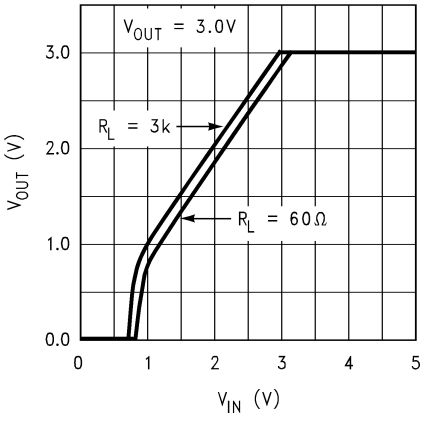


Figure 6. Dropout Characteristics

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

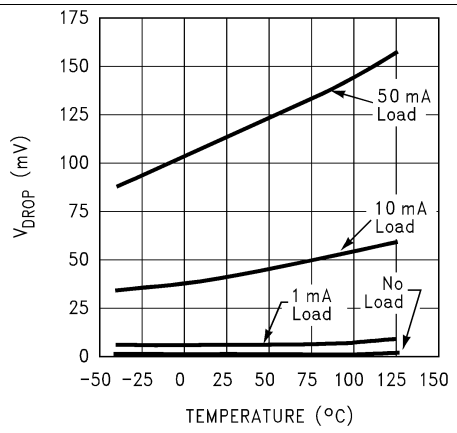


Figure 7. Dropout Voltage vs Temperature

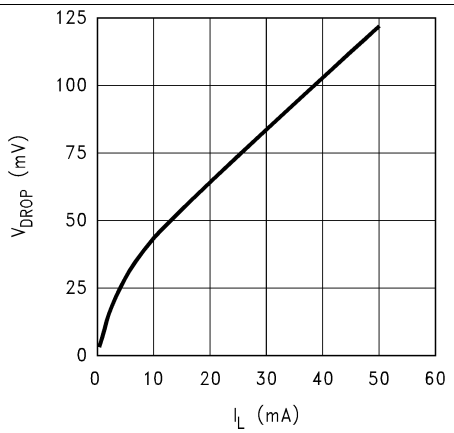


Figure 8. Dropout Voltage vs Load Current

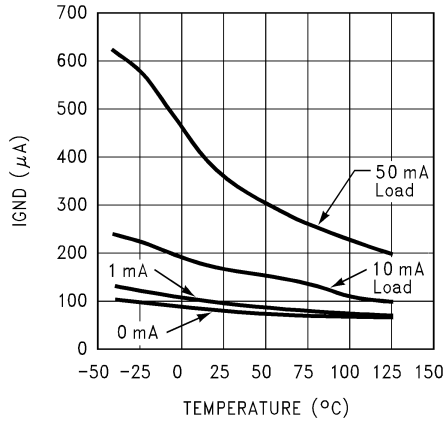


Figure 9. GND Pin Current vs Temperature

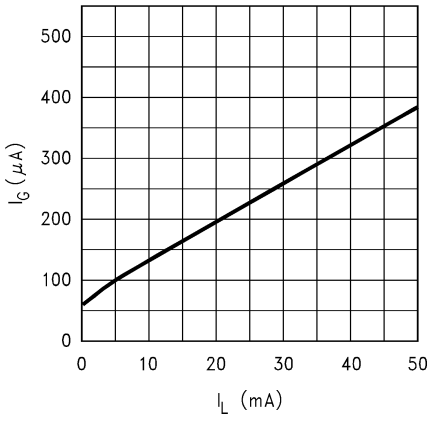


Figure 10. GND Pin Current vs Load Current

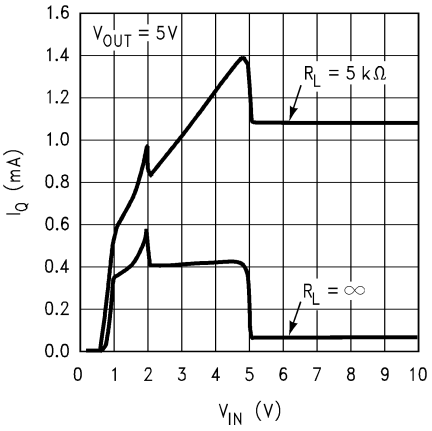


Figure 11. Input Current vs V_{IN}

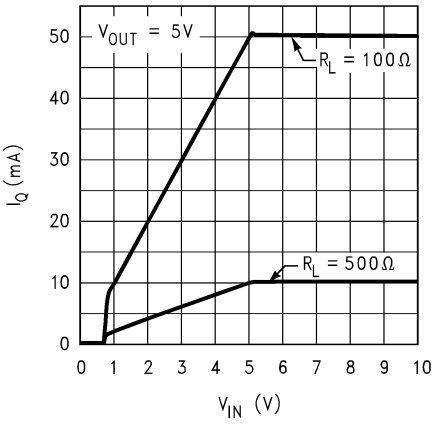


Figure 12. Input Current vs V_{IN}

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

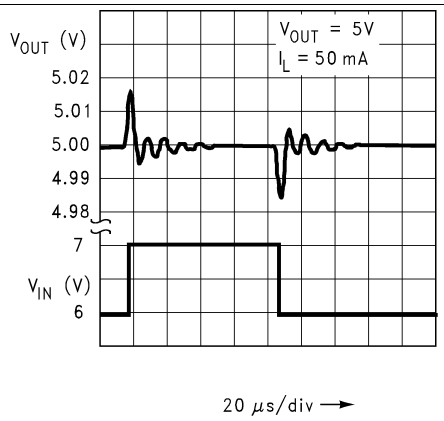


Figure 13. Line Transient Response

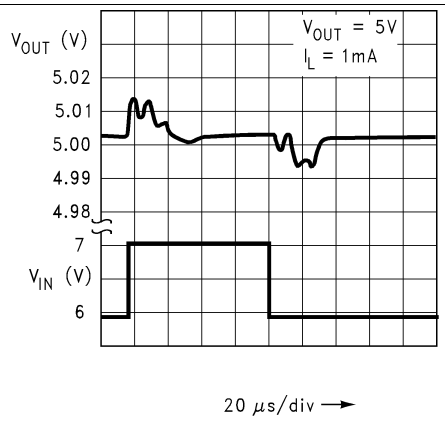


Figure 14. Line Transient Response

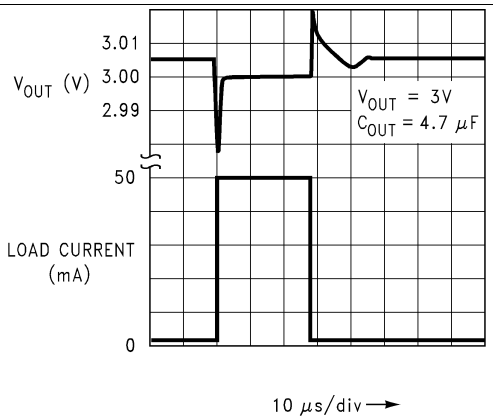


Figure 15. Load Transient Response

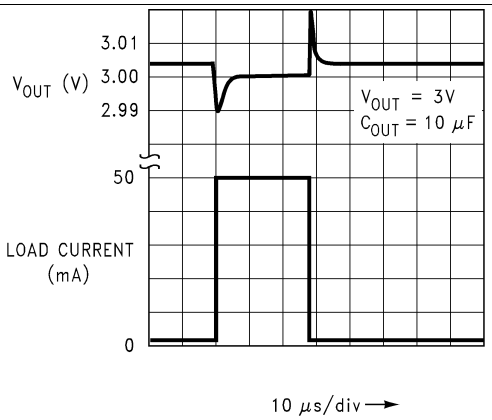


Figure 16. Load Transient Response

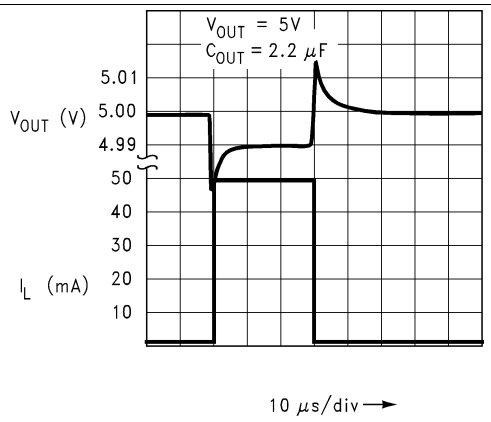


Figure 17. Load Transient Response

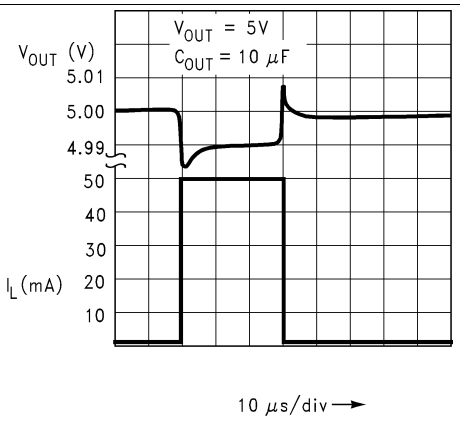


Figure 18. Load Transient Response

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

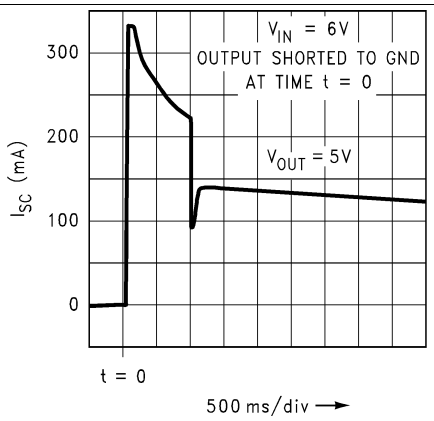


Figure 19. Short-Circuit Current

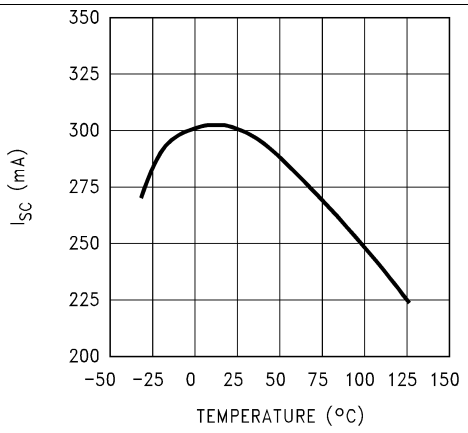


Figure 20. Instantaneous Short-Circuit Current vs Temperature

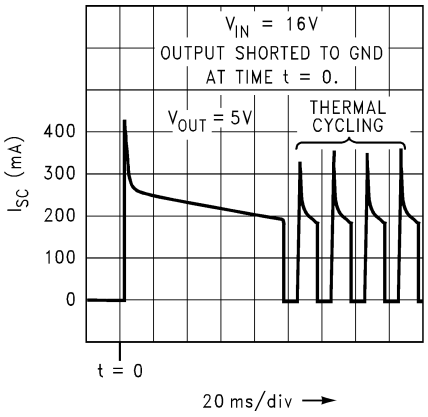


Figure 21. Short-Circuit Current

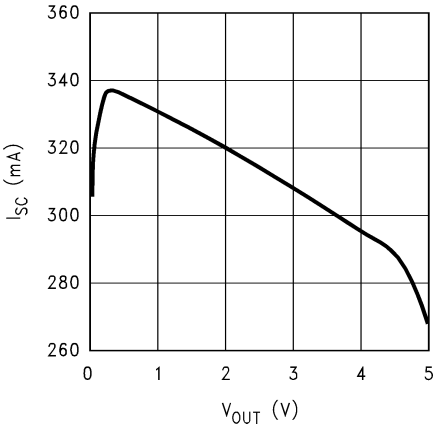


Figure 22. Instantaneous Short Circuit Current vs Output Voltage

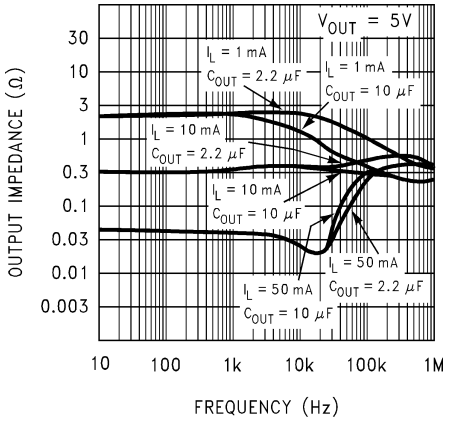


Figure 23. Output Impedance vs Frequency

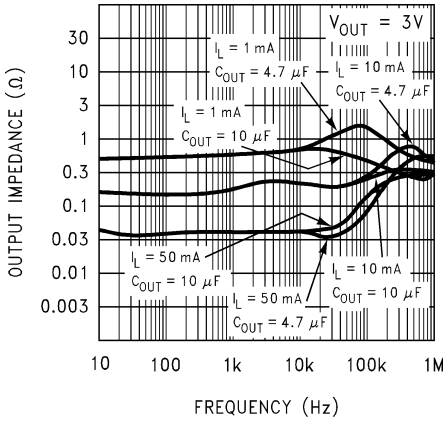


Figure 24. Output Impedance vs Frequency

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

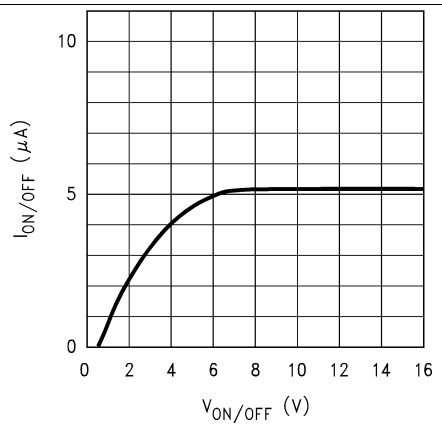


Figure 25. ON/$\overline{OFF}$ Pin Current Vs$V_{ON/OFF}$

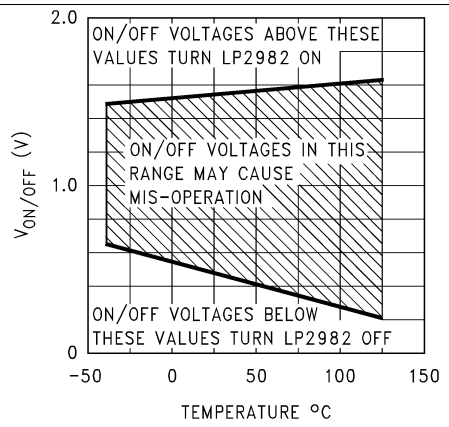


Figure 26. ON/$\overline{OFF}$ Threshold vs Temperature

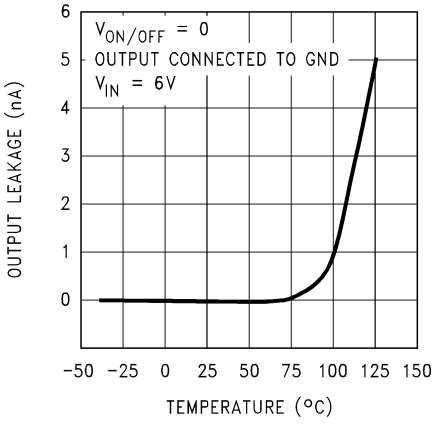


Figure 27. Input-to-Output Leakage vs Temperature

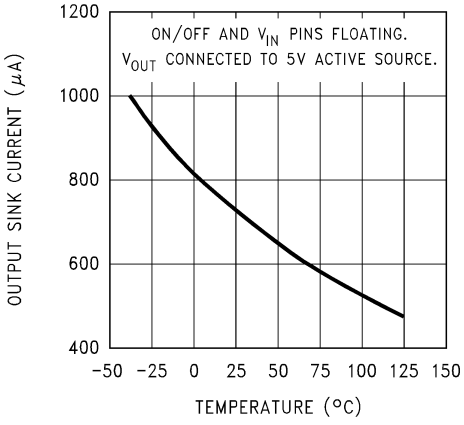


Figure 28. Output Reverse Leakage vs Temperature

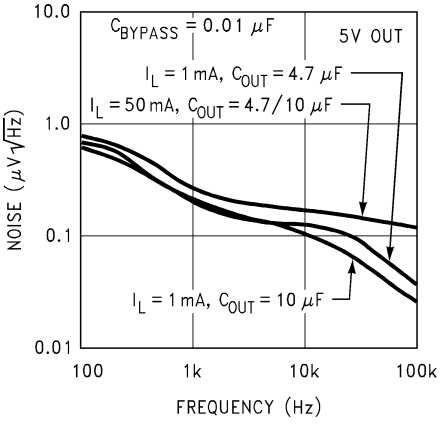


Figure 29. Output Noise Density

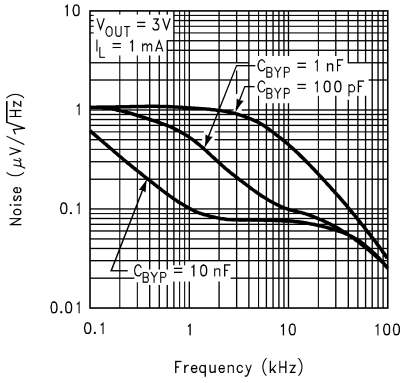


Figure 30. Output Noise Density

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

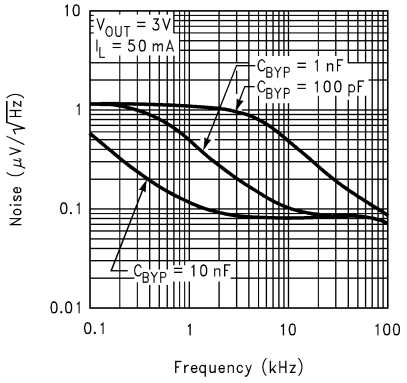


Figure 31. Output Noise Density

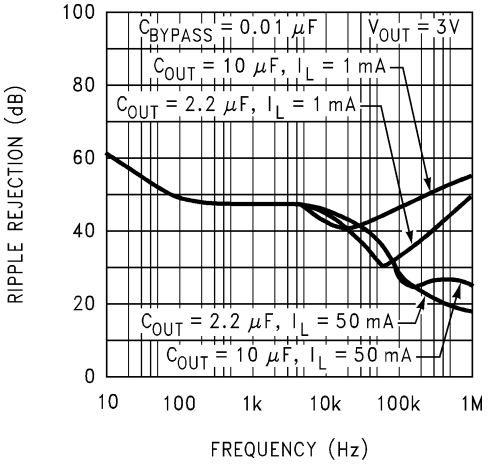


Figure 32. Ripple Rejection

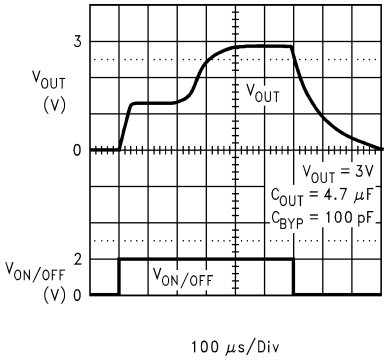


Figure 33. Turnon Waveform

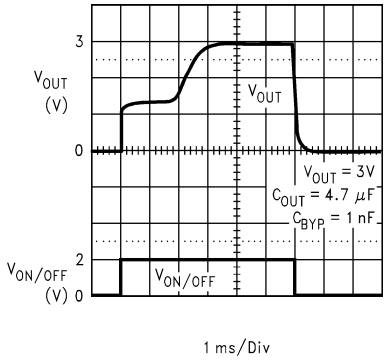


Figure 34. Turnon Waveform

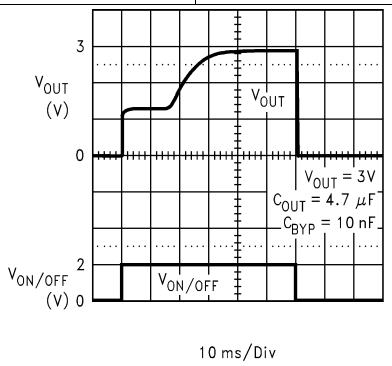


Figure 35. Turnon Waveform

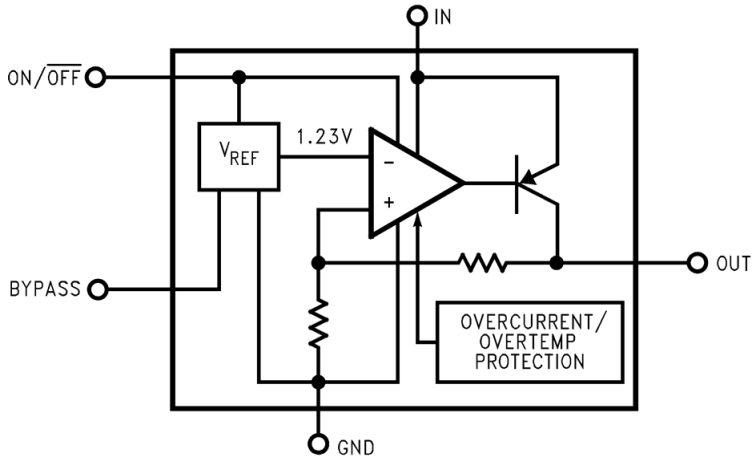
7 Detailed Description

7.1 Overview

The LP2982 is a 50-mA, fixed-output voltage regulator designed specifically to meet the requirements of battery-powered applications. Available in assorted output voltages (refer to the package option addendum (POA) at the back of this datasheet for the available voltage and package options), the device has an output tolerance of 1% for the A grade (1.5% for the non-A version). Using a VIP process, the LP2982 contains these features to facilitate battery-powered designs:

- Fixed 5-V, 3.3-V, and 3-V output versions
- Very high-accuracy 1.23-V reference
- Low-dropout voltage, typical dropout of 120 mV at a 50-mA load current and 7 mV at 1-mA load
- Low ground current, typically 375 μA at 50-mA load and 80 μA at 1-mA load
- A sleep-mode feature is available, allowing the regulator to consume only 1 μA (typical) when the ON/$\overline{\text{OFF}}$ pin is pulled low.
- Overtemperature protection and overcurrent protection circuitry is designed to safeguard the device during unexpected conditions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Multiple Voltage Options

To meet the different application requirements, the LP2982 provides multiple fixed output options (see *POA*).

7.3.2 High-Accuracy Output Voltage

With special careful design to minimize all contributions to the output voltage error, the LP2982 distinguishes itself as a very high-accuracy output voltage micropower LDO. This includes a tight initial tolerance (1% typical), extremely good line regulation (0.007%/V typical), and a very low output voltage temperature coefficient, making the device an ideal low-power voltage reference.

7.3.3 Ultra-Low-Dropout Voltage

Generally speaking, the dropout voltage often refers to the voltage difference between the input and output voltage ($V_{DO} = V_{IN} – V_{OUT}$), where the main current pass element (PNP) is fully on and is characterized by the classic $V_{CE(SAT)}$ of the transistor. V_{DO} indirectly specifies a minimum input voltage above the nominal programmed output voltage at which the output voltage is expected to remain within its accuracy boundary.

Feature Description (continued)

7.3.4 Low Ground Current

The LP2982 uses a vertical PNP process which allows for quiescent currents that are considerably lower than those associated with traditional lateral PNP regulators, typically 375 μA at 50-mA load and 80 μA at 1-mA load.

7.3.5 Sleep Mode

When pulling the ON/$\overline{\text{OFF}}$ pin to a low level ($V_{ON/OFF}$ < 0.15 V), LP2982 enters sleep mode, and less than 1-μA quiescent current is consumed. This function is designed for the application which needs a sleep mode to effectively enhance battery life cycle.

7.3.6 Short-Circuit Protection (Current Limit)

The internal current-limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. If a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO resulting in a thermal shutdown of the output. A foldback feature limits the short-circuit current to protect the regulator from damage under all load conditions. If OUT is forced below 0 V before EN goes high, and the load current required exceeds the foldback current limit, the device may not start up correctly.

7.3.7 Thermal Protection

The LP2982 contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. The thermal time-constant of the semiconductor die is fairly short, and thus the output cycles on and off at a high rate when thermal shutdown is reached until the power dissipation is reduced. The internal protection circuitry of the LM2982 is designed to protect against thermal overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown degrades its reliability.

7.4 Device Functional Modes

7.4.1 Operation with $V_{OUT(TARGET)}$ + 1 V ≤ V_{IN} < 16 V

The device operates if the input voltage is equal to, or exceeds, $V_{OUT(TARGET)}$ + 0.6 V. At input voltages below the minimum V_{IN} requirement, the device does not operate correctly, and output voltage may not reach target value.

7.4.2 Operation With ON/$\overline{\text{OFF}}$ Control

If the voltage on the ON/OFF pin is less than 0.15 V, the device is disabled, and the shutdown current does not exceed 1 μA. Raising ON/OFF above 1.4 V initiates the start-up sequence of the device.

8 Application and Implementation

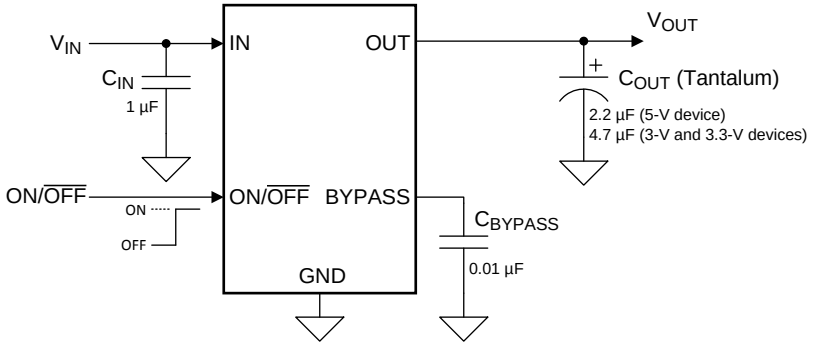
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP2982 is a linear voltage regulator operating from 2.1 V to 16 V on the input and regulates voltages between 3 V to 5 V with 1% accuracy and 50-mA maximum output current. Efficiency is defined by the ratio of output voltage to input voltage because the LP2982 is a linear voltage regulator. To achieve high efficiency, the dropout voltage ($V_{IN} – V_{OUT}$) must be as small as possible, thus requiring a very-low-dropout LDO. Successfully implementing an LDO in an application depends on the application requirements. If the requirements are simply input voltage and output voltage, compliance specifications (such as internal power dissipation or stability) must be verified to ensure a solid design. If timing, start-up, noise, power supply rejection ratio (PSRR), or any other transient specification is required, then the design becomes more challenging.

8.2 Typical Application



ON/$\overline{OFF}$ input must be actively terminated. Tie to V_{IN} if this function is not to be used.
Minimum output capacitance is shown to insure stability over full load current range. More capacitance provides superior dynamic performance and additional stability margin (see *Capacitor Characteristics*).

Figure 36. LP2982 Typical Application

8.2.1 Design Requirements

PARAMETER	DESIGN REQUIREMENT
Input voltage	5 V ±10%
Output voltage	3.3 V ±3.5%
Output current	50 mA
Ambient temperature	85°C

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

Like any low-dropout regulator, the external capacitors used with the LP2982 must be carefully selected to assure regulator loop stability.

8.2.2.1.1 Input Capacitor

An input capacitor with a value ≥ 1 μF is required with the LP2982 (amount of capacitance can be increased without limit).

This capacitor must be located a distance of not more than 0.5 inches from the input pin of the LP2982 and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor.

8.2.2.1.2 Output Capacitor

The output capacitor must meet both the requirement for minimum amount of capacitance and equivalent series resistance (ESR) value. Curves are provided which show the allowable ESR range as a function of load current for various output voltages and capacitor values (refer to Figure 40 and Figure 41).

NOTE

Important: The output capacitor must maintain its ESR in the stable region over the full operating temperature range to ensure stability. Also, capacitor tolerance and variation with temperature must be considered to ensure the minimum amount of capacitance is provided at all times.

This capacitor must be located not more than 0.5 inches from the OUT pin of the LP2982 and returned to a clean analog ground.

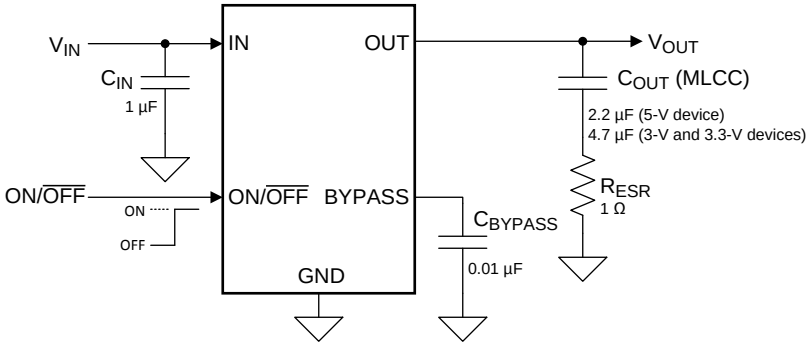


Figure 37. Typical Application With Ceramic C_{OUT} Series R

8.2.2.1.3 Bypass Capacitor

The 0.01-μF capacitor connected to the bypass pin to reduce noise must have very low leakage.

The current flowing out of the bypass pin comes from the bandgap reference, which is used to set the output voltage.

This capacitor leakage current causes the output voltage to decline by an amount proportional to the current. Typical values are −0.015%/nA at −40°C, −0.021%/nA at 25°C, and −0.035%/nA at 125°C.

This data is valid up to a maximum leakage current of about 500 nA, beyond which the bandgap is so severely loaded that it can not function.

Care must be taken to ensure that the capacitor selected does not have excessive leakage current over the operating temperature range of the application.

A high-quality ceramic capacitor which uses either NPO or COG type dielectric material typically has very low leakage. Small surface mount polypropylene or polycarbonate film capacitors also have extremely low leakage, but are slightly larger than ceramics.

8.2.2.2 Capacitor Characteristics

8.2.2.2.1 Tantalum

Tantalum capacitors are the best choice for use with the LP2982. Most good quality tantalums can be used with the LP2982, but check the manufacturer's data sheet to be sure the ESR is in range.

It is important to remember that ESR increases at lower temperatures and a capacitor that is near the upper limit for stability at room temperature can cause instability when it gets cold.

In applications which must operate at very low temperatures, it may be necessary to parallel the output tantalum capacitor with a ceramic capacitor to prevent the ESR from going up too high (see *Ceramic* for important information on ceramic capacitors).

8.2.2.2.2 Ceramic

TI does not recommend use of ceramic capacitors at the output of the LP2982. This is because the ESR of a ceramic can be low enough to go below the minimum stable value for the LP2982. A 2.2-μF ceramic was measured and found to have an ESR of about 15 mΩ, which is low enough to cause oscillations.

If a ceramic capacitor is used on the output, a 1-Ω resistor must be placed in series with the capacitor.

8.2.2.2.3 Aluminum

Because of large physical size, aluminum electrolytics are not typically used with the LP2982. They must meet the same ESR requirements over the operating temperature range, more difficult because of their steep increase at cold temperature.

An aluminum electrolytic can exhibit an ESR increase of as much as 50× when going from 20°C to −40°C. Also, some aluminum electrolytics are not operational below −25°C because the electrolyte can freeze.

8.2.2.3 Reverse Current Path

The internal PNP power transistor used as the pass element in the LP2982 has an inherent diode connected between the regulator output and input. During normal operation (where the input voltage is higher than the output) this diode is reverse biased (see Figure 38).

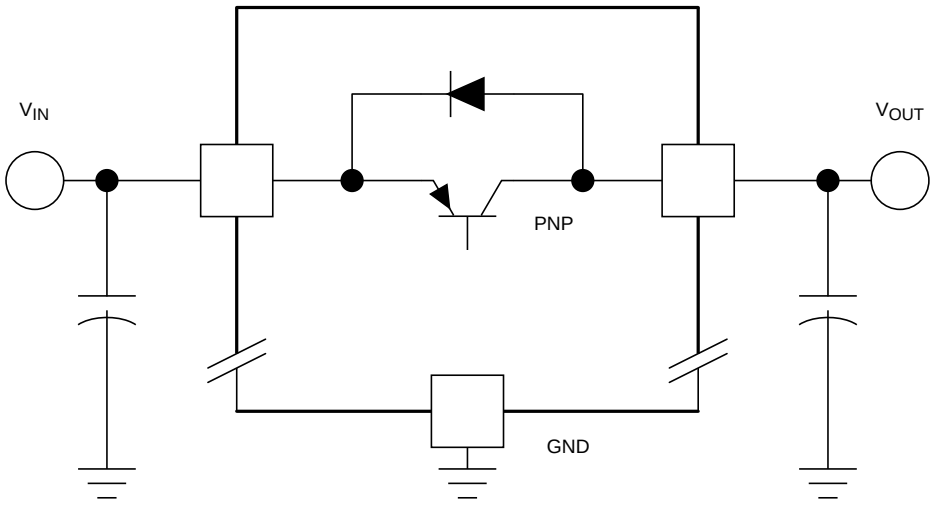


Figure 38. LP2982 Reverse Current Path

However, if the input voltage is more than a V_{BE} below the output voltage, this diode will turn ON and current will flow into the regulator output. In such cases, a parasitic SCR can latch which will allow a high current to flow into the V_{IN} pin and out the ground pin, which can damage the part.

The internal diode can also be turned on if the input voltage is abruptly stepped down to a voltage which is a V_{BE} below the output voltage.

In any application where the output voltage may be higher than the input voltage, an external Schottky diode must be connected from V_{IN} to V_{OUT} (cathode on V_{IN}, anode on V_{OUT}; see Figure 39), to limit the reverse voltage across the LP2982 to 0.3 V (see *Absolute Maximum Ratings*).

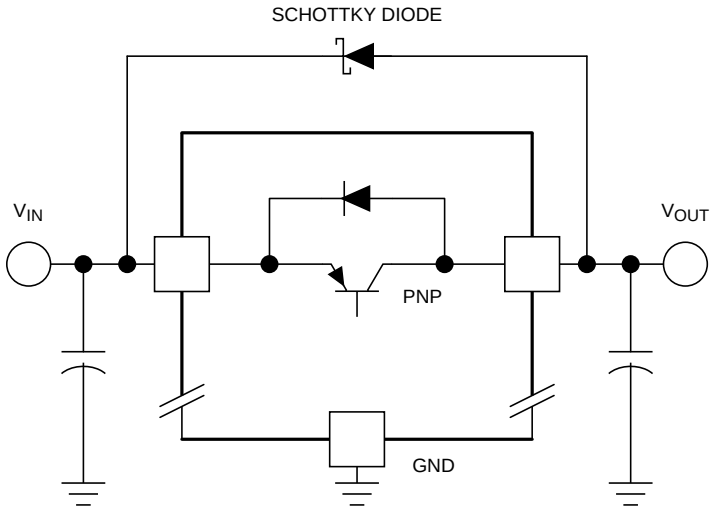


Figure 39. Adding External Schottky Diode Protection

8.2.2.4 ON/$\overline{OFF}$ Input Operation

The LP2982 is shut off by pulling the ON/$\overline{OFF}$ input low, and turned on by driving the input high. If this feature is not to be used, the ON/$\overline{OFF}$ input should be tied to V_{IN} to keep the regulator on at all times (the ON/$\overline{OFF}$ input must **not** be left floating).

To ensure proper operation, the signal source used to drive the ON/$\overline{OFF}$ input must be able to swing above and below the specified turnon/turnoff voltage thresholds which specify an ON or $\overline{OFF}$ state (see *Electrical Characteristics*).

The ON/$\overline{OFF}$ signal may come from either a totem-pole output, or an open-collector output with pullup resistor to the LP2982 input voltage or another logic supply. The high-level voltage may exceed the LP2982 input voltage, but must remain within the *Absolute Maximum Ratings* for the ON/$\overline{OFF}$ pin.

It is also important that the turnon/turnoff voltage signals applied to the ON/$\overline{OFF}$ input have a slew rate which is greater than 40 mV/μs.

NOTE

IMPORTANT: The regulator shutdown function does not operate correctly if a slow-moving signal is applied to the ON/$\overline{OFF}$ input.

8.2.2.5 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane connected to the tab or pad is critical to ensuring reliable operation. Device power dissipation depends on input voltage, output voltage, and load conditions and can be calculated with Equation 1.

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT} \quad (1)$$

Power dissipation can be minimized, and greater efficiency can be achieved, by using the lowest available voltage drop option that is greater than the dropout voltage (V_{DO}). However, keep in mind that higher voltage drops result in better dynamic (that is, PSRR and transient) performance.

On the LP2982 SOT-23 (DBV) package, the primary conduction path for heat is through the five leads to the PCB. The ground pin (pin 2) is attached directly to the back side of the die and should be accorded extra copper area on the PCB. The maximum allowable junction temperature ($T_{J(MAX)}$) determines maximum power dissipation allowed ($P_{D(MAX)}$) for the device package. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 2 or Equation 3:

$$T_{J(MAX)} = T_{A(MAX)} + (R_{\theta JA} \times P_{D(MAX)}) \quad (2)$$

$$P_D = (T_{J(MAX)} - T_{A(MAX)}) / R_{\theta JA} \quad (3)$$

Unfortunately, this $R_{\theta JA}$ is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in *Thermal Information* is determined by the specific EIA/JEDEC JESD51-7 standard for PCB and copper-spreading area and is to be used only as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-board thermal resistance ($R_{\theta JB}$) plus the thermal resistance contribution by the PCB copper area acting as a heat sink.

8.2.2.6 Estimating Junction Temperature

The EIA/JEDEC standard recommends the use of psi (Ψ) thermal characteristics to estimate the junction temperatures of surface mount devices on a typical PCB board application. These characteristics are not true thermal resistance values, but rather package specific thermal characteristics that offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal characteristics (Ψ_{JT} and Ψ_{JB}) are given in *Thermal Information* and are used in accordance with Equation 4 or Equation 5.

$$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)})$$

where

- $P_{D(MAX)}$ is explained in Equation 3
- T_{TOP} is the temperature measured at the center-top of the device package. (4)

$$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)})$$

where

- $P_{D(MAX)}$ is explained in Equation 3.
- T_{BOARD} is the PCB surface temperature measured 1 mm from the device package and centered on the package edge. (5)

For more information about the thermal characteristics Ψ_{JT} and Ψ_{JB}, see *Semiconductor and IC Package Thermal Metrics* (SPRA953); for more information about measuring T_{TOP} and T_{BOARD}, see *Using New Thermal Metrics* (SBVA025); and for more information about the EIA/JEDEC JESD51 PCB used for validating $R_{\theta JA}$, see the TI Application Report *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017). These application notes are available at www.ti.com.

8.2.3 Application Curves

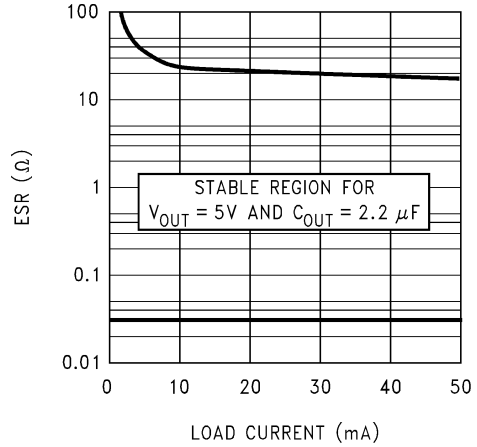


Figure 40. 5-V, 2.2-µF ESR Curves

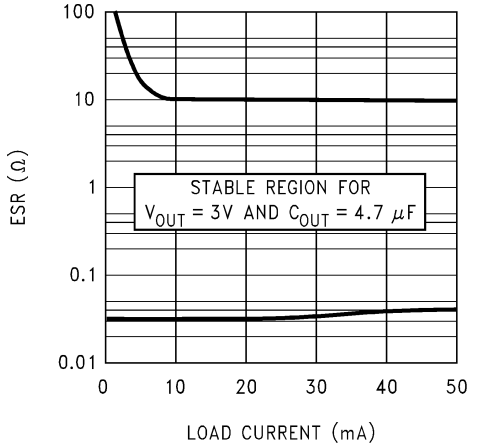


Figure 41. 3-V, 4.7-µF ESR Curves

9 Power Supply Recommendations

The LP2982 is designed to operate from an input voltage supply range between between $V_{OUT(NOM)}$ + 1 V and 16 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

10.2 Layout Example

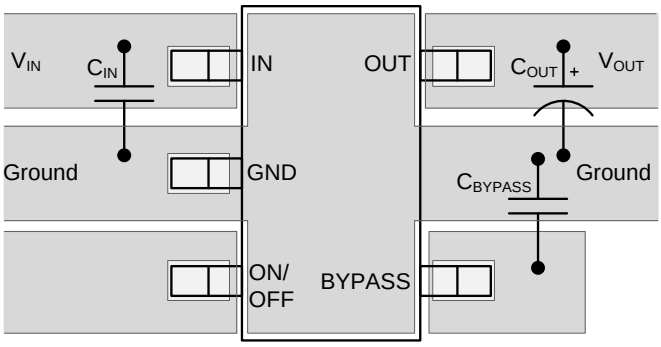


Figure 42. LP2982 Layout Example

11 Device and Documentation Support

11.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Documentation Support

11.2.1 Related Documentation

For additional information, see the following:

- TI Application Report *Semiconductor and IC Package Thermal Metrics* (SPRA953)
- TI Application Report *Using New Thermal Metrics* (SBVA025)
- TI Application Report *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017)

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2982AIM5-3.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L20A	Samples
LP2982AIM5-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L19A	Samples
LP2982AIM5-5.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L18A	Samples
LP2982AIM5X-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L20A	Samples
LP2982AIM5X-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L19A	Samples
LP2982AIM5X-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L18A	Samples
LP2982IM5-3.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L20B	Samples
LP2982IM5-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L19B	Samples
LP2982IM5-5.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L18B	Samples
LP2982IM5X-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L20B	Samples
LP2982IM5X-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L19B	Samples
LP2982IM5X-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L18B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

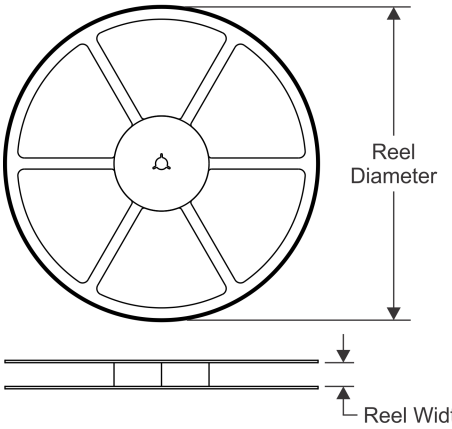
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

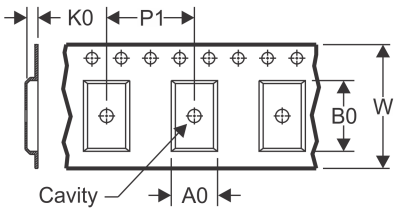
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

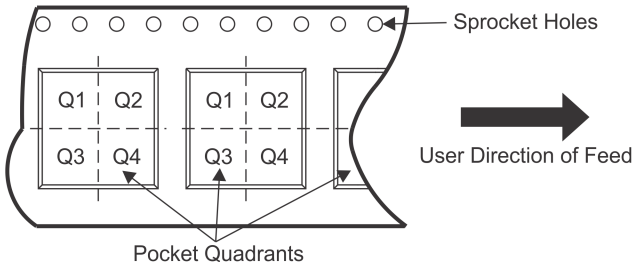


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

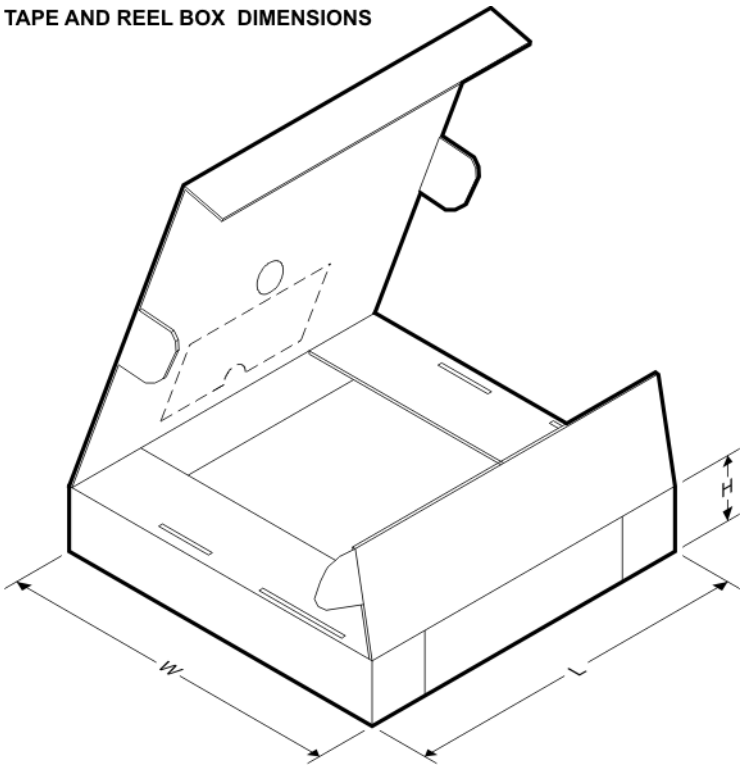
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2982AIM5-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5-5.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5X-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5-5.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5X-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

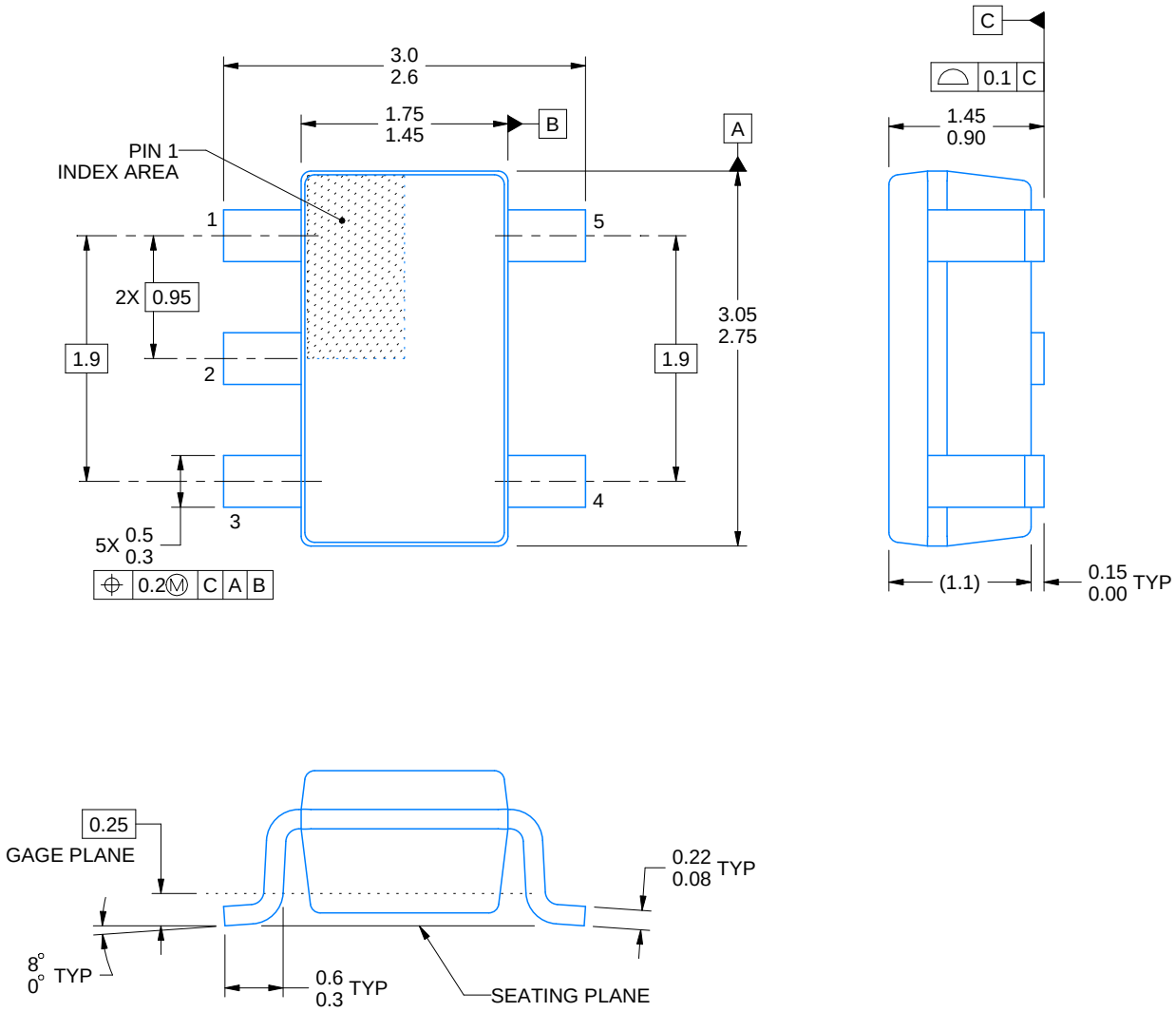
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2982AIM5-3.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2982AIM5-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2982AIM5-5.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2982AIM5X-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2982AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2982AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2982IM5-3.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2982IM5-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2982IM5-5.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2982IM5X-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2982IM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2982IM5X-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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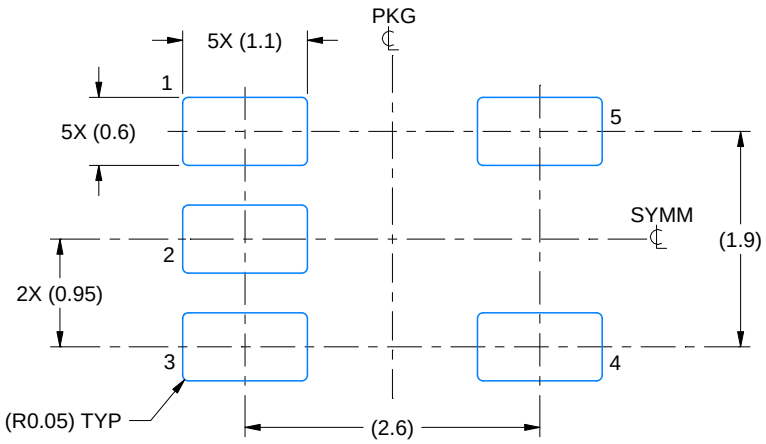
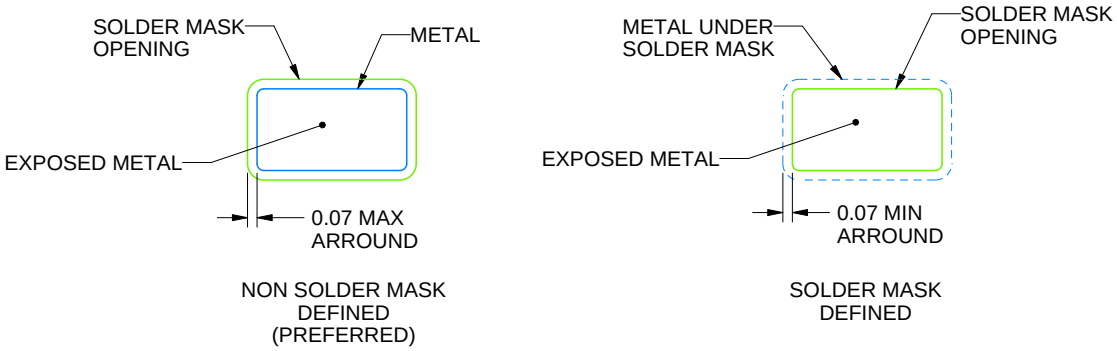
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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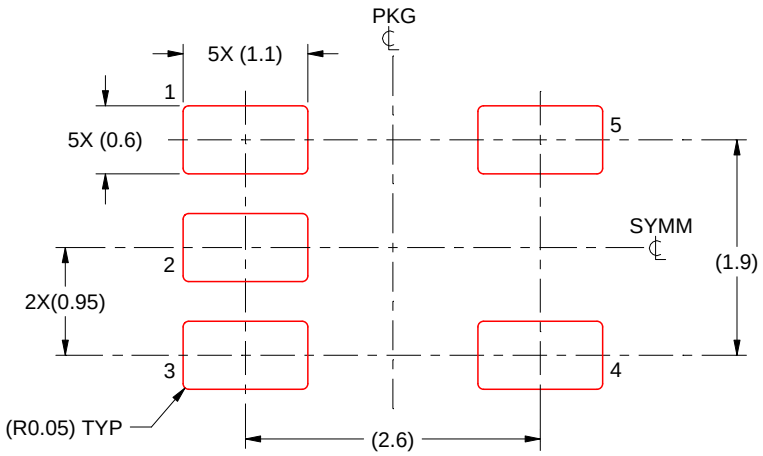
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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