PCAL9555A

Low-voltage 16-bit I²C-bus GPIO with Agile I/O, interrupt and weak pull-up

Rev. 2 — 19 December 2014 Product data sheet

1. General description

The PCAL9555A is a low-voltage 16-bit General Purpose Input/Output (GPIO) expander with interrupt and weak pull-up resistors for I²C-bus/SMBus applications. NXP I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum, for example, in ACPI power switches, sensors, push buttons, LEDs, fan control, etc.

In addition to providing a flexible set of GPIOs, the wide V_{DD} range of 1.65 V to 5.5 V allows the PCAL9555A to interface with next-generation microprocessors and microcontrollers where supply levels are dropping down to conserve power.

The PCAL9555A contains the PCA9555 register set of four pairs of 8-bit Configuration, Input, Output, and Polarity Inversion registers, and additionally, the PCAL9555A has Agile I/O, which are additional features specifically designed to enhance the I/O. These additional features are: programmable output drive strength, latchable inputs, programmable pull-up/pull-down resistors, maskable interrupt, interrupt status register, programmable open-drain or push-pull outputs.

The PCAL9555A is a pin-to-pin replacement to the PCA9555, however, the PCAL9555A powers up with all I/O interrupts masked. This mask default allows for a board bring-up free of spurious interrupts at power-up.

The PCAL9555A open-drain interrupt ($\overline{\text{INT}}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

$\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. Thus, the PCAL9555A can remain a simple slave device.

The device outputs have 25 mA sink capabilities for directly driving LEDs while consuming low device current.

The power-on reset sets the registers to their default values and initializes the device state machine.

The device powers on with weak pull-up resistors enabled that can replace external components.

Three hardware pins (A0, A1, A2) select the fixed I²C-bus address and allow up to eight devices to share the same I²C-bus/SMBus.

2. Features and benefits

- I^2C-bus to parallel port expander
- Operating power supply voltage range of 1.65 V to 5.5 V
- Low standby current consumption:
  - 1.5 μA (typical at 5 V V_{DD})
  - 1.0 μA (typical at 3.3 V V_{DD})
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
  - $V_{hys} = 0.10 \times V_{DD}$ (typical)
- 5 V tolerant I/Os
- Open-drain active LOW interrupt output ($\overline{INT}$)
- 400 kHz Fast-mode I^2C-bus
- Internal power-on reset
- Power-up with all channels configured as inputs and weak pull-up resistors
- No glitch on power-up
- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD78, Class II
- ESD protection exceeds JESD22
  - 2000 V Human Body Model (A114-A)
  - 1000 V Charged-Device Model (C101)
- Packages offered: TSSOP24, HVQFN24

2.1 Agile I/O features

- Pin to pin replacement for PCA9555 and PCA9555A with interrupts disabled at power-up
  - Software backward compatible with PCA9555 and PCA9555A
- Output port configuration: bank selectable push-pull or open-drain output stages
- Interrupt status: read-only register identifies the source of an interrupt
- Bit-wise I/O programming features:
  - Output drive strength: four programmable drive strengths to reduce rise and fall times in low capacitance applications
  - Input latch: Input Port register values changes are kept until the Input Port register is read
  - Pull-up/pull-down enable: floating input or pull-up/down resistor enable
  - Pull-up/pull-down selection: 100 kΩ pull-up/down resistor selection
  - Interrupt mask: mask prevents the generation of the interrupt when input changes state

3. Ordering information

Table 1. Ordering information

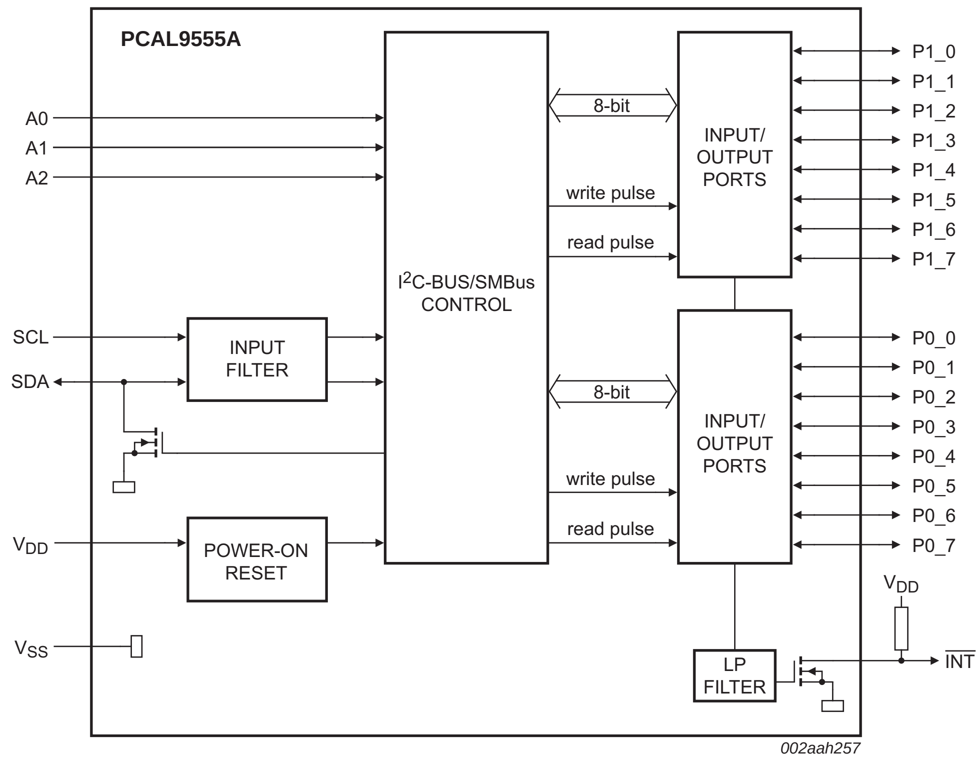
Type number	Topside mark	Package		
		Name	Description	Version
PCAL9555AHF	L55A	HWQFN24	plastic thermal enhanced very very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.75 mm	SOT994-1
PCAL9555APW	PCAL9555A	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCAL9555AHF	PCAL9555AHF,128	HWQFN24	Reel pack, SMD, 13-inch, Turned	6000	T_{amb} = –40 °C to +85 °C
PCAL9555APW	PCAL9555APW,118	TSSOP24	Reel pack, SMD, 13-inch	2500	T_{amb} = –40 °C to +85 °C

4. Block diagram



Remark: All I/Os are set to inputs at reset.

Fig 1. Block diagram of PCAL9555A

5. Pinning information

5.1 Pinning

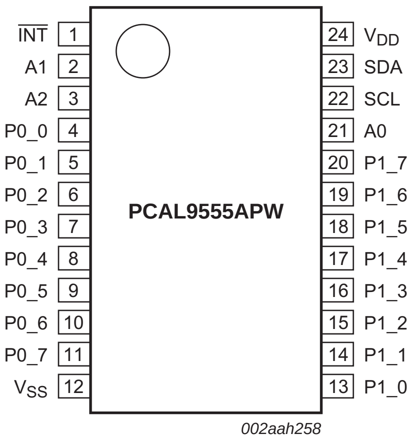


Fig 2. Pin configuration for TSSOP24

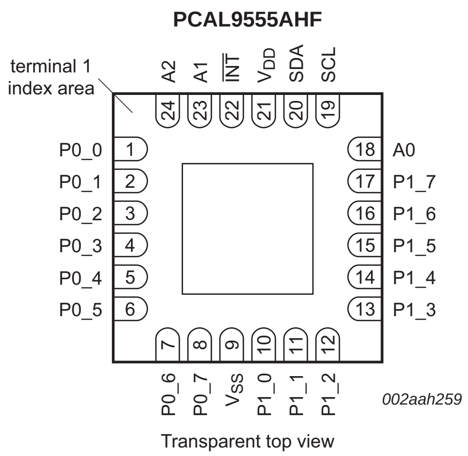


Fig 3. Pin configuration for HWQFN24

5.2 Pin description

Table 3. Pin description

Symbol	Pin		Type	Description
	TSSOP24	HWQFN24		
INT	1	22	O	Interrupt output. Connect to V_{DD} through a pull-up resistor.
A1	2	23	I	Address input 1. Connect directly to V_{DD} or V_{SS}.
A2	3	24	I	Address input 2. Connect directly to V_{DD} or V_{SS}.
P0_0[2]	4	1	I/O	Port 0 input/output 0.
P0_1[2]	5	2	I/O	Port 0 input/output 1.
P0_2[2]	6	3	I/O	Port 0 input/output 2.
P0_3[2]	7	4	I/O	Port 0 input/output 3.
P0_4[2]	8	5	I/O	Port 0 input/output 4.
P0_5[2]	9	6	I/O	Port 0 input/output 5.
P0_6[2]	10	7	I/O	Port 0 input/output 6.
P0_7[2]	11	8	I/O	Port 0 input/output 7.
V_{SS}	12	9[1]	power	Ground.
P1_0[3]	13	10	I/O	Port 1 input/output 0.
P1_1[3]	14	11	I/O	Port 1 input/output 1.
P1_2[3]	15	12	I/O	Port 1 input/output 2.
P1_3[3]	16	13	I/O	Port 1 input/output 3.
P1_4[3]	17	14	I/O	Port 1 input/output 4.
P1_5[3]	18	15	I/O	Port 1 input/output 5.
P1_6[3]	19	16	I/O	Port 1 input/output 6.

Table 3. Pin description *...continued*

Symbol	Pin		Type	Description
	TSSOP24	HWQFN24		
P1_7[3]	20	17	I/O	Port 1 input/output 7.
A0	21	18	I	Address input 0. Connect directly to V_{DD} or V_{SS}.
SCL	22	19	I	Serial clock bus. Connect to V_{DD} through a pull-up resistor.
SDA	23	20	I/O	Serial data bus. Connect to V_{DD} through a pull-up resistor.
V_{DD}	24	21	power	Supply voltage.

[1] HWQFN24 package die supply ground is connected to both V_{SS} pin and exposed center pad. V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

[2] Pins P0_0 to P0_7 correspond to bits P0.0 to P0.7. At power-up, all I/O are configured as high-impedance inputs.

[3] Pins P1_0 to P1_7 correspond to bits P1.0 to P1.7. At power-up, all I/O are configured as high-impedance inputs.

6. Functional description

Refer to Figure 1 “Block diagram of PCAL9555A”.

6.1 Device address

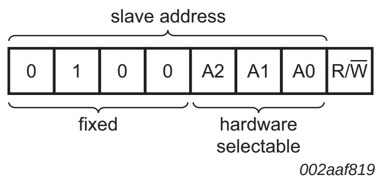


Fig 4. PCAL9555A device address

A2, A1 and A0 are the hardware address package pins and are held to either HIGH (logic 1) or LOW (logic 0) to assign one of the eight possible slave addresses. The last bit of the slave address (R/$\overline{W}$) defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

6.2 Registers

6.2.1 Pointer register and command byte

Following the successful acknowledgement of the address byte, the bus master sends a command byte, which is stored in the Pointer register in the PCAL9555A. The lower three bits of this data byte state the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that will be affected. Bit 6 in conjunction with the lower four bits of the Command byte are used to point to the extended features of the device (Agile I/O). This register is write only.

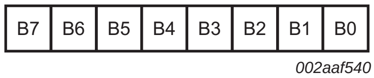


Fig 5. Pointer register bits

Table 4. Command byte

Pointer register bits								Command byte (hexadecimal)	Register	Protocol	Power-up default
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00h	Input port 0	read byte	xxxx xxxx[1]
0	0	0	0	0	0	0	1	01h	Input port 1	read byte	xxxx xxxx
0	0	0	0	0	0	1	0	02h	Output port 0	read/write byte	1111 1111
0	0	0	0	0	0	1	1	03h	Output port 1	read/write byte	1111 1111
0	0	0	0	0	1	0	0	04h	Polarity Inversion port 0	read/write byte	0000 0000
0	0	0	0	0	1	0	1	05h	Polarity Inversion port 1	read/write byte	0000 0000
0	0	0	0	0	1	1	0	06h	Configuration port 0	read/write byte	1111 1111
0	0	0	0	0	1	1	1	07h	Configuration port 1	read/write byte	1111 1111
0	1	0	0	0	0	0	0	40h	Output drive strength register 0	read/write byte	1111 1111
0	1	0	0	0	0	0	1	41h	Output drive strength register 0	read/write byte	1111 1111
0	1	0	0	0	0	1	0	42h	Output drive strength register 1	read/write byte	1111 1111
0	1	0	0	0	0	1	1	43h	Output drive strength register 1	read/write byte	1111 1111
0	1	0	0	0	1	0	0	44h	Input latch register 0	read/write byte	0000 0000
0	1	0	0	0	1	0	1	45h	Input latch register 1	read/write byte	0000 0000
0	1	0	0	0	1	1	0	46h	Pull-up/pull-down enable register 0	read/write byte	1111 1111
0	1	0	0	0	1	1	1	47h	Pull-up/pull-down enable register 1	read/write byte	1111 1111
0	1	0	0	1	0	0	0	48h	Pull-up/pull-down selection register 0	read/write byte	1111 1111
0	1	0	0	1	0	0	1	49h	Pull-up/pull-down selection register 1	read/write byte	1111 1111
0	1	0	0	1	0	1	0	4Ah	Interrupt mask register 0	read/write byte	1111 1111
0	1	0	0	1	0	1	1	4Bh	Interrupt mask register 1	read/write byte	1111 1111
0	1	0	0	1	1	0	0	4Ch	Interrupt status register 0	read byte	0000 0000
0	1	0	0	1	1	0	1	4Dh	Interrupt status register 1	read byte	0000 0000
0	1	0	0	1	1	1	1	4Fh	Output port configuration register	read/write byte	0000 0000

[1] Undefined.

6.2.2 Input port register pair (00h, 01h)

The Input port registers (registers 0 and 1) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port registers are read only; writes to these registers have no effect. The default value ‘X’ is determined by the externally applied logic level. An Input port register read operation is performed as described in Section 7.2 “Reading the port registers”.

Table 5. Input port 0 register (address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 6. Input port 1 register (address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

6.2.3 Output port register pair (02h, 03h)

The Output port registers (registers 2 and 3) show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, **not** the actual pin value. A register pair write is described in Section 7.1 and a register pair read is described in Section 7.2.

Table 7. Output port 0 register (address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 8. Output port 1 register (address 03h)

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

6.2.4 Polarity inversion register pair (04h, 05h)

The Polarity inversion registers (registers 4 and 5) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with ‘1’), the corresponding port pin’s polarity is inverted in the Input register. If a bit in this register is cleared (written with a ‘0’), the corresponding port pin’s polarity is retained. A register pair write is described in Section 7.1 and a register pair read is described in Section 7.2.

Table 9. Polarity inversion port 0 register (address 04h)

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 10. Polarity inversion port 1 register (address 05h)

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

6.2.5 Configuration register pair (06h, 07h)

The Configuration registers (registers 6 and 7) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output. A register pair write is described in Section 7.1 and a register pair read is described in Section 7.2.

Table 11. Configuration port 0 register (address 06h)

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 12. Configuration port 1 register (address 07h)

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

6.2.6 Output drive strength register pairs (40h, 41h, 42h, 43h)

The Output drive strength registers control the output drive level of the GPIO. Each GPIO can be configured independently to a certain output current level by two register control bits. For example, Port 0.7 is controlled by register 41 bits CC0.7 (bits [7:6]), Port 0.6 is controlled by register 41 CC0.6(bits [5:4]). The output drive level of the GPIO is programmed 00b = 0.25×, 01b = 0.50×, 10b = 0.75×, or 11b = 1× of the maximum drive capability of the I/O. See Section 8.2 “Output drive strength control”. A register pair write is described in Section 7.1 and a register pair read is described in Section 7.2.

Table 13. Current control port 0 register (address 40h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC0.3		CC0.2		CC0.1		CC0.0	
Default	1	1	1	1	1	1	1	1

Table 14. Current control port 0 register (address 41h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC0.7		CC0.6		CC0.5		CC0.4	
Default	1	1	1	1	1	1	1	1

Table 15. Current control port 1 register (address 42h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC1.3		CC1.2		CC1.1		CC1.0	
Default	1	1	1	1	1	1	1	1

Table 16. Current control port 1 register (address 43h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC1.7		CC1.6		CC1.5		CC1.4	
Default	1	1	1	1	1	1	1	1

6.2.7 Input latch register pair (44h, 45h)

The input latch registers (registers 44 and 45) enable and disable the input latch of the I/O pins. These registers are effective only when the pin is configured as an input port. When an input latch register bit is 0, the corresponding input pin state is not latched. A state change of the corresponding input pin generates an interrupt. A read of the input register clears the interrupt. If the input goes back to its initial logic state before the input port register is read, then the interrupt is cleared.

When an input latch register bit is 1, the corresponding input pin state is latched. A change of state in the input generates an interrupt and the input logic value is loaded into the corresponding bit of the input port register (registers 0 and 1). A read of the input port register clears the interrupt. If the input pin returns to its initial logic state before the input port register is read, then the interrupt is not cleared and the corresponding bit of the input port register keeps the logic value that initiated the interrupt. See Figure 12 “Read input port register (latch enabled), scenario 3”.

For example, if the P0_4 input was as logic 0 and the input goes to logic 1 then back to logic 0, the input port 0 register will capture this change and an interrupt is generated (if unmasked). When the read is performed on the input port 0 register, the interrupt is cleared, assuming there were no additional input(s) that have changed, and bit 4 of the input port 0 register will read ‘1’. The next read of the input port 0 register bit 4 register should now read ‘0’.

An interrupt remains active when a non-latched input simultaneously switches state with a latched input and then returns to its original state. A read of the input register reflects only the change of state of the latched input and also clears the interrupt. The interrupt is not cleared if the input latch register changes from latched to non-latched configuration. If the input pin is changed from latched to non-latched input, a read from the input port register reflects the current port logic level. If the input pin is changed from non-latched to latched input, the read from the input register reflects the latched logic level. A register pair write is described in Section 7.1 and a register pair read is described in Section 7.2.

Table 17. Input latch port 0 register (address 44h)

Bit	7	6	5	4	3	2	1	0
Symbol	L0.7	L0.6	L0.5	L0.4	L0.3	L0.2	L0.1	L0.0
Default	0	0	0	0	0	0	0	0

Table 18. Input latch port 1 register (address 45h)

Bit	7	6	5	4	3	2	1	0
Symbol	L1.7	L1.6	L1.5	L1.4	L1.3	L1.2	L1.1	L1.0
Default	0	0	0	0	0	0	0	0

6.2.8 Pull-up/pull-down enable register pair (46h, 47h)

These registers allow the user to enable or disable pull-up/pull-down resistors on the I/O pins. Setting the bit to logic 1 enables the selection of pull-up/pull-down resistors. Setting the bit to logic 0 disconnects the pull-up/pull-down resistors from the I/O pins. Also, the resistors will be disconnected when the outputs are configured as open-drain outputs (see Section 6.2.12). Use the pull-up/pull-down registers to select either a pull-up or pull-down resistor. A register pair write is described in Section 7.1 and a register pair read is described in Section 7.2.

Table 19. Pull-up/pull-down enable port 0 register (address 46h)

Bit	7	6	5	4	3	2	1	0
Symbol	PE0.7	PE0.6	PE0.5	PE0.4	PE0.3	PE0.2	PE0.1	PE0.0
Default	1	1	1	1	1	1	1	1

Table 20. Pull-up/pull-down enable port 1 register (address 47h)

Bit	7	6	5	4	3	2	1	0
Symbol	PE1.7	PE1.6	PE1.5	PE1.4	PE1.3	PE1.2	PE1.1	PE1.0
Default	1	1	1	1	1	1	1	1

6.2.9 Pull-up/pull-down selection register pair (48h, 49h)

The I/O port can be configured to have a pull-up or pull-down resistor by programming the pull-up/pull-down selection register. Setting a bit to logic 1 selects a 100 kΩ pull-up resistor for that I/O pin. Setting a bit to logic 0 selects a 100 kΩ pull-down resistor for that I/O pin. If the pull-up/pull-down feature is disconnected, writing to this register will have no effect on I/O pin. Typical value is 100 kΩ with minimum of 50 kΩ and maximum of 150 kΩ. A register pair write is described in Section 7.1 and a register pair read is described in Section 7.2.

Table 21. Pull-up/pull-down selection port 0 register (address 48h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD0.7	PUD0.6	PUD0.5	PUD0.4	PUD0.3	PUD0.2	PUD0.1	PUD0.0
Default	1	1	1	1	1	1	1	1

Table 22. Pull-up/pull-down selection port 1 register (address 49h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD1.7	PUD1.6	PUD1.5	PUD1.4	PUD1.3	PUD1.2	PUD1.1	PUD1.0
Default	1	1	1	1	1	1	1	1

6.2.10 Interrupt mask register pair (4Ah, 4Bh)

Interrupt mask registers are set to logic 1 upon power-on, disabling interrupts during system start-up. Interrupts may be enabled by setting corresponding mask bits to logic 0. If an input changes state and the corresponding bit in the Interrupt mask register is set to 1, the interrupt is masked and the interrupt pin will not be asserted. If the corresponding bit in the Interrupt mask register is set to 0, the interrupt pin will be asserted.

When an input changes state and the resulting interrupt is masked (interrupt mask bit is 1), setting the input mask register bit to 0 will cause the interrupt pin to be asserted. If the interrupt mask bit of an input that is currently the source of an interrupt is set to 1, the interrupt pin will be de-asserted. A register pair write is described in Section 7.1 and a register pair read is described in Section 7.2.

Table 23. Interrupt mask port 0 register (address 4Ah) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	M0.7	M0.6	M0.5	M0.4	M0.3	M0.2	M0.1	M0.0
Default	1	1	1	1	1	1	1	1

Table 24. Interrupt mask port 1 register (address 4Bh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	M1.7	M1.6	M1.5	M1.4	M1.3	M1.2	M1.1	M1.0
Default	1	1	1	1	1	1	1	1

6.2.11 Interrupt status register pair (4Ch, 4Dh)

These read-only registers are used to identify the source of an interrupt. When read, a logic 1 indicates that the corresponding input pin was the source of the interrupt. A logic 0 indicates that the input pin is not the source of an interrupt.

When a corresponding bit in the interrupt mask register is set to 1 (masked), the interrupt status bit will return logic 0. A register pair write is described in Section 7.1 and a register pair read is described in Section 7.2.

Table 25. Interrupt status port 0 register (address 4Ch) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	S0.7	S0.6	S0.5	S0.4	S0.3	S0.2	S0.1	S0.0
Default	0	0	0	0	0	0	0	0

Table 26. Interrupt status port 1 register (address 4Dh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	S1.7	S1.6	S1.5	S1.4	S1.3	S1.2	S1.1	S1.0
Default	0	0	0	0	0	0	0	0

6.2.12 Output port configuration register (4Fh)

The output port configuration register selects port-wise push-pull or open-drain I/O stage. A logic 0 configures the I/O as push-pull (Q1 and Q2 are active, see Figure 6). A logic 1 configures the I/O as open-drain (Q1 is disabled, Q2 is active) and the recommended command sequence to program this register (4Fh) before the configuration registers (06h, 07h) sets the port pins as outputs.

ODEN0 configures Port 0_x and ODEN1 configures Port 1_x.

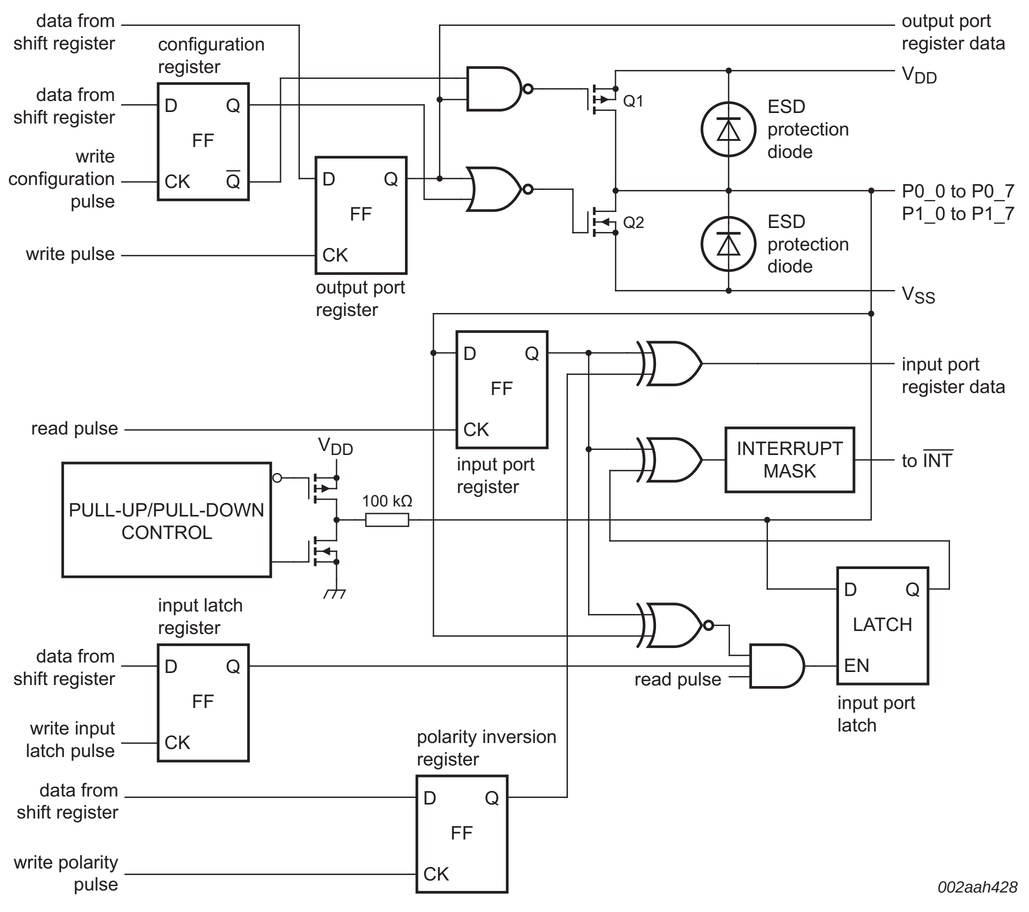
Table 27. Output port configuration register (address 4Fh)

Bit	7	6	5	4	3	2	1	0
Symbol	reserved						ODEN1	ODEN0
Default	0	0	0	0	0	0	0	0

6.3 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either V_{DD} or V_{SS}. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.



At power-on reset, all registers return to default values.

Fig 6. Simplified schematic of the I/Os (P0_0 to P0_7, P1_0 to P1_7)

6.4 Power-on reset

When power (from 0 V) is applied to V_{DD}, an internal power-on reset holds the PCAL9555A in a reset condition until V_{DD} has reached V_{POR}. At that time, the reset condition is released and the PCAL9555A registers and I^2C-bus/SMBus state machine initializes to their default states. After that, V_{DD} must be lowered to below V_{PORF} and back up to the operating voltage for a power-reset cycle. See Section 8.3 “Power-on reset requirements”.

6.5 Interrupt output

An interrupt is generated by any rising or falling edge of the port inputs in the Input mode. After time $t_{v(INT)}$, the signal $\overline{INT}$ is valid. The interrupt is reset when data on the port changes back to the original value or when data is read form the port that generated the interrupt (see Figure 10). Resetting occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Any change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register.

The $\overline{INT}$ output has an open-drain structure and requires pull-up resistor to V_{DD}.

When using the input latch feature, the input pin state is latched. The interrupt is reset only when data is read from the port that generated the interrupt. The reset occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

7. Bus transactions

The PCAL9555A is an I^{2}C-bus slave device. Data is exchanged between the master and PCAL9555A through write and read commands using I^{2}C-bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Writing to the port registers

Data is transmitted to the PCAL9555A by sending the device address and setting the least significant bit to a logic 0 (see Figure 4 “PCAL9555A device address”). The command byte is sent after the address and determines which register will receive the data following the command byte.

Twenty-two registers within the PCAL9555A are configured to operate as eleven register pairs. The eleven pairs are input port, output port, polarity inversion, configuration, output drive strength (two 16-bit registers), input latch, pull-up/pull-down enable, pull-up/pull-down selection, interrupt mask, and interrupt status registers. After sending data to one register, the next data byte is sent to the other register in the pair (see Figure 7 and Figure 8). For example, if the first byte is sent to Output Port 1 (register 3), the next byte is stored in Output Port 0 (register 2).

There is no limitation on the number of data bytes sent in one write transmission. In this way, the host can continuously update a register pair independently of the other registers, or the host can simply update a single register.

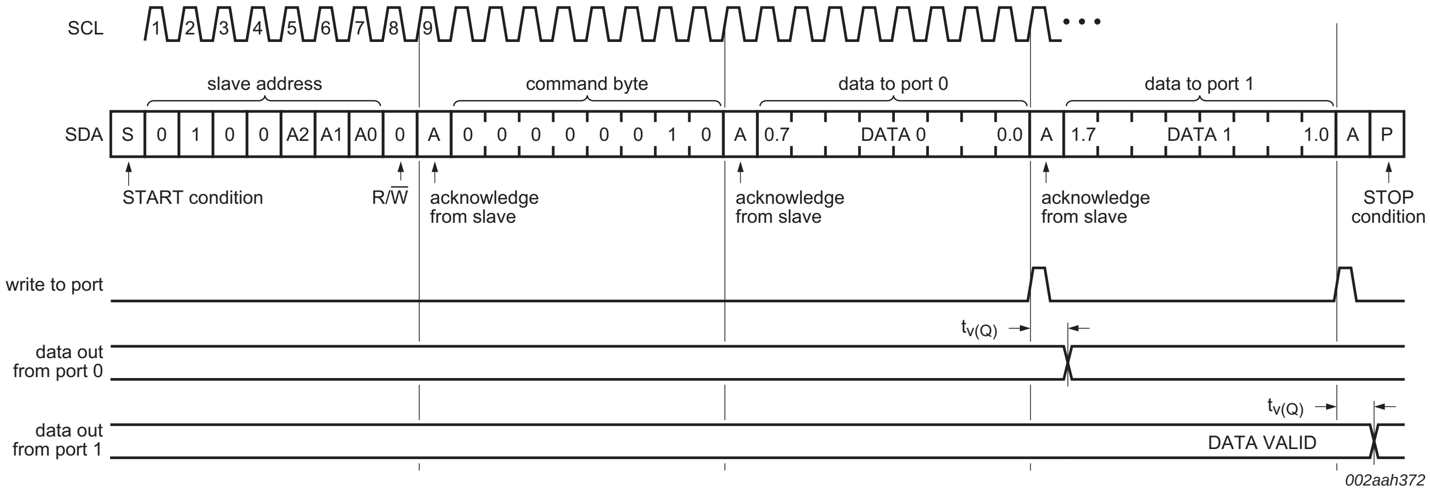


Fig 7. Write to output port registers

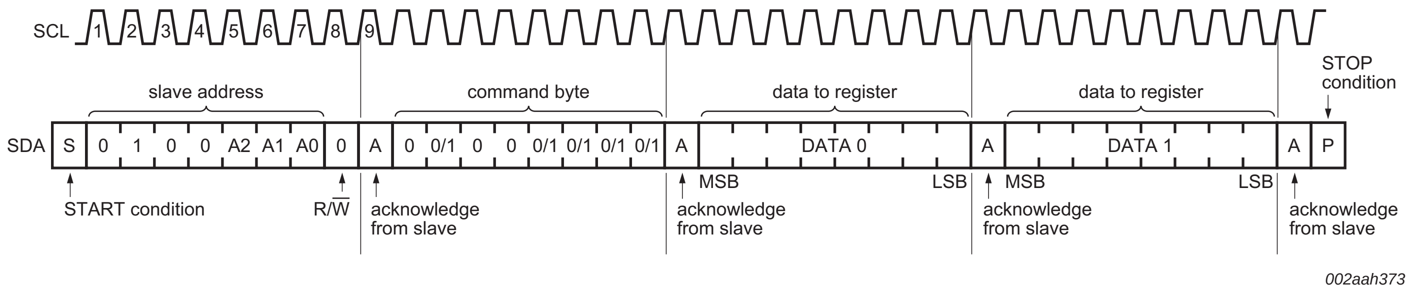
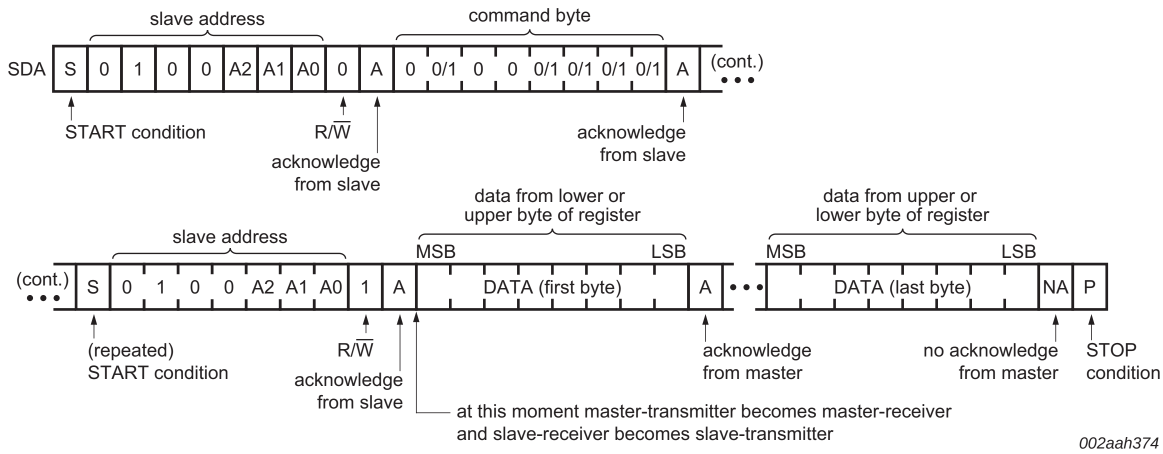


Fig 8. Write to Control registers

7.2 Reading the port registers

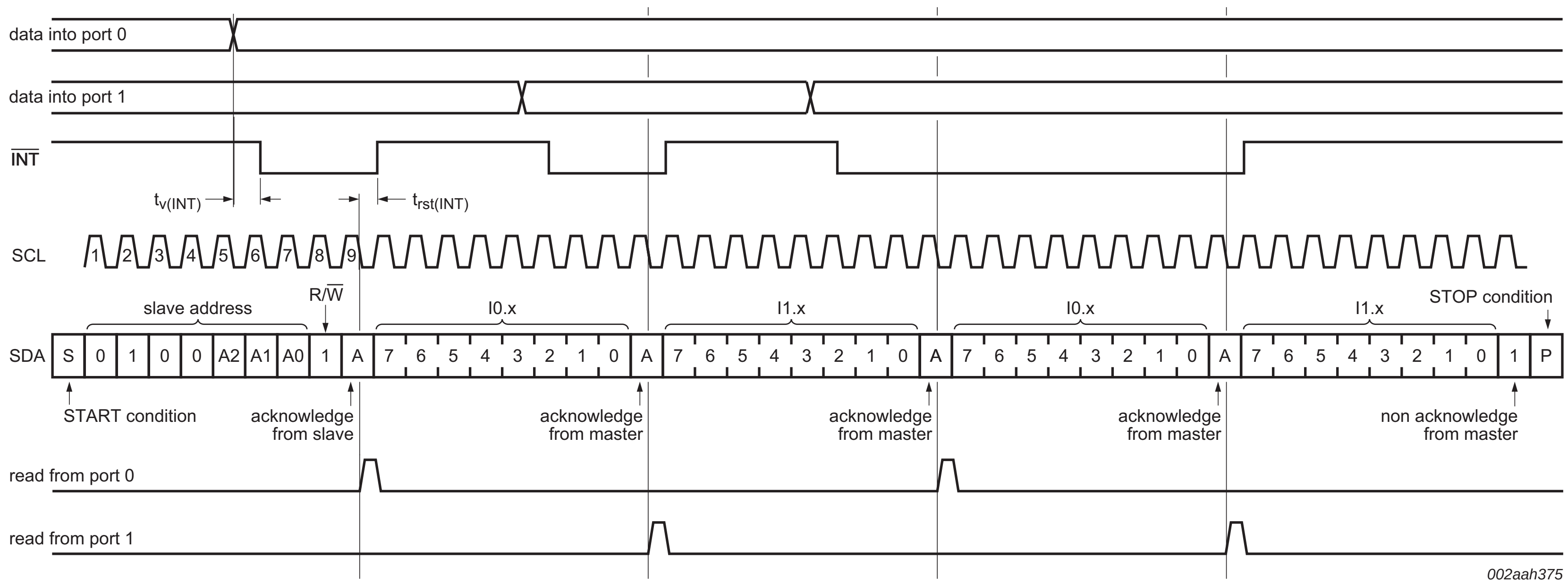
In order to read data from the PCAL9555A, the bus master must first send the PCAL9555A address with the least significant bit set to a logic 0 (see Figure 4 "PCAL9555A device address"). The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte is sent by the PCAL9555A (see Figure 9, Figure 10 and Figure 11). Data is clocked into the register on the falling edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data now reflects the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0. There is no limit on the number of data bytes received in one read transmission, but on the final byte received the bus master must not acknowledge the data.

After a subsequent restart, the command byte contains the value of the next register to be read in the pair. For example, if Input Port 1 was read last before the restart, the register that is read after the restart is the Input Port 0.



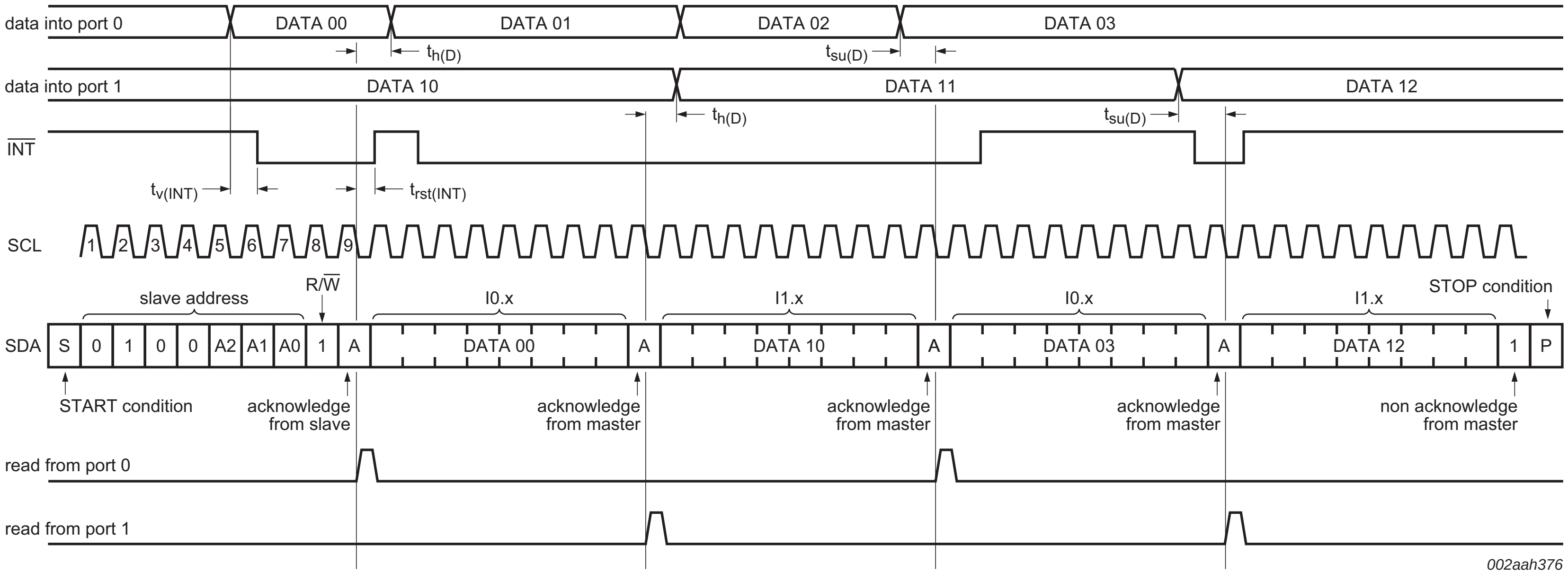
Remark: Transfer can be stopped at any time by a STOP condition.

Fig 9. Read from register



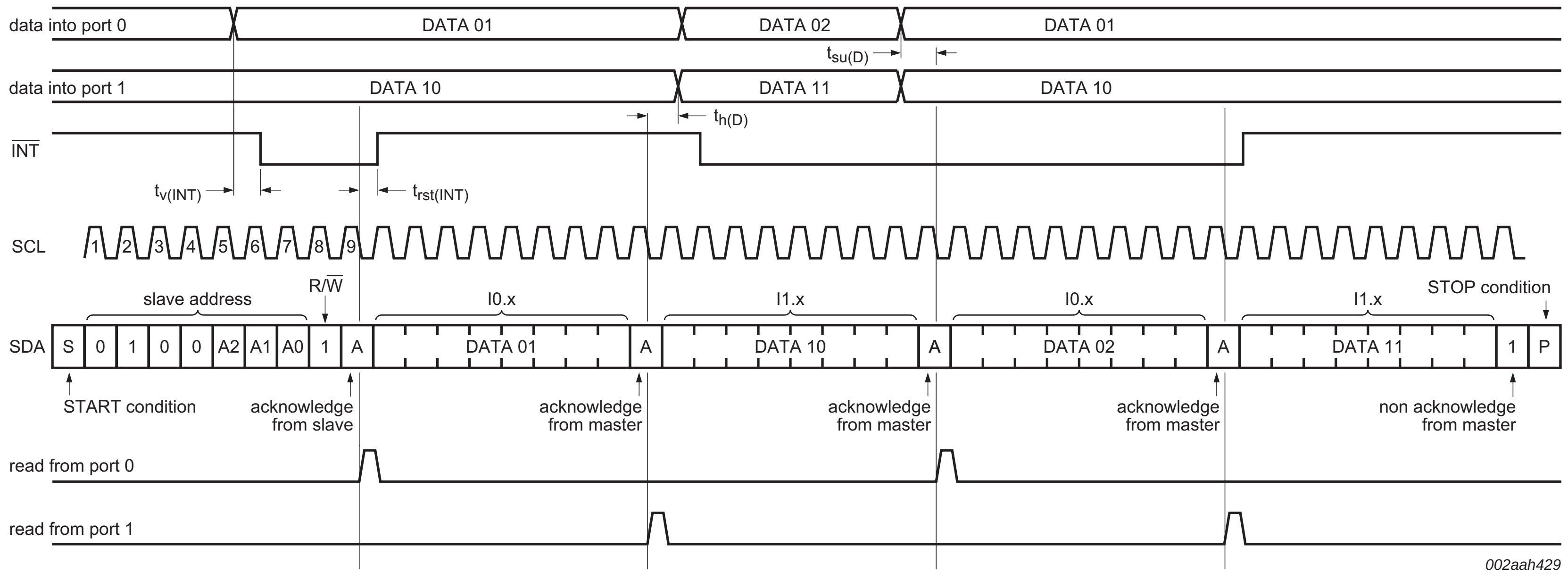
Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to ‘00’ (read input port register).

Fig 10. Read input port register (input latch disabled), scenario 1



Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to ‘00’ (read input port register).

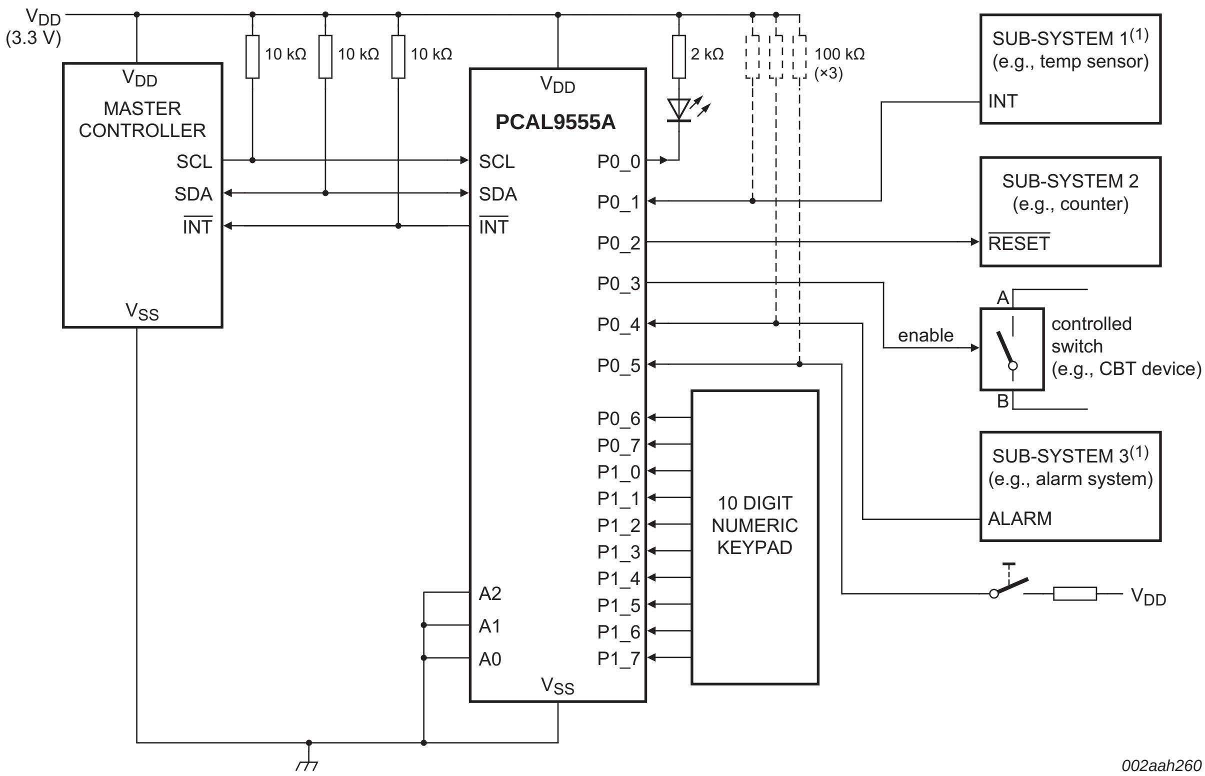
Fig 11. Read input port register (non-latched), scenario 2



Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to ‘00’ (read input port register).

Fig 12. Read input port register (latch enabled), scenario 3

8. Application design-in information



Device address configured as 0100 000X for this example.

P0_0, P0_2, P0_3 configured as outputs.

P0_1, P0_4, P0_5 configured as inputs.

P0_6, P0_7 and (P1_0 to P1_7) configured as inputs.

(1) External resistors are required for inputs (on P port) that may float. Also, internal pull-up or pull-down may be used to eliminate the need for external components. If a driver to an input will never let the input float, a resistor is not needed. If an output in the P port is configured as a push-pull output there is no need for external pull-up resistors. If an output in the P port is configured as an open-drain output, external pull-up resistors are required.

Fig 13. Typical application

8.1 Minimizing I_{DD} when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 13. Since the LED acts as a diode, when the LED is off the I/O V_I is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_I becomes lower than V_{DD}.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 14 shows a high value resistor in parallel with the LED. Figure 15 shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_I at or above V_{DD} and prevents additional supply current consumption when the LED is off.

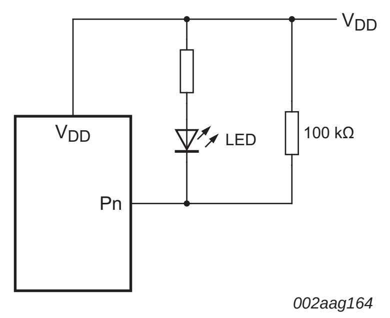


Fig 14. High value resistor in parallel with the LED

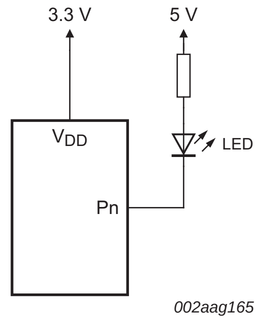


Fig 15. Device supplied by a lower voltage

8.2 Output drive strength control

The Output drive strength registers allow the user to control the output drive level of the GPIO. Each GPIO can be configured independently to one of the four possible output current levels. By programming these bits the user is changing the number of transistor pairs or 'fingers' that drive the I/O pad.

Figure 16 shows a simplified output stage. The behavior of the pad is affected by the Configuration register, the output port data, and the current control register. When the Current Control register bits are programmed to 10b, then only two of the fingers are active, reducing the current drive capability by 50 %.

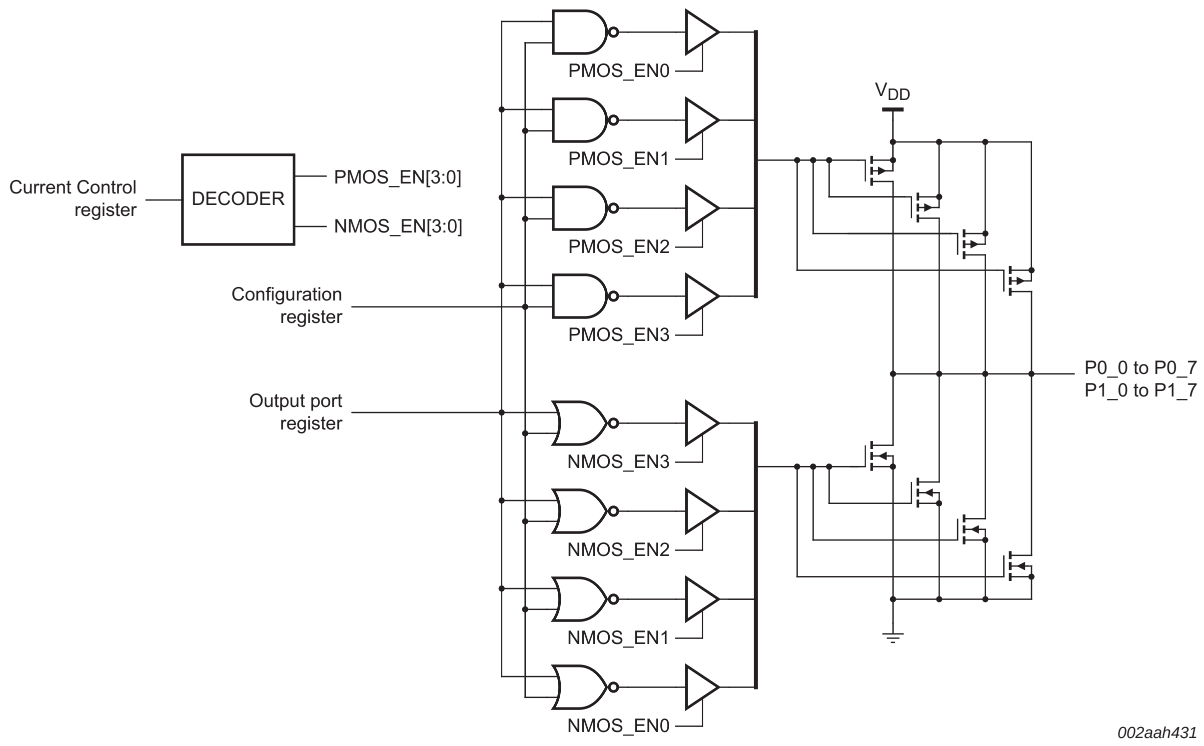


Fig 16. Simplified output stage

Reducing the current drive capability may be desirable to reduce system noise. When the output switches (transitions from H/L), there is a peak current that is a function of the output drive selection. This peak current runs through V_{DD} and V_{SS} package inductance and will create noise (some radiated, but more critically Simultaneous Switching Noise (SSN)). In other words, switching many outputs at the same time will create ground and supply noise. The output drive strength control through the Current Control registers allows the user to mitigate SSN issues without the need of additional external components.

8.3 Power-on reset requirements

In the event of a glitch or data corruption, PCAL9555A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 17 and Figure 18.

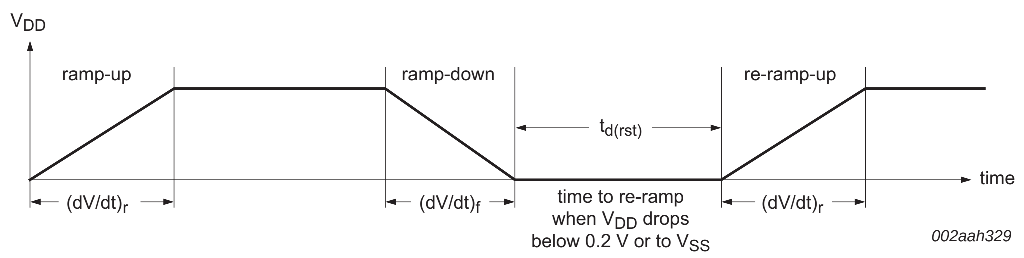


Fig 17. V_{DD} is lowered below 0.2 V or to 0 V and then ramped up to V_{DD}

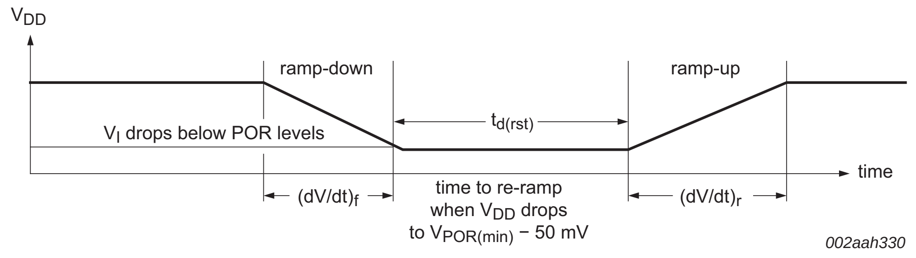


Fig 18. V_{DD} is lowered below the POR threshold, then ramped back up to V_{DD}

Table 28 specifies the performance of the power-on reset feature for PCAL9555A for both types of power-on reset.

Table 28. Recommended supply sequencing and ramp rates
T_{amb} = 25 °C (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition		Min	Typ	Max	Unit
$(dV/dt)_f$	fall rate of change of voltage	Figure 17		0.1	-	2000	ms
$(dV/dt)_r$	rise rate of change of voltage	Figure 17		0.1	-	2000	ms
$t_{d(rst)}$	reset delay time	Figure 17; re-ramp time when V_{DD} drops below 0.2 V or to V_{SS}		1	-	-	µs
		Figure 18; re-ramp time when V_{DD} drops to $V_{POR(min)}$ − 50 mV		1	-	-	µs
$\Delta V_{DD(gl)}$	glitch supply voltage difference	Figure 19	[1]	-	-	1	V
$t_{w(gl)VDD}$	supply voltage glitch pulse width	Figure 19	[2]	-	-	10	µs
$V_{POR(trip)}$	power-on reset trip voltage	falling V_{DD}		0.7	-	-	V
		rising V_{DD}		-	-	1.4	V

[1] Level that V_{DD} can glitch down to with a ramp rate of 0.4 µs/V, but not cause a functional disruption when $t_{w(gl)VDD}$ < 1 µs.

[2] Glitch width that will not cause a functional disruption when $\Delta V_{DD(gl)} = 0.5 \times V_{DD}$.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ($t_{w(gl)VDD}$) and glitch height ($\Delta V_{DD(gl)}$) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 19 and Table 28 provide more information on how to measure these specifications.

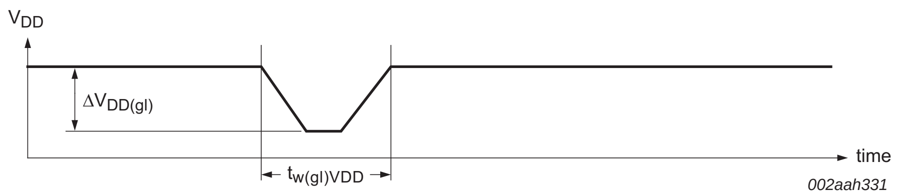


Fig 19. Glitch width and glitch height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C-bus/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{DD} being lowered to or from 0 V. Figure 20 and Table 28 provide more details on this specification.

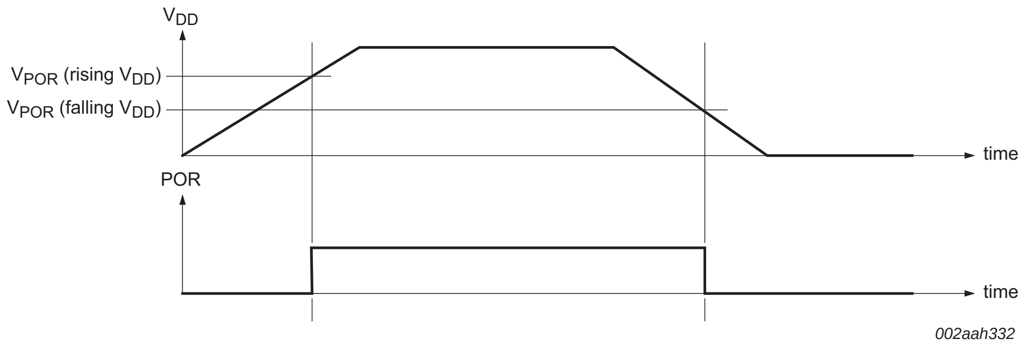


Fig 20. Power-on reset voltage (V_{POR})

8.4 Device current consumption with internal pull-up and pull-down resistors

The PCAL9555A integrates programmable pull-up and pull-down resistors to eliminate external components when pins are configured as inputs and pull-up or pull-down resistors are required (for example, nothing is driving the inputs to the power supply rails. Since these pull-up and pull-down resistors are internal to the device itself, they contribute to the current consumption of the device and must be considered in the overall system design.

The pull-up or pull-down function is selected in registers 48h and 49h, while the resistor is connected by the enable registers 46h and 47h. The configuration of the resistors is shown in Figure 6.

If the resistor is configured as a pull-up, that is, connected to V_{DD}, a current will flow from the V_{DD} pin through the resistor to ground when the pin is held LOW. This current will appear as additional I_{DD} upsetting any current consumption measurements.

In the same manner, if the resistor is configured as a pull-down and the pin is held HIGH, current will flow from the power supply through the pin to the V_{SS} pin. While this current will not be measured as part of I_{DD}, one must be mindful of the 200 mA limiting value through V_{SS}.

The pull-up and pull-down resistors are simple resistors and the current is linear with voltage. The resistance specification for these devices spans from 50 kΩ with a nominal 100 kΩ value. Any current flow through these resistors is additive by the number of pins held HIGH or LOW and the current can be calculated by Ohm's law. See Figure 24 for a graph of supply current versus the number of pull-up resistors.

9. Limiting values

Table 29. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+6.5	V
V_I	input voltage	[1]	–0.5	+6.5	V
V_O	output voltage	[1]	–0.5	+6.5	V
I_{IK}	input clamping current	A0, A1, A2, SCL; $V_I < 0$ V	-	±20	mA
I_{OK}	output clamping current	$\overline{INT}$; $V_O < 0$ V	-	±20	mA
I_{IOK}	input/output clamping current	P port; $V_O < 0$ V or $V_O > V_{DD}$	-	±20	mA
		SDA; $V_O < 0$ V or $V_O > V_{DD}$	-	±20	mA
I_{OL}	LOW-level output current	continuous; I/O port	-	50	mA
		continuous; SDA, $\overline{INT}$	-	25	mA
I_{OH}	HIGH-level output current	continuous; P port	-	25	mA
I_{DD}	supply current		-	160	mA
I_{SS}	ground supply current		-	200	mA
P_{tot}	total power dissipation		-	200	mW
T_{stg}	storage temperature		–65	+150	°C
$T_{j(max)}$	maximum junction temperature		-	125	°C

[1] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

10. Recommended operating conditions

Table 30. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		1.65	5.5	V
V_{IH}	HIGH-level input voltage	SCL, SDA	$0.7 \times V_{DD}$	5.5	V
		A0, A1, A2, P1_7 to P0_0	$0.7 \times V_{DD}$	5.5	V
V_{IL}	LOW-level input voltage	SCL, SDA	–0.5	$0.3 \times V_{DD}$	V
		A0, A1, A2, P1_7 to P0_0	–0.5	$0.3 \times V_{DD}$	V
I_{OH}	HIGH-level output current	P1_7 to P0_0	-	10	mA
I_{OL}	LOW-level output current	P1_7 to P0_0	-	25	mA
T_{amb}	ambient temperature	operating in free air	–40	+85	°C

11. Thermal characteristics

Table 31. Thermal characteristics

Symbol	Parameter	Conditions	Max	Unit
$Z_{th(j-a)}$	transient thermal impedance from junction to ambient	TSSOP24 package [1]	88	K/W
		HWQFN24 package [1]	66	K/W

[1] The package thermal impedance is calculated in accordance with JESD 51-7.

12. Static characteristics

Table 32. Static characteristics

T_{amb} = –40 °C to +85 °C; V_{DD} = 1.65 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	I_I = –18 mA	–1.2	-	-	V
V_{POR}	power-on reset voltage	V_I = V_{DD} or V_{SS}; I_O = 0 mA	-	1.1	1.4	V
V_{OH}	HIGH-level output voltage[2]	P port; I_{OH} = –8 mA; CCX.X = 11b				
		V_{DD} = 1.65 V	1.2	-	-	V
		V_{DD} = 2.3 V	1.8	-	-	V
		V_{DD} = 3 V	2.6	-	-	V
		V_{DD} = 4.5 V	4.1	-	-	V
		P port; I_{OH} = –2.5 mA and CCX.X = 00b; I_{OH} = –5 mA and CCX.X = 01b; I_{OH} = –7.5 mA and CCX.X = 10b; I_{OH} = –10 mA and CCX.X = 11b;				
		V_{DD} = 1.65 V	1.1	-	-	V
		V_{DD} = 2.3 V	1.7	-	-	V
		V_{DD} = 3 V	2.5	-	-	V
		V_{DD} = 4.5 V	4.0	-	-	V
V_{OL}	LOW-level output voltage[2]	P port; I_{OL} = 8 mA; CCX.X = 11b				
		V_{DD} = 1.65 V	-	-	0.45	V
		V_{DD} = 2.3 V	-	-	0.25	V
		V_{DD} = 3 V	-	-	0.25	V
		V_{DD} = 4.5 V	-	-	0.2	V
		P port; I_{OL} = 2.5 mA and CCX.X = 00b; I_{OL} = 5 mA and CCX.X = 01b; I_{OL} = 7.5 mA and CCX.X = 10b; I_{OL} = 10 mA and CCX.X = 11b;				
		V_{DD} = 1.65 V	-	-	0.5	V
		V_{DD} = 2.3 V	-	-	0.3	V
		V_{DD} = 3 V	-	-	0.25	V
		V_{DD} = 4.5 V	-	-	0.2	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 1.65 V to 5.5 V				
		SDA	3	-	-	mA
		$\overline{INT}$	3	15[3]	-	mA
I_I	input current	V_{DD} = 1.65 V to 5.5 V				
		SCL, SDA; V_I = V_{DD} or V_{SS}	-	-	±1	μA
		A0, A1, A2; V_I = V_{DD} or V_{SS}	-	-	±1	μA
I_{IH}	HIGH-level input current	P port; V_I = V_{DD}; V_{DD} = 1.65 V to 5.5 V	-	-	1	μA
I_{IL}	LOW-level input current	P port; V_I = V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	-	1	μA

Table 32. Static characteristics *...continued*

T_{amb} = −40 °C to +85 °C; V_{DD} = 1.65 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{DD}	supply current	SDA, P port, A0, A1, A2; V_I on SDA = V_{DD} or V_{SS}; V_I on P port and A0, A1, A2 = V_{DD}; I_O = 0 mA; I/O = inputs; f_{SCL} = 400 kHz				
		V_{DD} = 3.6 V to 5.5 V	-	10	25	μA
		V_{DD} = 2.3 V to 3.6 V	-	6.5	15	μA
		V_{DD} = 1.65 V to 2.3 V	-	4	9	μA
		SCL, SDA, P port, A0, A1, A2; V_I on SCL, SDA = V_{DD} or V_{SS}; V_I on P port and A0, A1, A2 = V_{DD}; I_O = 0 mA; I/O = inputs; f_{SCL} = 0 kHz				
		V_{DD} = 3.6 V to 5.5 V	-	1.5	7	μA
		V_{DD} = 2.3 V to 3.6 V	-	1	3.2	μA
		V_{DD} = 1.65 V to 2.3 V	-	0.5	1.7	μA
		Active mode; P port, A0, A1, A2; V_I on P port and A0, A1, A2 = V_{DD}; I_O = 0 mA; I/O = inputs; f_{SCL} = 400 kHz, continuous register read				
		V_{DD} = 3.6 V to 5.5 V	-	60	125	μA
		V_{DD} = 2.3 V to 3.6 V	-	40	75	μA
		V_{DD} = 1.65 V to 2.3 V	-	20	45	μA
		with pull-ups enabled; P port, A0, A1, A2; V_I on SCL, SDA = V_{DD} or V_{SS}; V_I on P port = V_{SS}; V_I on A0, A1, A2 = V_{DD} or V_{SS}; I_O = 0 mA; I/O = inputs with pull-up enabled; f_{SCL} = 0 kHz				
		V_{DD} = 1.65 V to 5.5 V	-	1.1	1.5	mA
ΔI_{DD}	additional quiescent supply current[4]	SCL, SDA; one input at V_{DD} − 0.6 V, other inputs at V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	-	25	μA
		P port, A0, A1, A2; one input at V_{DD} − 0.6 V, other inputs at V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	-	80	μA
C_i	input capacitance	V_I = V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	6	7	pF
C_{io}	input/output capacitance	$V_{I/O}$ = V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	7	8	pF
		$V_{I/O}$ = V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	7.5	8.5	pF
$R_{pu(int)}$	internal pull-up resistance	input/output	50	100	150	kΩ
$R_{pd(int)}$	internal pull-down resistance	input/output	50	100	150	kΩ

[1] For I_{DD}, all typical values are at nominal supply voltage (1.8 V, 2.5 V, 3.3 V, 3.6 V or 5 V V_{DD}) and T_{amb} = 25 °C. Except for I_{DD}, the typical values are at V_{DD} = 3.3 V and T_{amb} = 25 °C.

[2] The total current sourced by all I/Os must be limited to 160 mA.

[3] Typical value for T_{amb} = 25 °C. V_{OL} = 0.4 V and V_{DD} = 3.3 V. Typical value for V_{DD} < 2.5 V, V_{OL} = 0.6 V.

[4] Internal pull-up/pull-down resistors disabled.

12.1 Typical characteristics

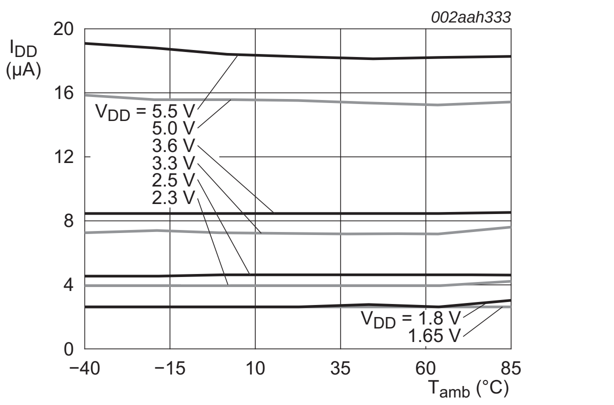


Fig 21. Supply current versus ambient temperature

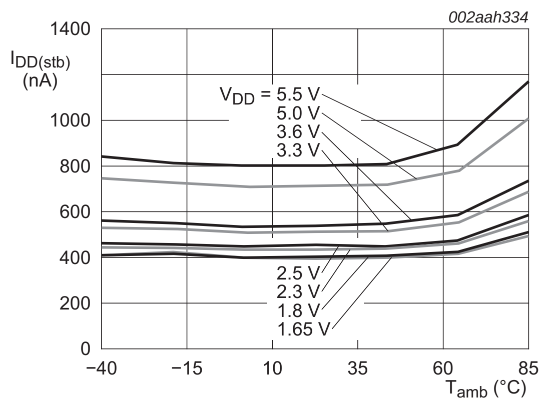
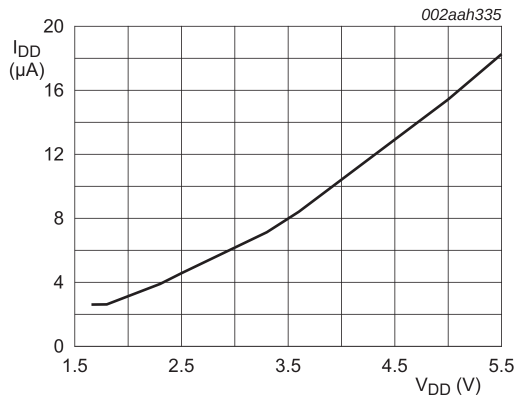
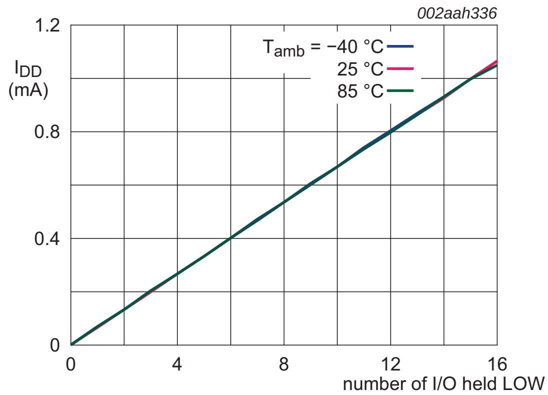


Fig 22. Standby supply current versus ambient temperature



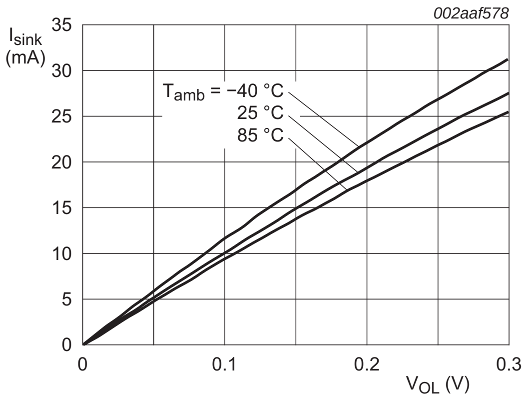
Tamb = 25 °C

Fig 23. Supply current versus supply voltage

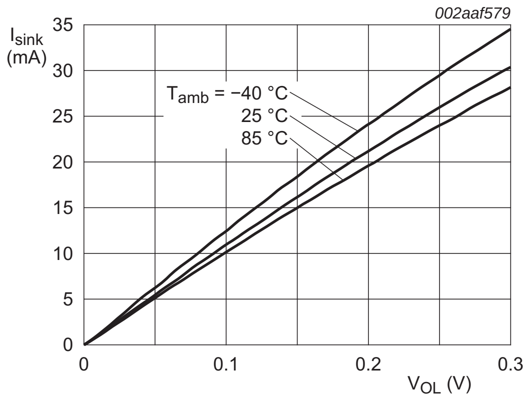


VDD = 5 V

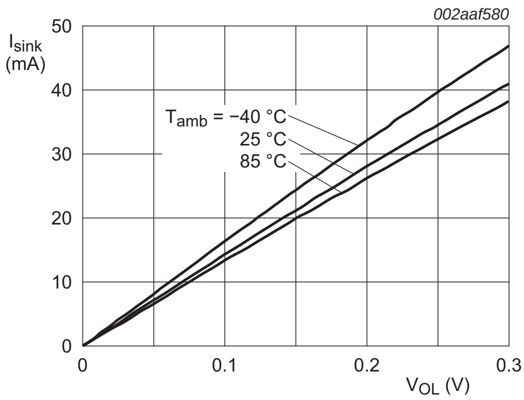
Fig 24. Supply current versus number of I/O held LOW



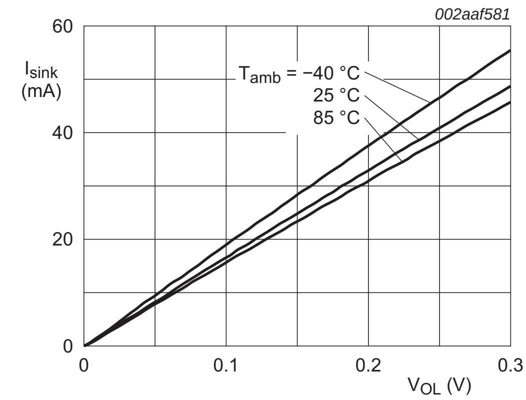
a. V_{DD} = 1.65 V



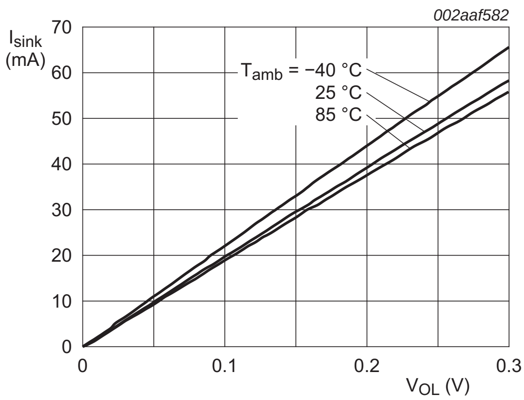
b. V_{DD} = 1.8 V



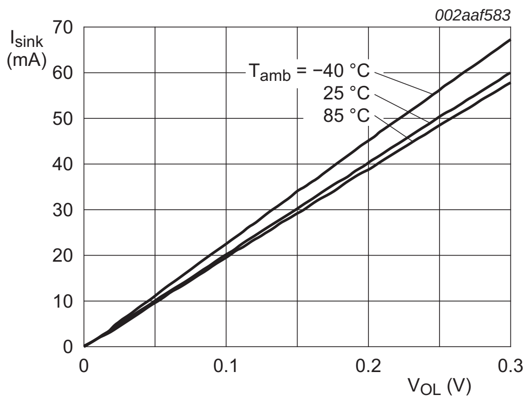
c. V_{DD} = 2.5 V



d. V_{DD} = 3.3 V

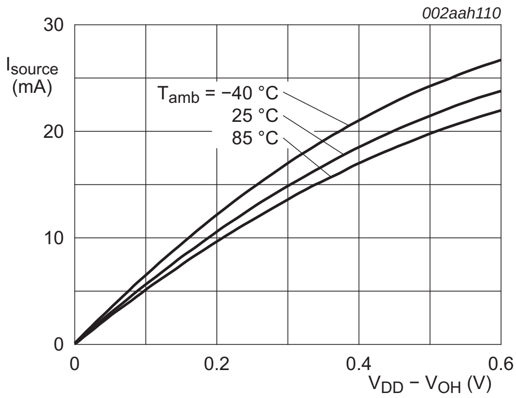


e. V_{DD} = 5.0 V

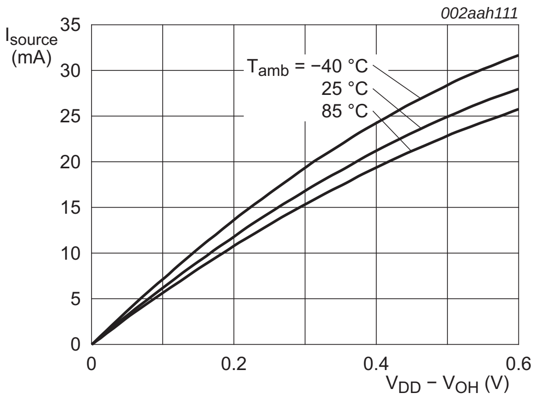


f. V_{DD} = 5.5 V

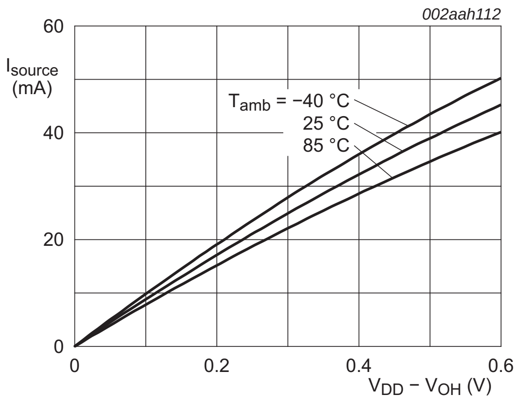
Fig 25. I/O sink current versus LOW-level output voltage with CCX.X = 11b



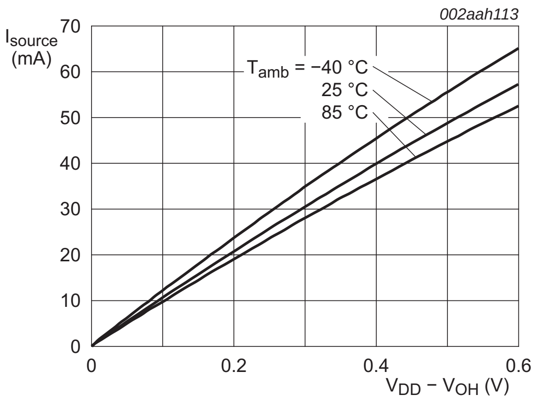
a. V_{DD} = 1.65 V



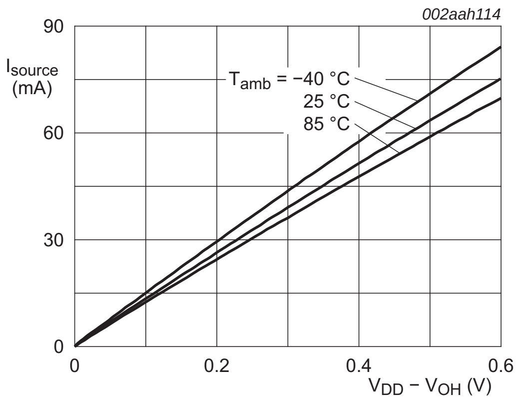
b. V_{DD} = 1.8 V



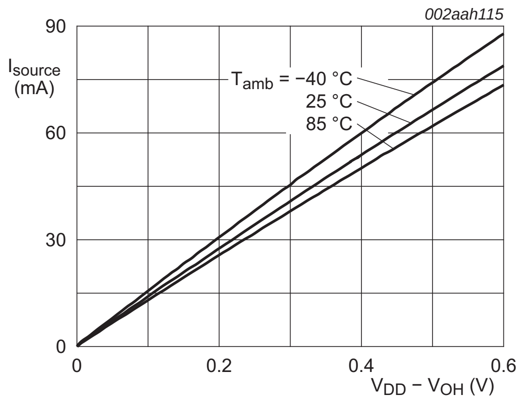
c. V_{DD} = 2.5 V



d. V_{DD} = 3.3 V

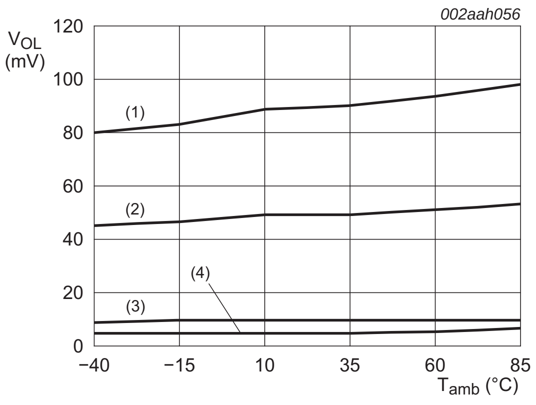


e. V_{DD} = 5.0 V



f. V_{DD} = 5.5 V

Fig 26. I/O source current versus HIGH-level output voltage with CCX.X = 11b



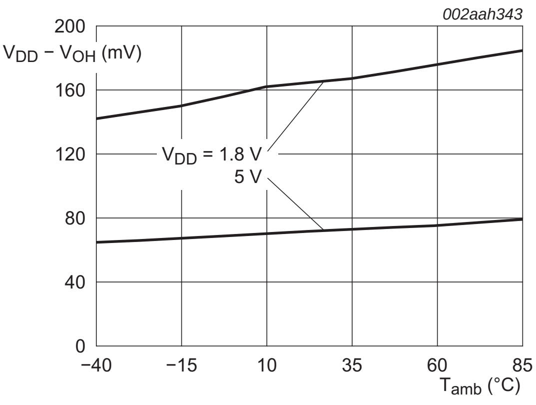
(1) V_{DD} = 1.8 V; I_{sink} = 10 mA

(2) V_{DD} = 5 V; I_{sink} = 10 mA

(3) V_{DD} = 1.8 V; I_{sink} = 1 mA

(4) V_{DD} = 5 V; I_{sink} = 1 mA

Fig 27. LOW-level output voltage versus temperature



I_{source} = −10 mA

Fig 28. I/O high voltage versus temperature

13. Dynamic characteristics

Table 33. I²C-bus interface timing requirements

Over recommended operating free air temperature range, unless otherwise specified. See Figure 29.

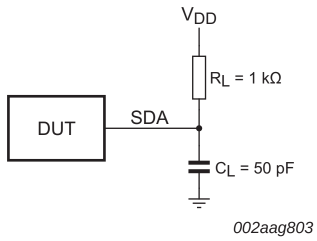
Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{HIGH}	HIGH period of the SCL clock		4	-	0.6	-	μs
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	μs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		0	50	0	50	ns
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
$t_{HD;DAT}$	data hold time		0	-	0	-	ns
t_r	rise time of both SDA and SCL signals		-	1000	20	300	ns
t_f	fall time of both SDA and SCL signals		-	300	$20 \times (V_{DD} / 5.5$ V	300	ns
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	μs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	μs
$t_{HD;STA}$	hold time (repeated) START condition		4	-	0.6	-	μs
$t_{SU;STO}$	set-up time for STOP condition		4	-	0.6	-	μs
$t_{VD;DAT}$	data valid time	SCL LOW to SDA output valid	-	3.45	-	0.9	μs
$t_{VD;ACK}$	data valid acknowledge time	ACK signal from SCL LOW to SDA (out) LOW	-	3.45	-	0.9	μs

Table 34. Switching characteristics

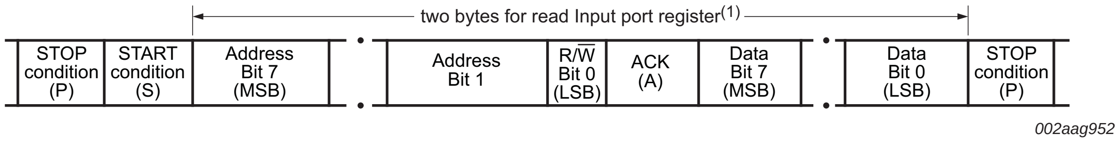
Over recommended operating free air temperature range; $C_L \leq 100$ pF; unless otherwise specified. See Figure 30.

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
$t_{v(INT)}$	valid time on pin $\overline{INT}$	from P port to $\overline{INT}$	-	1	-	1	μs
$t_{rst(INT)}$	reset time on pin $\overline{INT}$	from SCL to $\overline{INT}$	-	1	-	1	μs
$t_{v(Q)}$	data output valid time	from SCL to P port	-	400	-	400	ns
$t_{su(D)}$	data input set-up time	from P port to SCL	0	-	0	-	ns
$t_{h(D)}$	data input hold time	from P port to SCL	300	-	300	-	ns

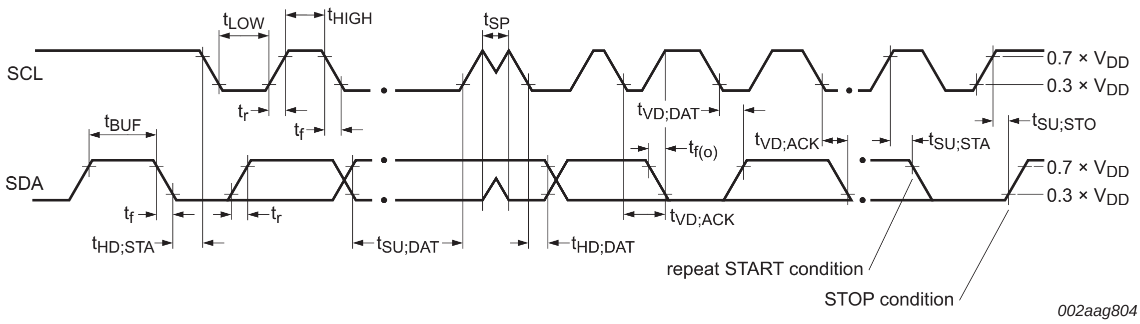
14. Parameter measurement information



a. SDA load configuration



b. Transaction format



c. Voltage waveforms

C_L includes probe and jig capacitance.

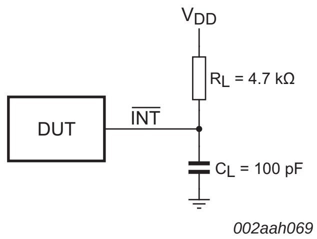
All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

All parameters and waveforms are not applicable to all devices.

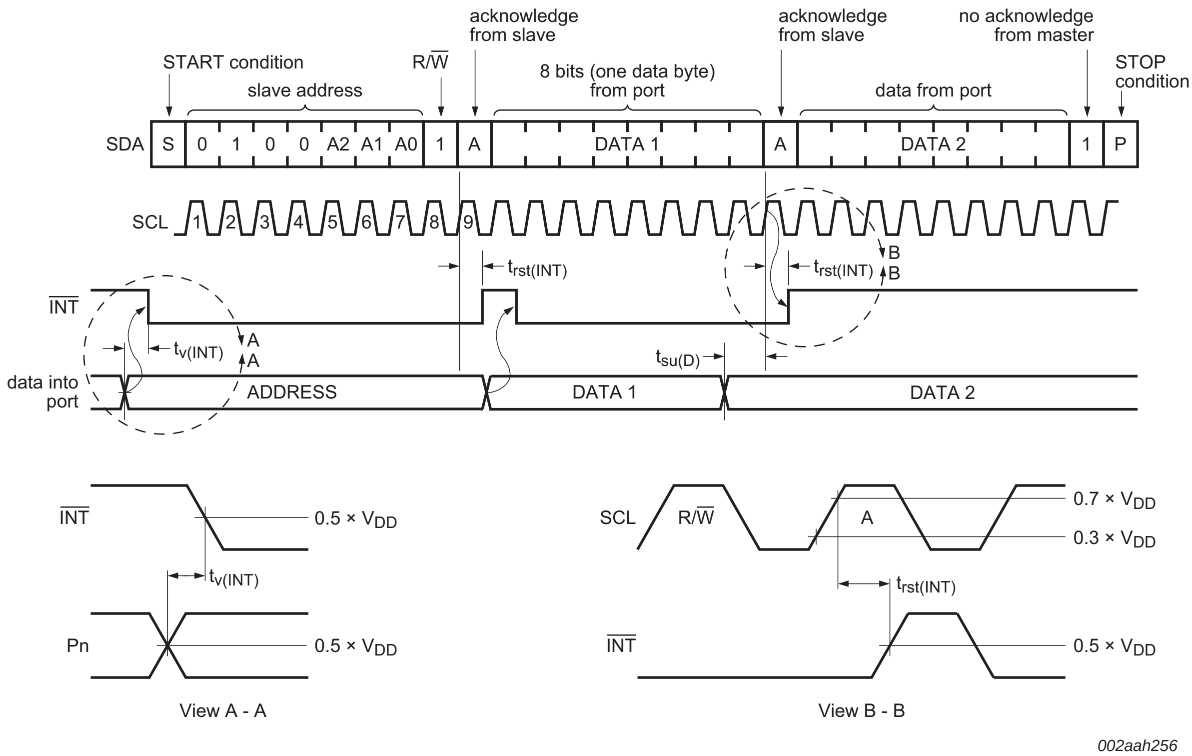
Byte 1 = I^2C-bus address; Byte 2, byte 3 = P port data.

(1) See Figure 9.

Fig 29. I^2C-bus interface load circuit and voltage waveforms



a. Interrupt load configuration



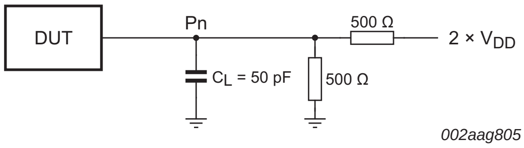
b. Voltage waveforms

C_L includes probe and jig capacitance.

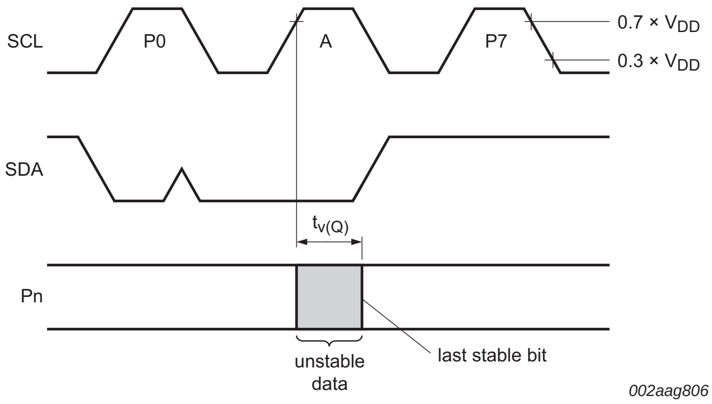
All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

All parameters and waveforms are not applicable to all devices.

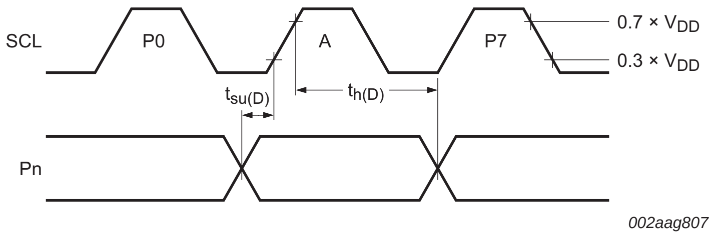
Fig 30. Interrupt load circuit and voltage waveforms



a. P port load configuration



b. Write mode (R/$\overline{W}$ = 0)



c. Read mode (R/$\overline{W}$ = 1)

C_L includes probe and jig capacitance.

$t_{v(Q)}$ is measured from 0.7 × V_{DD} on SCL to 50 % I/O (Pn) output.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

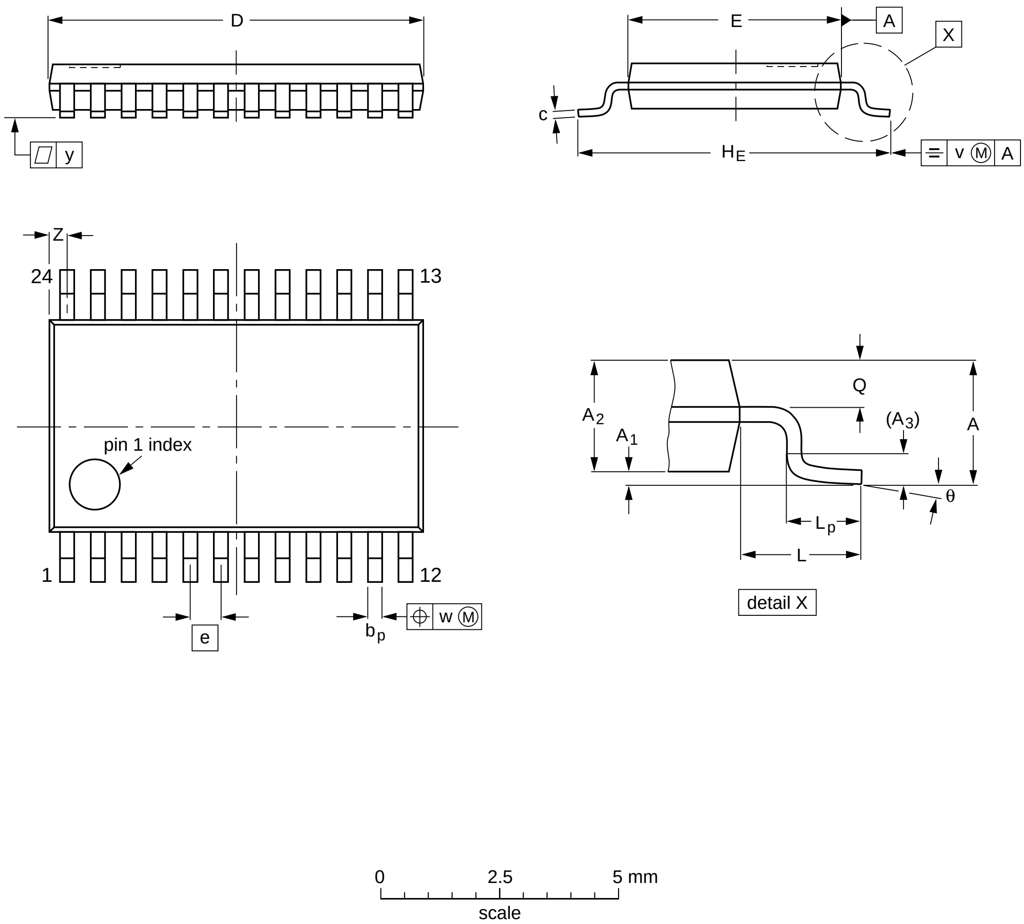
The outputs are measured one at a time, with one transition per measurement.

All parameters and waveforms are not applicable to all devices.

Fig 31. P port load circuit and voltage waveforms

15. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

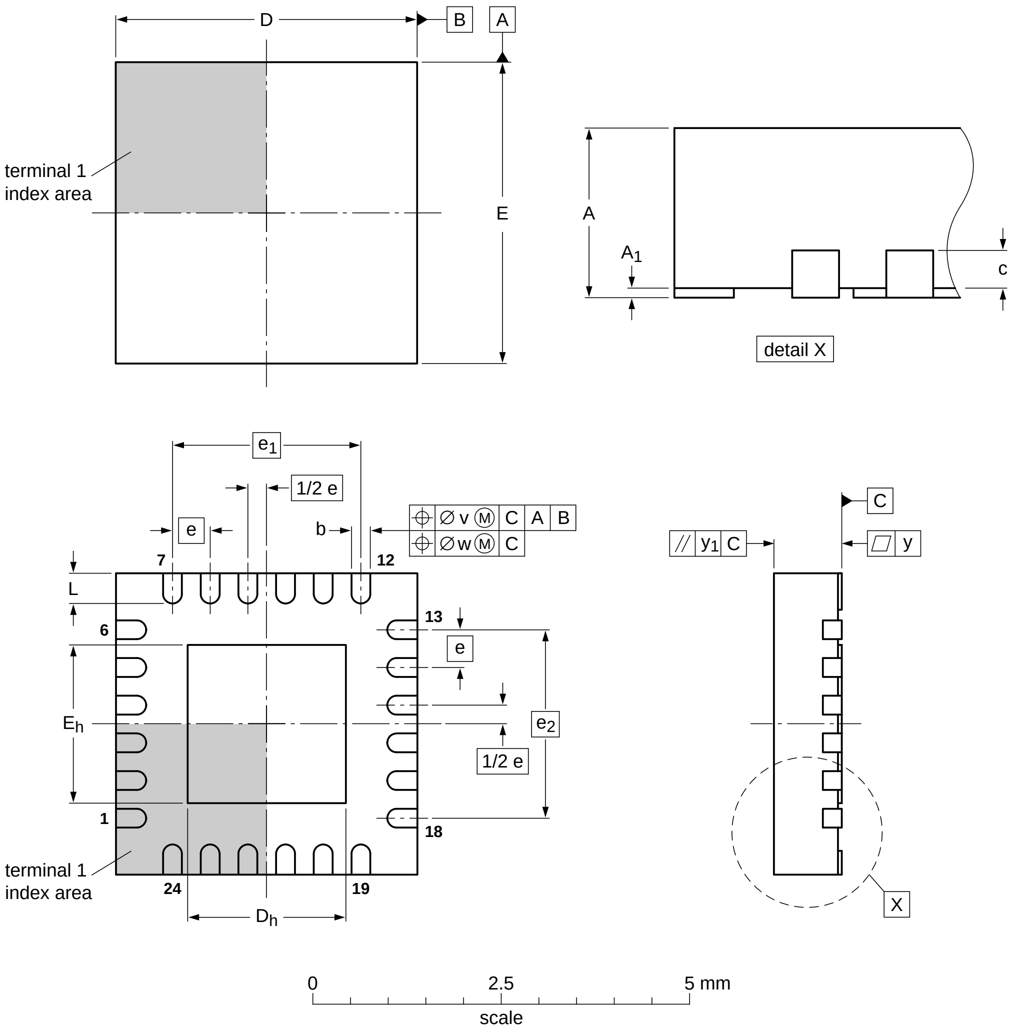
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 32. Package outline SOT355-1 (TSSOP24)

HWQFN24: plastic thermal enhanced very very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.75 mm **SOT994-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	0.8	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT994-1	- - -	MO-220	- - -			~~07-02-07~~ 07-03-03

Fig 33. Package outline SOT994-1 (HWQFN24)

16. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 34) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 35 and 36

Table 35. SnPb eutectic process (from J-STD-020D)

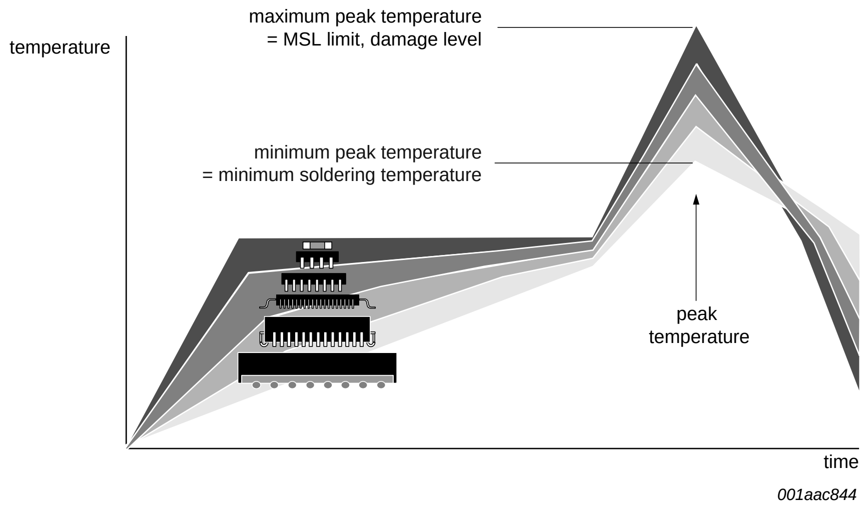
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 36. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 34.



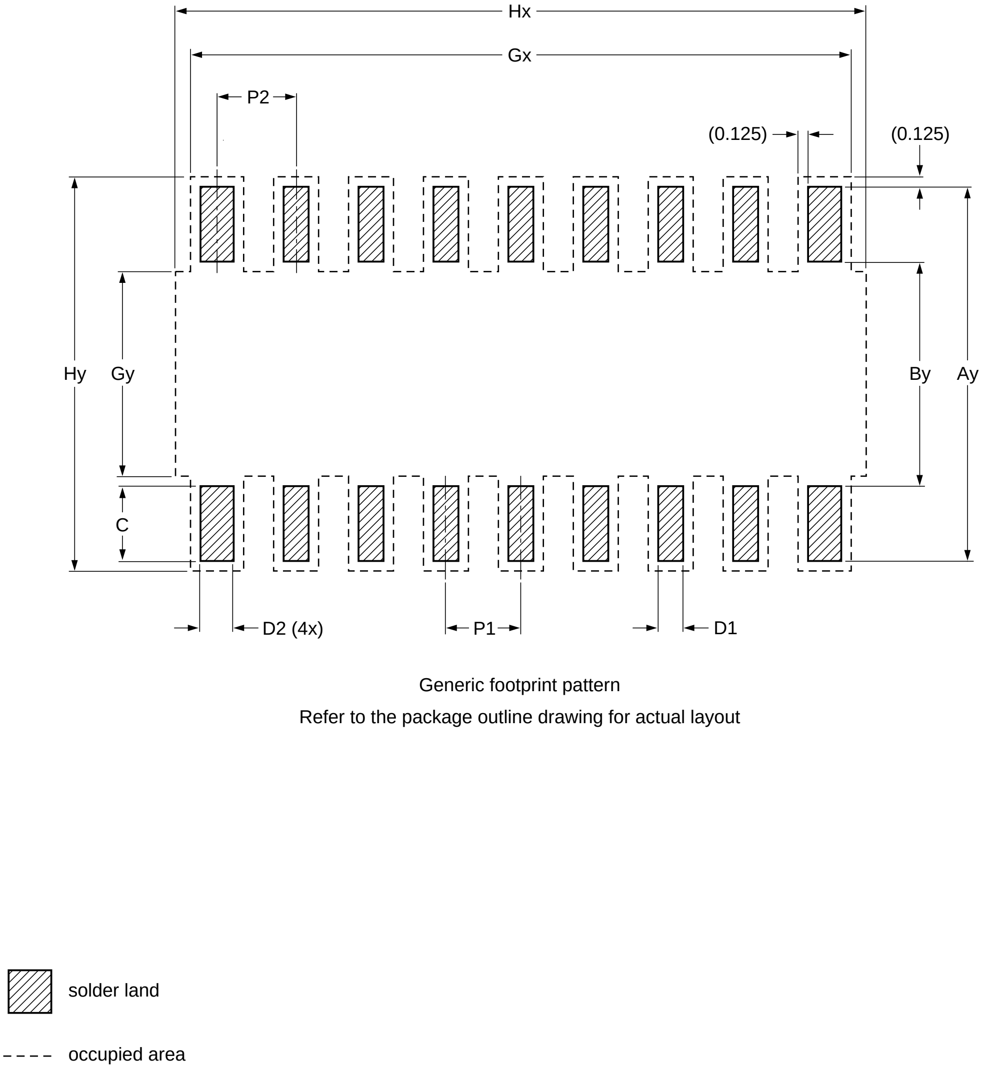
MSL: Moisture Sensitivity Level

Fig 34. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

18. Soldering: PCB footprints

Footprint information for reflow soldering of TSSOP24 package **SOT355-1**



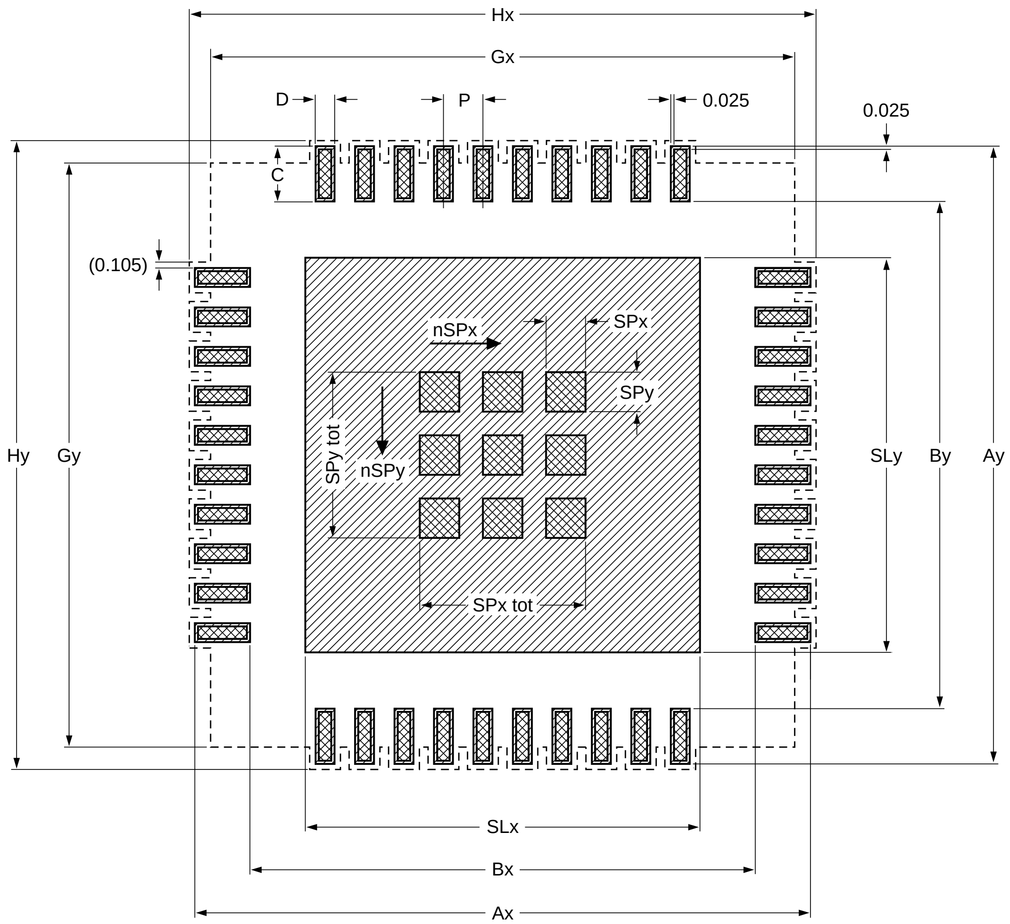
DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	8.200	5.300	8.600	7.450

sot355-1_fr

Fig 35. PCB footprint for SOT355-1 (TSSOP24); reflow soldering

Footprint information for reflow soldering of HVQFN24 package **SOT994-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

solder paste deposit

solder land plus solder paste

---- occupied area

nSPx	nSPy
2	2

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.500	5.000	5.000	3.200	3.200	0.900	0.240	2.100	2.100	1.200	1.200	0.450	0.450	4.300	4.300	5.250	5.250

Issue date ~~07-09-24~~ 09-06-15

sot994-1_fr

Fig 36. PCB footprint for SOT994-1 (HWQFN24); reflow soldering

19. Abbreviations

Table 37. Abbreviations

Acronym	Description
ACPI	Advanced Configuration and Power Interface
CBT	Cross-Bar Technology
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
FF	Flip-Flop
GPIO	General Purpose Input/Output
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light Emitting Diode
PCB	Printed-Circuit Board
POR	Power-On Reset
SMBus	System Management Bus

20. Revision history

Table 38. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCAL9555A v.2	20141219	Product data sheet	-	PCAL9555A v.1
Modifications:	• Table 4 "Command byte" 46h, 47h power-up default changed from "0000 0000" to "1111 1111".			
PCAL9555A v.1	20121003	Product data sheet	-	-

21. Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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22. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

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