WM8569

24-bit, 192kHz Stereo CODEC with Volume Control

DESCRIPTION

The WM8569 is a stereo audio codec ideal for DVD, PVR, LCD-TV and automotive applications. Independent ADC and DAC clocking permits separate record and playback sampling rates.

A stereo 24-bit multi-bit sigma delta DAC with oversampling and digital interpolation filters provides the output signal. Digital audio input word lengths from 16-24 bits and sampling rates from 8kHz to 192kHz are supported.

A stereo 24-bit multi-bit sigma delta ADC is used. Digital audio output word lengths from 16-24 bits and sampling rates from 32kHz to 96kHz are supported. The DAC and ADC support independent sampling rates.

The audio data interface supports I^2S, left justified, right justified and DSP digital audio formats.

The device is controlled via a 3-wire serial interface. The interface provides access to all features including volume controls, mutes, de-emphasis and power management facilities. A hardware control interface allows access to a limited feature set. The WM8569 is available in a 28-lead SSOP.

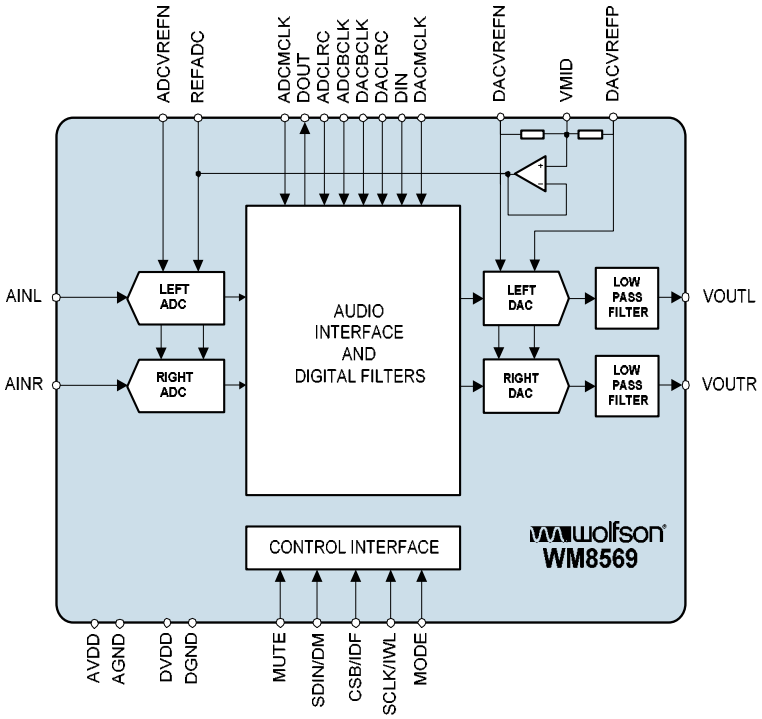
FEATURES

- Audio Performance
  - 103dB SNR ('A' weighted @ 48kHz) DAC
  - DAC Sampling Frequency: 8kHz – 192kHz
  - 100dB SNR ('A' weighted @ 48kHz) ADC
  - ADC Sampling Frequency: 32kHz – 96kHz
- Independent Sampling Rates for ADC and DAC
- 3-wire SPI Serial or Hardware Control Interface
- Audio Mute and De-Emphasis Functions
- Programmable Audio Data Interface Modes
  - 16/20/24/32 bit Word Lengths
  - I^2S, Left, Right Justified or DSP
- 2.7V to 5.5V Analogue Supply
- 2.7V to 3.6V Digital Supply
- 28-lead SSOP Package

APPLICATIONS

- DVD Recorder
- Personal Video Recorder
- PC Sound Card
- Automotive Audio
- LCD-TV

BLOCK DIAGRAM



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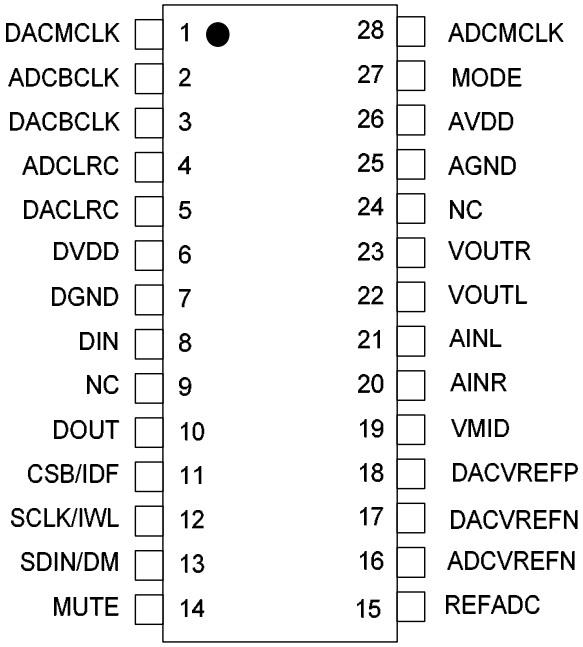
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8569SEDS/V	-25 to +85°C	28-lead SSOP (Pb-free)	MSL3	260°C
WM8569SEDS/RV	-25 to +85°C	28-lead SSOP (Pb-free, tape and reel)	MSL3	260°C

Note: Reel quantity = 2,000

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	DACMCLK	Digital Input	Master DAC clock: 256fs, 384fs, 512fs or 768fs
2	ADCBCLK	Digital Input	ADC audio interface bit clock
3	DACBLCK	Digital Input/Output	DAC audio interface bit clock
4	ADCLRC	Digital Input/Output	ADC left/right word clock
5	DACLRC	Digital Input/Output	DAC left/right word clock
6	DVDD	Supply	Digital positive supply
7	DGND	Supply	Digital ground
8	DIN	Digital input	DAC data input
9	NC	No Connect	No Connect
10	DOUT	Digital output	ADC data output
11	CSB/IDF	Digital input	Software Mode: Serial control interface latch signal Hardware Mode: Input audio data format
12	SCLK/IWL	Digital input	Software Mode: Serial control interface clock Hardware Mode: Audio data input word length
13	SDIN/DM	Digital input	Software Mode: Serial control interface data Hardware Mode: De-emphasis selection
14	MUTE	Digital input/output	DAC Zero Flag output or DAC mute input
15	REFADC	Analogue output	ADC reference buffer decoupling pin; 10uF external decoupling
16	ADCVREFN	Supply	ADC negative reference supply
17	DACVREFN	Supply	DAC negative reference supply
18	DACVREFP	Supply	DAC positive reference supply
19	VMID	Analogue output	Midrail divider decoupling pin; 10uF external decoupling
20	AINR	Analogue input	ADC right input
21	AINL	Analogue input	ADC left input
22	VOUTL	Analogue output	DAC left output
23	VOUTR	Analogue output	DAC right output
24	NC	No Connect	No Connect
25	AGND	Supply	Analogue negative supply and substrate connection
26	AVDD	Supply	Analogue positive supply
27	MODE	Digital Input	Control format selection: 0 = Software mode 1 = Hardware mode
28	ADCMCLK	Digital Input	Master ADC clock: 256fs, 384fs, 512fs or 768fs

Note: Digital input pins have Schmitt trigger input buffers.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+5V
Analogue supply voltage	-0.3V	+7V
Voltage range digital inputs [1]	DGND -0.3V	DVDD +0.3V
Voltage range analogue inputs [1]	AGND -0.3V	AVDD +0.3V
Master Clock Frequency		37MHz
Operating temperature range, T_A	-25°C	+85°C
Storage temperature after soldering	-65°C	+150°C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		2.7		3.6	V
Analogue supply range	AVDD, VREFP		2.7		5.5	V
Ground	AGND, VREFN, DGND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V

Note: Digital supply DVDD must never be more than 0.3V greater than AVDD.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD, VREFP = 5V, DVDD = 3.3V, AGND, VREFN = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC Performance (Load = 10kΩ, 50pF)						
0dBFs Full scale output voltage				1.0 x VREFP/5		V_{rms}
SNR (Note 1,2,4)		A-weighted, @ fs = 48kHz	95	103		dB
SNR (Note 1,2,4)		A-weighted @ fs = 96kHz		102		dB
SNR (Note 1,2,4)		A-weighted @ fs = 192kHz		101		dB
SNR (Note 1,2,4)		A-weighted @ fs = 48kHz, AVDD = 3.3V		99		dB
SNR (Note 1,2,4)		A-weighted @ fs = 96kHz, AVDD = 3.3V		99		dB
Dynamic Range (Note 2,4)	DNR	A-weighted, -60dB full scale input	90	103		dB
Total Harmonic Distortion (THD)		1kHz, 0dB.Fs		-90	-80	dB
Mute Attenuation		1kHz Input, 0dB gain		100		dB
DAC channel separation				100		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mV_{p-p}		50		dB
		20Hz to 20kHz 100mV_{p-p}		45		dB
ADC Performance						
Input Signal Level (0dB)				2.0 x REFADC/5		V_{rms}
Input resistance				20		kΩ
Input capacitance				10		pF
SNR (Note 1,2,4)		A-weighted, 0dB gain @ fs = 48kHz	80	100		dB
SNR (Note 1,2,4)		A-weighted, 0dB gain @ fs = 96kHz		100		dB
SNR (Note 1,2,4)		A-weighted, 0dB gain @ fs = 48kHz, AVDD = 3.3V		93		dB
SNR (Note 1,2,4)		A-weighted, 0dB gain @ fs = 96kHz, AVDD = 3.3V		93		dB
Total Harmonic Distortion (THD)		1kHz, -1dBFs		-82	-72	dB
ADC Channel Separation		1kHz Input		90		dB

Test Conditions

AVDD, VREFP = 5V, DVDD = 3.3V, AGND, VREFN = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Mute Attenuation		1kHz Input, 0dB gain		90		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Digital Logic Levels (CMOS Levels)						
Input LOW level	V_{IL}				0.3 x DVDD	V
Input HIGH level	V_{IH}		0.7 x DVDD			V
Input leakage current				±0.2	±1	µA
Input capacitance				5		pF
Output LOW	V_{OL}	I_{OL}=1mA			0.1 x DVDD	V
Output HIGH	V_{OH}	I_{OH}= -1mA	0.9 x DVDD			V
Analogue Reference Levels						
Reference voltage	V_{VMID}		VREFP/2 – 50mV	VREFP/2	VREFP/2 + 50mV	V
Potential divider resistance	R_{VMID}	VREFP to VMID and VMID to VREFN		50		kΩ
Supply Current						
Analogue supply current		AVDD, VREFP = 5V		TBD		mA
Digital supply current		DVDD = 3.3V		TBD		mA

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted.
2. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD (dB) - THD is a ratio, of the rms values, of Distortion/Signal.
4. Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
5. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
6. Pass-Band Ripple - Any variation of the frequency response in the pass-band region.

MASTER CLOCK TIMING

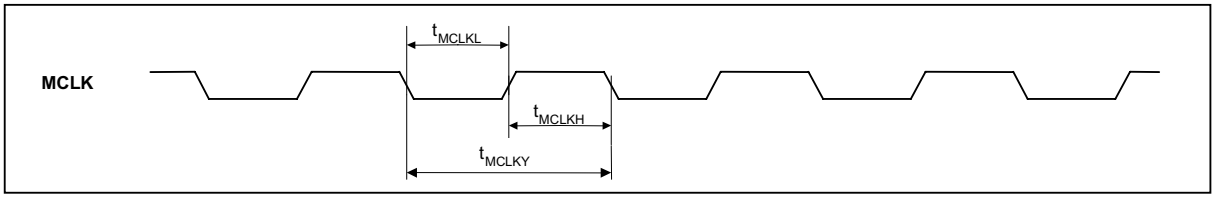


Figure 1 ADC and DAC Master Clock Timing Requirements

Test Conditions

AVDD, VREFP = 5V, DVDD = 3.3V, AGND, VREFN = 0V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, DACMCLK and ADCMCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK System clock pulse width high	t_{MCLKH}		11			ns
MCLK System clock pulse width low	t_{MCLKL}		11			ns
MCLK System clock cycle time	t_{MCLKY}		28			ns
MCLK Duty cycle			40:60		60:40	

Table 1 Master Clock Timing Requirements

DIGITAL AUDIO INTERFACE – MASTER MODE

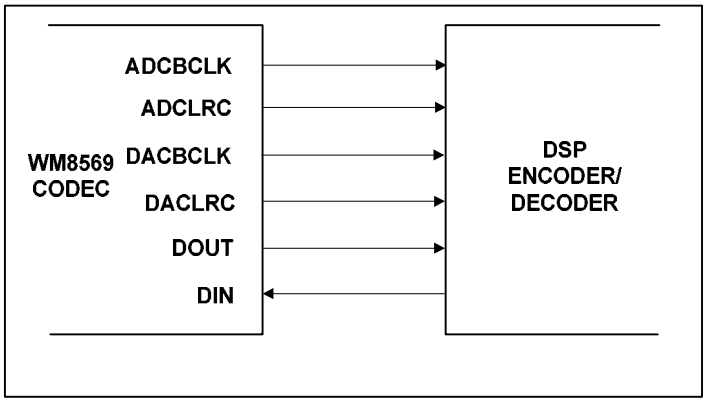


Figure 2 Audio Interface – Master Mode

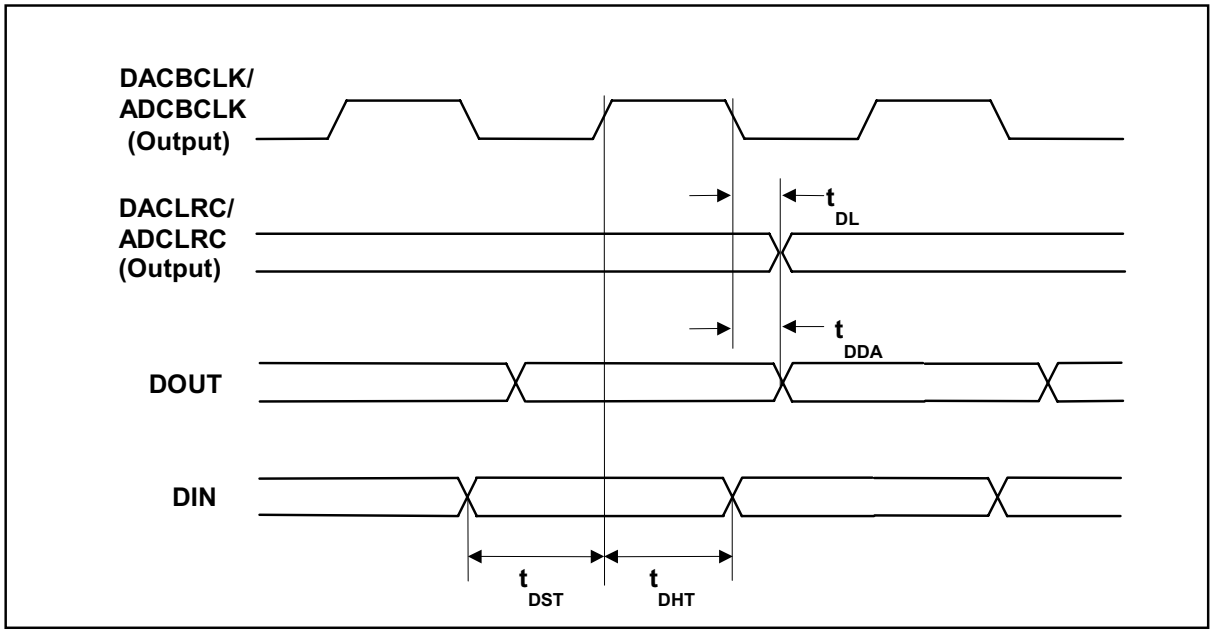


Figure 3 Digital Audio Data Timing – Master Mode

Test Conditions

AVDD, VREFP = 5V, DVDD = 3.3V, AGND, VREFN, DGND = 0V, T_A = +25°C, Master Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
DACLRC/ADCLRC propagation delay from DACBCLK/ADCBCLK falling edge	t_{DL}		0		10	ns
DOUT propagation delay from ADCBCLK falling edge	t_{DDA}		0		10	ns
DIN setup time to DACBCLK rising edge	t_{DST}		10			ns
DIN hold time from DACBCLK rising edge	t_{DHT}		10			ns

Table 2 Digital Audio Data Timing – Master Mode

DIGITAL AUDIO INTERFACE – SLAVE MODE

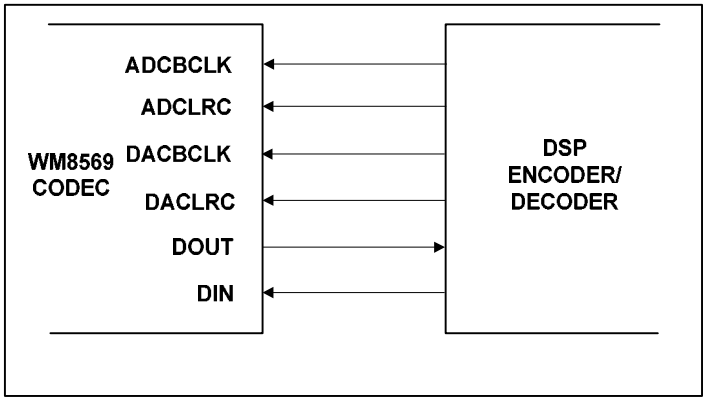


Figure 4 Audio Interface – Slave Mode

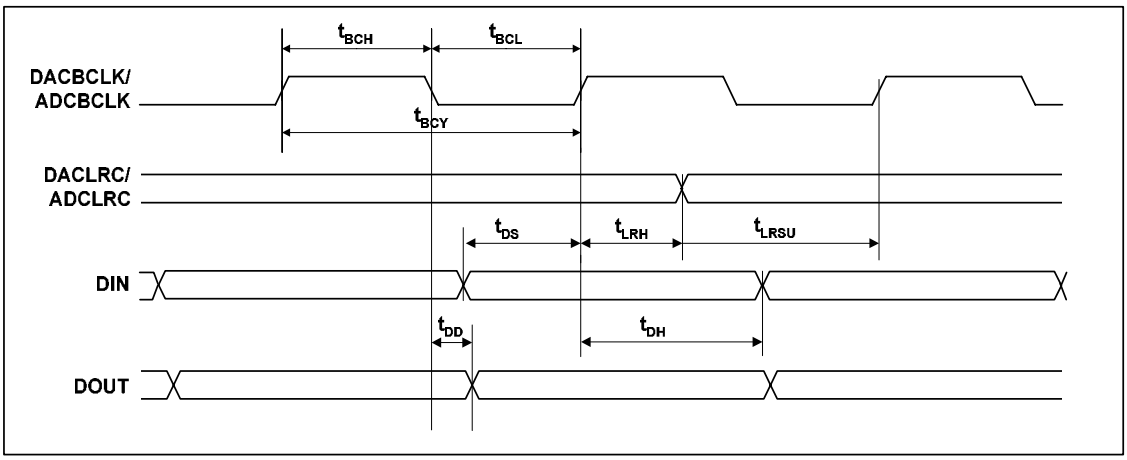


Figure 5 Digital Audio Data Timing – Slave Mode

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, DACMCLK and ADCMCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
ADCBCLK/DACBCLK cycle time	t_{BCY}		50			ns
ADCBCLK/DACBCLK pulse width high	t_{BCH}		20			ns
ADCBCLK/DACBCLK pulse width low	t_{BCL}		20			ns
ADCLRC/DACLRC set-up time to ADCBCLK/DACBCLK rising edge	t_{LRSU}		10			ns
ADCLRC/DACLRC hold time from ADCBCLK/DACBCLK rising edge	t_{LRH}		10			ns
DIN set-up time to DACBCLK rising edge	t_{DS}		10			ns
DIN hold time from DACBCLK rising edge	t_{DH}		10			ns
DOUT propagation delay from ADCBCLK falling edge	t_{DD}		0		10	ns

Table 3 Digital Audio Data Timing – Slave Mode

MPU INTERFACE TIMING

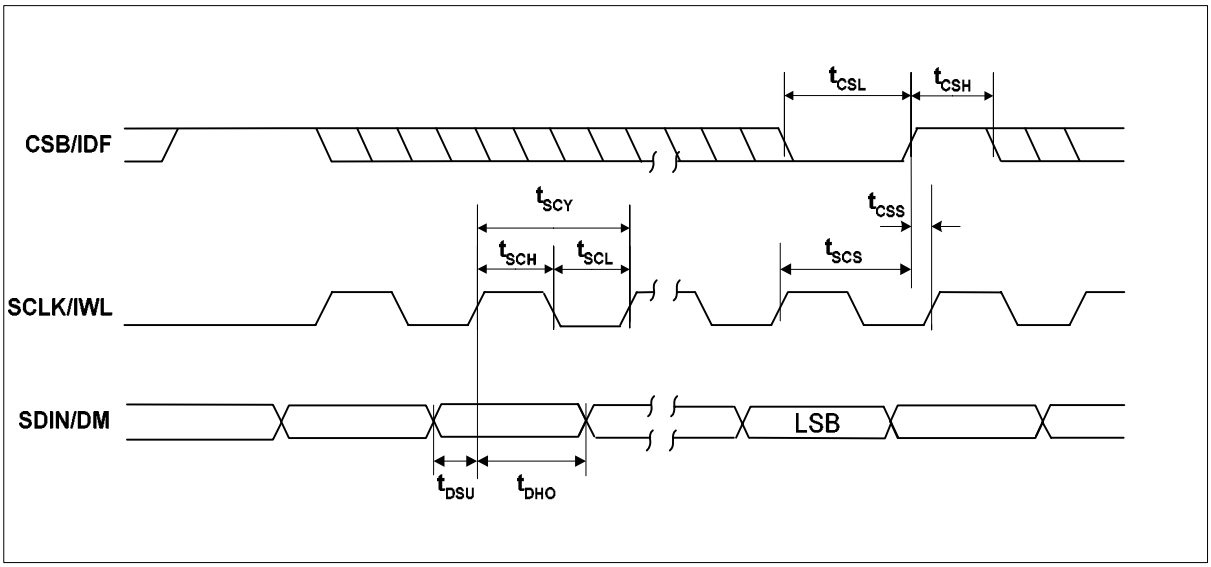


Figure 6 SPI Compatible Control Interface Input Timing

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, DACMCLK and ADCMCLK = 256fs unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SCLK/IWL rising edge to CSB/IDF rising edge	t_{SCS}	60			ns
SCLK/IWL pulse cycle time	t_{SCY}	80			ns
SCLK/IWL pulse width low	t_{SCL}	30			ns
SCLK/IWL pulse width high	t_{SCH}	30			ns
SDIN/DM to SCLK/IWL set-up time	t_{DSU}	20			ns
SCLK/IWL to SDIN/DM hold time	t_{DHO}	20			ns
CSB/IDF pulse width low	t_{CSL}	20			ns
CSB/IDF pulse width high	t_{CSH}	20			ns
CSB/IDF rising to SCLK/IWL rising	t_{CSS}	20			ns

Table 4 3-Wire SPI Compatible Control Interface Input Timing Information

INTERNAL POWER ON RESET CIRCUIT

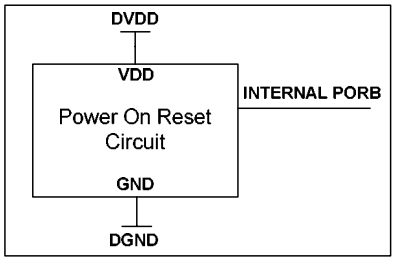


Figure 7 Internal Power on Reset Circuit Schematic

The WM8569 includes an internal Power-On-Reset Circuit, as shown in Figure 7, which is used reset the digital logic into a default state after power up. The POR circuit is powered from DVDD and monitors DVDD. It asserts PORB low if DVDD is below a minimum threshold.

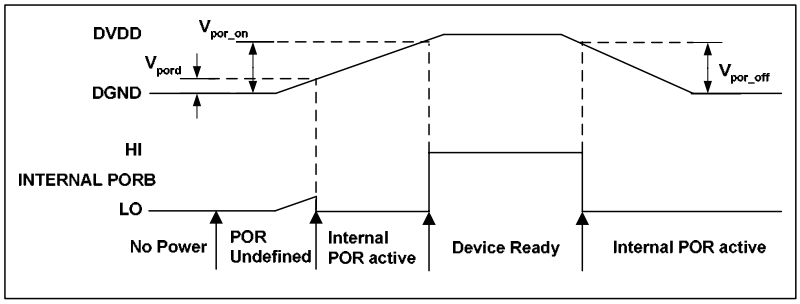


Figure 8 Typical Power-Up Sequence

Figure 8 shows a typical power-up sequence. When DVDD goes above the minimum threshold, Vpord, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When DVDD rises to Vpor_on, PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, PORB is asserted low whenever DVDD drops below the minimum threshold Vpor_off.

SYMBOL	MIN	TYP	MAX	UNIT
V_{pord}	0.3	0.5	0.8	V
V_{por_on}	1.3	1.7	2.0	V
V_{por_off}	1.3	1.7	2.0	V

Table 5 Typical POR Operation (typical values, not tested)

DEVICE DESCRIPTION

INTRODUCTION

WM8569 is a complete 2-channel audio codec, including digital interpolation and decimation filters, multi-bit sigma delta stereo ADC, and switched capacitor multi-bit sigma delta DAC with volume control and output smoothing filter.

The device is implemented as a separate stereo DAC and a stereo ADC in a single package and controlled by a single 3-wire software or hardware interface.

The DAC has its own data input DIN, DAC word clock DACLRC, DAC bit clock DACBCLK and DAC master clock DACMCLK while the stereo ADC has its own data output DOUT, word clock ADCLRC, bit clock ADCBCLK and ADC master clock ADCMCLK. This allows the ADC and DAC to operate independently.

The Audio Interface may be configured to operate in either master or slave mode. In Slave mode DACLRC/ADCLRC and DACBCLK/ADCBCLK are all inputs. In Master mode DACLRC/ADCLRC and DACBCLK/ADCBCLK are all outputs.

The DAC has its own digital volume control that is adjustable in 0.5dB steps. A zero cross detect circuit is provided. The digital volume control detects a transition through the zero point before updating the volume. This minimises audible clicks and 'zipper' noise as the gain values change.

Control of internal functionality of the device is by 3-wire serial or pin programmable control interface.

Operation using master clocks of 128fs, 192fs, 256fs, 384fs, 512fs or 768fs is provided for the DAC, for operation of both the ADC and DAC master clocks of 256fs, 384fs, 512fs and 768fs is provided. In Slave mode, selection between clock rates is automatically controlled. In master mode, the sample rate is set by control bits DACRATE and ADCRATE. Audio sample rates (fs) from less than 8kHz up to 192kHz are allowed for the DAC and from less than 32kHz up to 96kHz for the ADC, provided the appropriate master clock is input.

The audio data interface supports right-justified, left-justified and I^2S interface formats along with a highly flexible DSP serial port interface.

AUDIO DATA SAMPLING RATES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. The external master system clock can be applied directly through the ADC and DAC MCLK input pin(s) with no software configuration necessary. In a system where there are a number of possible sources for the reference clock it is recommended that the clock source with the lowest jitter be used to optimise the performance of the ADC and DAC.

The DAC master clock for WM8569 supports audio sampling rates from 128fs to 768fs, where fs is the audio sampling frequency (DACLRC) typically 32kHz, 44.1kHz, 48kHz, 96kHz or 192kHz. The ADC master clock for WM8569 supports audio sampling rates from 256fs to 768fs, where fs is the audio sampling frequency (ADCLRC) typically 32kHz, 44.1kHz, 48kHz or 96kHz. The master clock is used to operate the digital filters and the noise shaping circuits.

In Slave mode the WM8569 has a master clock detection circuit that automatically determines the relationship between the system clock frequency and the sampling rate (to within +/- 32 master clocks). If there is a greater than 32 clocks error the interface defaults to 768fs mode. The master clocks must be synchronised with LRC, although the WM8569 is tolerant of phase variations or jitter on this clock. Table 6 shows the typical master clock frequency inputs for the WM8569.

The signal processing for the WM8569 typically operates at an oversampling rate of 128fs for both ADC and DAC. The exception to this for the DAC is for operation with a 128/192fs system clock, e.g. for 192kHz operation, when the oversampling rate is 64fs. For ADC operation at 96kHz it is recommended that the user set the ADCOSR bit. This changes the ADC signal processing oversample rate to 64fs.

SAMPLING RATE (DACLRC/ ADCLRC)	System Clock Frequency (MHz)					
	128fs	192fs	256fs	384fs	512fs	768fs
	DAC only	DAC only				
32kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1kHz	5.6448	8.467	11.2896	16.9340	22.5792	33.8688
48kHz	6.144	9.216	12.288	18.432	24.576	36.864
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable

Table 6 System Clock Frequencies Versus Sampling Rate

HARDWARE CONTROL MODES

When the MODE pin is held high, the following hardware modes of operation are available.

Note: When in hardware mode the ADC and DAC will only run in slave mode.

MUTE AND AUTOMUTE OPERATION

In both hardware and software modes, MUTE controls the selection of MUTE directly, and can be used to enable and disable the automute function. This pin becomes an output when left floating and indicates infinite ZERO detect (IZD) has been detected.

	DESCRIPTION
0	Normal Operation
1	Mute DAC channels
Floating	Enable IZD, MUTE becomes an output to indicate when IZD occurs. L=IZD detected, H=IZD not detected.

Table 7 Mute and Automute Control

Figure 9 shows the application and release of MUTE whilst a full amplitude sinusoid is being played at 48kHz sampling rate. When MUTE (lower trace) is asserted, the output (upper trace) begins to decay exponentially from the DC level of the last input sample. The output will decay towards V_{MID} with a time constant of approximately 64 input samples. If MUTE is applied to all channels for 1024 or more input samples the outputs will be connected directly to V_{MID} if IZD is set. When MUTE is de-asserted, the output will restart immediately from the current input sample.

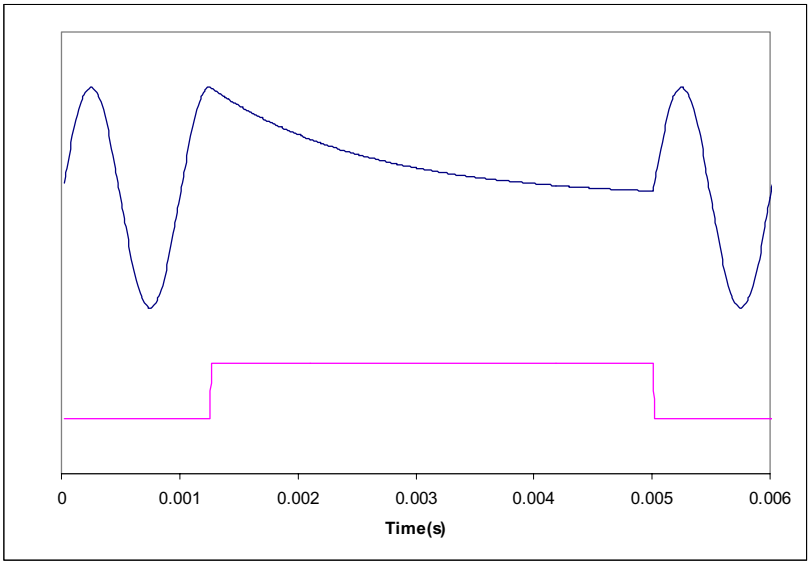


Figure 9 Application and Release of Soft Mute

The MUTE pin is an input to select mute or not mute. MUTE is active high; taking the pin high causes the filters to soft mute, ramping down the audio signal over a few milliseconds. Taking MUTE low again allows data into the filter.

The automute function detects a series of ZERO value audio samples of 1024 samples long being applied to both channels. After such an event, a latch is set whose output (AUTOMUTED) is wire OR'd through a 10kΩ resistor to the MUTE pin. Thus if the MUTE pin is not being driven, the automute function will assert mute.

If MUTE is tied low, AUTOMUTED is overridden and will not mute unless the IZD register bit is set. If MUTE is driven from a bi-directional source, then both MUTE and automute functions are available. If MUTE is not driven, AUTOMUTED appears as a weak output (10kΩ source impedance) and can be used to drive external mute circuits. AUTOMUTED will be removed as soon as any channel receives a non-ZERO input.

A diagram showing how the various Mute modes interact is shown below.

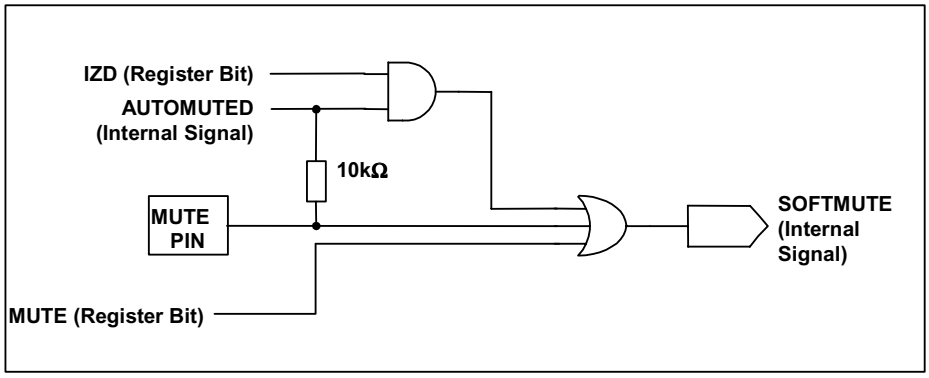


Figure 10 Control of MUTE Modes

INPUT FORMAT SELECTION

In hardware mode, CSB/IDF and SCLK/IWL become input controls for selection of input data format type and input data word length for both the ADC and DAC.

CSB/IDF	SCLK/IWL	INPUT DATA MODE
0	0	24-bit right justified
0	1	20-bit right justified
1	0	16-bit I^2S
1	1	24-bit I^2S

Table 8 Input Format Selection

Note:

In 24 bit I^2S mode, any width of 24 bits or less is supported provided that the left/right clocks (ADCLRC and DACLRC) are high for a minimum of 24 bit clocks (ADCBCLK and DACBCLK) and low for a minimum of 24 bit clocks.

DE-EMPHASIS CONTROL

In hardware mode, the SDIN/DM pin becomes an input control for selection of de-emphasis filtering to be applied.

SDIN/DM	DE-EMPHASIS
0	Off
1	On

Table 9 De-emphasis Control

DIGITAL AUDIO INTERFACE

MASTER AND SLAVE MODES

The audio interface operates in either Slave or Master mode, selectable using the DACMS and ADCMS control bits. In both Master and Slave modes DIN is always an input to the WM8569 and DOUT is always an output. The default is Slave mode.

In Slave mode, DACLRC, ADCLRC, DACBCLK and ADCBCLK are inputs to the WM8569 (Figure 11). DIN and DACLRC are sampled by the WM8569 on the rising edge of DACBCLK. ADC data is output on DOUT and changes on the falling edge of ADCBCLK.

By setting the control bit DACBCP the polarity of DACBCLK may be reversed so that DIN is sampled on the falling edge of DACBCLK. By setting the control bit ADCBCP, the polarity of ADCBCLK may be reversed so that DOUT changes on the rising edge of ADCBCLK.

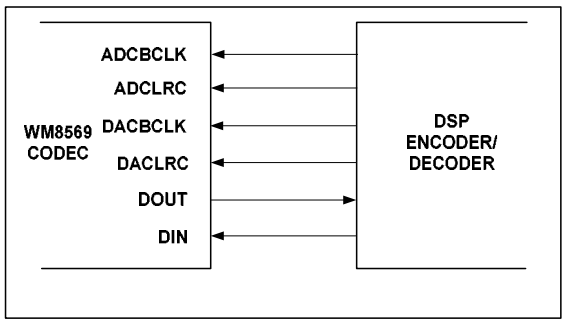


Figure 11 Slave Mode

In Master mode, DACLRC, ADCLRC, DACBCLK and ADCBCLK are outputs from the WM8569 (Figure 12). DACLRC, ADCLRC, DACBCLK and ADCBCLK are generated by the WM8569. DIN is sampled by the WM8569 on the rising edge of DACBCLK so the controller must output DAC data that changes on the falling edge of DACBCLK. ADC data is output on DOUT and changes on the falling edge of ADCBCLK.

By setting the control bit DACBCP the polarity of DACBCLK may be reversed so that DIN is sampled on the falling edge of DACBCLK. By setting the control bit ADCBCP, the polarity of ADCBCLK may be reversed so that DOUT changes on the rising edge of ADCBCLK.

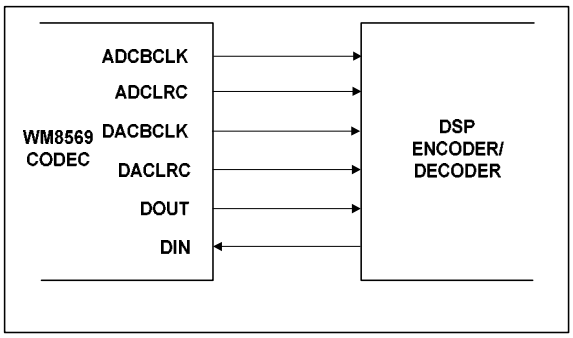


Figure 12 Master Mode

AUDIO INTERFACE FORMATS

Audio data is applied to the internal DAC filters or output from the ADC filters, via the Digital Audio Interface. 5 popular interface formats are supported:

- Left Justified mode
- Right Justified mode
- I^2S mode
- DSP Mode A
- DSP Mode B

All 5 formats send the MSB first and support word lengths of 16, 20, 24 and 32 bits, with the exception of 32 bit right justified mode, which is not supported.

In left justified, right justified and I^2S modes, the digital audio interface receives DAC data on the DIN input and outputs ADC data on DOUT. Audio Data for each stereo channel is time multiplexed with DACLRC/ADCLRC indicating whether the left or right channel is present. DACLRC/ADCLRC is also used as a timing reference to indicate the beginning or end of the data words.

In left justified, right justified and I^2S modes, the minimum number of BCLKs per LRC period is 2 times the selected word length. LRC must be high for a minimum of word length BCLKs and low for a minimum of word length BCLKs. Any mark to space ratio on LRC is acceptable provided the above requirements are met.

In DSP mode A or B, the DAC channels are time multiplexed onto DIN. LRC is used as a frame sync signal to identify the MSB of the first word. The minimum number of DACBCLKs per DACLRC period is 6 times the selected word length. Any mark to space ratio is acceptable on DACLRC provided the rising edge is correctly positioned. The ADC data may also be output in DSP mode A or B, with ADCLRC used as a frame sync to identify the MSB of the first word. The minimum number of ADCBCLKs per ADCLRC period is 2 times the selected word length if only the ADC is being operated.

LEFT JUSTIFIED MODE

In left justified mode, the MSB of DIN is sampled by the WM8569 on the first rising edge of DACBCLK following a DACLRC transition. The MSB of the ADC data is output on DOUT and changes on the same falling edge of ADCBCLK as ADCLRC and may be sampled on the rising edge of BCLK. LRC is high during the left samples and low during the right samples (Figure 13).

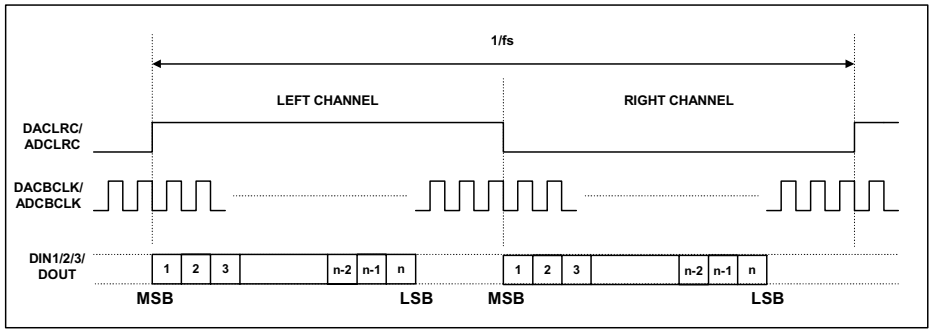


Figure 13 Left Justified Mode Timing Diagram

RIGHT JUSTIFIED MODE

In right justified mode, the LSB of DIN is sampled by the WM8569 on the rising edge of DACBCLK preceding a DACLRC transition. The LSB of the ADC data is output on DOUT and changes on the falling edge of ADCBCLK preceding a ADCLRC transition and may be sampled on the rising edge of ADCBCLK. LRC are high during the left samples and low during the right samples (Figure 14).

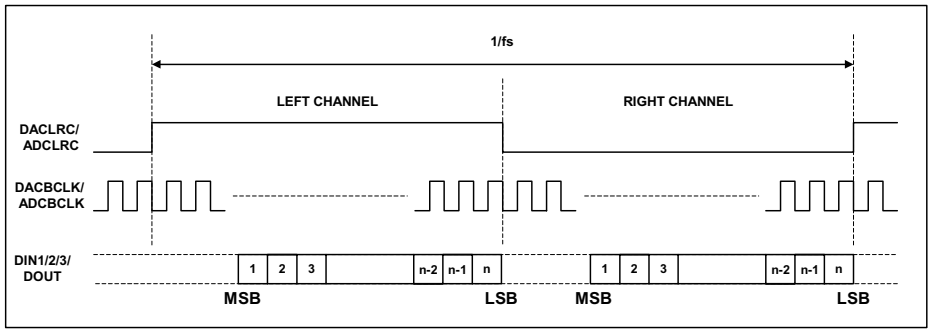


Figure 14 Right Justified Mode Timing Diagram

I²S MODE

In I²S mode, the MSB of DIN is sampled by the WM8569 on the second rising edge of DACBCLK following a DACLRC transition. The MSB of the ADC data is output on DOUT and changes on the first falling edge of ADCBCLK following an ADCLRC transition and may be sampled on the rising edge of ADCBCLK. LRC are low during the left samples and high during the right samples.

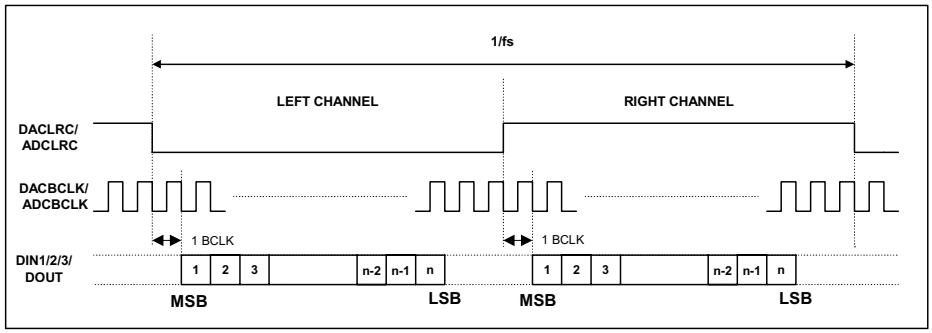


Figure 15 I²S Mode Timing Diagram

DSP MODE A

In DSP mode A, the MSB of DAC left channel data is sampled by the WM8569 on the second rising edge on DACBCLK following a DACLRC rising edge. DAC right channel follows DAC left channel (Figure 16).

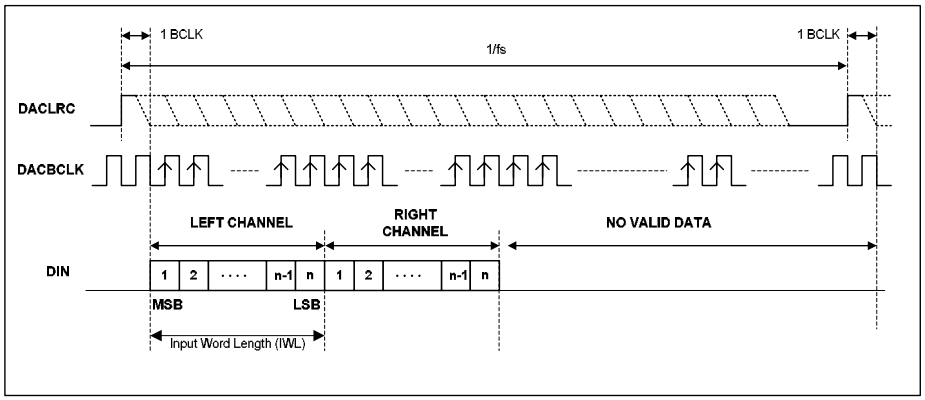


Figure 16 DSP Mode A Timing Diagram – DAC Data Input

The MSB of the left channel ADC data is output on DOUT and changes on the first falling edge of ADCBCLK following a low to high ADCLRC transition and may be sampled on the rising edge of ADCBCLK. The right channel ADC data is contiguous with the left channel data (Figure 17)

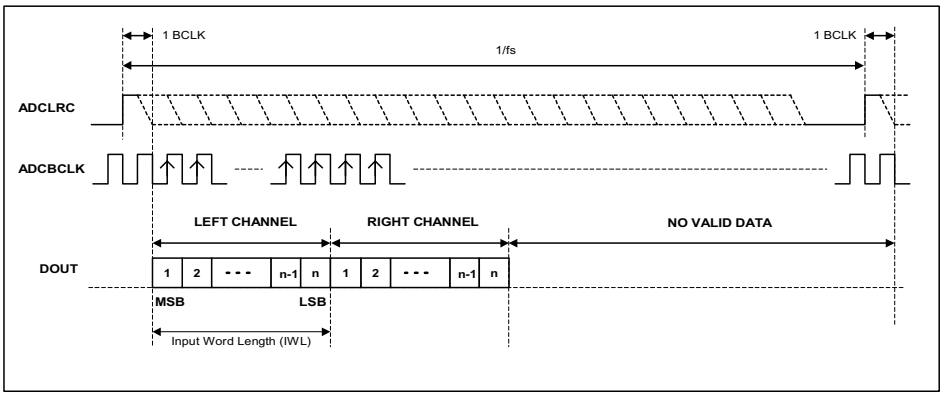


Figure 17 DSP Mode A Timing Diagram – ADC Data Output

DSP MODE B

In DSP mode B, the MSB of DAC left channel data is sampled by the WM8569 on the first DACBCLK rising edge following a DACLRC rising edge. (Figure 18).

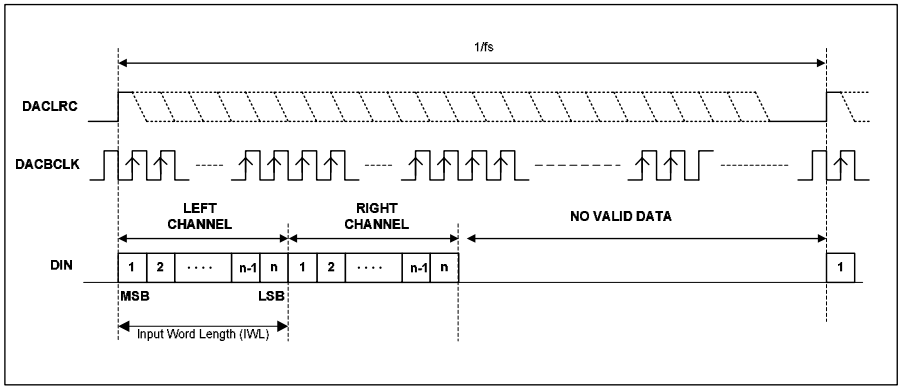


Figure 18 DSP Mode B Timing Diagram – DAC Data Input

The MSB of the left channel ADC data is output on DOUT and changes on the same falling edge of ADCBCLK as the low to high ADCLRC transition and may be sampled on the rising edge of ADCBCLK. The right channel ADC data is contiguous with the left channel data (Figure 19).

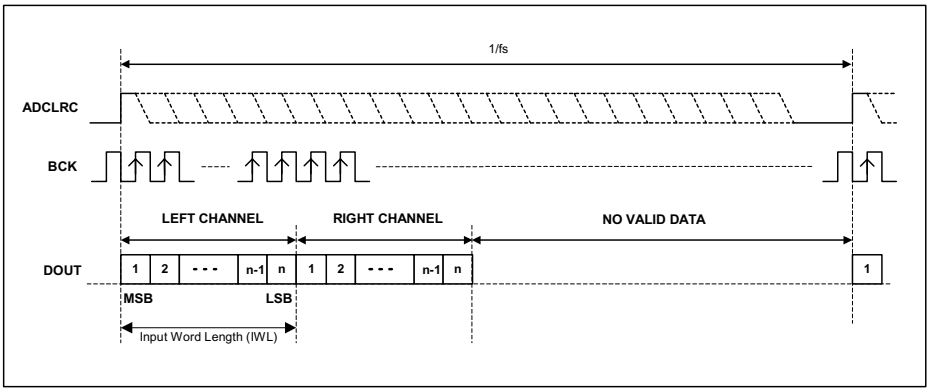


Figure 19 DSP Mode B Timing Diagram – ADC Data Output

POWERDOWN MODES

The WM8569 has powerdown control bits allowing specific parts of the WM8569 to be powered off when not being used. Control bit ADCPD powers off the ADC. The three stereo DACs each have a separate powerdown control bit, DACPD[2:0] allowing individual stereo DACs to be powered off when not in use. Setting ADCPD and DACPD[2:0] will powerdown everything except the references VMID and REFADC. These may be powered down by setting PDWN. Setting PDWN will override all other powerdown control bits. It is recommended that the ADC and DACs are powered down before setting PDWN.

ZERO DETECT

The WM8569 has a zero detect circuit for each DAC channel that detects when 1024 consecutive zero samples have been input. The MUTE pin output may be programmed to output the zero detect signal which may then be used to control external muting circuits. A '1' on MUTE indicates a zero detect. The zero detect may also be used to automatically enable DAC mute by setting IZD.

SOFTWARE CONTROL INTERFACE OPERATION

The WM8569 is controlled using a 3-wire serial interface in software mode or pin programmable in hardware mode.

The control mode is selected by the state of the MODE pin.

3-WIRE (SPI COMPATIBLE) SERIAL CONTROL MODE

SDIN/DM is used for the program data, SCLK/IWL is used to clock in the program data and CSB/IDF is used to latch the program data. SDIN/DM is sampled on the rising edge of SCLK/IWL. The 3-wire interface protocol is shown in Figure 20.

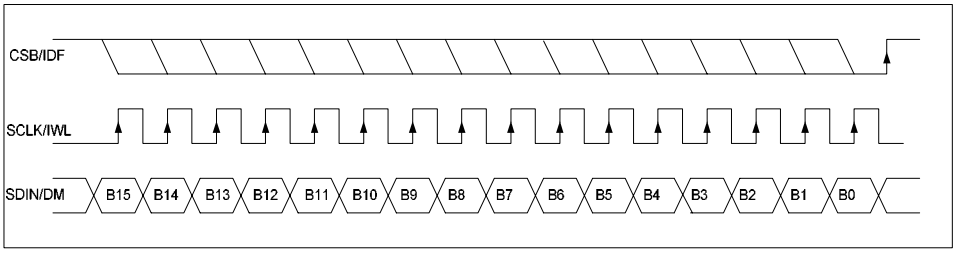


Figure 20 3-Wire SPI Compatible Interface

Notes:

1. B[15:9] are Control Address Bits
2. B[8:0] are Control Data Bits
3. CSB/IDF is edge sensitive – the data is latched on the rising edge of CSB/IDF.

REGISTER MAP

The complete register map is shown below. The detailed description can be found in the relevant text of the device description. The WM8569 can be configured using the Control Interface. All unused bits should be set to '0'.

REGISTER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
R0(00h)	0	0	0	0	0	0	0	UPDATE	LDA[7:0]								011111111
R1(01h)	0	0	0	0	0	0	1	UPDATE	RDA[7:0]								011111111
R2(02h)	0	0	0	0	0	1	0	PL[8:5]				IZD	ATC	0	0	0	100100000
R3(03h)	0	0	0	0	0	1	1	0	0	PHASE	DACIWL[5:4]		DACBCP	DACLRP	DACFMT[1:0]		000000000
R8(08h)	0	0	0	1	0	0	0	UPDATE	MASTDA[7:0]								011111111
R9(09h)	0	0	0	1	0	0	1	0	0	DEEMP	0	0	DMUTE	0	0	ZCD	000000000
R10(0Ah)	0	0	0	1	0	1	0	DACRATE[8:6]			DACMS	PWRDNALL	0	0	DACPD	ADCPD	010000000
R11(0Bh)	0	0	0	1	0	1	1	ADC OSR	ADCRATE[7:5]			ADCMS	ADCIWL[3:2]		ADCFMT[1:0]		001000000
R12(0Ch)	0	0	0	1	1	0	0	0	0	MPD	ADCBCP	ADCLRP	ADCHP	AMUTE ALL	AMUTEL	AMUTER	000000000
R31(1Fh)	0	0	1	1	1	1	1	RESET									000000000

CONTROL INTERFACE REGISTERS

ATTENUATOR CONTROL MODE

Setting the ATC register bit causes the left channel attenuation settings to be applied to both the left and right channel of the DAC from the next audio input sample. No update to the attenuation registers is required for ATC to take effect.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000010 DAC Channel Control	3	ATC	0	Attenuator Control Mode: 0: Right channel use right attenuations 1: Right channel use left attenuations

INFINITE ZERO DETECT ENABLE

Setting the IZD register bit will enable the internal infinite zero detect function:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000010 DAC Channel Control	4	IZD	0	Infinite Zero Mute Enable 0 : Disable inifinite zero mute 1: Enable infinite zero mute

With IZD enabled, applying 1024 consecutive zero input samples each stereo channel will cause that stereo channel outputs to be muted to V_{MID}. Mute will be removed as soon as that stereo channel receives a non-zero input.

DAC OUTPUT CONTROL

The DAC output control word determines how the left and right input to the audio Interface are applied to the left and right DAC:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION		
0000010 DAC Control	8:5	PL[3:0]	1001	PL[3:0]	Left Output	Right Output
				0000	Mute	Mute
				0001	Left	Mute
				0010	Right	Mute
				0011	(L+R)/2	Mute
				0100	Mute	Left
				0101	Left	Left
				0110	Right	Left
				0111	(L+R)/2	Left
				1000	Mute	Right
				1001	Left	Right
				1010	Right	Right
				1011	(L+R)/2	Right
				1100	Mute	(L+R)/2
				1101	Left	(L+R)/2
				1110	Right	(L+R)/2
				1111	(L+R)/2	(L+R)/2

DAC DIGITAL AUDIO INTERFACE CONTROL REGISTER

Interface format is selected via the DACFMT[1:0] register bits:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000011 Interface Control	1:0	DACFMT [1:0]	00	Interface Format Select: 00 : Right justified mode 01: Left justified mode 10: I^2S mode 11: DSP mode A orB

In left justified, right justified or I^2S modes, the DACLRP register bit controls the polarity of DACLRC. If this bit is set high, the expected polarity of DACLRC will be the opposite of that shown Figure 13, Figure 14 and Figure 15. Note that if this feature is used as a means of swapping the left and right channels, a 1 sample phase difference will be introduced. In DSP modes, the DACLRP register bit is used to select between modes A and B.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000011 Interface Control	2	DACLRP	0	In left/right/I^2S Modes: DACLRC Polarity (normal) 0 : Normal DACLRC polarity 1: Inverted DACLRC polarity
				In DSP Mode: 0 : Mode A 1: Mode B

By default, DACLRC and DIN are sampled on the rising edge of DACBCLK and should ideally change on the falling edge. Data sources that change DACLRC and DIN on the rising edge of DACBCLK can be supported by setting the DACBCP register bit. Setting DACBCP to 1 inverts the polarity of DACBCLK to the inverse of that shown in Figure 13 to Figure 19.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000011 Interface Control	3	DACBCP	0	DACBCLK Polarity (DSP Modes): 0: Normal BCLK polarity 1: Inverted BCLK polarity

The DACIWL[1:0] bits are used to control the input word length.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000011 Interface Control	5:4	DACIWL [1:0]	00	Input Word Length: 00 : 16 bit data 01: 20 bit data 10: 24 bit data 11: 32 bit data

Note: 32-bit right justified mode is not supported.

In all modes, the data is signed 2's complement. The digital filters always input 24-bit data. If the DAC is programmed to receive 16 or 20 bit data, the WM8569 pads the unused LSBs with zeros. If the DAC is programmed into 32 bit mode, the 8 LSBs are ignored.

Note: In 24 bit I^2S mode, any width of 24 bits or less is supported provided that LRC is high for a minimum of 24 BCLKs and low for a minimum of 24 BCLKs.

A number of options are available to control how data from the Digital Audio Interface is applied to the DAC channels.

DAC OUTPUT PHASE

The DAC Phase control word determines whether the output of the DAC is non-inverted or inverted

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000011 DAC Phase	6	PHASE	0	0 = non-inverted 1 = inverted

DIGITAL ZERO CROSS-DETECT

The Digital volume control also incorporates a zero cross detect circuit which detects a transition through the zero point before updating the digital volume control with the new volume. This is enabled by control bit ZCD.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001001 DAC Control	0	ZCD	0	DAC Digital Volume Zero Cross Disable: 0: Zero cross detect enabled 1: Zero cross detect disabled

DAC MUTE MODES

The WM8569 has a mute for the DAC channels. Setting MUTE will apply a 'soft' mute to the input of the digital filters.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001001 DAC Mute	3	DMUTE	0	DAC Soft Mute Select 0 = Not mute 1 = Mute

Refer to Figure 9 for the plot of application and release of soft mute.

Note that all other means of muting the DAC channels: setting the PL[3:0] bits to 0, setting the PDWN bit or setting attenuation to 0 will cause much more abrupt muting of the output.

ADC MUTE MODES

Each ADC channel also has a mute control bit, which mutes the inputs to the ADC.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001100 ADC Mute	0	AMUTER	0	ADC Mute Select: 0 : Normal operation 1: mute ADC right
	1	AMUTEL	0	ADC Mute Select: 0 : Normal operation 1: mute ADC left
	2	AMUTEALL	0	ADC Mute Select: 0 : Normal operation 1: mute both ADC channels

DE-EMPHASIS MODE

Each stereo DAC channel has an individual de-emphasis control bit:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001001 DAC De-Emphahsis Control	6	DEEMPH	0	De-emphasis Channel Selection Select: 0 = Not de-emphasis 1 = De-emphasis

POWERDOWN MODE AND ADC/DAC DISABLE

The ADC and DAC may be powered down individually by setting the ADCPD and DACPD disable bits. Setting ADCPD will disable the ADC and select a low power mode. The ADC digital filters will be reset and will reinitialise when ADCPD is unset. Setting DACPD will disable the DAC and select a low power mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001010 Powerdown Control	0	ADCPD	0	ADC Disable: 0: Active 1: Disable
	1	DACPD	0	DAC Disable

MASTER POWERDOWN

This control bit powers down the references for the whole chip. Therefore for complete powerdown, both the ADC and DACs should be powered down first before setting this bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001010 Interface Control	4	PWRDNALL	0	Master Power Down Bit: 0: Not powered down 1: Powered down

DAC MASTER MODE SELECT

Control bit DACMS selects between audio interface Master and Slave Modes. In Master mode, DACLRC and DACBCLK are outputs and are generated by the WM8569. In Slave mode DACLRC and DACBCLK are inputs to WM8569.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001010 Interface Control	5	DACMS	0	DAC Audio Interface Master/Slave Mode Select: 0: Slave mode 1: Master mode

MASTER MODE DACLRC FREQUENCY SELECT

In Master mode the WM8569 generates DACLRC and DACBCLK. These clocks are derived from the master clock and the ratio of DACMCLK to DACLRC is set by DACRATE.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001010 Interface Control	8:6	DACRATE [2:0]	010	Master Mode MCLK:LRC Ratio Select: 000: 128fs (DAC only) 001: 192fs (DAC only) 010: 256fs 011: 384fs 100: 512fs 101: 768fs

ADC DIGITAL AUDIO INTERFACE CONTROL REGISTER

Interface format is selected via the ADCFMT[1:0] register bits:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001011 Interface Control	1:0	ADCFMT[1:0]	00	Interface Format Select 00: Right justified mode 01: Left justified mode 10: I^2S mode 11: DSP mode A or B

The ADCIWL[1:0] bits are used to control the input word length.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001011 Interface Control	3:2	ADCIWL[1:0]	00	Input Word Length 00: 16 bit data 01: 20 bit data 10: 24 bit data 11: 32 bit data

Note: 32-bit right justified mode is not supported.

In all modes, the data is signed 2's complement.

ADC MASTER MODE SELECT

Control bit ADCMS selects between audio interface Master and Slave Modes. In Master mode ADCLRC and ADCBCLK are outputs and are generated by the WM8569. In Slave mode ADCLRC and ADCBCLK are inputs to WM8569.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001011 Interface Control	4	ADCMS	0	ADC Audio Interface Master/Slave Mode Select: 0: Slave mode 1: Master mode

MASTER MODE ADCLRC FREQUENCY SELECT

In Master mode the WM8569 generates ADCLRC and ADCBCLK. These clocks are derived from the master clock and the ratio of ADCMCLK to ADCLRC is set by ADCRATE.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001011 ADCLRC and ADCBCLK Frequency Select	7:5	ADCRATE [2:0]	010	Master Mode ADCMCLK:ADCLRC Ratio Select: 010: 256fs 011: 384fs 100: 512fs 101: 768fs

ADC OVERSAMPLING RATE SELECT

For ADC operation at 96kHz it is recommended that the user set the ADCOSR bit. This changes the ADC signal processing oversampling rate to 64fs. The 64fs oversampling rate is only available in modes were a 96KHz rate is supported, i.e. 256fs or 384fs. In all other modes the ADC will stay in a 128fs oversampling rate irrespective of what this bit is set to.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001011 ADC Oversampling Rate	8	ADCOSR	0	ADC Oversampling Rate Select: 0: 128x oversampling 1: 64x oversampling

ADC HIGHPASS FILTER DISABLE

The ADC digital filters contain a digital highpass filter. This defaults to enabled and can be disabled using software control bit ADCHPD.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001100 ADC Control	3	ADCHPD	0	ADC Highpass Filter Disable: 0: Highpass filter enabled 1: Highpass filter disabled

In left justified, right justified or I^2S modes, the ADCLRP register bit controls the polarity of ADCLRC. If this bit is set high, the expected polarity of ADCLRC will be the opposite of that shown in Figure 13, Figure 14 and Figure 15. Note that if this feature is used as a means of swapping the left and right channels, a 1 sample phase difference will be introduced. In DSP modes, the ADCLRP register bit is used to select between modes A and B.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001100 Interface Control	4	ADCLRP	0	In Left/Right/I^2S Modes: ADCLRC Polarity (normal) 0: normal DACLRC polarity 1: inverted DACLRC polarity
				In DSP Mode: 0: DSP mode A 1: DSP mode B

By default, ADCLRC and DOUT are sampled on the rising edge of ADCBCLK and should ideally change on the falling edge. Data sources that change ADCLRC and DOUT on the rising edge of ADCBCLK can be supported by setting the ADCBCP register bit. Setting ADCBCP to 1 inverts the polarity of ADCBCLK to the inverse of that shown in Figure 13 to Figure 19

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001100 Interface Control	5	ADCBCP	0	ADCBCLK Polarity (DSP Modes): 0: normal BCLK polarity 1: inverted BCLK polarity

MUTE PIN DECODE

The MUTE pin can either be used an output or an input. As an output it indicated 1024 consecutive zero samples to the DAC. By default selecting the MUTE to represent if the DAC has received more than 1024 midrail samples will cause the MUTE to be asserted as a softmute on the DAC. Disabling the decode block will cause any logical high on the MUTE pin to apply a softmute to the DAC.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001100 ADC Control	6	MPD	0	MUTE Pin Decode Disable: 0: MUTE pin decode enable 1: MUTE pin decode disable

DAC DIGITAL VOLUME CONTROL

The DAC volume may also be adjusted in the digital domain using independent digital attenuation control registers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000000 Digital Attenuation DACL	7:0	LDA[7:0]	11111111 (0dB)	Digital Attenuation data for Left channel DACL in 0.5dB steps. See Table 10
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store LDA in intermediate latch (no change to output) 1: Store LDA and update attenuation on all channels
0000001 Digital Attenuation DACR	7:0	RDA[6:0]	11111111 (0dB)	Digital Attenuation data for Right channel DACR in 0.5dB steps. See Table 10
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store RDA in intermediate latch (no change to output) 1: Store RDA and update attenuation on all channels.
0001000 Master Digital Attenuation (all channels)	7:0	MASTDA [7:0]	11111111 (0dB)	Digital Attenuation data for all DAC channels in 0.5dB steps. See Table 10
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store gain in intermediate latch (no change to output) 1: Store gain and update attenuation on all channels.

L/RDAX[7:0]	ATTENUATION LEVEL
00(hex)	-∞ dB (mute)
01(hex)	-127dB
:	:
:	:
:	:
FE(hex)	-0.5dB
FF(hex)	0dB

Table 10 Digital Volume Control Attenuation Levels

SOFTWARE REGISTER RESET

Writing to register 11111 will cause a register reset, resetting all register bits to their default values. The device will be held in this reset state until a subsequent register write to any address is completed.

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter					
Passband	±0.01 dB	0		0.4535fs	
	-6dB		0.5fs		
Passband ripple				±0.01	dB
Stopband		0.5465fs			
Stopband Attenuation	f > 0.5465fs	-65			dB
DAC Filter					
Passband	±0.05 dB			0.444fs	
	-3dB		0.487fs		
Passband ripple				±0.05	dB
Stopband		0.555fs			
Stopband Attenuation	f > 0.555fs	-60			dB

Table 11 Digital Filter Characteristics

DAC FILTER RESPONSES

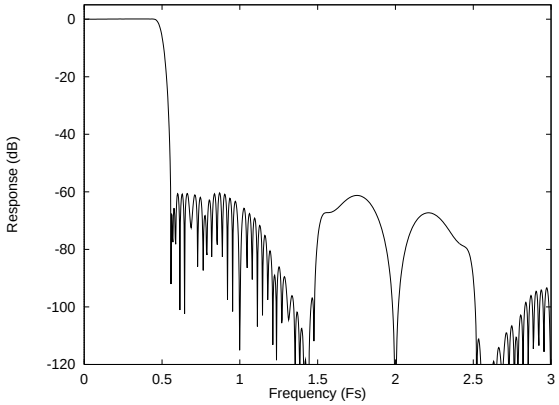


Figure 21 DAC Digital Filter Frequency Response – 44.1, 48 and 96kHz

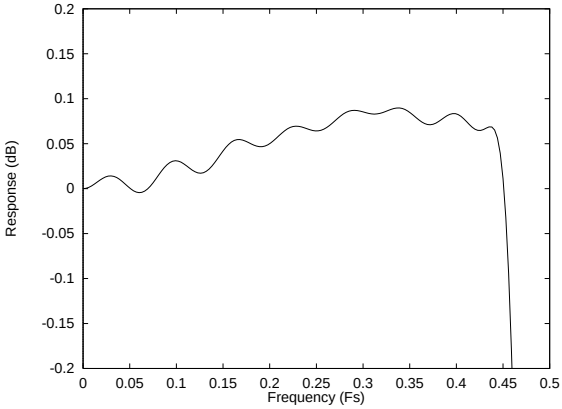


Figure 22 DAC Digital Filter Ripple –44.1, 48 and 96kHz

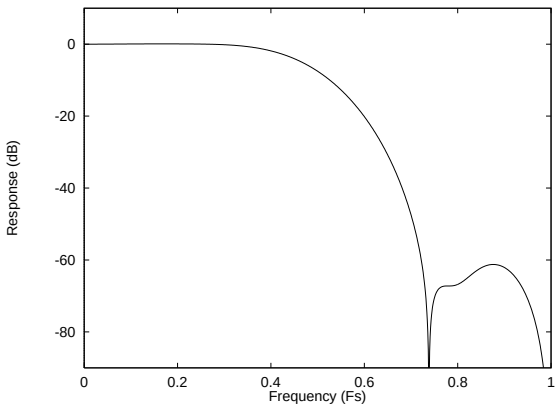


Figure 23 DAC Digital Filter Frequency Response – 192kHz

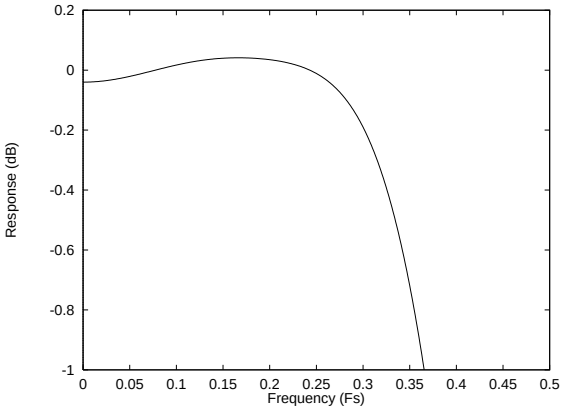


Figure 24 DAC Digital Filter Ripple – 192kHz

ADC FILTER RESPONSES

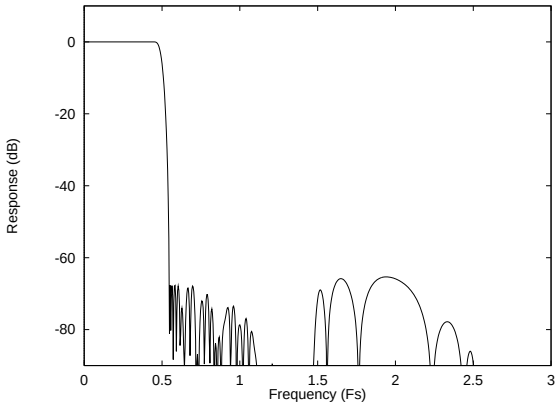


Figure 25 ADC Digital Filter Frequency Response

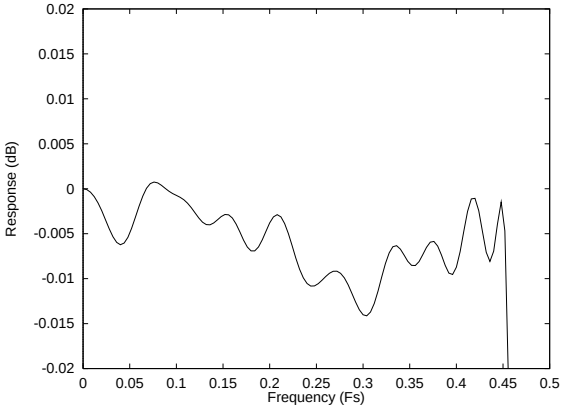


Figure 26 ADC Digital Filter Ripple

ADC HIGH PASS FILTER

The WM8569 has a selectable digital high pass filter to remove DC offsets. The filter response is characterised by the following polynomial.

$$H(z) = \frac{1 - z^{-1}}{1 - 0.9995z^{-1}}$$

DIGITAL DE-EMPHASIS CHARACTERISTICS

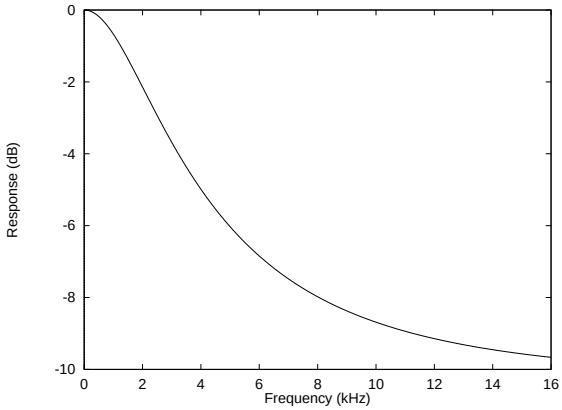


Figure 27 De-Emphasis Frequency Response (32kHz)

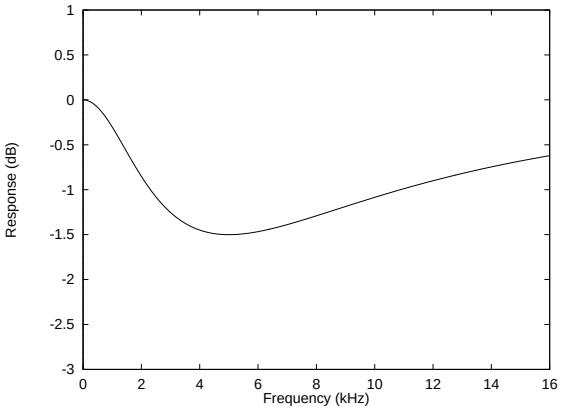


Figure 28 De-Emphasis Error (32kHz)

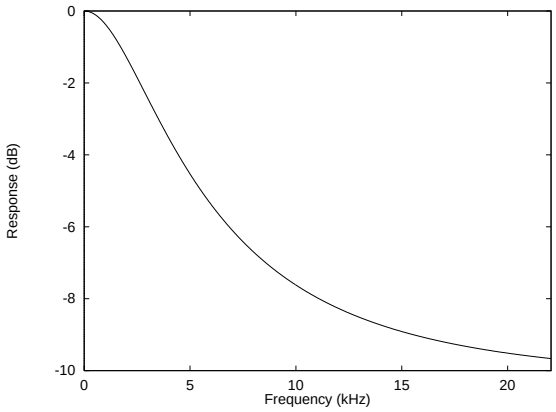


Figure 29 De-Emphasis Frequency Response (44.1kHz)

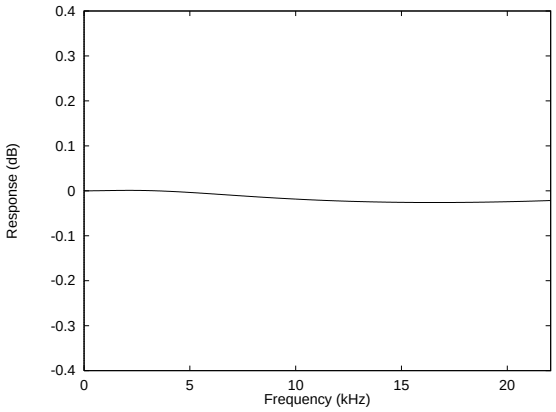


Figure 30 De-Emphasis Error (44.1kHz)

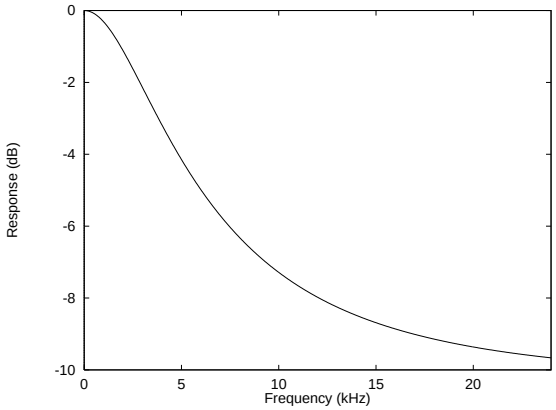


Figure 31 De-Emphasis Frequency Response (48kHz)

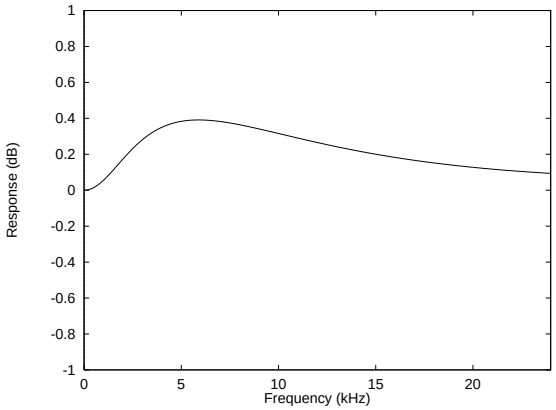
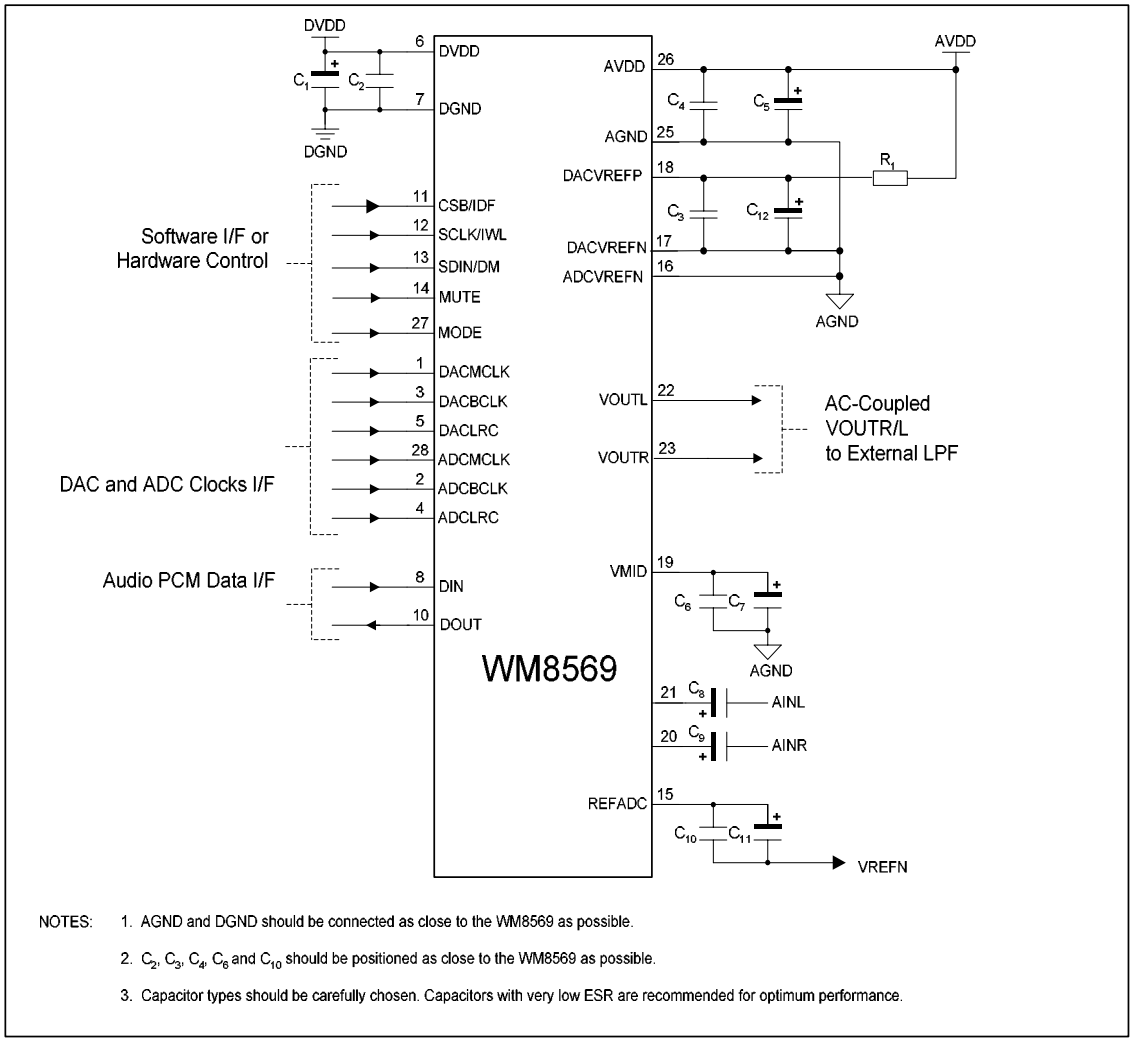


Figure 32 De-Emphasis Error (48kHz)

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS



NOTES:
1. AGND and DGND should be connected as close to the WM8569 as possible.
2. C_2, C_3, C_4, C_6 and C_{10} should be positioned as close to the WM8569 as possible.
3. Capacitor types should be carefully chosen. Capacitors with very low ESR are recommended for optimum performance.

Figure 33 Recommended External Components Diagram

RECOMMENDED EXTERNAL COMPONENTS VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1 and C5	10µF	De-coupling for DVDD and AVDD.
C2 to C4	0.1µF	De-coupling for DVDD and AVDD.
C8 and C9	1µF	Analogue input high pass filter capacitors
C6 and C10	0.1µF	Reference de-coupling capacitors for VMID and ADCREF pin.
C7 and C11	10µF	
C12	10µF	Filtering for VREFP. Omit if AVDD low noise.
R1	33Ω	Filtering for VREP. Use 0Ω if AVDD low noise.

Table 12 Recommended External Components Description

Note: Further details for filtering on reference pins are available in Wolfson Application Note WAN0144.

SUGGESTED ANALOGUE LOW PASS POST DAC FILTERS

It is recommended that a lowpass filter be applied to the output from each DAC channel for Hi Fi applications. Typically a second order filter is suitable and provides sufficient attenuation of high frequency components (the unique low order, high bit count multi-bit sigma delta DAC structure used in WM8569 produces much less high frequency output noise than normal sigma delta DACs. This filter is typically also used to provide the 2x gain needed to provide the standard 2Vrms output level from most consumer equipment.

Wolfson Application Note WAN0171 provides details of suitable post-DAC filter circuits.

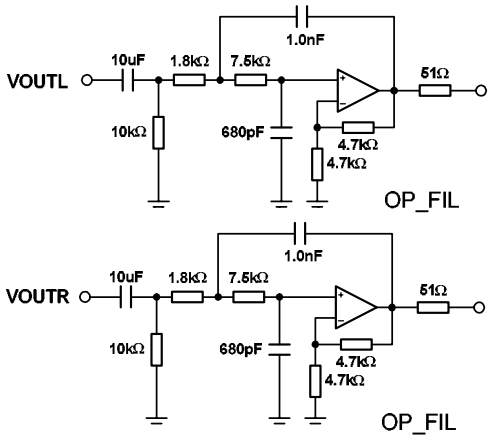
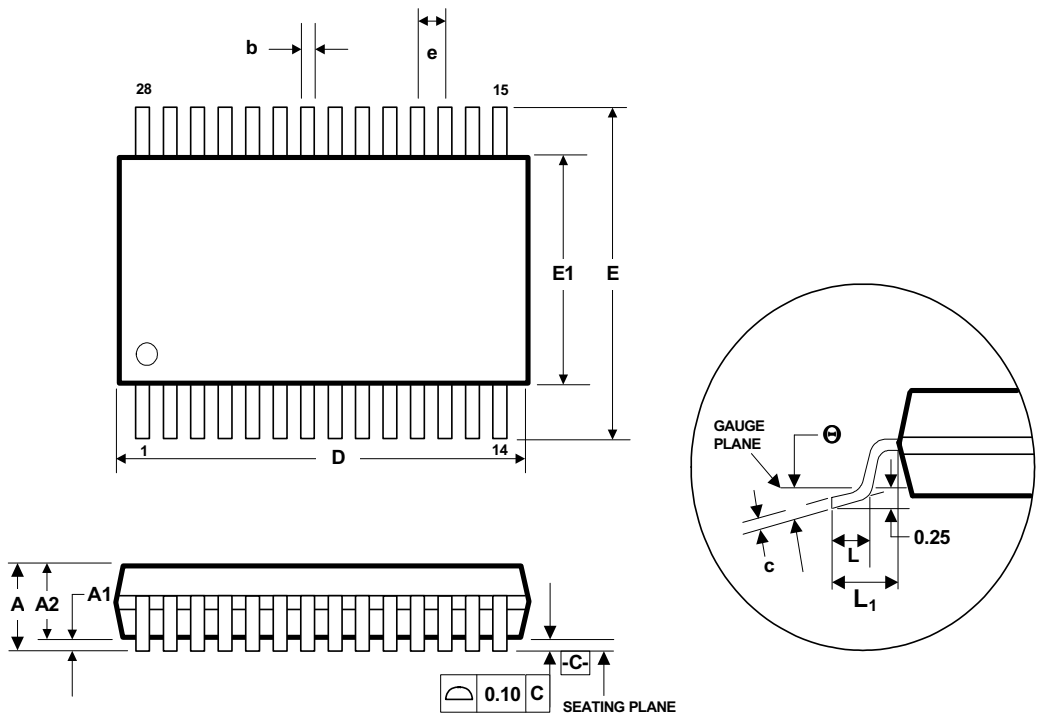


Figure 34 Recommended Post DAC Filter Circuit

PACKAGE DIMENSIONS

DS: 28 PIN SSOP (10.2 x 5.3 x 1.75 mm) **DM007.E**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	2.0
A_1	0.05	-----	0.25
A_2	1.65	1.75	1.85
b	0.22	0.30	0.38
c	0.09	-----	0.25
D	9.90	10.20	10.50
e		0.65 BSC	
E	7.40	7.80	8.20
E_1	5.00	5.30	5.60
L	0.55	0.75	0.95
L_1		1.25 REF	
θ	0^o	4^o	8^o
REF:	JEDEC.95, MO-150		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
D. MEETS JEDEC.95 MO-150, VARIATION = AH. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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