1.5-A 42-V STEP-DOWN SWIFT™ DC/DC CONVERTER WITH Eco-mode™ CONTROL

Check for Samples: TPS54140-Q1

FEATURES

- **Qualified for Automotive Applications**
- **3.5-V to 42-V Input Voltage Range**
- **200-mΩ High-Side MOSFET**
- **High Efficiency at Light Loads With Pulse-Skipping Eco-mode™ Control Scheme**
- **116-μA Operating Quiescent Current**
- **1.3-μA Shutdown Current**
- **100-kHz to 2.5-MHz Switching Frequency**
- **Synchronizes to External Clock**
- **Adjustable Slow Start/Sequencing**
- **Undervoltage and Overvoltage Power-good Output**
- **Adjustable Undervoltage Lockout Voltage and Hysteresis**
- **0.8-V Internal Voltage Reference**
- **Supported by SwitcherPro™ Software Tool (http://focus.ti.com/docs/toolsw/folders/print/switcherpro.html)**
- **For SWIFT™ Documentation, See the TI Website at http://www.ti.com/swift**

APPLICATIONS

- **12-V and 24-V Industrial and Commercial Low Power Systems**
- **Aftermarket Automotive Accessories: Video, GPS, Entertainment**

DESCRIPTION

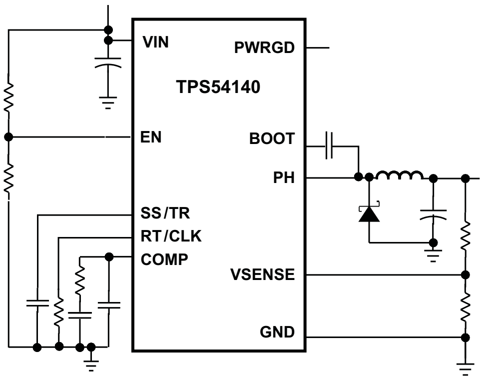
The TPS54140-Q1 device is a 42-V 1.5-A step-down regulator with an integrated high-side MOSFET. Current-mode control provides simple external compensation and flexible component selection. A low-ripple pulse-skip mode reduces the no load, input supply current to 116 μA. Using the enable pin, shutdown supply current is reduced to 1.3 μA.

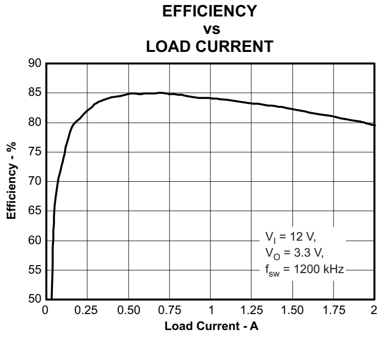
Undervoltage lockout is internally set at 2.5 V, but can be increased using the enable pin. The output voltage startup ramp is controlled by the slow start pin that can also be configured for sequencing or tracking. An open-drain power good signal indicates the output is within 92% to 109% of its nominal voltage.

A wide switching frequency range allows efficiency and external component size to be optimized. Frequency fold back and thermal shutdown protects the part during an overload condition.

The TPS54140-Q1 is available in a 10-pin thermally enhanced MSOP PowerPAD™ package (DGQ) and a 10-pin SON package (DRC).

SIMPLIFIED SCHEMATIC





Eco-mode, SwitcherPro, SWIFT, PowerPAD are trademarks of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)(2)

T_J	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 150°C	MSOP – DGQ	Reel of 2500	TPS54140QDGQRQ1	5414Q
	SON – DRC	Reel of 3000	TPS54140QDRCRQ1	5414Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

over operating temperature range (unless otherwise noted)

V_{IN}	Input voltage	VIN		–0.3 V to 47 V
		EN(2)		–0.3 V to 5 V
		BOOT		55 V
		VSENSE		–0.3 V to 3 V
		COMP		–0.3 V to 3 V
		PWRGD		–0.3 V to 6 V
		SS/TR		–0.3 V to 3 V
		RT/CLK		–0.3 V to 3.6 V
V_{OUT}	Output voltage	PH to BOOT		8 V
		PH		–0.6 V to 47 V
			200 ns	–1 V to 47 V
			30 ns	–2 V to 47 V
			Maximum dc voltage, T_J = -40°C	-0.85 V
V_{DIFF}	Differential voltage	PAD to GND		±200 mV
I_{SOURCE}	Source current	EN		100 μA
		BOOT		100 mA
		VSENSE		10 μA
		PH		Current Limit
		RT/CLK		100 μA
I_{SINK}	Sink current	VIN		Current Limit
		COMP		100 μA
		PWRGD		10 mA
		SS/TR		200 μA
ESD	Electrostatic discharge protection	Human-Body Model (HBM) QSS 009-105 (JESD22-A114A)		500 V
		Machine Model (MM) QSS 009-105 (JESD22-A115A)		50 V
		Charged-Device Model (CDM) QSS 009-147 (JESD22-C101B.01)		1000 V
T_J	Operating junction temperature range			–40°C to 150°C
T_{STG}	Storage temperature range			–65°C to 150°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure beyond absolute maximum rated conditions for extended periods may affect device reliability.

(2) See Enable and Adjusting Undervoltage Lockout for details.

THERMAL INFORMATION

THERMAL METRIC[1][2]		TPS54140-Q1		UNITS
		DGQ	DRC	
		10 PINS	10 PINS	
θ_{JA}	Junction-to-ambient thermal resistance (standard board)	62.5	56.5	°C/W
θ_{JA}	Junction-to-ambient thermal resistance (custom board)[3]	57	61.5	
θ_{JCtop}	Junction-to-case (top) thermal resistance	83	52.1	
θ_{JB}	Junction-to-board thermal resistance	28	20.6	
ψ_{JT}	Junction-to-top characterization parameter	1.7	0.9	
ψ_{JB}	Junction-to-board characterization parameter	20.1	20.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	21	5.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 150°C. This is the point where distortion starts to substantially increase. See power dissipation estimate in application section of this data sheet for more information.
(3) Test boards conditions:
(a) 3 inches x 3 inches, 2 layers, thickness: 0.062 inch
(b) 2 oz. copper traces located on the top of the PCB
(c) 2 oz. copper ground plane, bottom layer
(d) 6 thermal vias (13mil) located under the device package

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 150°C, VIN = 3.5 V to 42 V (unless otherwise noted)

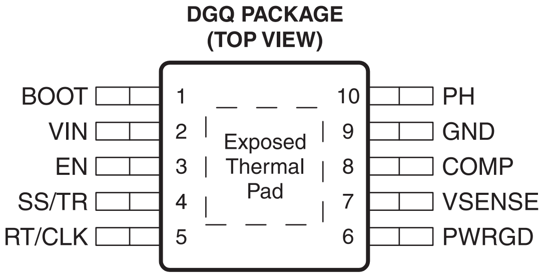
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Operating input voltage		3.5		42	V
Internal undervoltage lockout threshold	No voltage hysteresis, rising and falling		2.5		V
Shutdown supply current	EN = 0 V, 25°C, 3.5 V ≤ VIN ≤ 42 V		1.3	4	µA
	EN = 0 V, 125°C, 3.5 V ≤ VIN ≤ 42 V		1.9	6.5	
Operating : nonswitching supply current	VSENSE = 0.83 V, VIN = 12 V, 25°C		116	136	
ENABLE AND UVLO (EN PIN)					
Enable threshold voltage	No voltage hysteresis, rising and falling, 25°C	0.9	1.25	1.55	V
Input current	Enable threshold +50 mV		–3.8		µA
	Enable threshold –50 mV		–0.9		
Hysteresis current			–2.9		µA
VOLTAGE REFERENCE					
Voltage reference	T_J = 25°C	0.792	0.8	0.808	V
		0.784	0.8	0.816	
HIGH-SIDE MOSFET					
On-resistance	VIN = 3.5 V, BOOT-PH = 3 V		300		mΩ
	VIN = 12 V, BOOT-PH = 6 V		200	410	
ERROR AMPLIFIER					
Input current			50		nA
Error amplifier transconductance (g_m)	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V		97		µMhos
Error amplifier transconductance (g_m) during slow start	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V, V_{VSENSE} = 0.4 V		26		µMhos
Error amplifier dc gain	V_{VSENSE} = 0.8 V		10 000		V/V
Error amplifier bandwidth			2700		kHz
Error amplifier source/sink	$V_{(COMP)}$ = 1 V, 100 mV overdrive		±7		µA
COMP to switch current transconductance			6		A/V

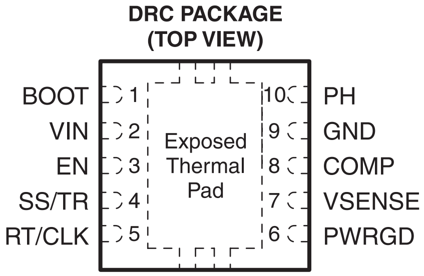
ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 150°C, VIN = 3.5 V to 42 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
	Current limit threshold	VIN = 12 V, T_J = 25°C	1.8	2.7		A
THERMAL SHUTDOWN						
	Thermal shutdown			182		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)						
	Switching frequency range using RT mode	VIN = 12 V	100		2500	kHz
f_{SW}	Switching frequency	VIN = 12 V, R_T = 200 kΩ	450	581	720	kHz
	Switching frequency range using CLK mode	VIN = 12 V	300		2200	kHz
	Minimum CLK pulse width			40		ns
	RT/CLK high threshold	VIN = 12 V		1.9	2.2	V
	RT/CLK low threshold	VIN = 12 V	0.45	0.7		V
	RT/CLK falling edge to PH rising edge delay	Measured at 500 kHz with RT resistor in series		60		ns
	PLL lock in time	Measured at 500 kHz		100		μs
SLOW START AND TRACKING (SS/TR)						
	Charge current	$V_{SS/TR}$ = 0.4 V		2		μA
	SS/TR-to-VSENSE matching	$V_{SS/TR}$ = 0.4 V		45		mV
	SS/TR-to-reference crossover	98% nominal		1		V
	SS/TR discharge current (overload)	VSENSE = 0 V, V(SS/TR) = 0.4 V		112		μA
	SS/TR discharge voltage	VSENSE = 0 V		54		mV
POWER-GOOD (PWRGD PIN)						
V_{VSENSE}	VSENSE threshold	VSENSE falling (Fault)		92		%
		VSENSE rising (Good)		94		
		VSENSE rising (Fault)		109		
		VSENSE falling (Good)		107		
	Hysteresis	VSENSE falling		2		
	Output high leakage	VSENSE = VREF, V(PWRGD) = 5.5 V, 25°C		10		nA
	On resistance	I(PWRGD) = 3 mA, VSENSE < 0.79 V		50		Ω
	Minimum VIN for defined output	V(PWRGD) < 0.5 V, II(PWRGD) = 100 μA		0.95	1.5	V

DEVICE INFORMATION

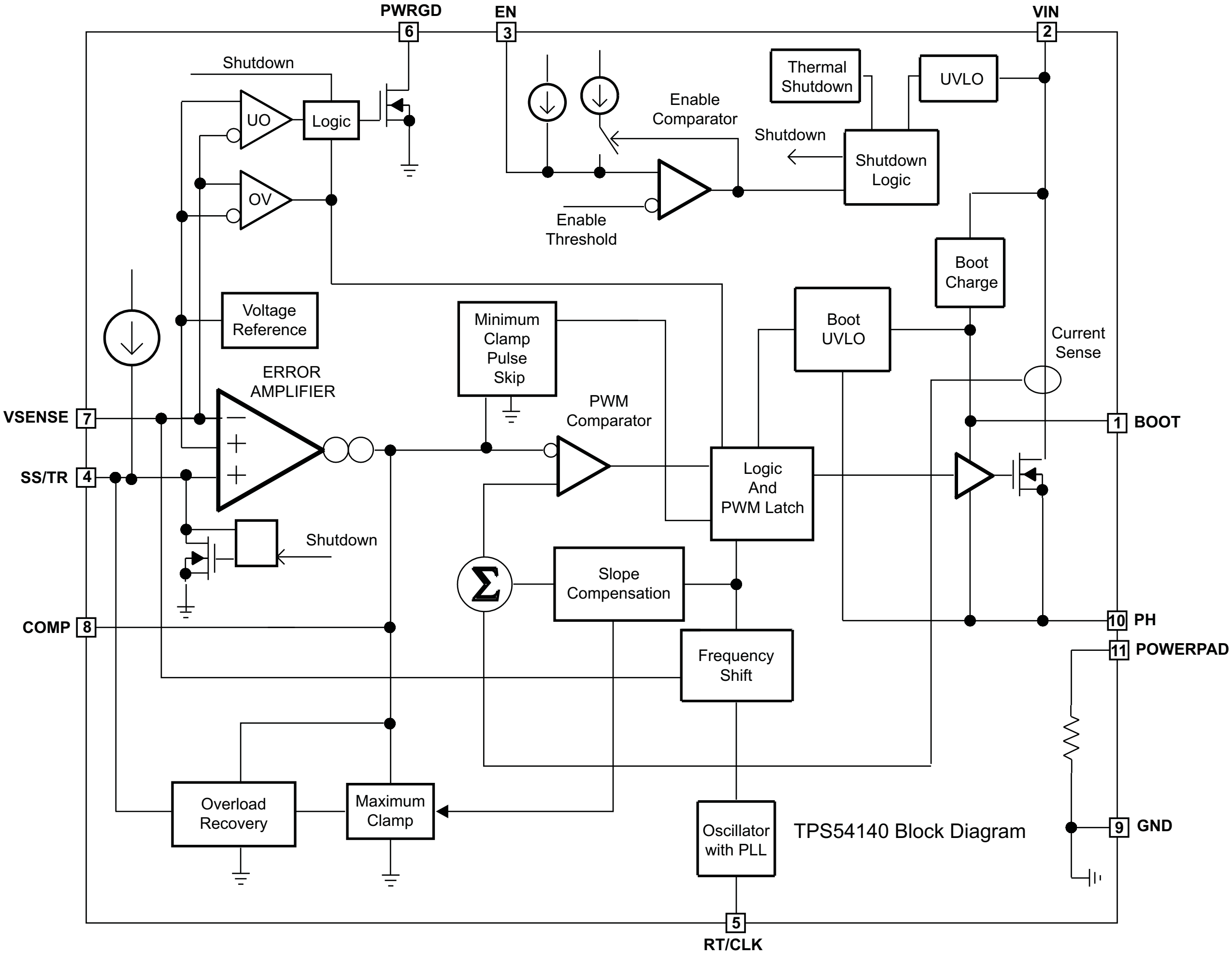




PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the output device, the output is forced to switch off until the capacitor is refreshed.
COMP	8	O	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
EN	3	I	Enable pin, internal pullup current source. Pull below 1.2 V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors.
GND	9	–	Ground
PH	10	I	The source of the internal high-side power MOSFET.
PWRGD	6	O	An open drain output, asserts low if output voltage is low due to thermal shutdown, dropout, over-voltage or EN shut down.
RT/CLK	5	I	Resistor Timing and External Clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the mode returns to a resistor set function.
SS/TR	4	I	Slow-start and Tracking. An external capacitor connected to this pin sets the output rise time. Since the voltage on this pin overrides the internal reference, it can be used for tracking and sequencing.
VIN	2	I	Input supply voltage, 3.5 V to 42 V.
VSENSE	7	I	Inverting node of the transconductance (gm) error amplifier.
Thermal Pad		–	GND pin must be electrically connected to the exposed pad on the printed circuit board for proper operation.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

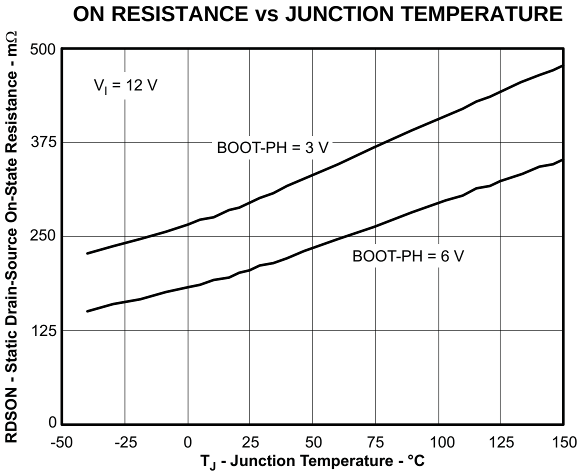

ON RESISTANCE vs JUNCTION TEMPERATURE

Figure 1.

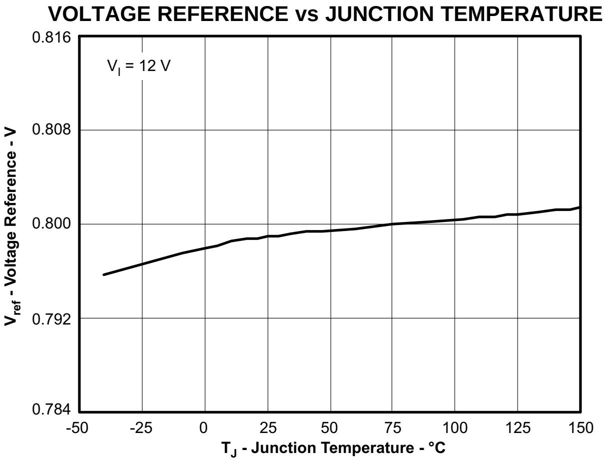

VOLTAGE REFERENCE vs JUNCTION TEMPERATURE

Figure 2.

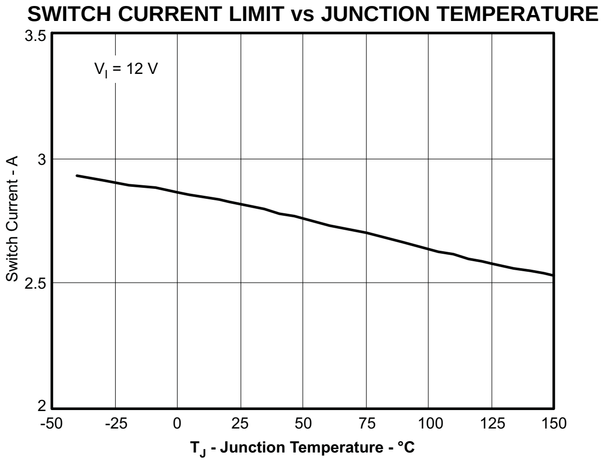

SWITCH CURRENT LIMIT vs JUNCTION TEMPERATURE

Figure 3.

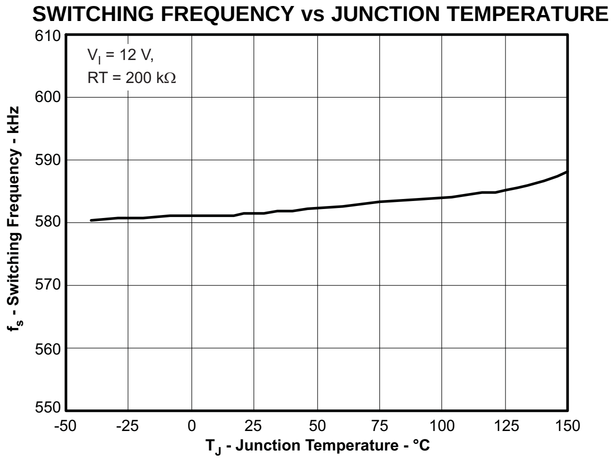

SWITCHING FREQUENCY vs JUNCTION TEMPERATURE

Figure 4.

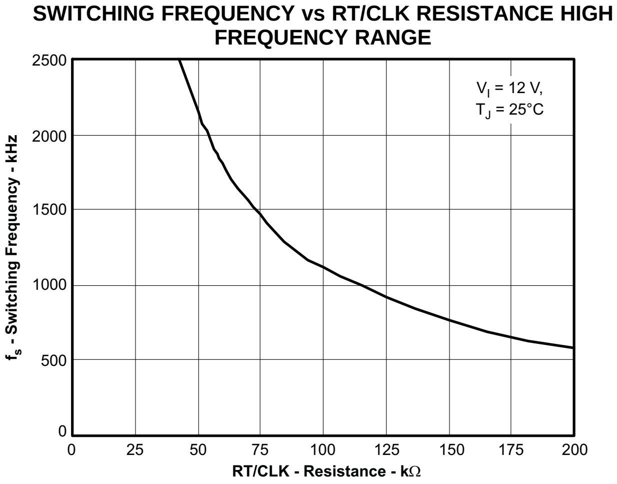

SWITCHING FREQUENCY vs RT/CLK RESISTANCE HIGH FREQUENCY RANGE

Figure 5.

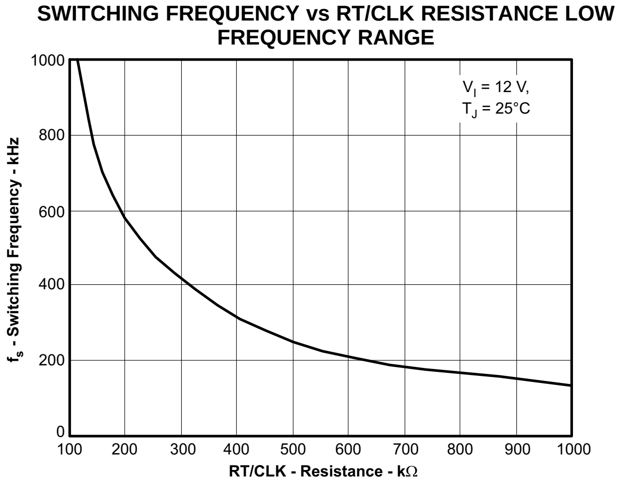

SWITCHING FREQUENCY vs RT/CLK RESISTANCE LOW FREQUENCY RANGE

Figure 6.

TYPICAL CHARACTERISTICS (continued)

EA TRANSCONDUCTANCE DURING SLOW START vs JUNCTION TEMPERATURE

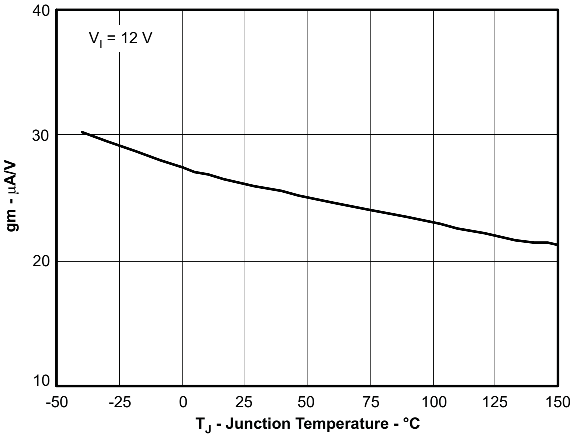


Figure 7.

EA TRANSCONDUCTANCE vs JUNCTION TEMPERATURE

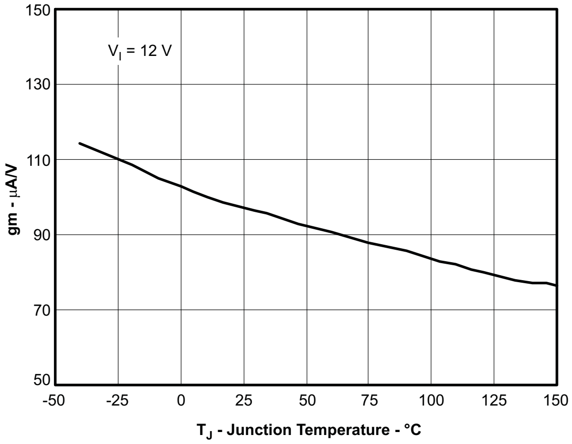


Figure 8.

EN PIN VOLTAGE vs JUNCTION TEMPERATURE

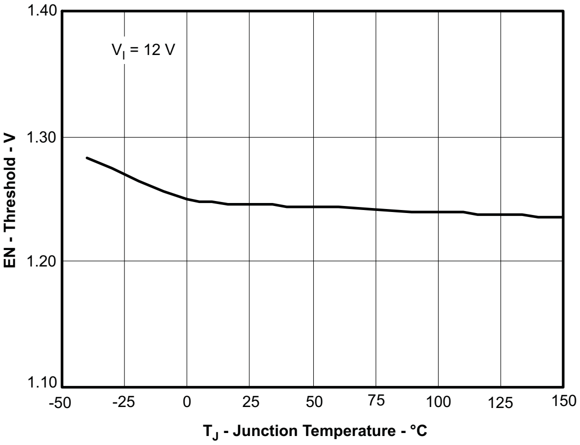


Figure 9.

EN PIN CURRENT vs JUNCTION TEMPERATURE

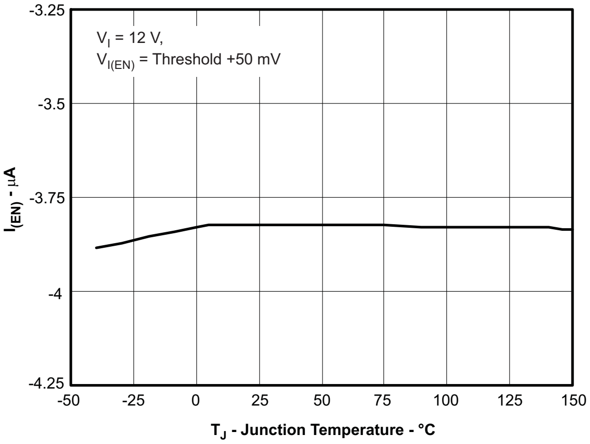


Figure 10.

EN PIN CURRENT vs JUNCTION TEMPERATURE

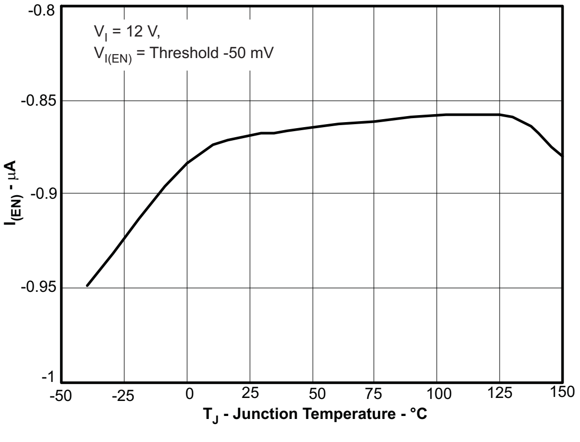


Figure 11.

SS/TR CHARGE CURRENT vs JUNCTION TEMPERATURE

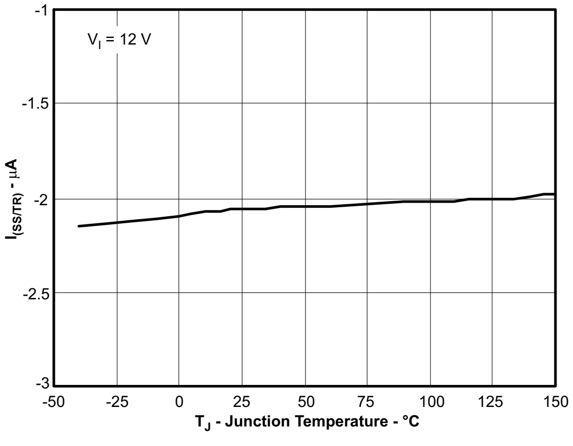


Figure 12.

TYPICAL CHARACTERISTICS (continued)

SS/TR DISCHARGE CURRENT vs JUNCTION TEMPERATURE

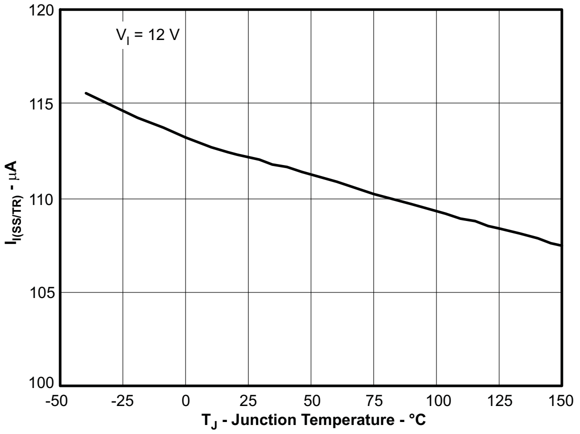


Figure 13.

SWITCHING FREQUENCY vs VSENSE

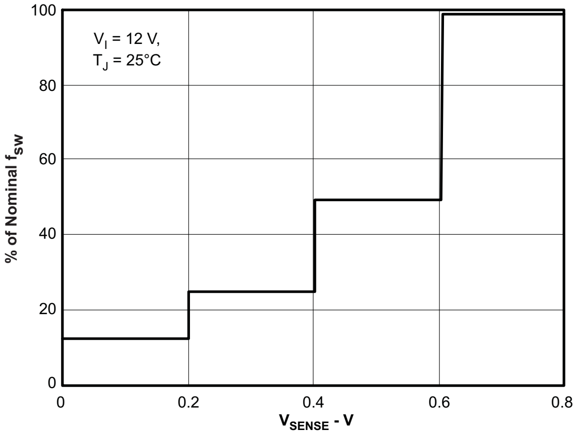


Figure 14.

SHUTDOWN SUPPLY CURRENT vs JUNCTION TEMPERATURE

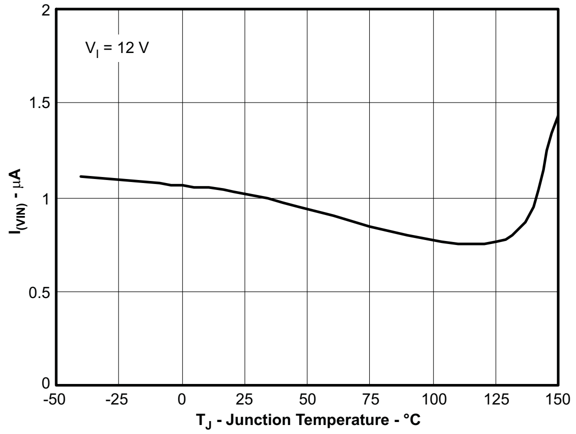


Figure 15.

SHUTDOWN SUPPLY CURRENT vs INPUT VOLTAGE (V_{in})

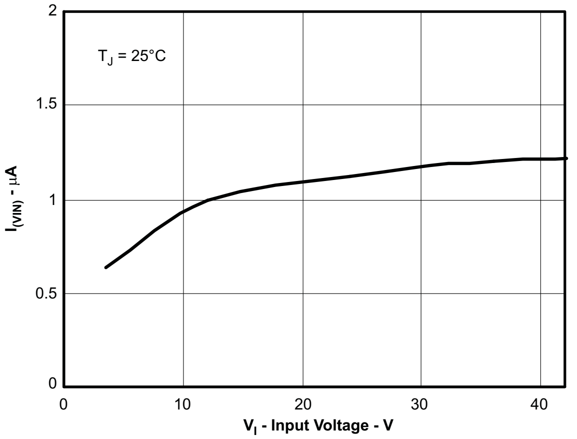


Figure 16.

VIN SUPPLY CURRENT vs JUNCTION TEMPERATURE

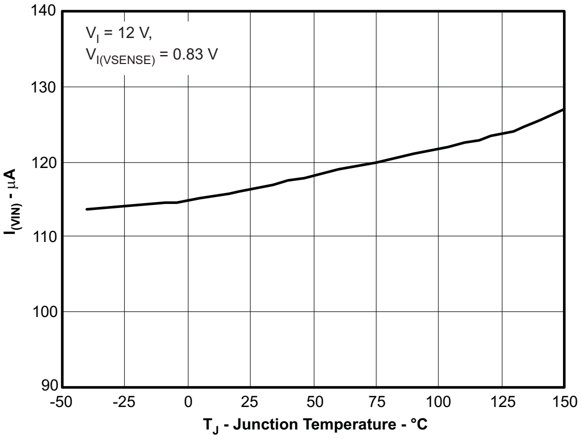


Figure 17.

VIN SUPPLY CURRENT vs INPUT VOLTAGE

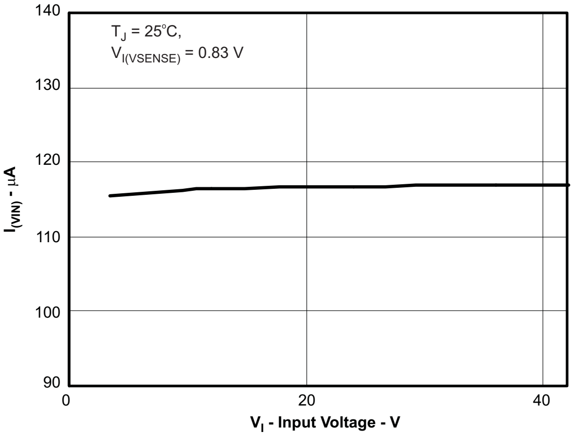


Figure 18.

TYPICAL CHARACTERISTICS (continued)

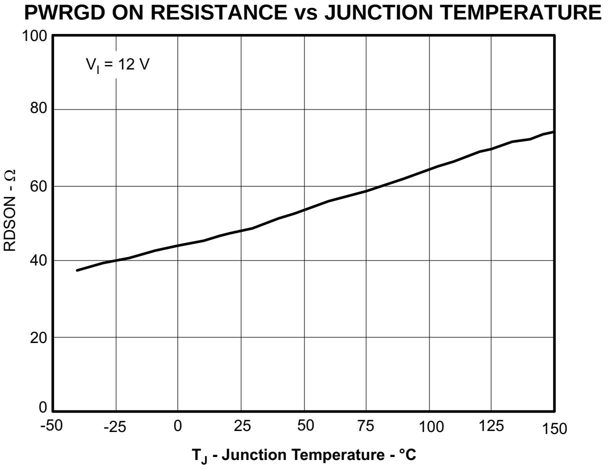


Figure 19.

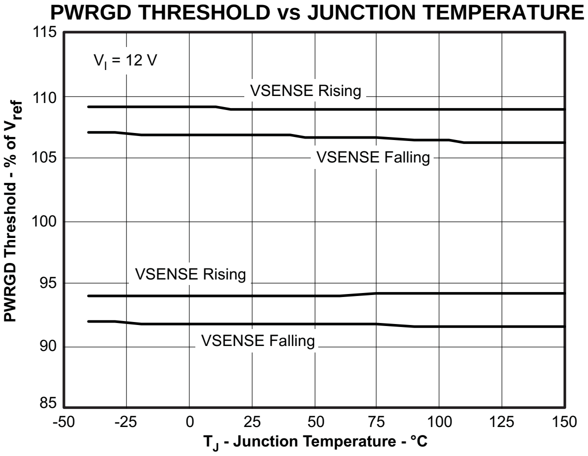


Figure 20.

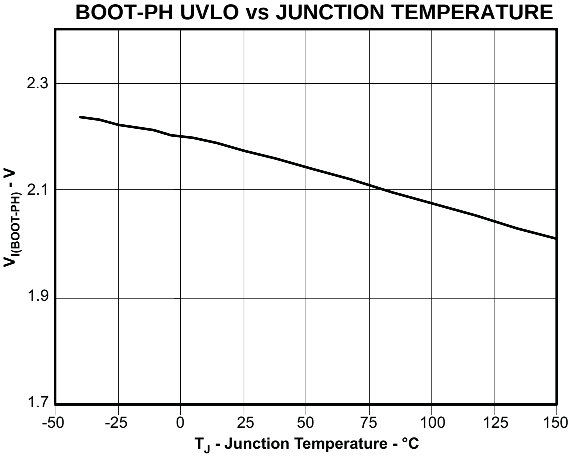


Figure 21.

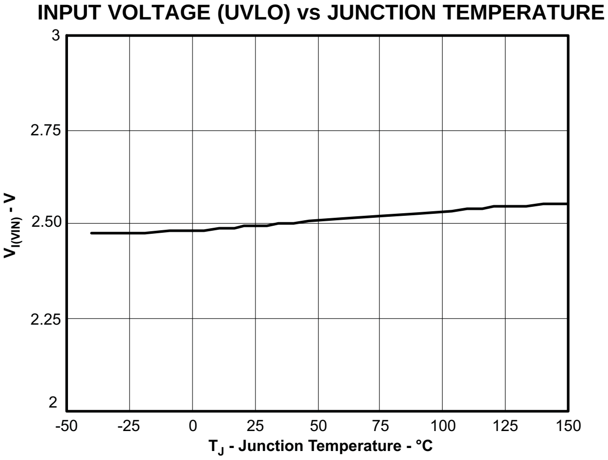


Figure 22.

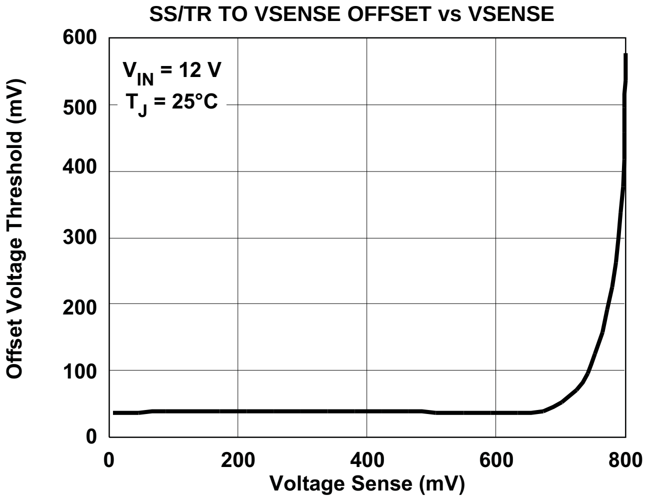


Figure 23.

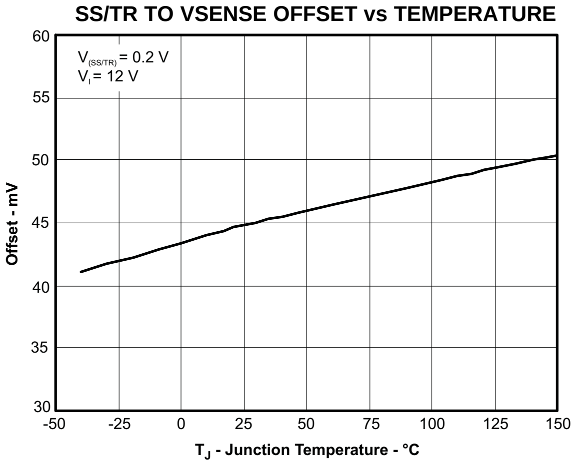


Figure 24.

OVERVIEW

The TPS54140-Q1 device is a 42-V, 1.5-A, step-down (buck) regulator with an integrated high side n-channel MOSFET. To improve performance during line and load transients the device implements a constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation design. The wide switching frequency of 100 kHz to 2500 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT/CLK pin. The device has an internal phase lock loop (PLL) on the RT/CLK pin that is used to synchronize the power switch turn on to a falling edge of an external system clock.

The TPS54140-Q1 has a default start up voltage of approximately 2.5 V. The EN pin has an internal pull-up current source that can be used to adjust the input voltage undervoltage lockout (UVLO) threshold with two external resistors. In addition, the pull up current provides a default condition. When the EN pin is floating the device will operate. The operating current is 116 μA when not switching and under no load. When the device is disabled, the supply current is 1.3 μA.

The integrated 200 mΩ high side MOSFET allows for high efficiency power supply designs capable of delivering 1.5 amperes of continuous current to a load. The TPS54140-Q1 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high side MOSFET is supplied by a capacitor on the BOOT to PH pin. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high side MOSFET off when the boot voltage falls below a preset threshold. The TPS54140-Q1 can operate at high duty cycles because of the boot UVLO. The output voltage can be stepped down to as low as the 0.8 V reference.

The TPS54140-Q1 has a power-good comparator (PWRGD) which asserts when the regulated output voltage is less than 92% or greater than 109% of the nominal output voltage. The PWRGD pin is an open drain output which de-asserts when the VSENSE pin voltage is between 94% and 107% of the nominal output voltage allowing the pin to transition high when a pull-up resistor is used.

The TPS54140-Q1 minimizes excessive output overvoltage (OV) transients by taking advantage of the OV power-good comparator. When the OV comparator is activated, the high side MOSFET is turned off and masked from turning on until the output voltage is lower than 107%.

The SS/TR (slow start/tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor should be coupled to the pin to adjust the slow start time. A resistor divider can be coupled to the pin for critical power supply sequencing requirements. The SS/TR pin is discharged before the output powers up. This discharging ensures a repeatable restart after an over-temperature fault, UVLO fault or a disabled condition.

The TPS54140-Q1, also, discharges the slow start capacitor during overload conditions with an overload recovery circuit. The overload recovery circuit will slow start the output from the fault voltage to the nominal regulation voltage once a fault condition is removed. A frequency foldback circuit reduces the switching frequency during startup and overcurrent fault conditions to help control the inductor current.

DETAILED DESCRIPTION

Fixed Frequency PWM Control

The TPS54140-Q1 uses an adjustable fixed frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output is compared to the high side power switch current. When the power switch current reaches the COMP voltage level the power switch is turned off. The COMP pin voltage will increase and decrease as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level. The Eco-Mode™ is implemented with a minimum clamp on the COMP pin.

Slope Compensation Output Current

The TPS54140-Q1 adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations. The available peak inductor current remains constant over the full duty cycle range.

Pulse Skip Eco-Mode

The TPS54140-Q1 enters the pulse skip mode when the voltage on the COMP pin is the minimum clamp value. The TPS54140-Q1 operates in a pulse skip mode at light load currents to improve efficiency. The peak switch current during the pulse skip mode will be the greater value of 50 mA or the peak inductor current that is a function of the minimum on time, input voltage, output voltage and inductance value. When the load current is low and the output voltage is within regulation the device will enter a sleep mode and draw only 116 µA input quiescent current. While the device is in sleep mode the output power is delivered by the output capacitor. As the load current decreases, the time the output capacitor supplies the load current increases and the switching frequency decreases reducing gate drive and switching losses. As the output voltage drops, the TPS54140-Q1 wakes up from the sleep mode and the power switch turns on to recharge the output capacitor, see Figure 25. The internal PLL remains operating when in sleep mode. When operating at light load currents in the pulse skip mode the switching transitions occur synchronously with the external clock signal.

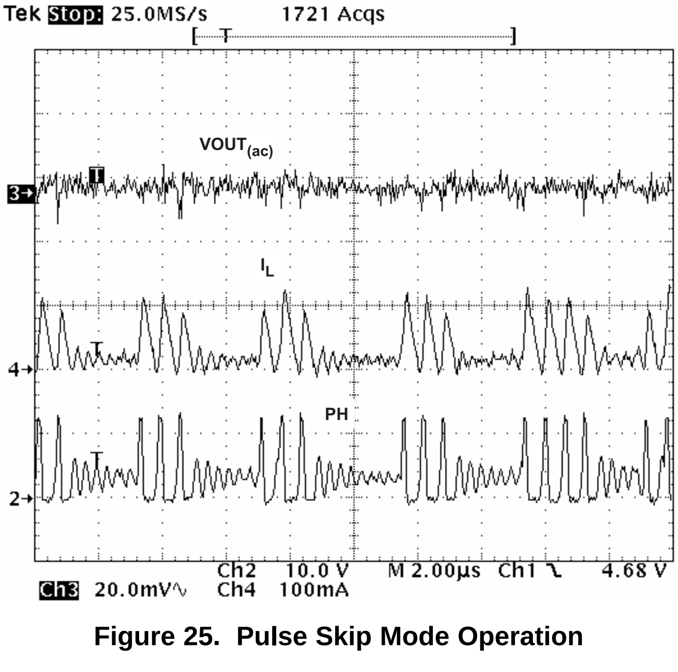


Figure 25. Pulse Skip Mode Operation

DETAILED DESCRIPTION (continued)

Bootstrap Voltage (BOOT)

The TPS54140-Q1 has an integrated boot regulator and requires a small ceramic capacitor between the BOOT and PH pin to provide the gate drive voltage for the high side MOSFET. The value of the ceramic capacitor should be 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage. To improve drop out, the TPS54140-Q1 is designed to operate at 100% duty cycle as long as the BOOT to PH pin voltage is greater than 2.1 V. When the voltage from BOOT to PH drops below 2.1 V, the high side MOSFET is turned off using an UVLO circuit allowing for the low side diode to conduct which allows refreshing of the BOOT capacitor. Since the supply current sourced from the BOOT capacitor is low, the high side MOSFET can remain on for more switching cycles than it refreshes, thus, the effective duty cycle limitation that is attributed to the boot regulator system is high.

Low Dropout Operation

The duty cycle during dropout of the regulator will be mainly determined by the voltage drops across the power MOSFET, inductor, low side diode and printed circuit board resistance. During operating conditions in which the input voltage drops, the high side MOSFET can remain on for 100% of the duty cycle to maintain output regulation or until the BOOT to PH voltage falls below 2.1 V.

Once the high side is off, the low side diode will conduct and the BOOT capacitor will be recharged. During this boot capacitor recharge time, the inductor current will ramp down until the high side MOSFET turns on. The recharge time is longer than the typical high side off time of previous switching cycles, and thus, the inductor current ripple is larger resulting in more ripple voltage on the output. The recharge time is a function of the input voltage, boot capacitor value, and the impedance of the internal boot recharge diode.

Attention needs to be taken in maximum duty cycle applications which experience extended time periods without a load current. When the voltage across the BOOT capacitors falls below the 2.1 V threshold in applications that have a difference in the input voltage and output voltage that is less than 3 V, the high side MOSFET will be turned off but there is not enough current in the inductor to pull the PH pin down to recharge the boot capacitor. The regulator will not switch because the boot capacitor is less than 2.1 V and the output capacitor will decay until the difference in the input voltage and output voltage is 2.1 V. At this time the boot undervoltage lockout is exceeded and the device will switch until the desired output voltage is reached.

The start and stop voltages are shown in Figure 26 and Figure 27 for 3.3-V and 5-V applications. The voltages are plotted versus the load current. The start voltage is defined as the input voltage needed to regulate within 1%. The stop voltage is defined as the input voltage at which the output drops by 5% or stops switching.

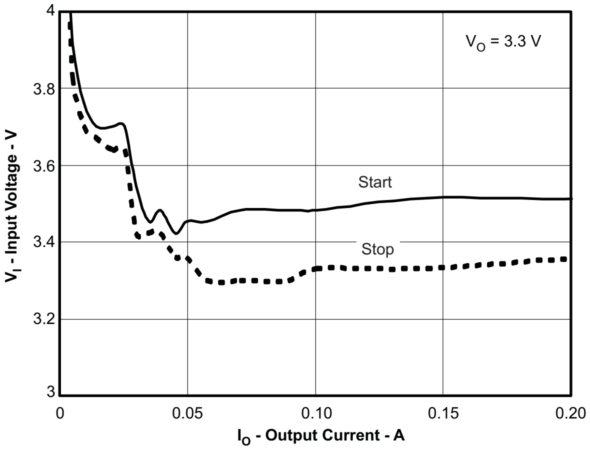


Figure 26. 3.3-V Start/Stop Voltage

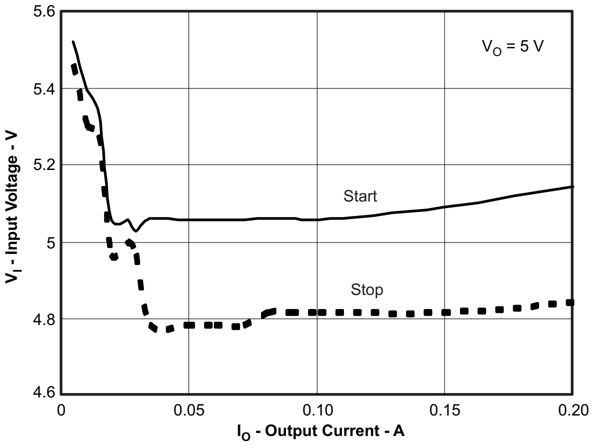


Figure 27. 5-V Start/Stop Voltage

DETAILED DESCRIPTION (continued)

Error Amplifier

The TPS54140-Q1 has a transconductance amplifier for the error amplifier. The error amplifier compares the VSENSE voltage to the lower of the SS/TR pin voltage or the internal 0.8-V voltage reference. The transconductance (gm) of the error amplifier is 97 μA/V during normal operation. During the slow start operation, the transconductance is a fraction of the normal operating gm. When the voltage of the VSENSE pin is below 0.8 V and the device is regulating using the SS/TR voltage, the gm is 25 μA/V.

The frequency compensation components (capacitor, series resistor and capacitor) are added from the COMP pin to ground.

Voltage Reference

The voltage reference system produces a precise ±2% voltage reference over temperature by scaling the output of a temperature stable bandgap circuit.

Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the VSENSE pin. It is recommended to use 1% tolerance or better divider resistors. Start with a 10 kΩ for the R2 resistor and use the Equation 1 to calculate R1. To improve efficiency at very light loads consider using larger value resistors. If the values are too high the regulator will be more susceptible to noise and voltage errors from the VSENSE input current will be noticeable

$$R1 = R2 \times \left(\frac{Vout - 0.8V}{0.8\ V} \right) \tag{1}$$

Enable and Adjusting Undervoltage Lockout

The TPS54140-Q1 is disabled when the VIN pin voltage falls below 2.5 V. If an application requires a higher undervoltage lockout (UVLO), use the EN pin as shown in Figure 28 to adjust the input voltage UVLO by using the two external resistors. Though it is not necessary to use the UVLO adjust resistors, for operation it is highly recommended to provide consistent power up behavior. The EN pin has an internal pull-up current source, I1, of 0.9 μA that provides the default condition of the TPS54140-Q1 operating when the EN pin floats. Once the EN pin voltage exceeds 1.25 V, an additional 2.9 μA of hysteresis, I_{HYS}, is added. This additional current facilitates input voltage hysteresis. Use Equation 2 to set the external hysteresis for the input voltage. Use Equation 3 to set the input start voltage.

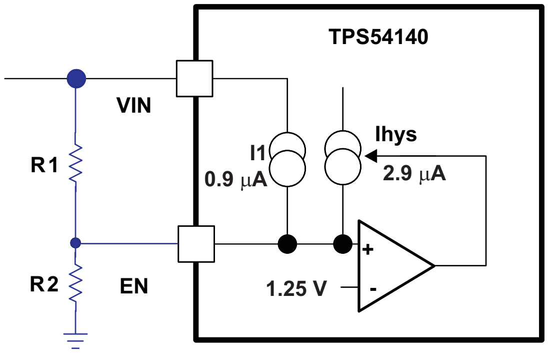


Figure 28. Adjustable Undervoltage Lockout (UVLO)

$$R1 = \frac{V_{START} - V_{STOP}}{I_{HYS}} \tag{2}$$

$$R2 = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R1} + I_1} \tag{3}$$

DETAILED DESCRIPTION (continued)

Another technique to add input voltage hysteresis is shown in Figure 29. This method may be used, if the resistance values are high from the previous method and a wider voltage hysteresis is needed. The resistor R3 sources additional hysteresis current into the EN pin.

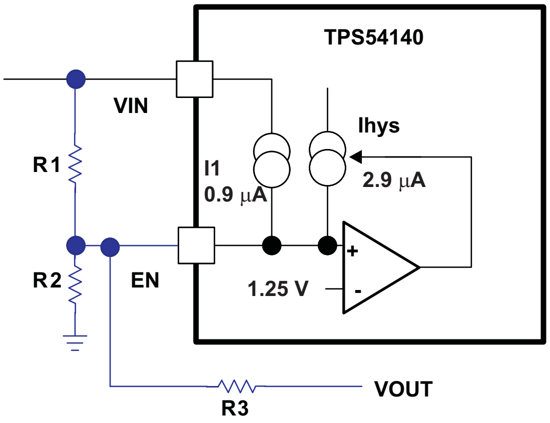


Figure 29. Adding Additional Hysteresis

$$R1 = \frac{V_{START} - V_{STOP}}{I_{HYS} + \frac{V_{OUT}}{R3}} \tag{4}$$

$$R2 = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R1} + I_1 - \frac{V_{ENA}}{R3}} \tag{5}$$

Do not place a low-impedance voltage source with greater than 5 V directly on the EN pin. Do not place a capacitor directly on the EN pin if V_{EN} > 5 V when using a voltage divider to adjust the start and stop voltage. The node voltage, (see Figure 30) must remain equal to or less than 5.8 V. The zener diode can sink up to 100 µA. The EN pin voltage can be greater than 5 V if the V_{IN} voltage source has a high impedance and does not source more than 100 µA into the EN pin.

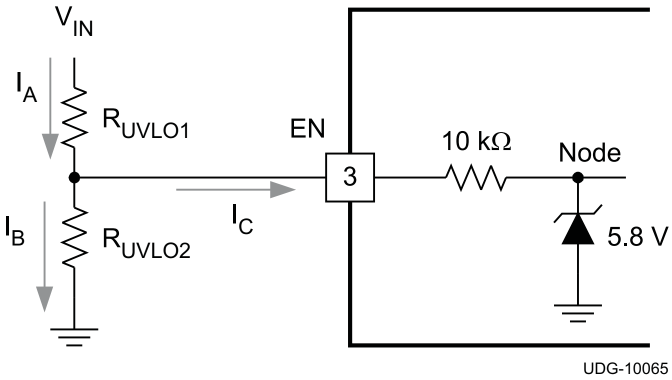


Figure 30. Node Voltage

DETAILED DESCRIPTION (continued)

Slow Start/Tracking Pin (SS/TR)

The TPS54140-Q1 effectively uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the reference voltage of the power-supply and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a slow start time. The TPS54140-Q1 has an internal pull-up current source of 2 μA that charges the external slow start capacitor. The calculations for the slow start time (10% to 90%) are shown in Equation 6. The voltage reference (V_{REF}) is 0.8 V and the slow start current (I_{SS}) is 2 μA. The slow start capacitor should remain lower than 0.47 μF and greater than 0.47 nF.

$$\text{Css(nF)} = \frac{\text{Tss(ms)} \times \text{Iss}(\mu\text{A})}{\text{Vref (V)} \times 0.8} \tag{6}$$

At power up, the TPS54140-Q1 will not start switching until the slow start pin is discharged to less than 40 mV to ensure a proper power up, see Figure 31.

Also, during normal operation, the TPS54140-Q1 will stop switching and the SS/TR must be discharged to 40 mV, when the VIN UVLO is exceeded, EN pin pulled below 1.25 V, or a thermal shutdown event occurs.

The VSENSE voltage will follow the SS/TR pin voltage with a 45-mV offset up to 85% of the internal voltage reference. When the SS/TR voltage is greater than 85% on the internal reference voltage the offset increases as the effective system reference transitions from the SS/TR voltage to the internal voltage reference (see Figure 23). The SS/TR voltage will ramp linearly until clamped at 1.7 V.

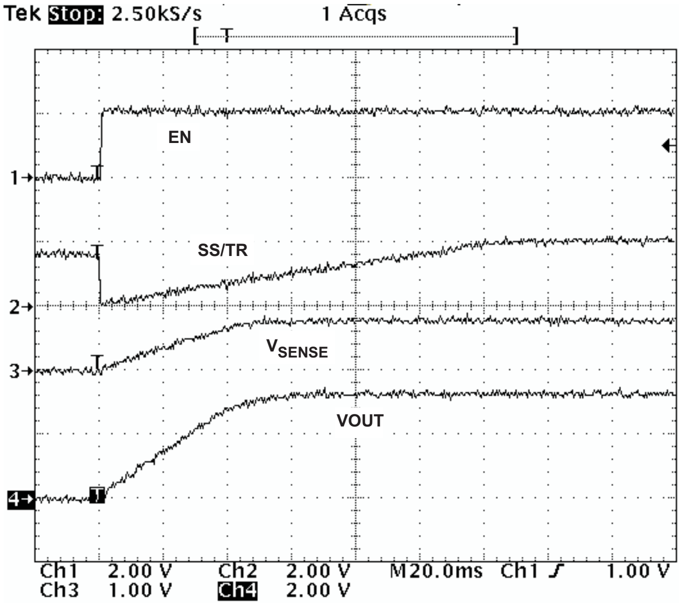


Figure 31. Operation of SS/TR Pin When Starting

Overload Recovery Circuit

The TPS54140-Q1 has an overload recovery (OLR) circuit. The OLR circuit will slow start the output from the overload voltage to the nominal regulation voltage once the fault condition is removed. The OLR circuit will discharge the SS/TR pin to a voltage slightly greater than the VSENSE pin voltage using an internal pull down of 100 μA when the error amplifier is changed to a high voltage from a fault condition. When the fault condition is removed, the output will slow start from the fault voltage to nominal output voltage.

DETAILED DESCRIPTION (continued)

Sequencing

Many of the common power supply sequencing methods can be implemented using the SS/TR, EN and PWRGD pins. The sequential method can be implemented using an open drain output of a power-on reset pin of another device. The sequential method is illustrated in Figure 32 using two TPS54140-Q1 devices. The power good is coupled to the EN pin on the TPS54140-Q1 which will enable the second power supply once the primary supply reaches regulation. If needed, a 1-nF ceramic capacitor on the EN pin of the second power supply will provide a 1-ms start up delay. Figure 33 shows the results of Figure 32.

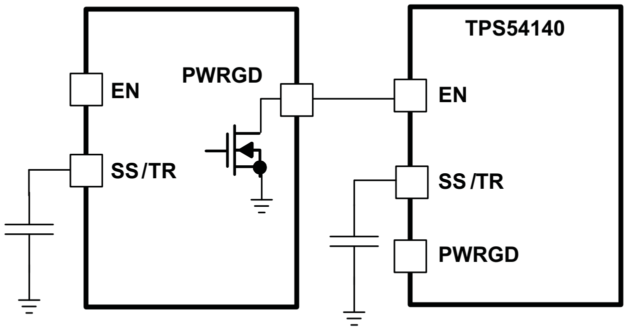


Figure 32. Schematic for Sequential Start-Up Sequence

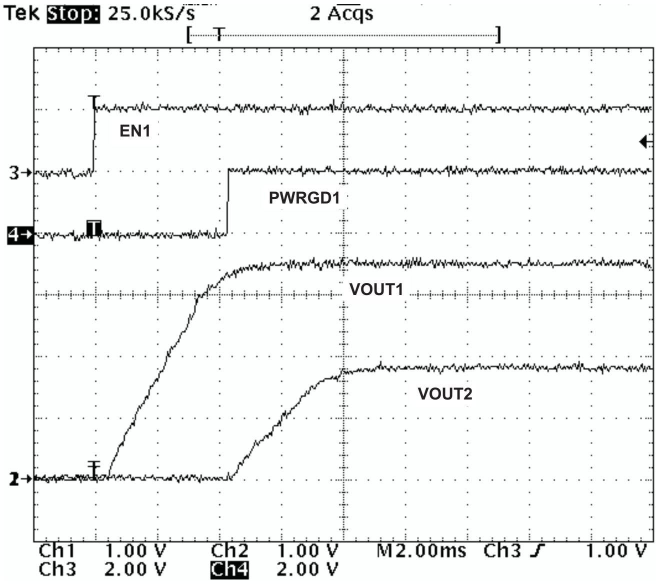


Figure 33. Sequential Startup using EN and PWRGD

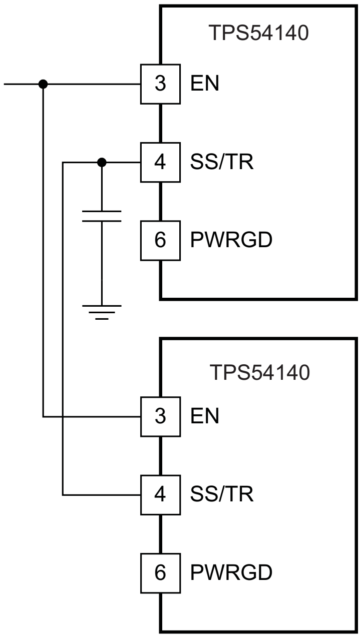


Figure 34. Schematic for Ratiometric Start-Up Using Coupled SS/TR Pins

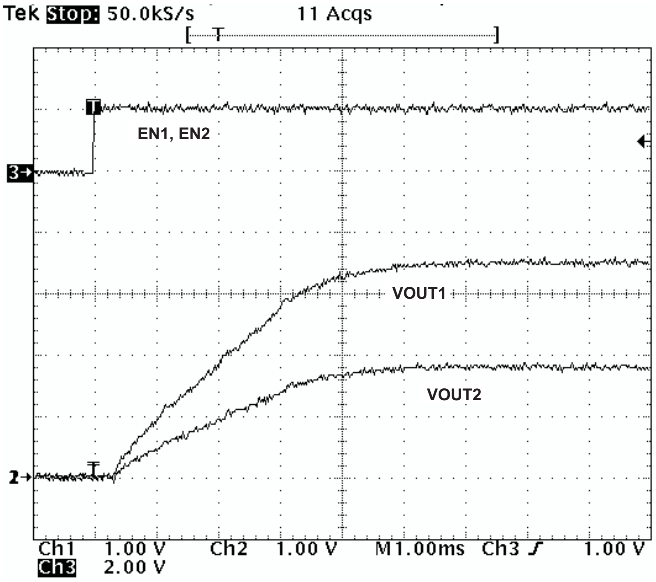


Figure 35. Ratiometric Startup Using Coupled SS/TR Pins

DETAILED DESCRIPTION (continued)

Figure 34 shows a method for ratiometric start up sequence by connecting the SS/TR pins together. The regulator outputs will ramp up and reach regulation at the same time. When calculating the slow start time the pullup current source must be doubled in Equation 6. Figure 35 shows the results of Figure 34.

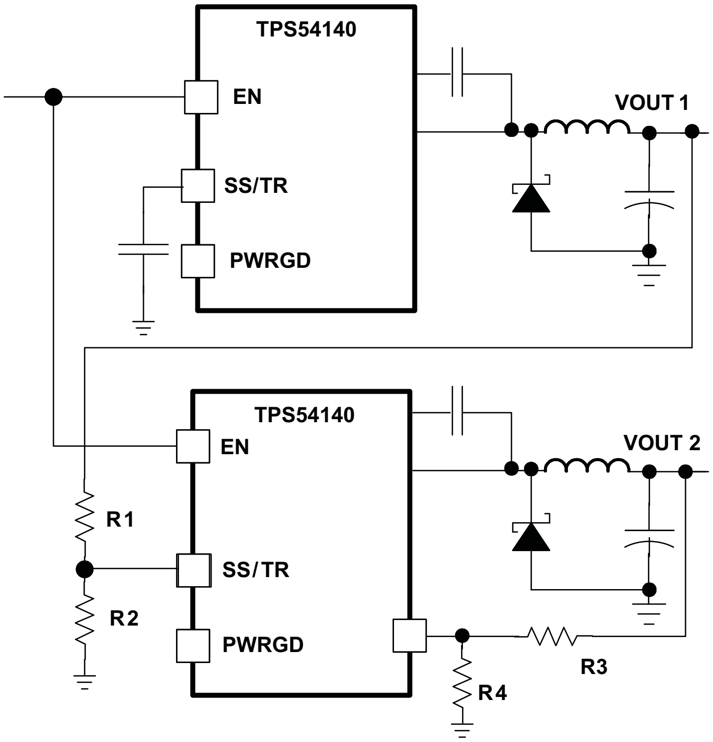


Figure 36. Schematic for Ratiometric and Simultaneous Start-Up Sequence

Ratiometric and simultaneous power supply sequencing can be implemented by connecting the resistor network of R1 and R2 shown in Figure 36 to the output of the power supply that needs to be tracked or another voltage reference source. Using Equation 7 and Equation 8, the tracking resistors can be calculated to initiate the V_{OUT2} slightly before, after or at the same time as V_{OUT1}. Equation 9 is the voltage difference between V_{OUT1} and V_{OUT2} at the 95% of nominal output regulation.

The ΔV variable is zero volts for simultaneous sequencing. To minimize the effect of the inherent SS/TR to VSENSE offset ($V_{SSOFFSET}$) in the slow start circuit and the offset created by the pullup current source (I_{SS}) and tracking resistors, the $V_{SSOFFSET}$ and LSS are included as variables in the equations.

To design a ratio-metric start up in which the V_{OUT2} voltage is slightly greater than the V_{OUT1} voltage when V_{OUT2} reaches regulation, use a negative number in Equation 7 through Equation 9 for ΔV. Equation 9 will result in a positive number for applications which the V_{OUT2} is slightly lower than V_{OUT1} when V_{OUT2} regulation is achieved.

Since the SS/TR pin must be pulled below 40 mV before starting after an EN, UVLO or thermal shutdown fault, careful selection of the tracking resistors is needed to ensure the device will restart after a fault. Make sure the calculated R1 value from Equation 7 is greater than the value calculated in Equation 10 to ensure the device can recover from a fault.

As the SS/TR voltage becomes more than 85% of the nominal reference voltage the $V_{SSOFFSET}$ becomes larger as the slow start circuits gradually handoff the regulation reference to the internal voltage reference. The SS/TR pin voltage needs to be greater than 1.3 V for a complete handoff to the internal voltage reference as shown in Figure 23.

$$R1 = \frac{\text{Vout2} + \text{deltaV}}{\text{VREF}} \times \frac{\text{Vssoffset}}{\text{Iss}} \tag{7}$$

$$R2 = \frac{\text{VREF} \times \text{R1}}{\text{Vout2} + \text{deltaV} - \text{VREF}} \tag{8}$$

DETAILED DESCRIPTION (continued)

$$\text{deltaV} = \text{Vout1} - \text{Vout2} \quad (9)$$

$$\text{R1} > 2800 \times \text{Vout1} - 180 \times \text{deltaV} \quad (10)$$

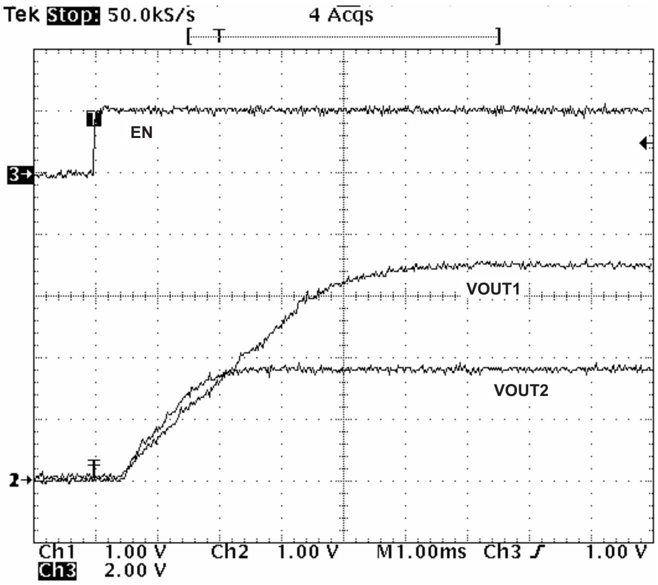


Figure 37. Ratiometric Startup with V_{OUT2} Leading V_{OUT1}

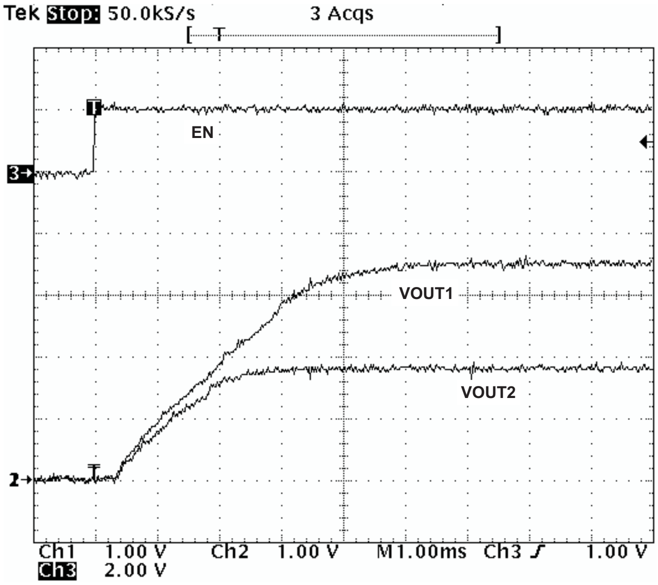


Figure 38. Ratiometric Startup with V_{OUT1} Leading V_{OUT2}

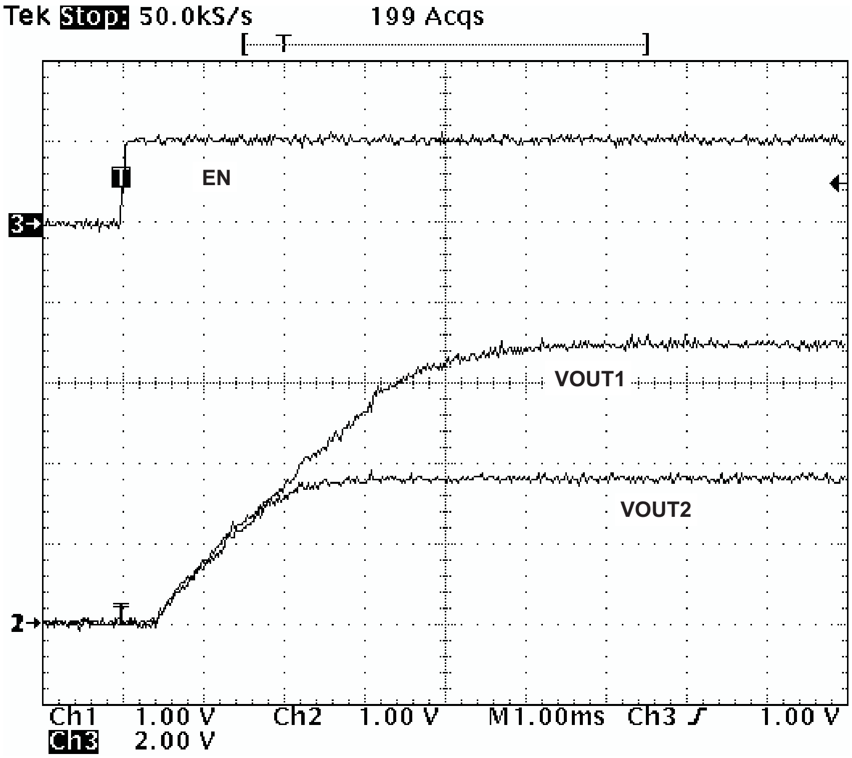


Figure 39. Simultaneous Startup With Tracking Resistor

DETAILED DESCRIPTION (continued)

Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS54140-Q1 is adjustable over a wide range from approximately 100 kHz to 2500 kHz by placing a resistor on the RT/CLK pin. The RT/CLK pin voltage is typically 0.5 V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 11 or the curves in Figure 40 or Figure 41. To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the supply efficiency, maximum input voltage and minimum controllable on time should be considered.

The minimum controllable on time is typically 130 ns and limits the maximum operating input voltage.

The maximum switching frequency is also limited by the frequency shift circuit. More discussion on the details of the maximum switching frequency is located below.

$$\text{RT (kOhm)} = \frac{206033}{f\text{sw (kHz)}^{1.0888}} \tag{11}$$

SWITCHING FREQUENCY vs RT/CLK RESISTANCE HIGH FREQUENCY RANGE

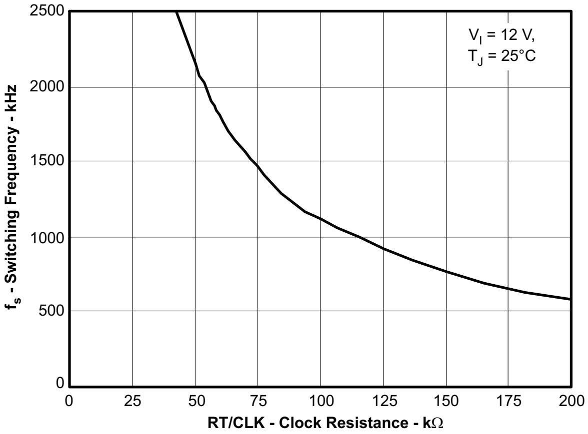


Figure 40. High Range RT

SWITCHING FREQUENCY vs RT/CLK RESISTANCE LOW FREQUENCY RANGE

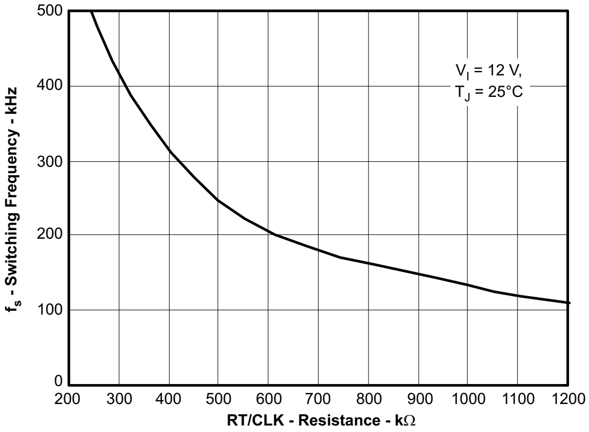


Figure 41. Low Range RT

Overcurrent Protection and Frequency Shift

The TPS54140-Q1 implements current mode control which uses the COMP pin voltage to turn off the high side MOSFET on a cycle by cycle basis. During each cycle the switch current and COMP pin voltage are compared, when the peak switch current intersects the COMP voltage, the high side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier will respond by driving the COMP pin high, increasing the switch current. The error amplifier output is clamped internally, which functions as a switch current limit.

To increase the maximum operating switching frequency at high input voltages the TPS54140-Q1 implements a frequency shift. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0 to 0.8 volts on VSENSE pin.

The device implements a digital frequency shift to enable synchronizing to an external clock during normal startup and fault conditions. Since the device can only divide the switching frequency by 8, there is a maximum input voltage limit in which the device operates and still have frequency shift protection.

During short-circuit events (particularly with high input voltage applications), the control loop has a finite minimum controllable on time and the output has a very low voltage. During the switch on time, the inductor current ramps to the peak current limit because of the high input voltage and minimum on time. During the switch off time, the inductor would normally not have enough off time and output voltage for the inductor to ramp down by the ramp up amount. The frequency shift effectively increases the off time allowing the current to ramp down.

DETAILED DESCRIPTION (continued)

Selecting the Switching Frequency

The switching frequency that is selected should be the lower value of the two equations, Equation 12 and Equation 13. Equation 12 is the maximum switching frequency limitation set by the minimum controllable on time. Setting the switching frequency above this value will cause the regulator to skip switching pulses.

Equation 13 is the maximum switching frequency limit set by the frequency shift protection. To have adequate output short circuit protection at high input voltages, the switching frequency should be set to be less than the $f_{SW(maxshift)}$ frequency. In Equation 13, to calculate the maximum switching frequency one must take into account that the output voltage decreases from the nominal voltage to 0 volts, the f_{DIV} integer increases from 1 to 8 corresponding to the frequency shift.

In Figure 42, the solid line illustrates a typical safe operating area regarding frequency shift and assumes the output voltage is zero volts, and the resistance of the inductor is 0.1 Ω, FET on resistance of 0.2 Ω and the diode voltage drop is 0.5 V. The dashed line is the maximum switching frequency to avoid pulse skipping. Enter these equations in a spreadsheet or other software or use the SwitcherPro design software to determine the switching frequency.

$$f_{SW(max\,skip)} = \frac{1}{t_{ON}} \times \left(\frac{I_L \times R_{dc} + V_{OUT} + V_d}{V_{IN} - I_L \times R_{DS(on)} + V_d} \right) \tag{12}$$

$$f_{SWshift} = \frac{f_{DIV}}{t_{ON}} \times \left(\frac{I_L \times R_{dc} + V_{OUT(sc)} + V_d}{V_{IN} - I_L \times R_{DS(on)} + V_d} \right) \tag{13}$$

I_L	inductor current
R_{dc}	inductor resistance
V_{IN}	maximum input voltage
V_{OUT}	output voltage
V_{OUTSC}	output voltage during short
V_d	diode voltage drop
$R_{DS(ON)}$	switch on resistance
t_{ON}	controllable on time
f_{DIV}	frequency divide equals (1, 2, 4, or 8)

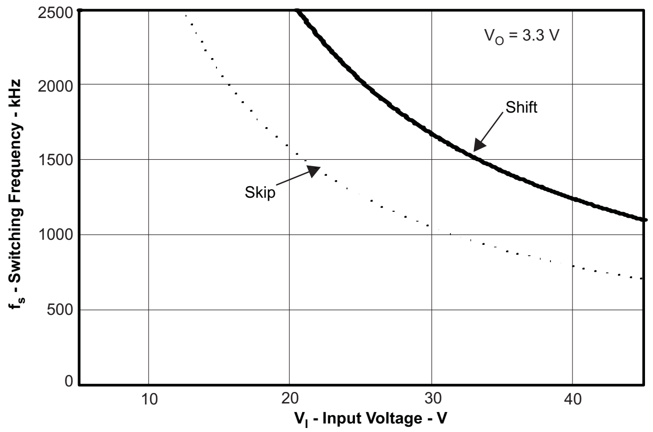


Figure 42. Maximum Switching Frequency vs. Input Voltage

DETAILED DESCRIPTION (continued)

How to Interface to RT/CLK Pin

The RT/CLK pin can be used to synchronize the regulator to an external system clock. To implement the synchronization feature connect a square wave to the RT/CLK pin through the circuit network shown in Figure 43. The square wave amplitude must transition lower than 0.5 V and higher than 2.2 V on the RT/CLK pin and have an on time greater than 40 ns and an off time greater than 40 ns. The synchronization frequency range is 300 kHz to 2200 kHz. The rising edge of the PH will be synchronized to the falling edge of RT/CLK pin signal. The external synchronization circuit should be designed in such a way that the device will have the default frequency set resistor connected from the RT/CLK pin to ground should the synchronization signal turn off. It is recommended to use a frequency set resistor connected as shown in Figure 43 through a 50-Ω resistor to ground. The resistor should set the switching frequency close to the external CLK frequency. It is recommended to ac couple the synchronization signal through a 10-pF ceramic capacitor to RT/CLK pin and a 4-kΩ series resistor. The series resistor reduces PH jitter in heavy load applications when synchronizing to an external clock and in applications which transition from synchronizing to RT mode. The first time the CLK is pulled above the CLK threshold the device switches from the RT resistor frequency to PLL mode. The internal 0.5-V voltage source is removed and the CLK pin becomes high impedance as the PLL starts to lock onto the external signal. Since there is a PLL on the regulator the switching frequency can be higher or lower than the frequency set with the external resistor. The device transitions from the resistor mode to the PLL mode and then will increase or decrease the switching frequency until the PLL locks onto the CLK frequency within 100 microseconds.

When the device transitions from the PLL to resistor mode the switching frequency will slow down from the CLK frequency to 150 kHz, then reapply the 0.5-V voltage and the resistor will then set the switching frequency. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0- to 0.8-volts on VSENSE pin. The device implements a digital frequency shift to enable synchronizing to an external clock during normal startup and fault conditions. Figure 44, Figure 45 and Figure 46 show the device synchronized to an external system clock in continuous conduction mode (CCM) discontinuous conduction (DCM) and pulse skip mode (PSM).

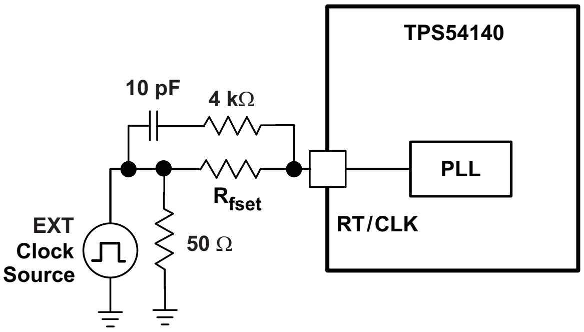


Figure 43. Synchronizing to a System Clock

DETAILED DESCRIPTION (continued)

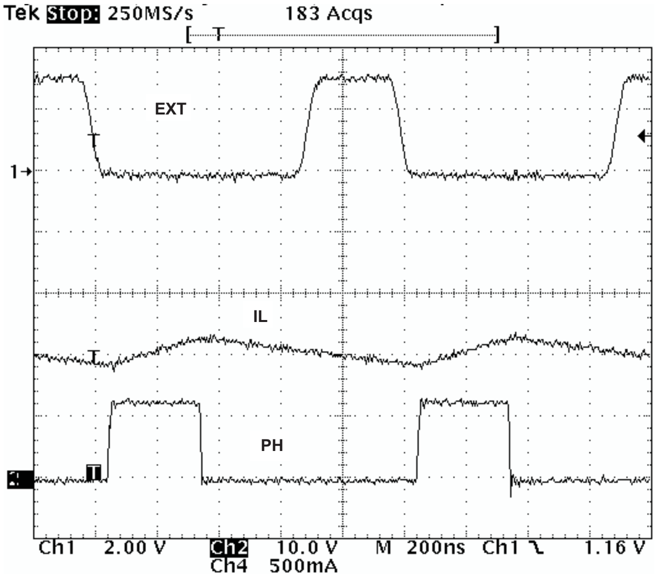


Figure 44. Plot of Synchronizing in CCM

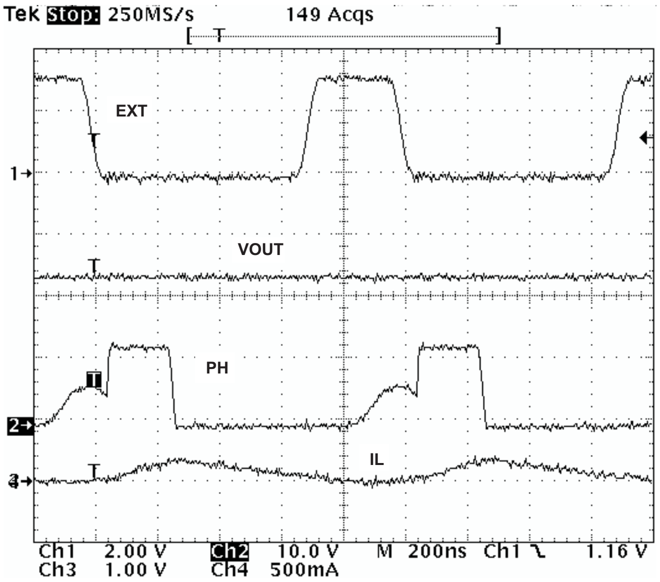


Figure 45. Plot of Synchronizing in DCM

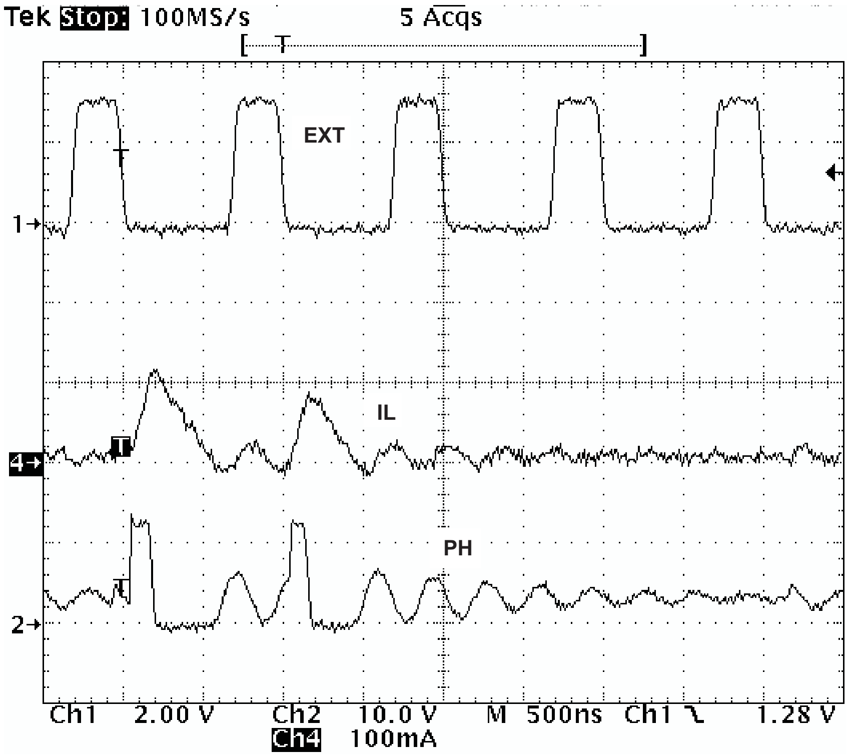


Figure 46. Plot of Synchronizing in PSM

Power-good (PWRGD Pin)

The PWRGD pin is an open drain output. Once the VSENSE pin is between 94% and 107% of the internal voltage reference the PWRGD pin is de-asserted and the pin floats. It is recommended to use a pull-up resistor between the values of 1 kΩ and 100 kΩ to a voltage source that is 5.5 V or less. The PWRGD is in a defined state once the V_{IN} input voltage is greater than 1.5 V but with reduced current sinking capability. The PWRGD will achieve full current sinking capability as V_{IN} input voltage approaches 3 V.

DETAILED DESCRIPTION (continued)

The PWRGD pin is pulled low when the VSENSE is lower than 92% or greater than 109% of the nominal internal reference voltage. Also, the PWRGD is pulled low, if the UVLO or thermal shutdown are asserted or the EN pin pulled low.

Overvoltage Transient Protection

The TPS54140-Q1 incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients on power supply designs with low value output capacitance. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier will respond by clamping the error amplifier output to a high voltage, thus requesting the maximum output current. Once the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state duty cycle. In some applications, the power supply output voltage can respond faster than the error amplifier output can respond, this actuality leads to the possibility of an output overshoot. The OVTP feature minimizes the output overshoot, when using a low value output capacitor, by implementing a circuit to compare the VSENSE pin voltage to OVTP threshold which is 109% of the internal voltage reference. If the VSENSE pin voltage is greater than the OVTP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVTP threshold, the high side MOSFET is allowed to turn on at the next clock cycle.

Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 182°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 182°C, the device reinitiates the power up sequence by discharging the SS/TR pin.

Small Signal Model for Loop Response

Figure 47 shows an equivalent model for the TPS54140-Q1 control loop which can be modeled in a circuit simulation program to check frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a gm_{EA} of 97 μA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor R_o and capacitor C_o model the open loop gain and frequency response of the amplifier. The 1-mV ac voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting c/a shows the small signal response of the frequency compensation. Plotting a/b shows the small signal response of the overall loop. The dynamic loop response can be checked by replacing R_L with a current source with the appropriate load step amplitude and step rate in a time domain analysis. This equivalent model is only valid for continuous conduction mode designs.

DETAILED DESCRIPTION (continued)

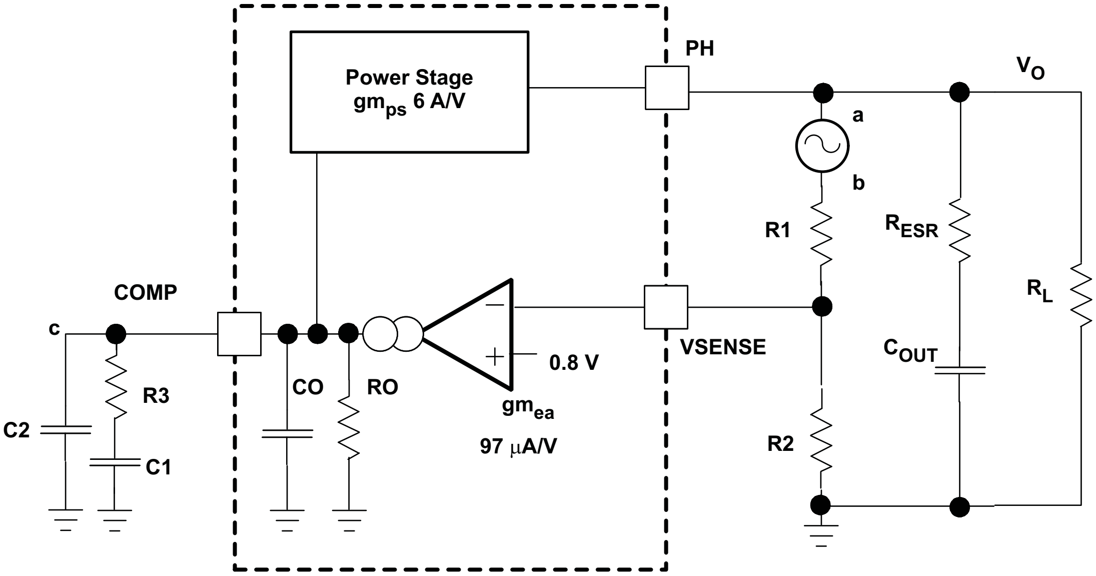


Figure 47. Small Signal Model for Loop Response

Simple Small Signal Model for Peak Current Mode Control

Figure 48 describes a simple small signal model that can be used to understand how to design the frequency compensation. The TPS54140-Q1 power stage can be approximated to a voltage-controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 14 and consists of a dc gain, one dominant pole, and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in Figure 47) is the power stage transconductance. The gm_{PS} for the TPS54140-Q1 is 6 A/V. The low-frequency gain of the power stage frequency response is the product of the transconductance and the load resistance as shown in Equation 15.

As the load current increases and decreases, the low-frequency gain decreases and increases, respectively. This variation with the load may seem problematic at first glance, but fortunately the dominant pole moves with the load current (see Equation 16). The combined effect is highlighted by the dashed line in the right half of Figure 48. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions which makes it easier to design the frequency compensation. The type of output capacitor chosen determines whether the ESR zero has a profound effect on the frequency compensation design. Using high ESR aluminum electrolytic capacitors may reduce the number frequency compensation components needed to stabilize the overall loop because the phase margin increases from the ESR zero at the lower frequencies (see Equation 17).

DETAILED DESCRIPTION (continued)

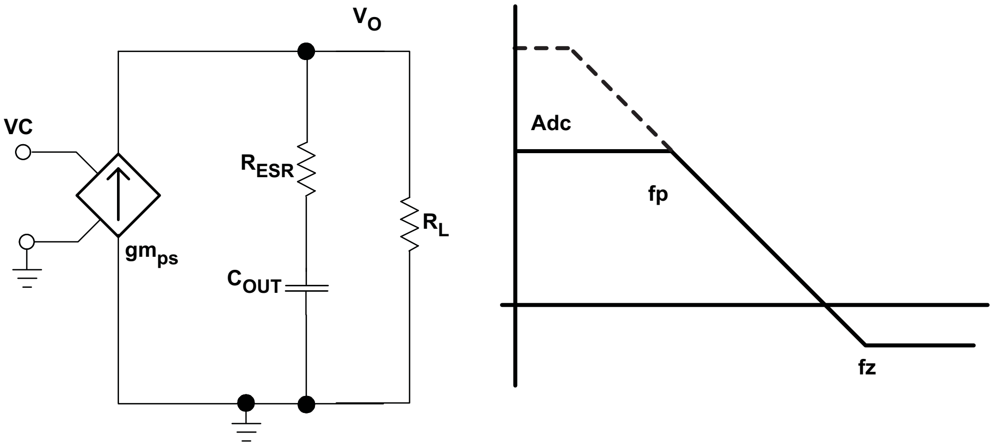


Figure 48. Simple Small Signal Model and Frequency Response for Peak Current Mode Control

$$\frac{V_{OUT}}{V_C} = Adc \times \frac{\left(1 + \frac{s}{2\pi \times f_Z}\right)}{\left(1 + \frac{s}{2\pi \times f_P}\right)} \quad (14)$$

$$Adc = gm_{ps} \times R_L \quad (15)$$

$$f_P = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad (16)$$

$$f_Z = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (17)$$

Small Signal Model for Frequency Compensation

The TPS54140-Q1 uses a transconductance amplifier for the error amplifier and readily supports three of the commonly-used frequency compensation circuits. Compensation circuits Type 2A, Type 2B, and Type 1 are shown in Figure 49. Type 2 circuits most likely implemented in high bandwidth power-supply designs using low ESR output capacitors. The Type 1 circuit is used with power-supply designs with high-ESR aluminum electrolytic or tantalum capacitors. Equation 18 and Equation 19 show how to relate the frequency response of the amplifier to the small signal model in Figure 49. The open-loop gain and bandwidth are modeled using the R_O and C_O shown in Figure 49. See the application section for a design example using a Type 2A network with a low ESR output capacitor.

Equation 18 through Equation 27 are provided as a reference for those who prefer to compensate using the preferred methods. Those who prefer to use prescribed method use the method outlined in the application section or use switched information.

DETAILED DESCRIPTION (continued)

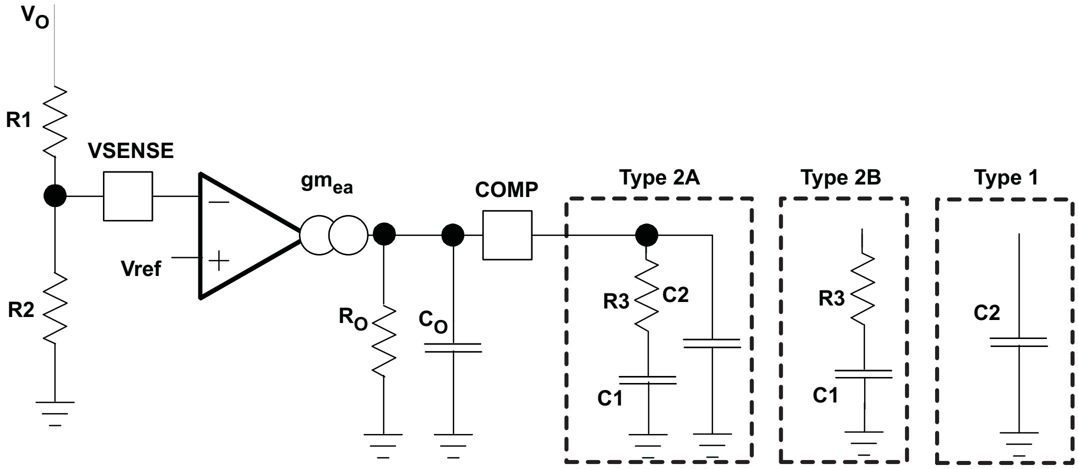


Figure 49. Types of Frequency Compensation

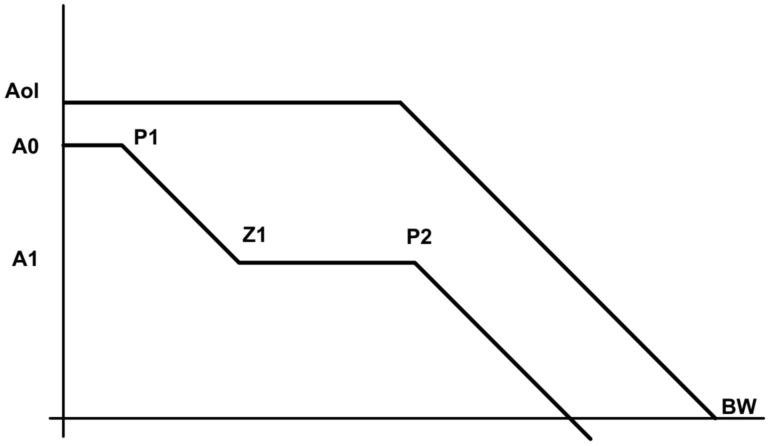


Figure 50. Frequency Response of the Type 2A and Type 2B Frequency Compensation

$$Ro = \frac{Aol(V/V)}{gm_{ea}} \tag{18}$$

$$C_{OUT} = \frac{gm_{ea}}{2\pi \times BW\ (Hz)} \tag{19}$$

$$EA = A0 \times \frac{\left(1 + \frac{s}{2\pi \times f_{Z1}}\right)}{\left(1 + \frac{s}{2\pi \times f_{P1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{P2}}\right)} \tag{20}$$

$$A0 = gm_{ea} \times Ro \times \frac{R2}{R1 + R2} \tag{21}$$

$$A1 = gm_{ea} \times Ro|\,|R3 \times \frac{R2}{R1 + R2} \tag{22}$$

$$P1 = \frac{1}{2\pi \times Ro \times C1} \tag{23}$$

DETAILED DESCRIPTION (continued)

$$Z1 = \frac{1}{2\pi \times R3 \times C1} \tag{24}$$

$$P2 = \frac{1}{2\pi \times R3 \,||\, R \times (C2 + C_{OUT})} \text{ type 2a} \tag{25}$$

$$P2 = \frac{1}{2\pi \times R3 \,||\, R \times C_{OUT}} \text{ type 2b} \tag{26}$$

$$P2 = \frac{1}{2\pi \times R \times (C2 + C_{OUT})} \text{ type 1} \tag{27}$$

APPLICATION INFORMATION

Design Guide — Step-By-Step Design Procedure

This example details the design of a high frequency switching regulator design using ceramic output capacitors. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level. For this example, we will start with the following known parameters:

Output Voltage	3.3 V
Transient Response 0- to 1.5-A load step	ΔV_{OUT} = 4%
Maximum Output Current	1.5 A
Input Voltage	12 V nom. 8 V to 18 V
Output Voltage Ripple	< 33 mV_{pp}
Start Input Voltage (rising VIN)	7.25 V
Stop Input Voltage (falling VIN)	6.25 V

Selecting the Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, the user will want to choose the highest switching frequency possible since this will produce the smallest solution size. The high switching frequency allows for lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. The switching frequency that can be selected is limited by the minimum on-time of the internal power switch, the input voltage and the output voltage and the frequency shift limitation.

Equation 12 and Equation 13 must be used to find the maximum switching frequency for the regulator, choose the lower value of the two equations. Switching frequencies higher than these values will result in pulse skipping or the lack of overcurrent protection during a short circuit.

The typical minimum on time, t_{onmin}, is 130 ns for the TPS54140-Q1. For this example, the output voltage is 3.3 V and the maximum input voltage is 18 V, which allows for a maximum switch frequency up to 1600 kHz when including the inductor resistance, on resistance and diode voltage in Equation 12. To ensure overcurrent runaway is not a concern during short circuits in your design use Equation 13 or the solid curve in Figure 42 to determine the maximum switching frequency. With an maximum input voltage of 20 V, assuming a diode voltage of 0.5 V, inductor resistance of 100 mΩ, switch resistance of 200 mΩ, an output current of 2.8 A, the maximum switching frequency is approximately 1600 kHz.

Choosing the lower of the two values and adding some margin a switching frequency of 1200 kHz is used. To determine the timing resistance for a given switching frequency, use Equation 11 or the curve in Figure 40.

The switching frequency is set by resistor R_t shown in Figure 51.

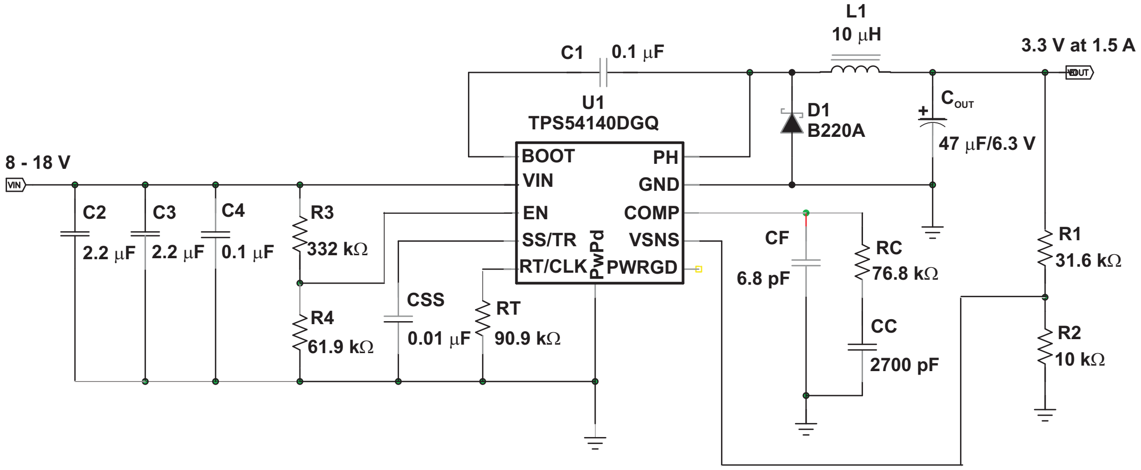


Figure 51. High Frequency, 3.3-V Output Power Supply Design with Adjusted UVLO.

Output Inductor Selection (L_O)

To calculate the minimum value of the output inductor, use Equation 28.

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current.

The inductor ripple current will be filtered by the output capacitor. Therefore, choosing high inductor ripple currents will impact the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, the following guidelines may be used.

For designs using low ESR output capacitors such as ceramics, a value as high as K_{IND} = 0.3 may be used. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results. Since the inductor ripple current is part of the PWM control system, the inductor ripple current should always be greater than 100 mA for dependable operation. In a wide input voltage regulator, it is best to choose an inductor ripple current on the larger side. This allows the inductor to still have a measurable ripple current with the input voltage at its minimum.

For this design example, use K_{IND} = 0.2 and the minimum inductor value is calculated to be 7.6 μH. For this design, a nearest standard value was chosen: 10 μH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 30 and Equation 31.

For this design, the RMS inductor current is 1.506 A and the peak inductor current is 1.62 A. The chosen inductor is a MSS6132-103. It has a saturation current rating of 1.64 A and an RMS current rating of 1.9 A.

As the equation set demonstrates, lower ripple currents will reduce the output voltage ripple of the regulator but will require a larger value of inductance. Selecting higher ripple currents will increase the output voltage ripple of the regulator but allow for a lower inductance value.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

$$\text{Lo min} = \frac{\text{Vinmax} - \text{Vout}}{\text{Io} \times K_{IND}} \times \frac{\text{Vout}}{\text{Vinmax} \times f\text{sw}} \tag{28}$$

$$I_{RIPPLE} \leq I_O \times K_{IND} \tag{29}$$

$$I_{L(rms)} = \sqrt{(I_O)^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times (\text{Vinmax} - V_{OUT})}{\text{Vinmax} \times L_O \times f_{SW}}\right)^2} \tag{30}$$

$$ILpeak = Iout + \frac{Iripple}{2} \tag{31}$$

Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor will determine the modulator pole, the output voltage ripple, and how the regulators responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator can not. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator also will temporarily not be able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as transitioning from no load to a full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for two clock cycles while only allowing a tolerable amount of droop in the output voltage. Calculate the minimum output capacitance necessary to accomplish this using Equation 32.

Where ΔI_{OUT} is the change in output current, f_{sw} is the regulators switching frequency and ΔV_{OUT} is the allowable change in the output voltage. For this example, the transient load response is specified as a 4% change in V_{OUT} for a load step from 0 A (no load) to 1.5 A (full load). For this example, $\Delta I_{OUT} = 1.5\text{-}0 = 1.5$ A and $\Delta V_{OUT} = 0.04 \times 3.3 = 0.132$ V. Using these numbers gives a minimum capacitance of 18.9 μF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. Aluminum electrolytic and tantalum capacitors have higher ESR that should be taken into account.

The catch diode of the regulator can not sink current so any stored energy in the inductor will produce an output voltage overshoot when the load current rapidly decreases, see Figure 52. The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high load current to a lower load current. The excess energy that gets stored in the output capacitor will increase the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. Use Equation 33 to calculate the minimum capacitance to keep the output voltage overshoot to a desired value. Where L is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, VF is the final peak output voltage, and Vi is the initial capacitor voltage. For this example, the worst case load step will be from 1.5 A to 0 A. The output voltage will increase during this load transition and the stated maximum in our specification is 4% of the output voltage. This will make VF = 1.04 × 3.3 = 3.432. Vi is the initial capacitor voltage which is the nominal output voltage of 3.3 V. Using these numbers in Equation 33 yields a minimum capacitance of 25.3 μF.

Use Equation 34 to calculate the minimum output capacitance needed to meet the output voltage ripple specification. Where f_{sw} is the switching frequency, $V_{oripple}$ is the maximum allowable output voltage ripple, and I_{ripple} is the inductor ripple current. Equation 34 yields 0.7 μF.

Equation 35 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 35 indicates the ESR should be less than 147 mΩ.

The most stringent criteria for the output capacitor is 25.3 μF of capacitance to keep the output voltage in regulation during an unload transient.

Additional capacitance de-ratings for aging, temperature and dc bias should be factored in which will increase this minimum value. For this example, a 47-μF 6.3-V X7R ceramic capacitor with 5 mΩ of ESR will be used.

Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the Root Mean Square (RMS) value of the maximum ripple current. Equation 36 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, Equation 36 yields 64.8 mA.

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \tag{32}$$

$$C_{OUT} > L_O \times \frac{\left((I_{OH})^2 - (I_{OL})^2\right)}{\left((V_f)^2 - (V_i)^2\right)} \tag{33}$$

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{1}{\left(\frac{V_{OUT(ripple)}}{I_{RIPPLE}}\right)} \tag{34}$$

$$R_{ESR} = \frac{V_{OUT(ripple)}}{I_{RIPPLE}} \tag{35}$$

$$I_{COUT(rms)} = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{\sqrt{12} \times V_{IN(max)} \times L_O \times f_{SW}} \tag{36}$$

Catch Diode

The TPS54140-Q1 requires an external catch diode between the PH pin and GND. The selected diode must have a reverse voltage rating equal to or greater than $V_{IN(max)}$. The peak current rating of the diode must be greater than the maximum inductor current. The diode should also have a low forward voltage. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator will be.

Typically, the higher the voltage and current ratings the diode has, the higher the forward voltage will be. Since the design example has an input voltage up to 18 V, a diode with a minimum of 20 V reverse voltage will be selected.

For the example design, the B220A Schottky diode is selected for its lower forward voltage and it comes in a larger package size which has good thermal characteristics over small devices. The typical forward voltage of the B220A is 0.50 volts.

The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time is multiplied by the forward voltage of the diode which equals the conduction losses of the diode. At higher switch frequencies, the ac losses of the diode need to be taken into account. The ac losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery. Equation 37 is used to calculate the total power dissipation, conduction losses plus ac losses, of the diode.

The B220A has a junction capacitance of 120 pF. Using Equation 37, the selected diode will dissipate 0.632 Watts. This power dissipation, depending on mounting techniques, should produce a 16°C temperature rise in the diode when the input voltage is 18 V and the load current is 1.5 A.

If the power supply spends a significant amount of time at light load currents or in sleep mode consider using a diode which has a low leakage current and slightly higher forward voltage drop.

$$P_D = \frac{\left(V_{IN(max)} - V_{OUT}\right) \times I_{OUT} \times V f d}{V_{IN(max)}} + \frac{C_j \times f_{SW} \times \left(V_{IN} + V f d\right)^2}{2} \tag{37}$$

Input Capacitor

The TPS54140-Q1 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 3 μF of effective capacitance and in some applications a bulk capacitance. The effective capacitance includes any dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54140-Q1. The input ripple current can be calculated using Equation 38.

The value of a ceramic capacitor varies significantly over temperature and the amount of dc bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the dc bias taken into account. The capacitance value of a capacitor decreases as the dc bias across a capacitor increases.

For this example design, a ceramic capacitor with at least a 20-V voltage rating is required to support the maximum input voltage. Common standard ceramic capacitor voltage ratings include 4 V, 6.3 V, 10 V, 16 V, 25 V, 50 V or 100 V so a 25-V capacitor should be selected. For this example, two 2.2-μF, 25-V capacitors in parallel have been selected. Table 1 shows a selection of high voltage capacitors. The input capacitance value determines the input ripple voltage of the regulator. The input ripple voltage can be calculated using Equation 39. Using the design example values, I_{outmax} = 1.5 A, C_{IN} = 4.4 μF, f_{SW} = 1200 kHz, yields an input voltage ripple of 71 mV and an RMS input ripple current of 0.701 A.

$$\text{Icirms} = \text{Iout} \times \sqrt{\frac{\text{Vout}}{\text{Vin min}} \times \frac{(\text{Vin min} - \text{Vout})}{\text{Vin min}}} \tag{38}$$

$$\Delta\text{Vin} = \frac{\text{Iout max} \times 0.25}{\text{Cin} \times f\text{sw}} \tag{39}$$

Table 1. Capacitor Types

VENDOR	VALUE (μF)	EIA Size	VOLTAGE	DIALECTRIC	COMMENTS
Murata	1 to 2.2	1210	100 V	X7R	GRM32 series
	1 to 4.7		50 V		
	1	1206	100 V		GRM31 series
	1 to 2.2		50 V		
Vishay	1 10 1.8	2220	50 V		VJ X7R series
	1 to 1.2		100 V		
	1 to 3.9	2225	50 V		
	1 to 1.8		100 V		
TDK	1 to 2.2	1812	100 V		C series C4532
	1.5 to 6.8		50 V		
	1. to 2.2	1210	100 V		C series C3225
	1 to 3.3		50 V		
AVX	1 to 4.7	1210	50 V		X7R dielectric series
	1		100 V		
	1 to 4.7	1812	50 V		
	1 to 2.2		100 V		

Slow Start Capacitor

The slow start capacitor determines the minimum amount of time it will take for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS54140-Q1 reach the current limit or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems.

The slow start time must be long enough to allow the regulator to charge the output capacitor up to the output voltage without drawing excessive current. Equation 40 can be used to find the minimum slow start time, T_{SS}, necessary to charge the output capacitor, C_{OUT}, from 10% to 90% of the output voltage, V_{OUT}, with an average slow start current of I_{SSAVG}. In the example, to charge the 47 μF output capacitor up to 3.3 V while only allowing the average input current to be 0.125 A would require a 1-ms slow start time.

Once the slow start time is known, the slow start capacitor value can be calculated using Equation 6. For the example circuit, the slow start time is not too critical since the output capacitor value is 47 μF which does not require much current to charge to 3.3 V. The example circuit has the slow start time set to an arbitrary value of 1-ms which requires a 3.3-nF capacitor.

$$\text{Tss} > \frac{\text{Cout} \times \text{Vout} \times 0.8}{\text{Issavg}} \tag{40}$$

Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT and PH pins for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have a 10-V or higher voltage rating.

Under Voltage Lock Out Set Point

The Under Voltage Lock Out (UVLO) can be adjusted using an external voltage divider on the EN pin of the TPS54140-Q1. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 7.25 V (enabled). After the regulator starts switching, it should continue to do so until the input voltage falls below 6.25 V (UVLO stop).

The programmable UVLO and enable voltages are set using a resistor divider between VIN and ground to the EN pin. Equation 2 through Equation 3 can be used to calculate the resistance values necessary. For the example application, a 332 kΩ between VIN and EN and a 61.9 kΩ between EN and ground are required to produce the 7.25- and 6.25-V start and stop voltages.

Output Voltage and Feedback Resistors Selection

For the example design, 10.0 kΩ was selected for R2. Using Equation 1, R1 is calculated as 31.25 kΩ. The nearest standard 1% resistor is 31.6 kΩ. Due to current leakage of the VSENSE pin, the current flowing through the feedback network should be greater than 1 µA in order to maintain the output voltage accuracy. This requirement makes the maximum value of R2 equal to 800 kΩ. Choosing higher resistor values will decrease quiescent current and improve efficiency at low output currents but may introduce noise immunity problems.

Compensation

There are several industry techniques used to compensate DC/DC regulators. The method presented here yields high phase margins. For most conditions, the regulator will have a phase margin between 60 and 90 degrees. The method presented here ignores the effects of the slope compensation that is internal to the TPS54140-Q1. Since the slope compensation is ignored, the actual cross over frequency is usually lower than the cross over frequency used in the calculations.

Use SwitcherPro software for a more accurate design.

The uncompensated regulator will have a dominant pole, typically located between 300 Hz and 3 kHz, due to the output capacitor and load resistance and a pole due to the error amplifier. One zero exists due to the output capacitor and the ESR. The zero frequency is higher than either of the two poles.

If left uncompensated, the double pole created by the error amplifier and the modulator would lead to an unstable regulator. To stabilize the regulator, one pole must be canceled out. One design approach is to locate a compensating zero at the modulator pole. Then select a cross over frequency that is higher than the modulator pole. The gain of the error amplifier can be calculated to achieve the desired cross over frequency. The capacitor used to create the compensation zero along with the output impedance of the error amplifier form a low frequency pole to provide a minus one slope through the cross over frequency. Then a compensating pole is added to cancel the zero due to the output capacitors ESR. If the ESR zero resides at a frequency higher than the switching frequency then it can be ignored.

To compensate the TPS54140-Q1 using this method, first calculate the modulator pole and zero using the following equations:

$$f\text{p mod} = \frac{\text{Ioutmax}}{2 \times \pi \times \text{Vout} \times \text{Cout}} \tag{41}$$

Where I_{OUTMAX} is the maximum output current, C_{OUT} is the output capacitance and V_{OUT} is the nominal output voltage.

$$f\text{z mod} = \frac{1}{2 \times \pi \times \text{Resr} \times \text{Cout}} \tag{42}$$

For the example design, the modulator pole is located at 1.5 kHz and the ESR zero is located at 338 kHz.

Next, the designer needs to select a crossover frequency which will determine the bandwidth of the control loop. The cross over frequency must be located at a frequency at least five times higher than the modulator pole. The cross over frequency must also be selected so that the available gain of the error amplifier at the cross over frequency is high enough to allow for proper compensation.

Equation 47 is used to calculate the maximum cross over frequency when the ESR zero is located at a frequency that is higher than the desired cross over frequency. This will usually be the case for ceramic or low ESR tantalum capacitors. Aluminum electrolytic and tantalum capacitors will typically produce a modulator zero at a low frequency due to their high ESR.

The example application is using a low ESR ceramic capacitor with 10 mΩ of ESR making the zero at 338 kHz.

This value is much higher than typical crossover frequencies so the maximum crossover frequency is calculated using both Equation 43 and Equation 46.

Using Equation 46 gives a minimum crossover frequency of 7.6 kHz and Equation 43 gives a maximum crossover frequency of 45.3 kHz.

A crossover frequency of 45 kHz is arbitrarily selected from this range.

$$F_{c\,max} \le 2100 \sqrt{\frac{F_{pmod}}{V_{out}}} \text{ for ceramic capacitors.} \tag{43}$$

$$F_{c\,max} \le \frac{51442}{\sqrt{V_{out}}} \text{ for Tantalum or Aluminum capacitors.} \tag{44}$$

$$F_{c\,max} \le \frac{F_{sw}}{5} \text{ for all cases.} \tag{45}$$

$$F_{c\,min} \ge 5 \times F_{pmod} \text{ for all cases.} \tag{46}$$

Once a cross over frequency, F_c, has been selected, the gain of the modulator at the cross over frequency is calculated. The gain of the modulator at the cross over frequency is calculated using Equation 47 .

$$G_{MOD(fc)} = \frac{gm_{(PS)} \times R_{LOAD} \times (2\pi \times f_C \times C_{OUT} \times R_{ESR} + 1)}{2\pi \times f_C \times C_{OUT} \times (R_{LOAD} + R_{ESR}) + 1} \tag{47}$$

For the example problem, the gain of the modulator at the cross over frequency is 0.542. Next, the compensation components are calculated. A resistor in series with a capacitor is used to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole. However, calculating the values of these components varies depending on if the ESR zero is located above or below the cross over frequency. For ceramic or low ESR tantalum output capacitors, the zero will usually be located above the cross over frequency. For aluminum electrolytic and tantalum capacitors, the modulator zero is usually located lower in frequency than the cross over frequency. For cases where the modulator zero is higher than the cross over frequency (ceramic capacitors).

$$R_C = \frac{V_{OUT}}{G_{MOD(fc)} \times gm_{(EA)} \times V_{REF}} \tag{48}$$

$$\text{Cc} = \frac{1}{\pi \times \text{Rc} \times f\text{p mod}} \tag{49}$$

$$C f = \frac{Co \times Resr}{Rc} \tag{50}$$

For cases where the modulator zero is less than the cross over frequency (aluminum or tantalum capacitors), the equations are:

$$R_C = \frac{V_{OUT}}{G_{MOD(fc)} \times f_{Z(mod)} \times gm_{(EA)} \times V_{REF}} \tag{51}$$

$$Cc = \frac{1}{\pi \times Rc \times fp\ mod} \tag{52}$$

$$C f = \frac{1}{2 \times \pi \times Rc \times fz\ mod} \tag{53}$$

For the example problem, the ESR zero is located at a higher frequency compared to the cross over frequency so Equation 50 through Equation 53 are used to calculate the compensation components. For the example problem, the components are calculated to be: R_c= 76.2 kΩ, C_c= 2710 pF, and C_f =6.17 pF.

The calculated value of the C_f capacitor is not a standard value so a value of 2700 pF will be used, 6.8 pF is used for C_c, and the R_c resistor sets the gain of the error amplifier which determines the cross over frequency. The calculated R_c resistor is not a standard value, so 76.8 kΩ will be used.

APPLICATION CURVES

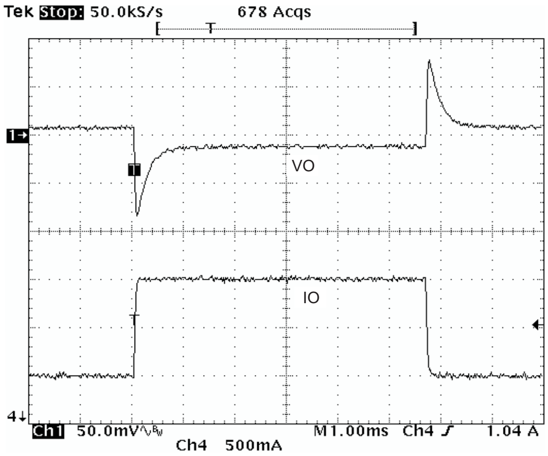


Figure 52. Load Transmit

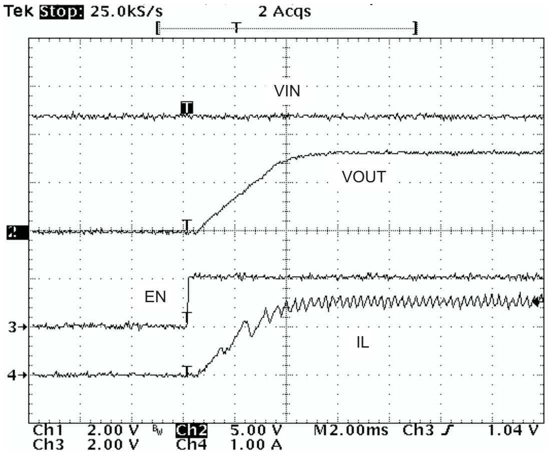


Figure 53. Startup With EN

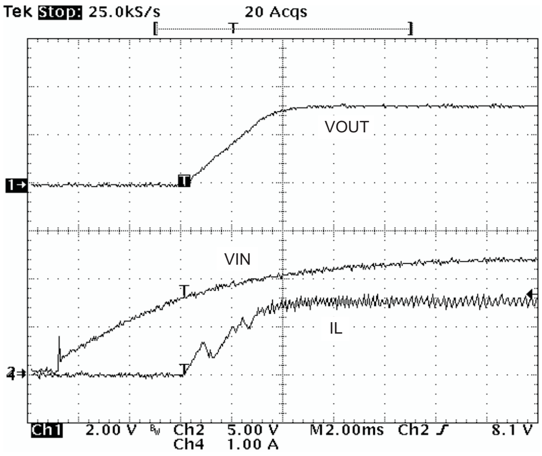


Figure 54. VIN Power Up

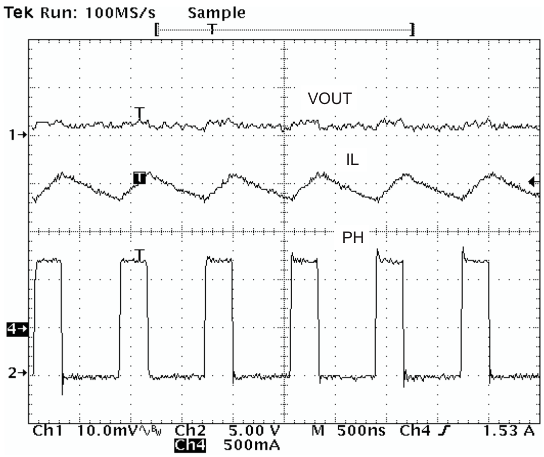


Figure 55. Output Ripple CCM

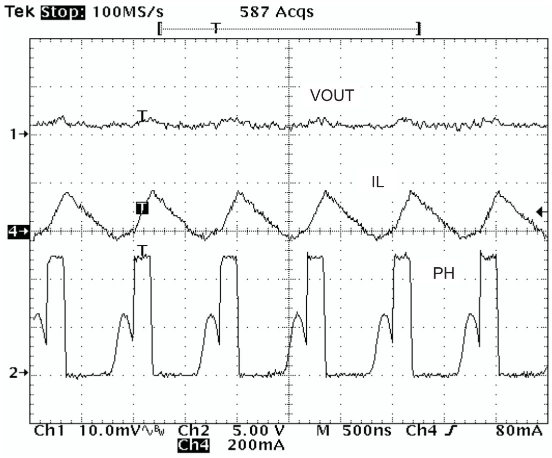


Figure 56. Output Ripple, DCM

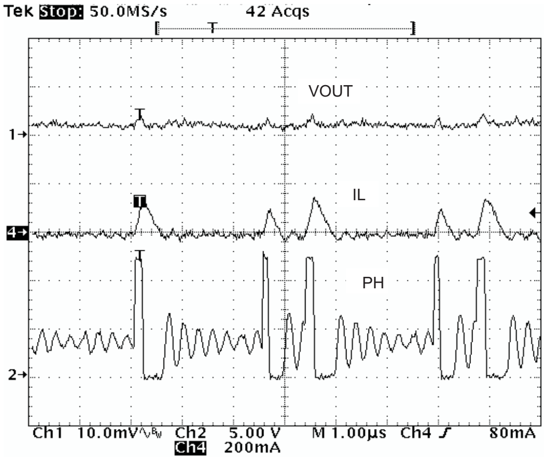


Figure 57. Output Ripple, PSM

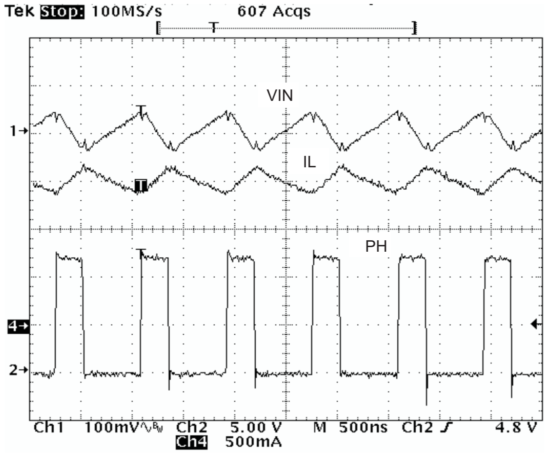


Figure 58. Input Ripple CCM

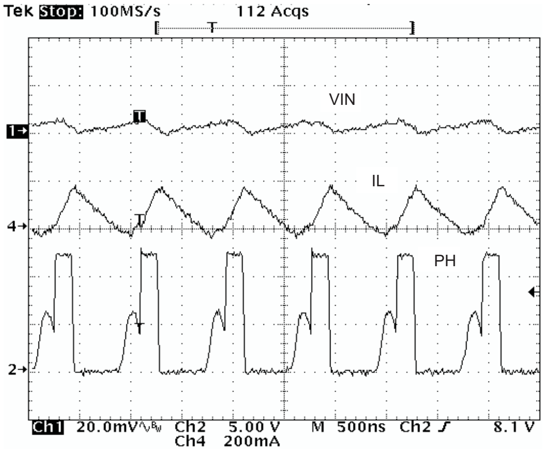


Figure 59. Input Ripple DCM

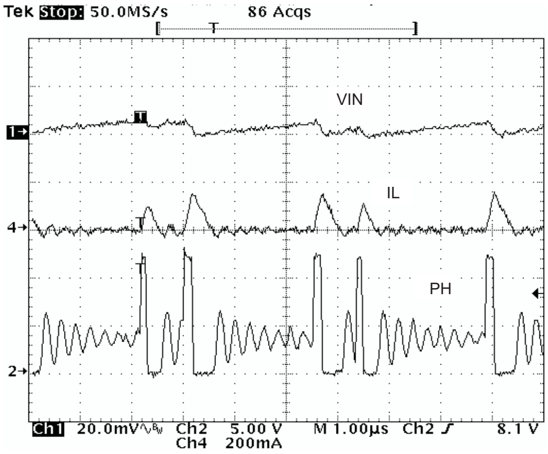


Figure 60. Input Ripple PSM

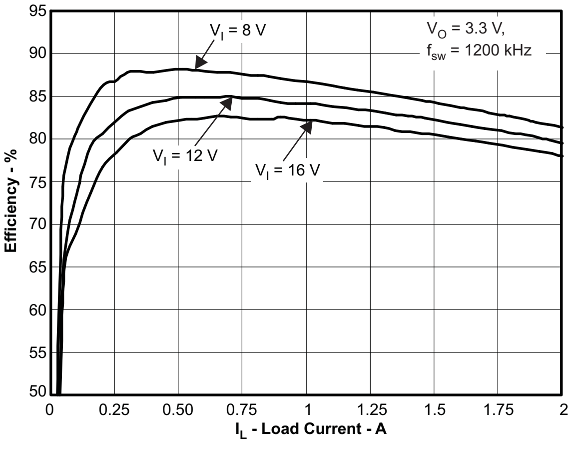


Figure 61. Efficiency vs Load Current

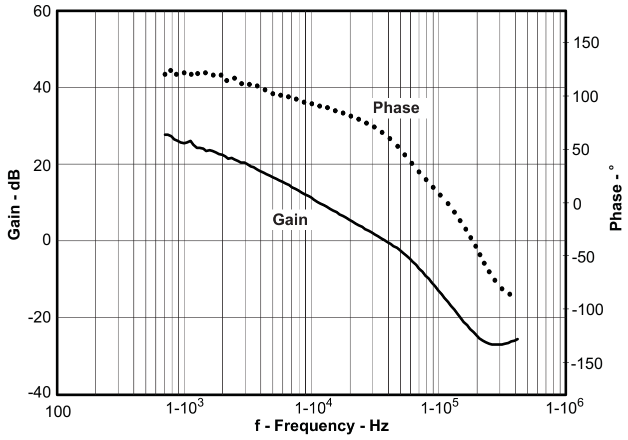


Figure 62. Overall Loop Frequency Response

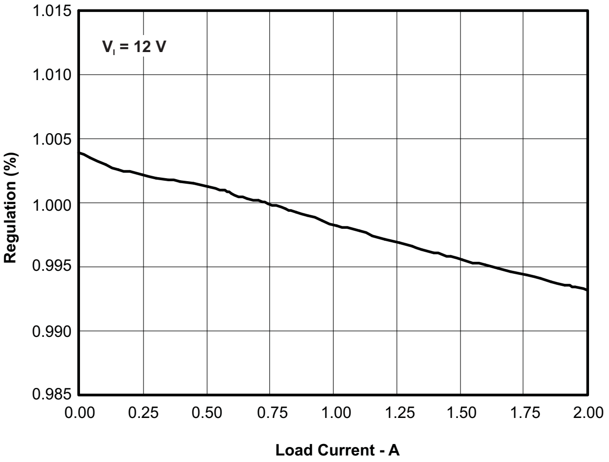


Figure 63. Regulation vs Load Current

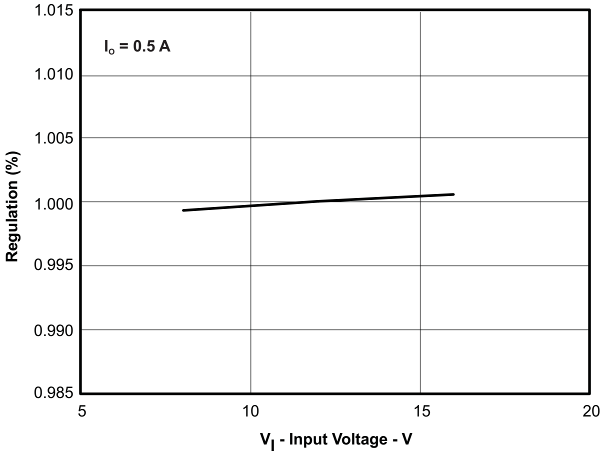


Figure 64. Regulation vs Input Voltage

Power Dissipation Estimate

The following formulas show how to estimate the IC power dissipation under continuous conduction mode (CCM) operation. These equations should not be used if the device is working in discontinuous conduction mode (DCM).

The power dissipation of the IC includes conduction loss (P_{con}), switching loss (P_{sw}), gate drive loss (P_{gd}) and supply current (P_q).

$$\text{Pcon} = \text{Io}^2 \times R_{DS(on)} \times \frac{\text{Vout}}{\text{Vin}} \tag{54}$$

$$P_{SW} = V_{IN}^{2} \times f_{SW} \times I_O \times 0.25\times10^{-9}\text{sec/V} \tag{55}$$

$$P_{gd} = V_{IN} \times 3\times10^{-9}\text{Asec} \times f_{SW} \tag{56}$$

$$P_q = 116\mu\text{A} \times V_{IN} \tag{57}$$

Where:

I_{OUT} is the output current (A).
$R_{DS(ON)}$ is the on-resistance of the high-side MOSFET (Ω).
V_{OUT} is the output voltage (V).
V_{IN} is the input voltage (V).
f_{SW} is the switching frequency (Hz).

So

$$\text{Ptot} = \text{Pcon} + \text{Psw} + \text{Pgd} + \text{Pq} \tag{58}$$

For given T_A,

$$\text{TJ} = \text{TA} + \text{Rth} \times \text{Ptot} \tag{59}$$

For given T_{JMAX} = 150°C

$$\text{TAmax} = \text{TJmax} - \text{Rth} \times \text{Ptot} \tag{60}$$

Where:

P_{tot} is the total device power dissipation (W).
T_A is the ambient temperature (°C).
T_J is the junction temperature (°C).
R_{th} is the thermal resistance of the package (°C/W).
T_{JMAX} is maximum junction temperature (°C).
T_{AMAX} is maximum ambient temperature (°C).

There will be additional power losses in the regulator circuit due to the inductor ac and dc losses, the catch diode and trace resistance that will impact the overall efficiency of the regulator.

Layout

Layout is a critical portion of good power supply design. There are several signals paths that conduct quickly changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supply performance. To reduce these problems, the VIN pin should be bypassed to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. See Figure 65 for a PCB layout example. The GND pin should be tied directly to the thermal pad under the IC and the exposed thermal pad.

The thermal pad should be connected to any internal PCB ground planes using multiple vias directly under the IC. The PH pin should be routed to the cathode of the catch diode and to the output inductor. Because the PH connection is the switching node, the catch diode and output inductor should be located very close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. The RT/CLK pin is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts; however, this layout has been shown to produce good results and is meant as a guideline.

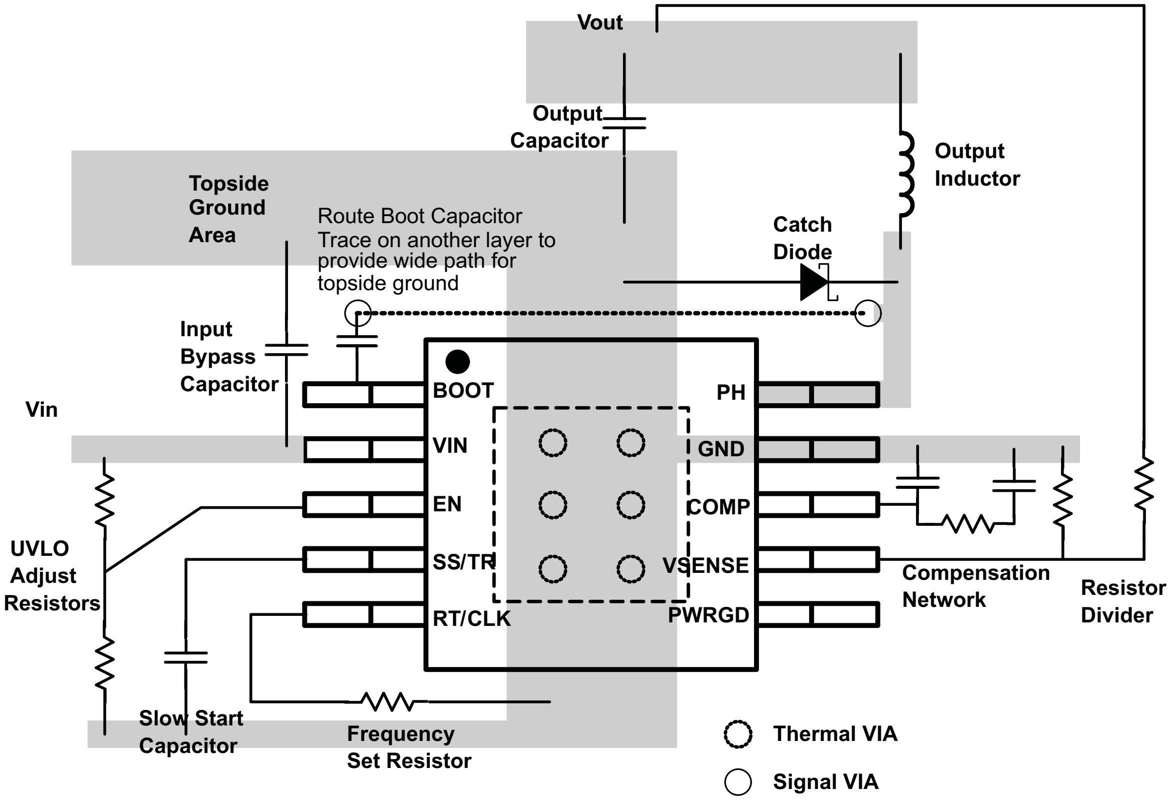


Figure 65. PCB Layout Example

REVISION HISTORY

Changes from Revision B (March 2011) to Revision C	Page
• Changed regulated output to input	1
• Changed 92 to 93% and 107 to 109% in description.	1
• Updated Abs Max footnote	2
• Changed enable threshold to –50 mV for Input current and changed typ values for input current and hysteresis current	3
• Removed input current max value; changed typ value from ±0.9 to –0.9	3
• Changed error amplifier test condition from ±2 µA to –2 µA; changed g_M to $g_m$in the parameter description	3
• Changed enable threshold to –50 mV for Input current and changed typ values for input current and hysteresis current	4
• Inserted page break in front of current limit section	4
• Changed RT/CLK low threshold min value from 0.5 to 0.45	4
• Added (Fault) and (Good) to VSENSE falling and rising	4
• Changed Figure 21 to match 57060-Q1	10
• Changed "are added to the COMP pin to ground" to "are added from the COMP pin to ground"	14
• Changed "use the UVLO adjust registers" to "use the UVLO adjust resistors"	14
• Changed "Each cycle the switch current" to "During each cycle the switch current"	20
• Changed "high voltage. Thus, requesting the" to "high voltage, thus requesting the"	24
• Changed "Equation 32 shows the minimum output capacitance necessary to accomplish this" to "Calculate the minimum output capacitance necessary to accomplish this using Equation 32."	31
• Changed "Equation 33 is used to calculate the" to "Use Equation 33 to calculate the minimum"	31
• Changed "Equation 34 calculates" to "Use equation 34 to"; changed "Equation 35 yields 0.7 µF" to "Equation 34 yields 0.7 µF"	31
• Changed "input voltage ripple" to "input ripple voltage"	33

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