LM2901x-Q1 Quadruple Differential Comparator

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C6
- Single Supply or Dual Supplies
- Low Supply-Current Drain Independent of Supply Voltage: 0.8 mA (Typical)
- Low Input Bias Current: 25 nA (Typical)
- Low Input Offset Current: 2 nA (Typical)
- Low Input Offset Voltage: 2 mV (Typical)
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage: ±36 V
- Low Output Saturation Voltage
- Output Compatible With TTL, MOS, and CMOS
- For Single Version in 5-Pin SOT-23, See the TL331-Q1 (SLVS969)

2 Applications

- Automotive
  - HEV/EV and Power Trains
  - Infotainment and Clusters
  - Body Control Modules
- Industrial
- Power Supervision
- Oscillators
- Peak Detectors
- Logic Voltage Translation

3 Description

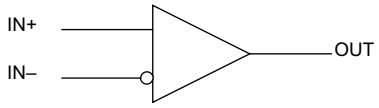
The LM2901x-Q1 family of devices consists of four independent voltage comparators, designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is possible, provided the difference between the two supplies is 2 V to 36 V, and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships. LM2901V-Q1 supports higher V_{CC} voltage and LM2901AV-Q1 supports higher V_{CC} and lower V_{IO}.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2901xx-Q1PW	TSSOP (14)	4.40 mm × 5.00 mm
LM2901xx-Q1D	SOIC (14)	3.91 mm × 8.65 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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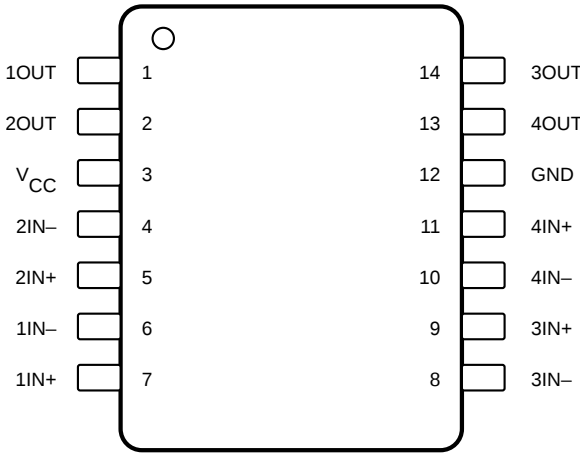
4 Revision History

Changes from Revision D (April 2008) to Revision E **Page**

- Added AEC-Q100 results to the *Features* section ... 1
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Added the common-mode voltage note to the V_{ICR} parameter in the *Electrical Characteristics* table ... 5

5 Pin Configuration and Functions

D and PW Packages
14-Pin SOIC and TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1OUT	O	Output of comparator 1
2	2OUT	O	Output of comparator 2
3	V_{CC}	—	Supply Pin
4	2IN–	I	Negative input of comparator 2
5	2IN+	I	Positive input of comparator 2
6	1IN–	I	Negative input of comparator 1
7	1IN+	I	Positive input of comparator 1
8	3IN–	I	Negative input of comparator 3
9	3IN+	I	Positive input of comparator 3
10	4IN–	I	Negative input of comparator 4
11	4IN+	I	Positive input of comparator 4
12	GND	—	Ground
13	4OUT	O	Output of comparator 4
14	3OUT	O	Output of comparator 3

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{CC}(2)		36	V
Differential input voltage, V_{ID}(3)		±36	
Input voltage range, V_I (either input)	–0.3	36	
Output voltage, V_O		36	
Output current, I_O		20	mA
Duration of output short circuit to ground(4)	Unlimited		
Lead temperature 1,6 mm (1/16 inch) from case for 10 s		260	°C
Operating virtual junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground.
(3) Differential voltages are at IN+ with respect to IN−.
(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	LM2901-Q1	2	30	V
		LM2901V-Q1, LM2901AV-Q1	2	32	
T_A	Ambient temperature		–40	125	°C
I_O	Output current (per comparator)		0	4	mA

6.4 Thermal Information

THERMAL METRIC(1)		LM2901x-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	88.6	119.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.1	47.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.0	60.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.6	5.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.7	60.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semicondctor and IC Package Thermal Metrics* application report, SPRA953.
(2) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A) / R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

6.5 Electrical Characteristics

V_{CC} = 5 V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		T_A(2)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR(min)}$, V_O = 1.4 V, V_{CC} = 5 V to MAX(3)	Non A devices	25°C		2	7	mV
				Full range			15	
			A suffix devices	25°C		1	2	
				Full range			4	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		5	50	nA
				Full range			200	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		–25	–250	nA
				Full range			–500	
V_{ICR}	Common-mode input-voltage range(4)			25°C	0		V_{CC} – 1.5	V
				Full range	0		V_{CC} – 2	
A_{VD}	Large-signal differential-voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, R_L ≥ 15 kΩ to V_{CC}		25°C	25	100		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1	50	nA
			V_{OH} = V_{CC} MAX(3)	Full range			1	µA
V_{OL}	Low-level output voltage	V_{ID} = –1 V	I_{OL} = 4 mA	25°C		150	400	mV
				Full range			700	
I_{OL}	Low-level output current	V_{ID} = –1 V	V_{OL} = 1.5 V	25°C	6	16		mA
I_{CC}	Supply current (four comparators)	V_O = 2.5 V, No load	V_{CC} = 5 V	25°C		0.8	2	
			V_{CC} = MAX(3)			1	2.5	

(1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(2) Full range (MIN to MAX) is −40°C to 125°C. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(3) V_{CC} MAX = 30 V for non-V devices and 32 V for V-suffix devices.
(4) The voltage at either the input or common mode should not be allowed to negative by more that 0.3 V. The upper end of the common-mode voltage range is V_{CC+} – 1.5 V; however, one input can exceed V_{CC}, and the comparator will provide a proper output state as long as the other input remains in the common-mode range. Either or both inputs can go to 30 V without damage.

6.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time(1)	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF(2)	100-mV input step with 5-mV overdrive		1.3		µs
		TTL-level input step		0.3		

(1) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.
(2) C_L includes probe and jig capacitance.

6.7 Typical Characteristics

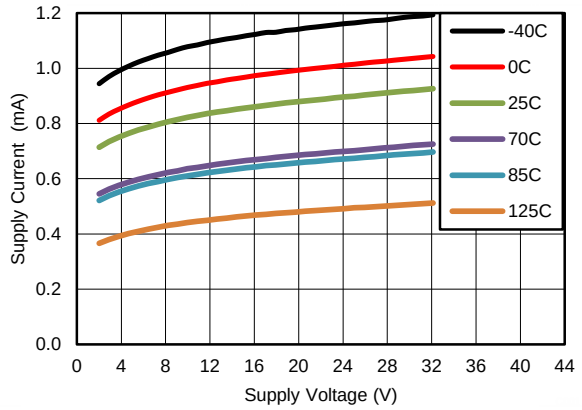


Figure 1. Supply Current vs Supply Voltage

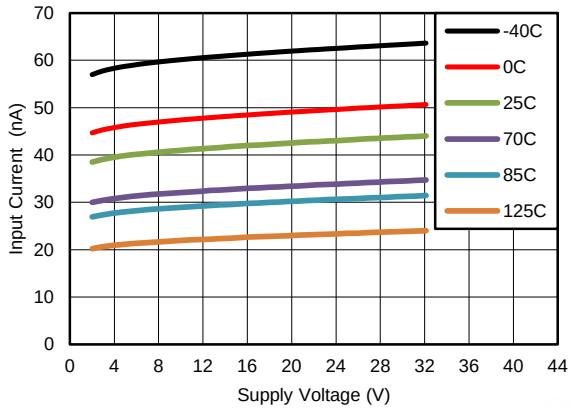


Figure 2. Input Bias Current vs Supply Voltage

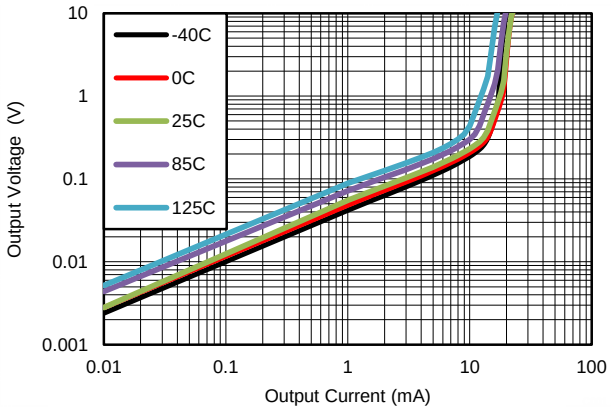


Figure 3. Output Saturation Voltage

7 Detailed Description

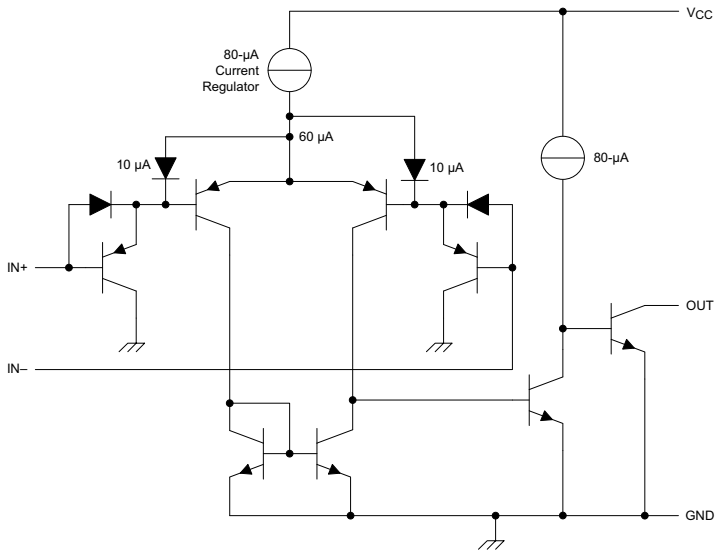
7.1 Overview

The LM2901x-Q1 family of devices is a quad comparator with the ability to operate up to an absolute maximum of 36 V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications because of the very wide supply voltage range (2 V to 30 V or 32 V), low I_Q, and fast response of the device.

This device is AEC-Q100 qualified and can operate over a wide temperature range (–40°C to 125°C).

The open-collector output allows the user to configure the logic-high voltage of the output (V_{OH}) independent of V_{CC} and can be used with multiple comparators in wired AND functionality.

7.2 Functional Block Diagram



7.3 Feature Description

The LM2901x-Q1 family of devices consists of a PNP Darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common-mode voltage ability, allowing the LM2901x-Q1 family of devices to accurately function from ground to V_{CC} – 2 V for the lower voltage input. The higher voltage input may go up to the maximum V_{CC}. This ability enables a wide input range even when using modern-day supplies of 3.3 V and 5 V.

The output consists of an open collector bipolar transistor. The transistor sinks current when the positive input voltage is higher than the negative input voltage and the offset voltage. The V_{OL} is resistive and scales with the output current. See Figure 3 in *Typical Characteristics* for the V_{OL} values with respect to the output current.

The special pinout of this device separates input pins from the output pins to reduce parasitic coupling between input and output.

7.4 Device Functional Modes

7.4.1 Voltage Comparison

The LM2901x-Q1 family of devices operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputs a logic low or high impedance (logic high with pullup) based on the input differential polarity.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM2901x-Q1 family of devices is typically used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open-drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes the LM2901x-Q1 family of devices optimal for level shifting to a higher or lower voltage.

8.2 Typical Application

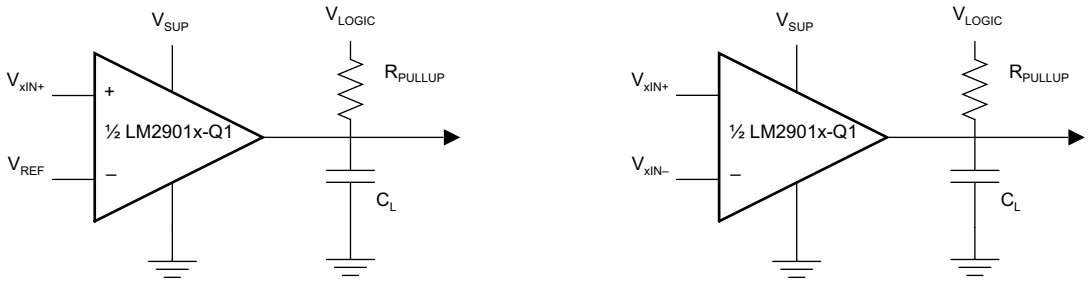


Figure 4. Single-Ended and Differential Comparator Configurations

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	0 V to V_{SUP} – 1.5 V
Supply voltage	2 V to 36 V
Logic supply voltage	2 V to 36 V
Output current (R_{PULLUP})	1 µA to 20 mA
Input overdrive voltage	100 mV
Reference voltage	2.5 V
Load capacitance (C_L)	15 pF

8.2.2 Detailed Design Procedure

8.2.2.1 Input Voltage Range

When selecting the input voltage range, the input common-mode voltage range (V_{ICR}) must be considered. If temperature operation is above or below 25°C the V_{ICR} can range from 0 V to V_{CC} – 2 V. The V_{ICR} range limits the input voltage range to as high as V_{CC} – 2 V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

The following lists some input voltage scenarios and the resulting outcomes:

- When both IN– and IN+ are both within the common-mode range:
  - If IN– is higher than IN+ and the offset voltage, then the output is low and the output transistor is sinking current.

  - If IN– is lower than IN+ and the offset voltage, then the output is in high impedance and the output transistor is not conducting.
- When IN– is higher than common-mode and IN+ is within common-mode, the output is low and the output transistor is sinking current.
- When IN+ is higher than common-mode and IN– is within common-mode, then the output is in high impedance and the output transistor is not conducting.
- When IN– and IN+ are both higher than common-mode, then the output is low and the output transistor is sinking current.

8.2.2.2 Minimum Overdrive Voltage

The overdrive voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). To make an accurate comparison the overdrive voltage (V_{OD}) must be higher than the input offset voltage (V_{IO}). The overdrive voltage can also determine the response time of the comparator, with the response time decreasing as the overdrive increases. Figure 5 and Figure 6 show positive and negative response times with respect to overdrive voltage.

8.2.2.3 Output and Drive Current

Output current is determined by the load or pullup resistance and logic or pullup voltage. The output current produces an output low voltage (V_{OL}) from the comparator. In which V_{OL} is proportional to the output current. Use Figure 3 to determine V_{OL} based on the output current.

The output current can also effect the transient response. See *Response Time* for more information.

8.2.2.4 Response Time

The transient response can be determined by the load capacitance (C_L), load or pullup resistance (R_{PULLUP}), and equivalent collector-emitter resistance (R_{CE}).

Use Equation 1 and Equation 2 to calculate the approximate values of the rise time (t_r) and fall time (t_f).

$$t_P \approx R_{PULLUP} \times C_L \quad (1)$$

$$t_N \approx R_{CE} \times C_L \quad (2)$$

To find the value of R_{CE}, use the slope of Figure 3 in the linear region at the desired temperature, or divide V_{OL} by I_O.

8.2.3 Application Curves

The following curves were generated with 5 V on V_{CC} and V_{LOGIC}, R_{PULLUP} = 5.1 kΩ, and 50-pF scope probe.

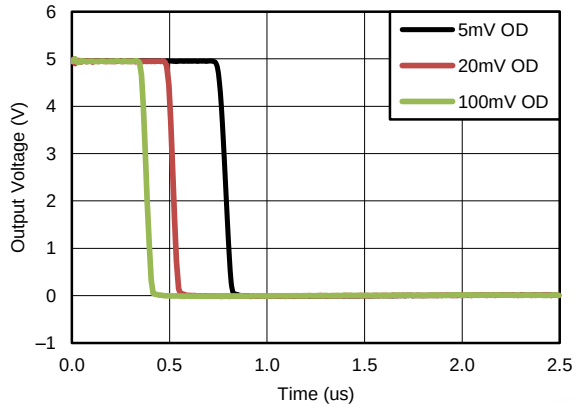


Figure 5. Response Time for Various Overdrives Negative Transition

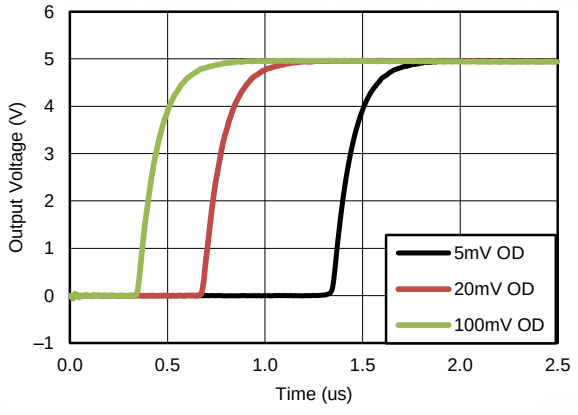


Figure 6. Response Time for Various Overdrives Positive Transition

9 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, TI recommends using a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can take away from some of the input common mode range of the comparator and create an inaccurate comparison.

10 Layout

10.1 Layout Guidelines

For accurate comparator applications without hysteresis, maintaining a stable power supply with minimized noise and glitches, which can affect the high-level input common-mode voltage range, is important. To achieve a stable power supply, place a bypass capacitor between the positive and negative (if available) supply voltage and ground. If a negative supply is not being used, do not put a capacitor between the GND pin of the IC and system ground.

10.2 Layout Example

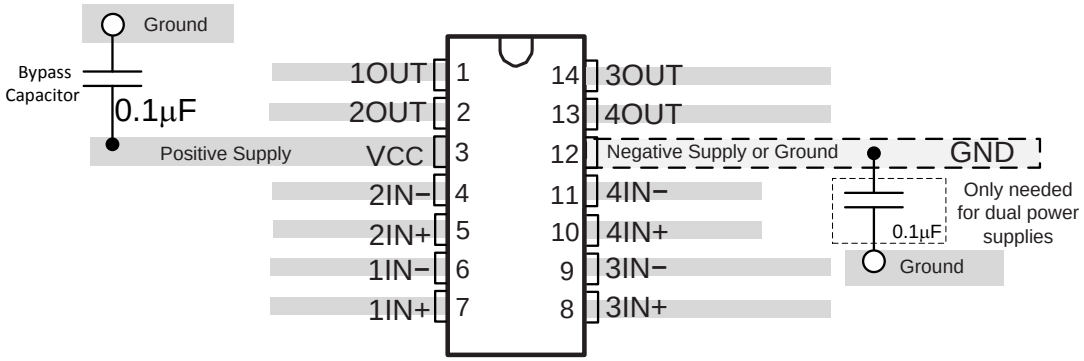


Figure 7. LM2901x-Q1 Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

TL331-Q1 *Single Differential Comparator*, SLVS969

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM2901-Q1	Click here	Click here	Click here	Click here	Click here
LM2901V-Q1	Click here	Click here	Click here	Click here	Click here
LM2901AV-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2901AVQDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901AVQ	Samples
LM2901AVQDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901AVQ	Samples
LM2901AVQPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901AVQ	Samples
LM2901AVQPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901AVQ	Samples
LM2901QDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901Q1	Samples
LM2901QDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901Q1	Samples
LM2901QPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901Q1	Samples
LM2901QPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901Q1	Samples
LM2901VQDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901VQ1	Samples
LM2901VQDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901VQ1	Samples
LM2901VQPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901VQ	Samples
LM2901VQPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2901VQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LM2901-Q1, LM2901AV-Q1, LM2901V-Q1 :

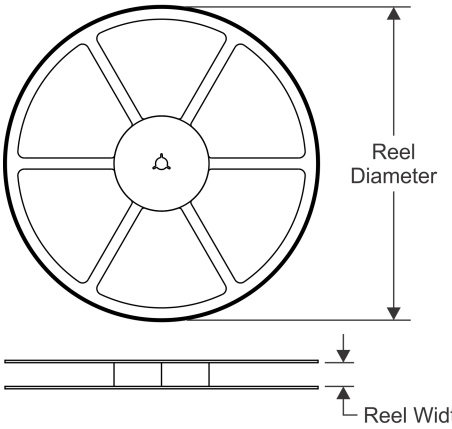
- Catalog: LM2901, LM2901AV, LM2901V

NOTE: Qualified Version Definitions:

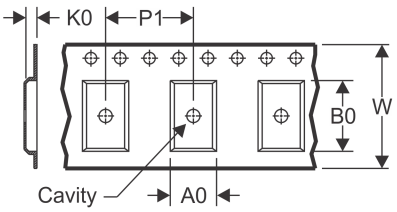
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

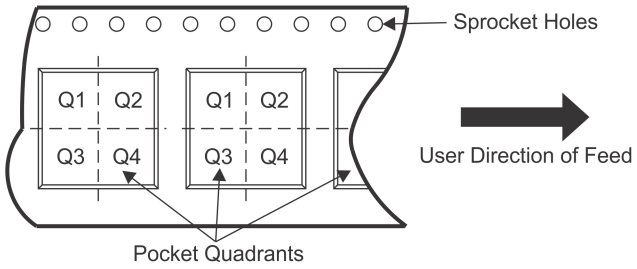


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

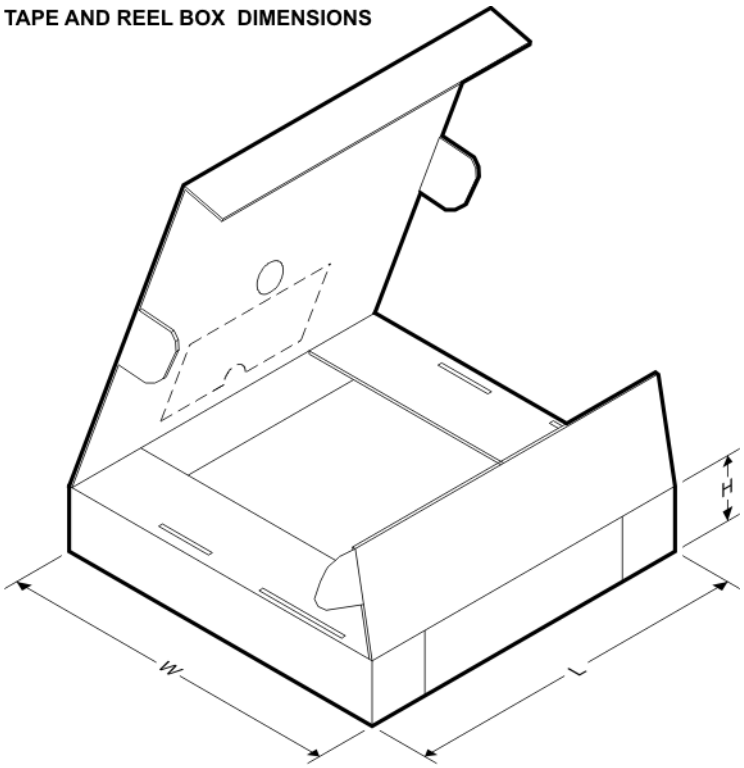
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2901AVQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901AVQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901VQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901VQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

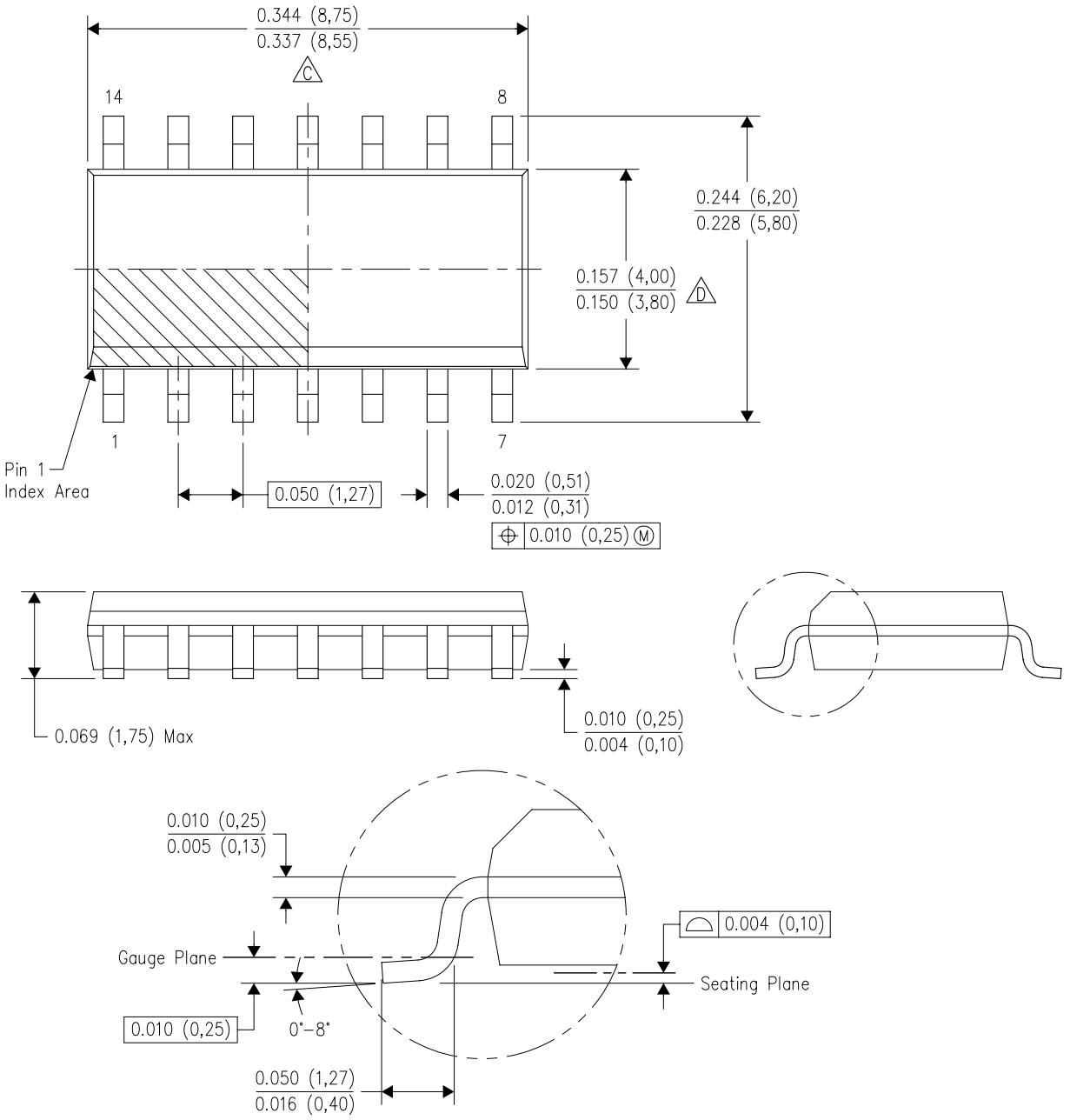
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2901AVQPWRG4Q1	TSSOP	PW	14	2000	367.0	367.0	35.0
LM2901AVQPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0
LM2901QPWRG4Q1	TSSOP	PW	14	2000	367.0	367.0	35.0
LM2901QPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0
LM2901VQPWRG4Q1	TSSOP	PW	14	2000	367.0	367.0	35.0
LM2901VQPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0

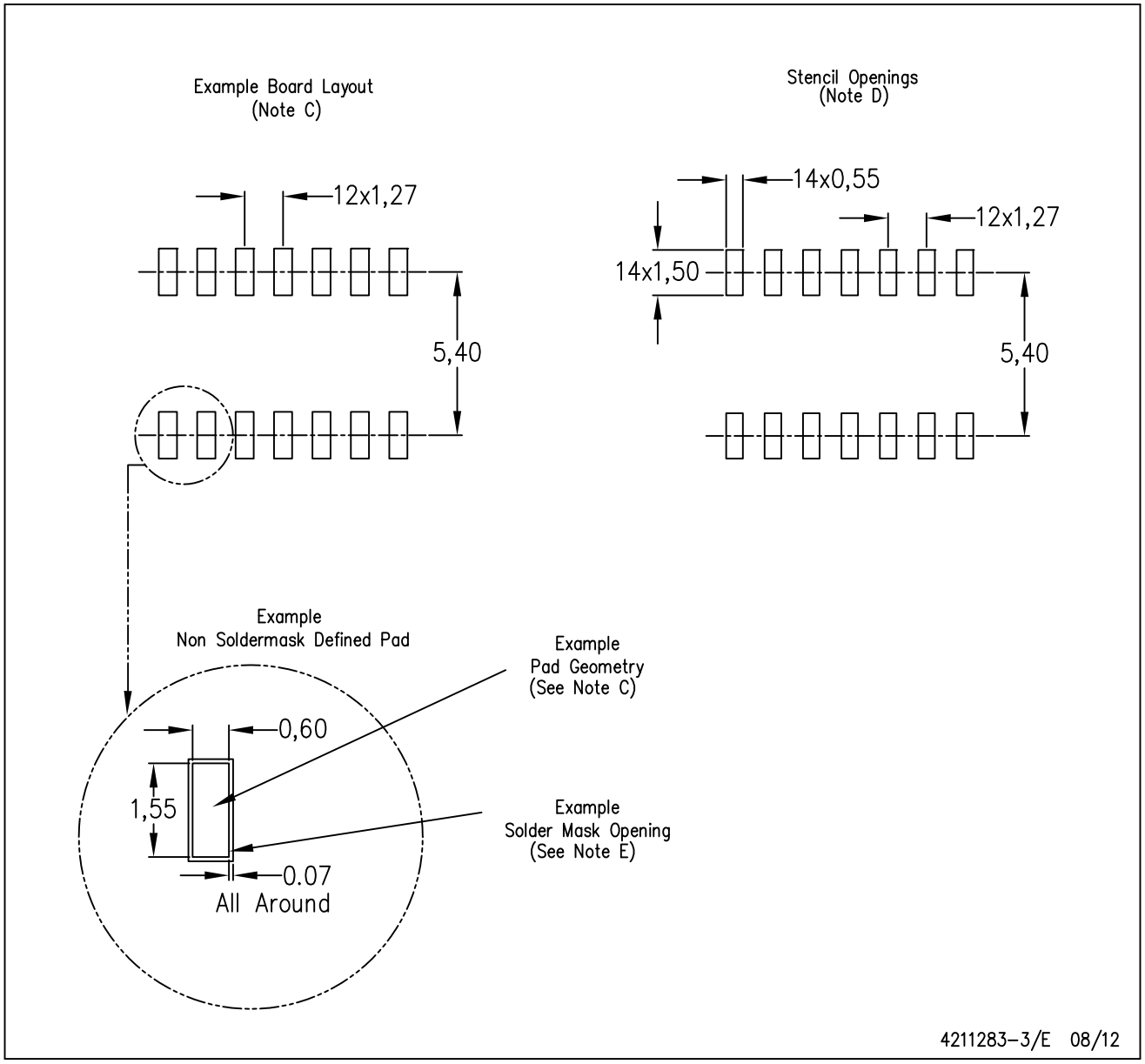
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

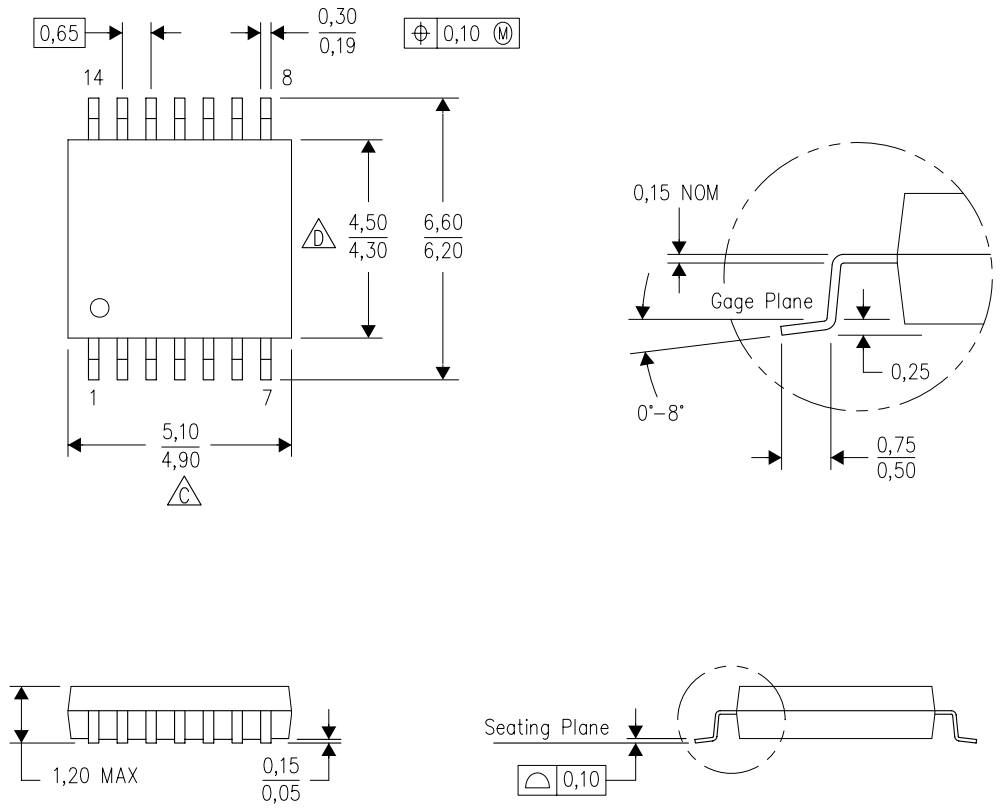
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

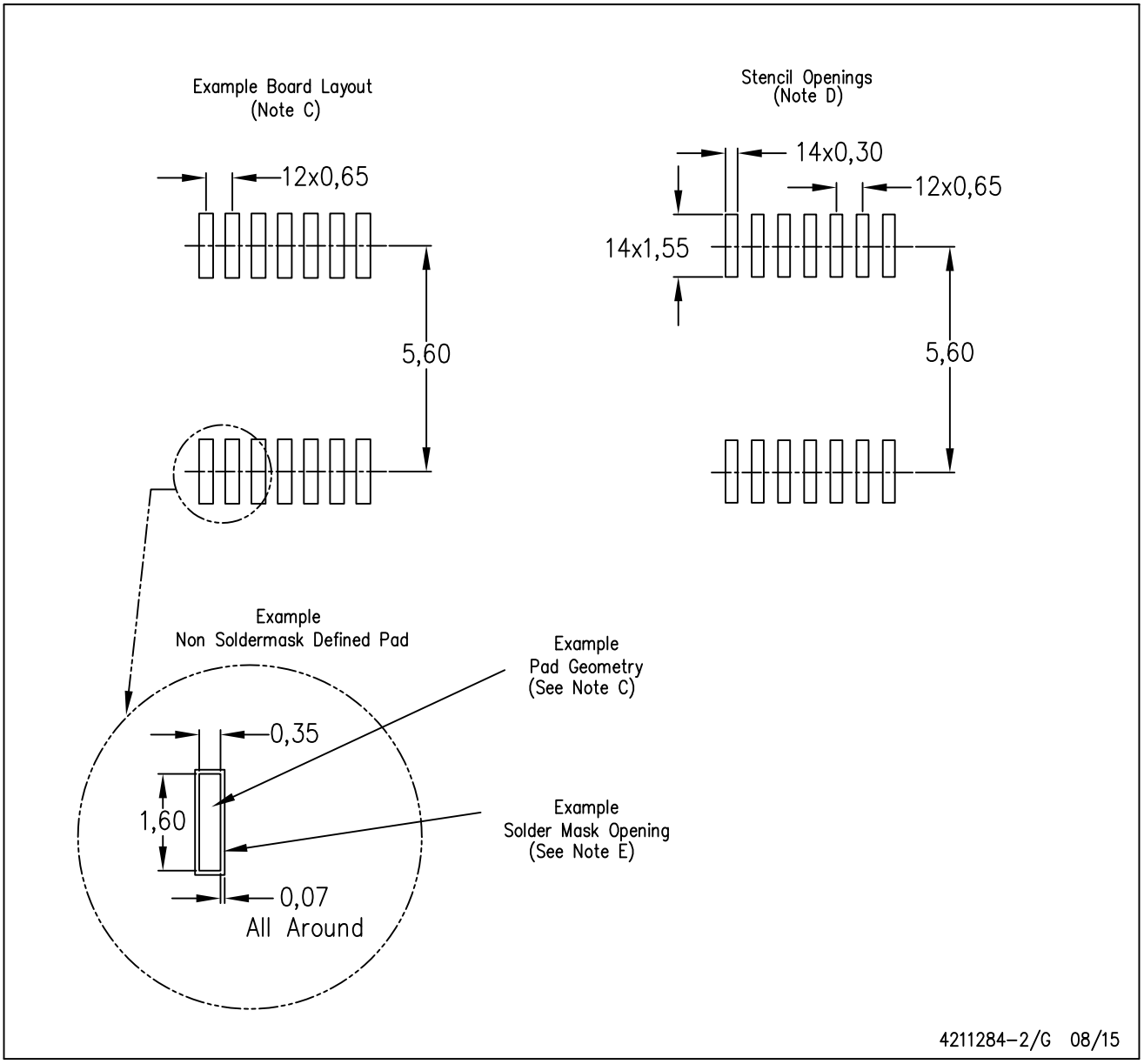
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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