# 3-A DUAL NON-SYNCHRONOUS CONVERTER WITH INTEGRATED HIGH-SIDE MOSFET

**Check for Samples: TPS54386-Q1**

## FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified With the Following Results:**
  - **Device Temperature Grade 2: –40°C to +105°C Ambient Operating Temperature**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C3B**
- **4.5-V to 28-V Input Range**
- **Output Voltage Range 0.8 V to 90% of Input Voltage**
- **Output Current Up to 3 A**
- **Fixed Switching Frequency: 600 kHz**
- **Three Selectable Levels of Overcurrent Protection (Output 2)**
- **0.8-V 1.5% Voltage Reference**
- **2.1-ms Internal Soft Start**
- **Dual PWM Outputs 180° Out-of-Phase**
- **Ratiometric or Sequential Startup Modes Selectable by a Single Pin**
- **85-mΩ Internal High-Side MOSFETs**
- **Current Mode Control**
- **Internal Compensation**
- **Pulse-by-Pulse Overcurrent Protection**
- **Thermal Shutdown Protection at 148°C**
- **14-Pin PowerPAD™ HTSSOP Package**

## APPLICATIONS

- **Power for DSP**
- **Consumer Electronics**

## CONTENTS

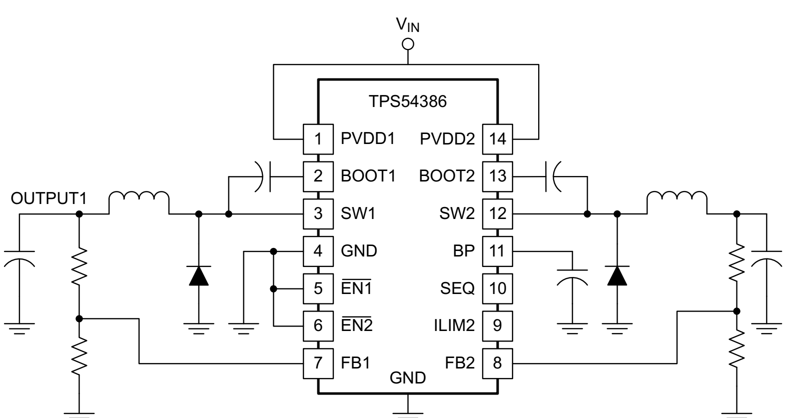


## DESCRIPTION

The TPS54386-Q1 are dual-output, non-synchronous buck converters capable of supporting 3-A output applications that operate from a 4.5-V to 28-V input supply voltage, and require output voltages between 0.8 V and 90% of the input voltage.

With an internally-determined operating frequency, soft-start time, and control-loop compensation, these converters provide many features with a minimum of external components. Channel-1 overcurrent protection is set at 4.5 A, whereas the channel-2 overcurrent protection level is selected by connecting a pin to ground, to BP, or left floating. The setting levels are used to allow for scaling of external components for applications that do not need the full load capability of both outputs.

The outputs may be enabled independently, or may be configured to allow either ratiometric or sequential start-up sequencing. Additionally, the two outputs may be powered from different sources.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Table 1. ORDERING INFORMATION(1)

| PART NUMBER | OPERATING FREQUENCY (kHz) | PACKAGE | MEDIA | UNITS | TOP-SIDE MARKING |
|---|---|---|---|---|---|
| TPS54386TPWPRQ1 | 600 | 14-HTSSOP package | Tape and reel | 2000 | 54386T |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

## DEVICE RATINGS

## ABSOLUTE MAXIMUM RATINGS(1)

| | | VALUE | UNIT |
|---|---|---|---|
| Input voltage range | PVDD1, PVDD2, $\overline{EN1}$, $\overline{EN2}$ | 30 | V |
| | BOOT1, BOOT2 | $V_{SW}$+ 7 | |
| | SW1, SW2 | –2 to 30 | |
| | SW1, SW2 transient (< 50 ns) | –3 to 31 | |
| | BP | 6.5 | |
| | SEQ, ILIM2 | –0.3 to 6.5 | |
| | FB1, FB2 | –0.3 to 3 | |
| | SW1, SW2 output current | 7 | A |
| | BP load current | 35 | mA |
| $T_{stg}$ | Storage temperature | –55 to 165 | °C |
| $T_A$ | Operating temperature | –40 to 105 | °C |
| ESD ratings | Human Body Model (HBM) AEC-Q100 Classification Level H2 | 2 | kv |
| | Charged Device Model (CDM) AEC-Q100 Classification Level C3B | 750 | V |

(1) Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{PVDD2}$ | Input voltage | | 4.5 | 28 | V |
| $T_A$ | Operating junction temperature | | –40 | 125 | °C |

## PACKAGE DISSIPATION RATINGS(1) (2) (3)

| PACKAGE | THERMAL IMPEDANCE JUNTION-TO-THERMAL PAD (°C/W) | $T_A$ = 25°C POWER RATING (W) | $T_A$ = 105°C POWER RATING (W) |
|---|---|---|---|
| Plastic 14-Pin HTSSOP (PWP) | 2.07(4) | 1.6 | 0.8 |

(1) For more information on the PWP package, see TI Technical Brief (SLMA002A).
(2) TI device packages are modeled and tested for thermal performance using printed circuit board designs outlined in JEDEC standards JESD 51-3 and JESD 51-7.
(3) For application information, see the *Power Derating* section.
(4) $T_{J-A}$ = 40°C/W.

## ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 105°C$, $V_{PVDD1} = V_{PVDD2} = 12$ V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT SUPPLY (PVDD)** | | | | | | |
| $V_{PVDD1}$ | Input voltage range | | 4.5 | | 28 | V |
| $V_{PVDD2}$ | | | 4.5 | | 28 | V |
| $IDD_{SDN}$ | Shutdown | $V_{\overline{EN1}} = V_{\overline{EN2}} = V_{PVDD2}$ | | 70 | 150 | µA |
| $IDD_Q$ | Quiescent, non-switching | $V_{FB}$ = 0.9 V, outputs off | | 1.8 | 3 | mA |
| $IDD_{SW}$ | Quiescent, while-switching | SW node unloaded; Measured as BP sink current | | 5 | | |
| $V_{UVLO}$ | Minimum turnon voltage | PVDD2 only | 3.8 | 4.1 | 4.4 | V |
| $V_{UVLO(hys)}$ | Hysteresis | | | 400 | | mV |
| $t_{START}$ [1] [2] | Time from start-up to soft-start begin | $C_{BP}$ = 10 µF, $\overline{EN1}$ and $\overline{EN2}$ go low simultaneously | | 2 | | ms |
| **ENABLE ($\overline{EN}$)** | | | | | | |
| $V_{\overline{EN1}}$ | Enable threshold | | 0.9 | 1.2 | 1.5 | V |
| $V_{\overline{EN2}}$ | | | 0.9 | 1.2 | 1.5 | V |
| | Hysteresis | | | 50 | | mV |
| $I_{\overline{EN1}}$ | Enable pullup current | $V_{\overline{EN1}} = V_{\overline{EN2}}$ = 0 V | | 6 | 12 | µA |
| $I_{\overline{EN2}}$ | | | | 6 | 12 | µA |
| $t_{\overline{EN}}$ [1] | Time from enable to soft-start begin | Other EN pin = GND | | 10 | | µs |
| **BP REGULATOR (BP)** | | | | | | |
| BP | Regulator voltage | 8 V < $P_{VDD2}$ < 28 V | 5 | 5.25 | 5.6 | V |
| $BP_{LDO}$ | Dropout voltage | $P_{VDD2}$ = 4.5 V; switching, no external load on BP | | 400 | | mV |
| $I_{BP}$ [1] | Regulator external load | | | | 2 | mA |
| $I_{BPS}$ | Regulator short circuit | 4.5 V < $P_{VDD2}$ < 28 V | 10 | 20 | 30 | mA |
| **OSCILLATOR** | | | | | | |
| $f_{SW}$ | Switching frequency | | 510 | 630 | 750 | kHz |
| $t_{DEAD}$ [1] | Clock dead time | | | 140 | | ns |
| **ERROR AMPLIFIER (EA) and VOLTAGE REFERENCE (REF)** | | | | | | |
| $V_{FB1}$ | Feedback input voltage | 0°C < $T_A$ < 85°C | 788 | 800 | 812 | mV |
| $V_{FB2}$ | | –40°C < $T_A$ < 125°C | 786 | | 812 | mV |
| $I_{FB1}$ | Feedback input bias current | | | 3 | 50 | nA |
| $I_{FB2}$ | | | | 3 | 50 | nA |
| $g_M1$ [1] | Transconductance | | | 30 | | µS |
| $g_M2$ [1] | | | | 30 | | µS |
| **SOFT START (SS)** | | | | | | |
| $T_{SS1}$ | Soft-start time | | 1.5 | 2.1 | 2.7 | ms |
| $T_{SS2}$ | | | 1.5 | 2.1 | 2.7 | ms |
| **OVERCURRENT PROTECTION** | | | | | | |
| $I_{CL1}$ | Current limit channel 1 | | 3.6 | 4.5 | 5.6 | A |
| $I_{CL2}$ | Current limit channel 2 | $V_{ILIM2} = V_{BP}$ | 3.6 | 4.5 | 5.6 | A |
| | | $V_{ILIM2}$ = (floating) | 2.4 | 3 | 3.6 | |
| | | $V_{ILIM2}$ = GND | 1.15 | 1.5 | 1.75 | |
| $V_{UV1}$ | Low-level output threshold to declare a fault | Measured at feedback pin | | 670 | | mV |
| $V_{UV2}$ | | | | 670 | | mV |
| $t_{HICCUP}$ [1] | Hiccup timeout | | | 10 | | ms |
| $t_{ON1(oc)}$ [1] | Minimum overcurrent pulse duration | | | 90 | 150 | ns |
| $t_{ON2(oc)}$ [1] | | | | 90 | 150 | ns |

(1) Ensured by design. Not production tested.
(2) When both outputs are started simultaneously, a 20-mA current source charges the BP capacitor. Faster times are possible with a lower BP capacitor value. More information can be found in the *Input UVLO and Startup* section.

## ELECTRICAL CHARACTERISTICS (continued)

$-40°C \leq T_A \leq 105°C$, $V_{PVDD1} = V_{PVDD2} = 12$ V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **BOOTSTRAP** | | | | | | |
| $R_{BOOT1}$, $R_{BOOT2}$ | Bootstrap switch resistance | From BP to BOOT1 or BP to BOOT2, $I_{EXT}$ = 50 mA | | 18 | | Ω |
| **OUTPUT STAGE (Channel 1 and Channel 2)** | | | | | | |
| $r_{DS(on)}$ (3) | MOSFET on-resistance plus bond-wire resistance | $T_A$ = 25°C, $V_{PVDD2}$ = 8 V | | 85 | | mΩ |
| | | –40°C < $T_A$ < 125°C, $V_{PVDD2}$ = 8 V | | 85 | 165 | mΩ |
| $t_{ON(min)}$ (3) | Minimum controllable pulse duration | $I_{SWx}$ peak current > 1 A (4) | | 100 | 200 | ns |
| $D_{MIN}$ | Minimum duty cycle | $V_{FB}$ = 0.9 V | | | 0% | |
| $D_{MAX}$ | Maximum duty cycle | $f_{SW}$ = 600 kHz | 85% | 90% | | |
| $I_{SW}$ | Switching-node leakage current (sourcing) | Outputs OFF | | 2 | 12 | µA |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SD}$ (3) | Shutdown temperature | | | 148 | | °C |
| $T_{SD(hys)}$ (3) | Hysteresis | | | 20 | | °C |

(3) Ensured by design. Not production tested.
(4) See Figure 14 for $I_{SWx}$ peak current <1 A.

## TYPICAL CHARACTERISTICS

**QUIESCENT CURRENT (NON-SWITCHING) vs JUNCTION TEMPERATURE**

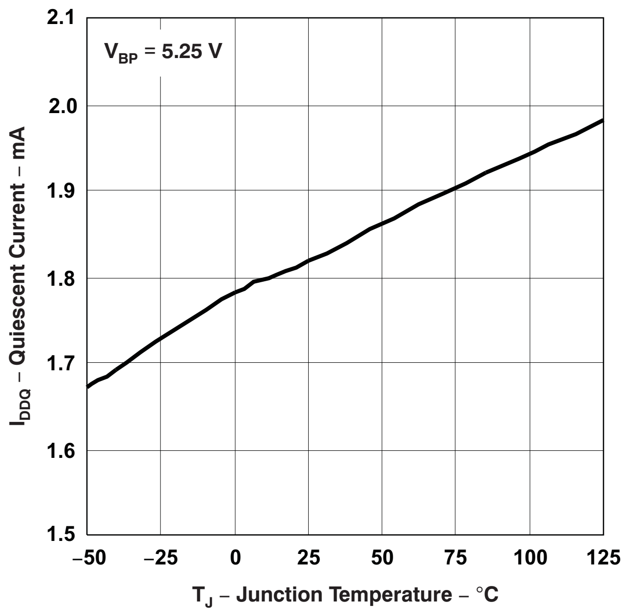



Figure 1.

**SHUTDOWN CURRENT vs JUNCTION TEMPERATURE**

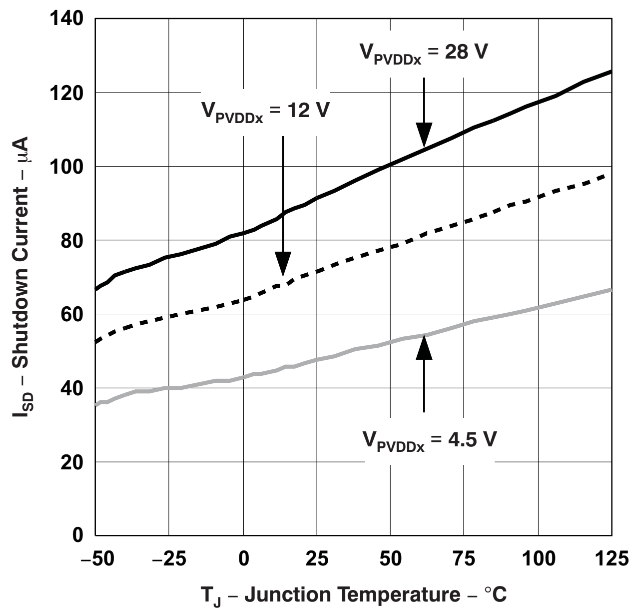



Figure 2.

**UNDERVOLTAGE LOCKOUT THRESHOLD vs JUNCTION TEMPERATURE**

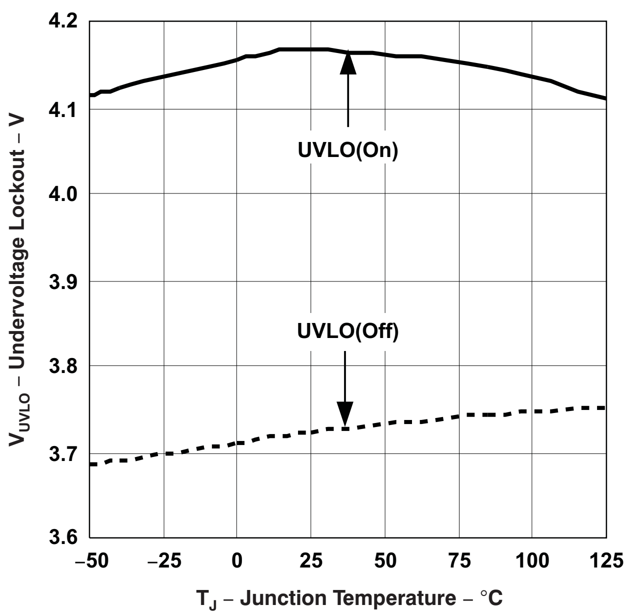



Figure 3.

**ENABLE THRESHOLDS vs JUNCTION TEMPERATURE**

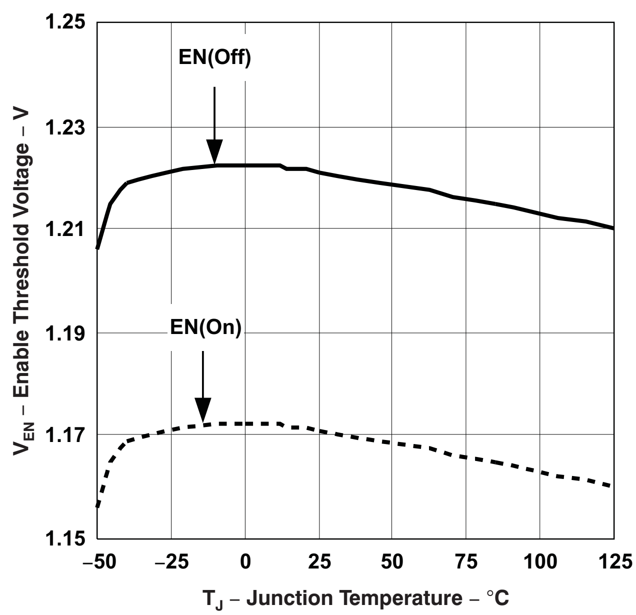



Figure 4.

## TYPICAL CHARACTERISTICS (continued)

**SOFT-START TIME vs JUNCTION TEMPERATURE**

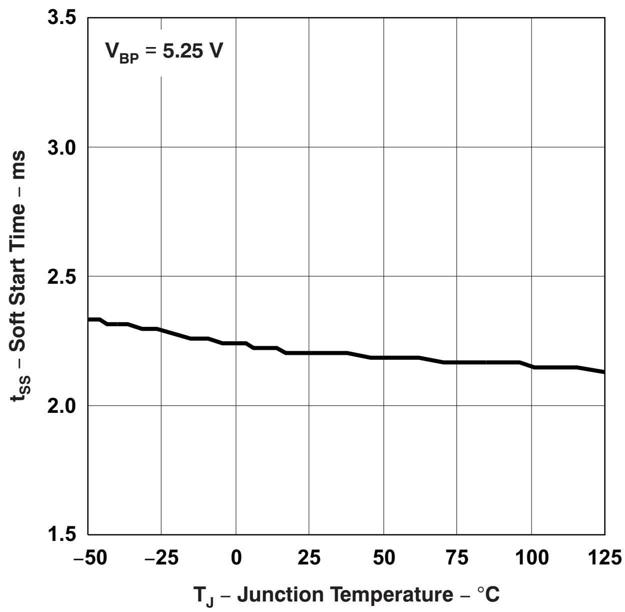



Figure 5.

**SWITCHING FREQUENCY (300 kHz) vs JUNCTION TEMPERATURE**

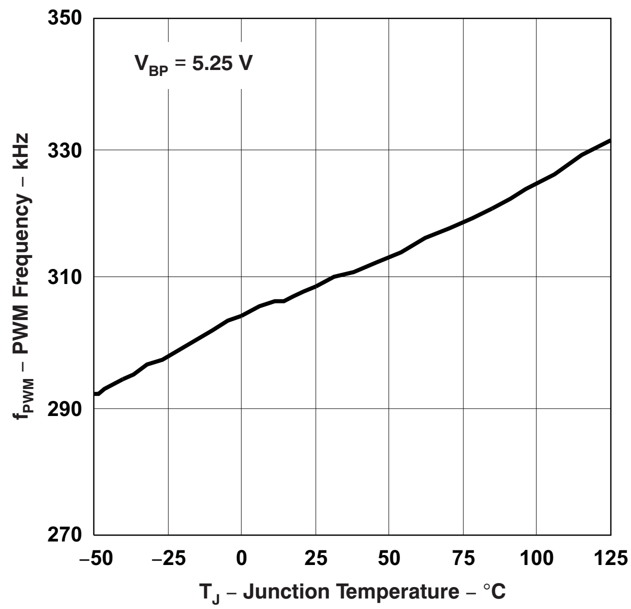



Figure 6.

**SWITCHING FREQUENCY (600 kHz) vs JUNCTION TEMPERATURE**

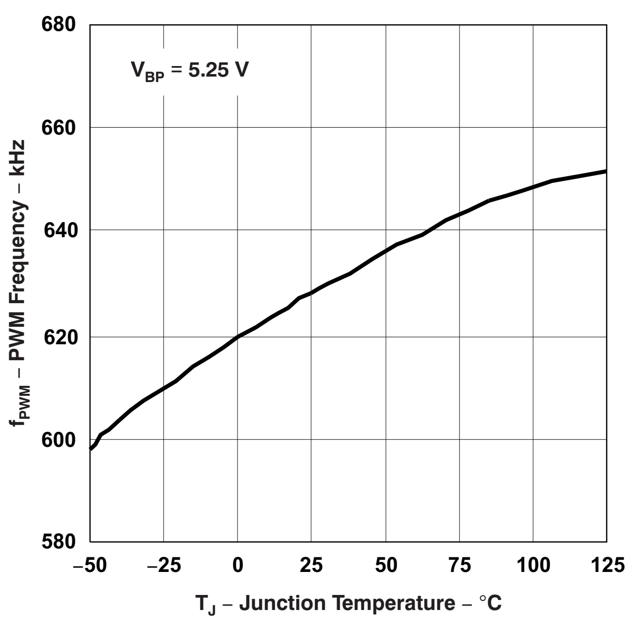



Figure 7.

**FEEDBACK BIAS CURRENT vs JUNCTION TEMPERATURE**

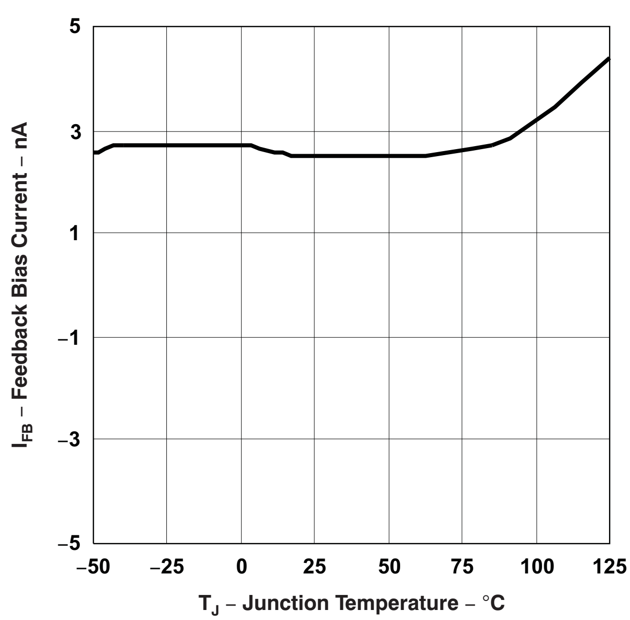



Figure 8.

## TYPICAL CHARACTERISTICS (continued)

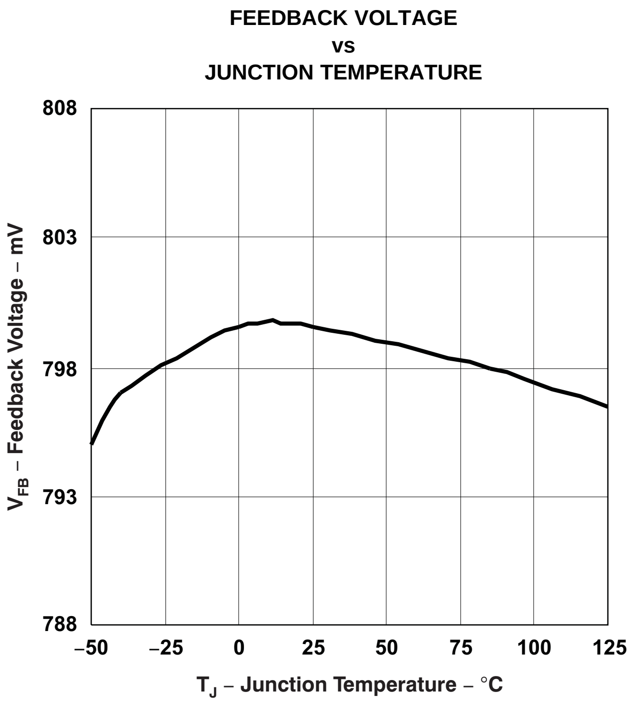



Figure 9.

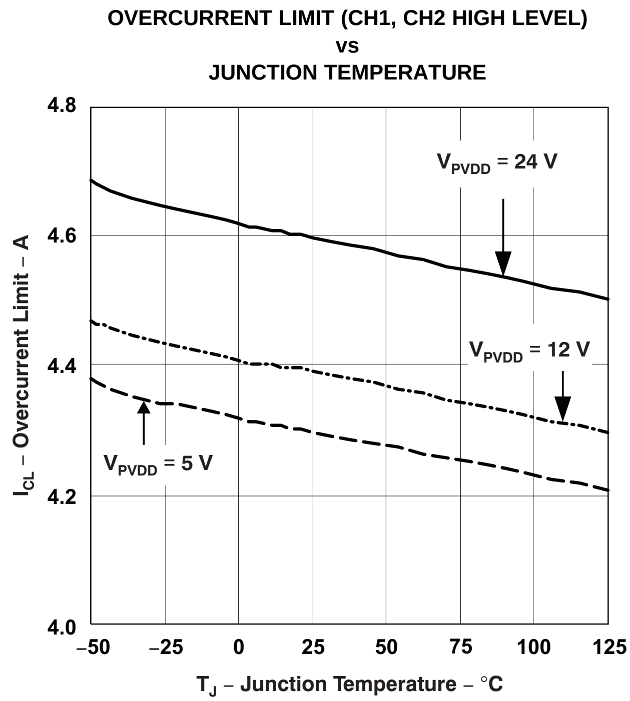



Figure 10.

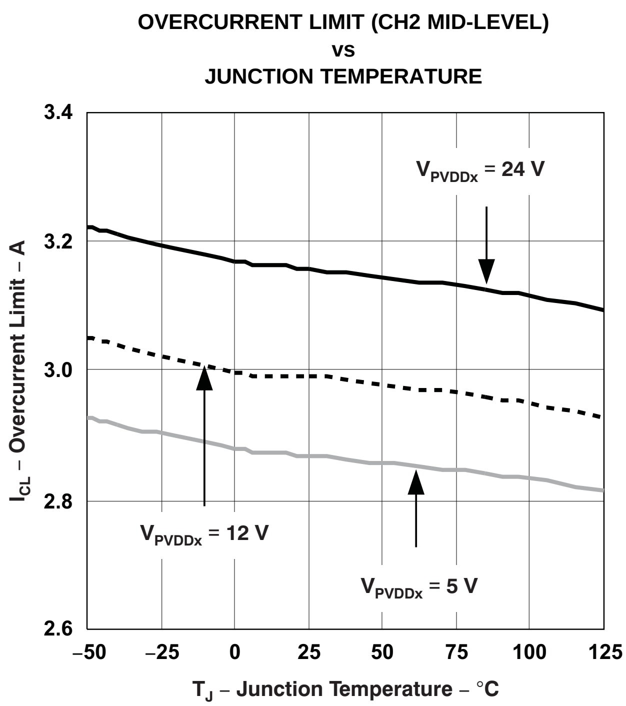



Figure 11.

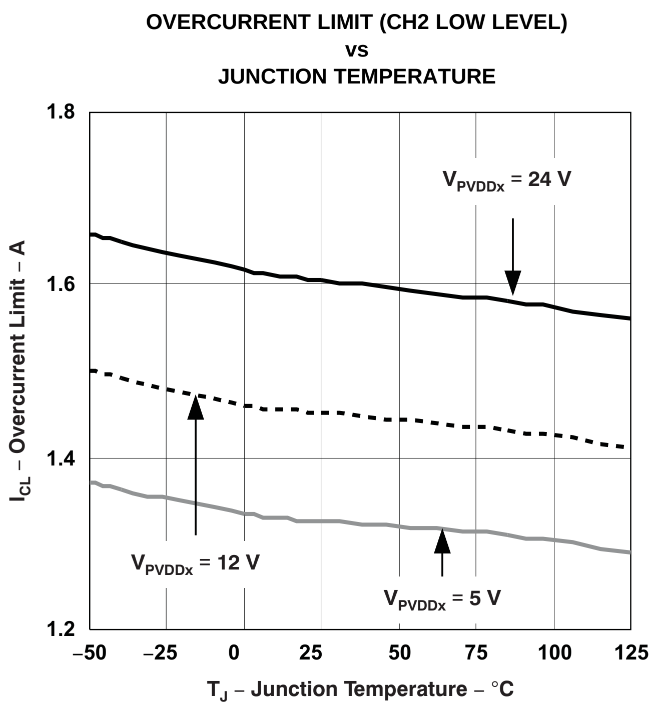



Figure 12.

## TYPICAL CHARACTERISTICS (continued)

SWITCHING NODE LEAKAGE CURRENT
vs
JUNCTION TEMPERATURE

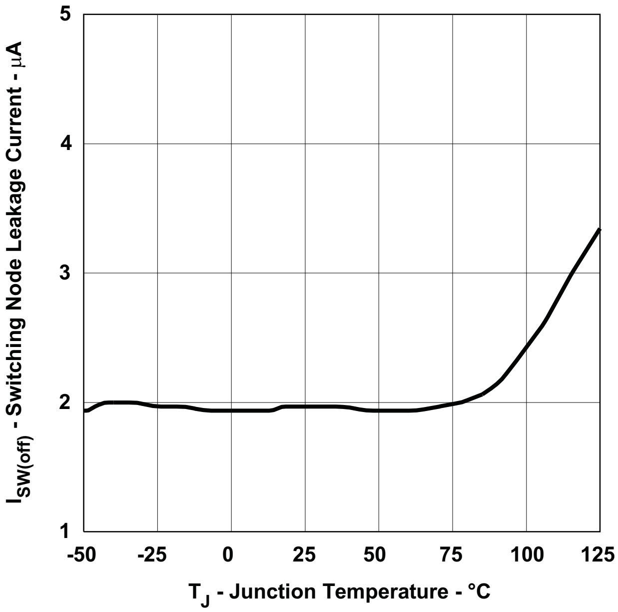



Figure 13.

MINUMUM CONTROLLABLE PULSE DURATION
vs
LOAD CURRENT

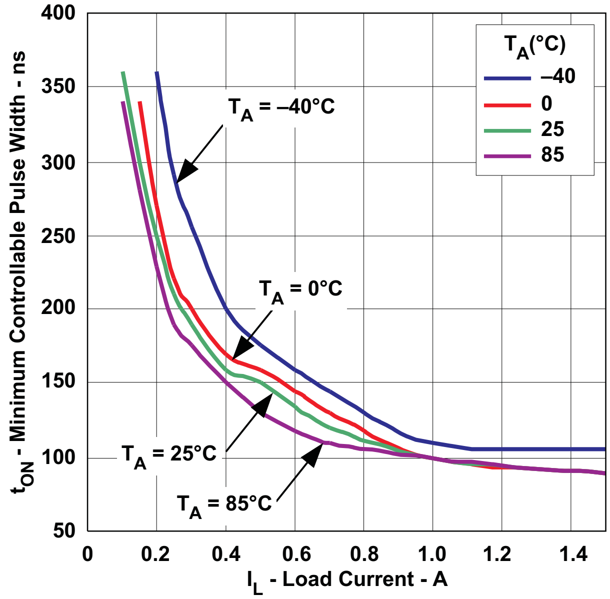



Figure 14.

OVERCURRENT LIMIT
vs
SUPPLY VOLTAGE

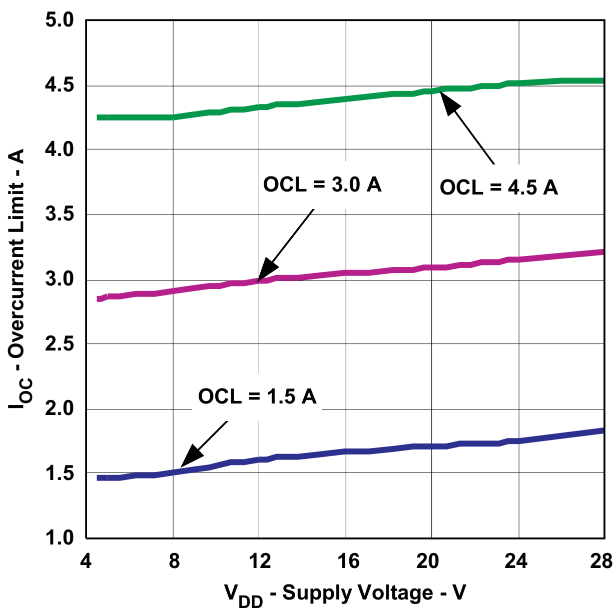
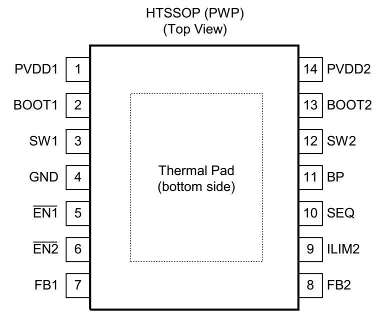



Figure 15.

# DEVICE INFORMATION

## PIN CONNECTIONS




### TERMINAL FUNCTIONS

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| BOOT1 | 2 | I | Input supply to the high-side gate driver for output 1. Connect a 22-nF to 82-nF capacitor from this pin to SW1. This capacitor is charged from the BP pin voltage through an internal switch. The switch is turned ON during the OFF time of the converter. To slow down the turn ON of the internal FET, a small resistor (1 Ω to 3 Ω) may be placed in series with the bootstrap capacitor. |
| BOOT2 | 13 | I | Input supply to the high-side gate driver for output 2. Connect a 22-nF to 82-nF capacitor from this pin to SW2. This capacitor is charged from the BP pin voltage through an internal switch. The switch is turned ON during the OFF time of the converter. To slow down the turn ON of the internal FET, a small resistor (1 Ω to 3 Ω) may be placed in series with the bootstrap capacitor. |
| BP | 11 | – | Regulated voltage to charge the bootstrap capacitors. Bypass this pin to GND with a low-ESR (4.7-µF to 10-µF X7R or X5R) ceramic capacitor. |
| $\overline{EN1}$ | 5 | I | Active-low enable input for output 1. If the voltage on this pin is greater than 1.55 V, output 1 is disabled (high-side switch is OFF). A voltage of less than 0.9 V enables output 1 and allows soft-start of output 1 to begin. An internal current source drives this pin to PVDD2 if left floating. Connect this pin to GND for *always ON* operation. |
| $\overline{EN2}$ | 6 | I | Active-low enable input for output 2. If the voltage on this pin is greater than 1.55 V, output 2 is disabled (high-side switch is OFF). A voltage of less than 0.9 V enables Output 2 and allows soft start of Output 2 to begin. An internal current source drives this pin to PVDD2 if left floating. Connect this pin to GND for *always ON* operation. |
| FB1 | 7 | I | Voltage feedback pin for output 1. The internal transconductance error amplifier adjusts the PWM for output 1 to regulate the voltage at this pin to the internal 0.8-V reference. A series resistor divider from output 1 to ground, with the center connection tied to this pin, determines the value of the regulated output voltage. Compensation for the feedback loop is provided internally to the device. See the Feedback Loop and Inductor-Capacitor ( L-C) Filter Selection section for further information. |
| FB2 | 8 | I | Voltage feedback pin for output 2. The internal transconductance error amplifier adjusts the PWM for output 2 to regulate the voltage at this pin to the internal 0.8-V reference. A series resistor divider from output 2 to ground, with the center connection tied to this pin, determines the value of the regulated output voltage. Compensation for the feedback loop is provided internally to the device. See the Feedback Loop and Inductor-Capacitor ( L-C) Filter Selection section for further information. |
| GND | 4 | – | Ground pin for the device. Connect directly to the thermal pad. |
| ILIM2 | 9 | I | Current limit adjust pin for output 2 only. This function is intended to allow a user with asymmetrical load currents (output 1 load current much greater than output 2 load current) to optimize component scaling of the lower-current output while maintaining proper component derating in a overcurrent fault condition. The discrete levels are available as shown in Table 3, *Current Limit Threshold Adjustment for Output 2*. Note: An internal 2-resistor divider (150-kΩ each) connects BP to ILIM2 and to GND. |
| PVDD1 | 1 | I | Power input to the output 1 high-side MOSFET only. This pin should be locally bypassed to GND with a low-ESR ceramic capacitor of 10-µF or greater. |
| PVDD2 | 14 | I | The PVDD2 pin provides power to the device control circuitry, provides the pull-up for the $\overline{EN1}$ and $\overline{EN2}$ pins and provides power to the output 2 high-side MOSFET. This pin should be locally bypassed to GND with a low-ESR ceramic capacitor of 10-µF or greater. The UVLO function monitors PVDD2 and enables the device when PVDD2 is greater than 4.1 V. |

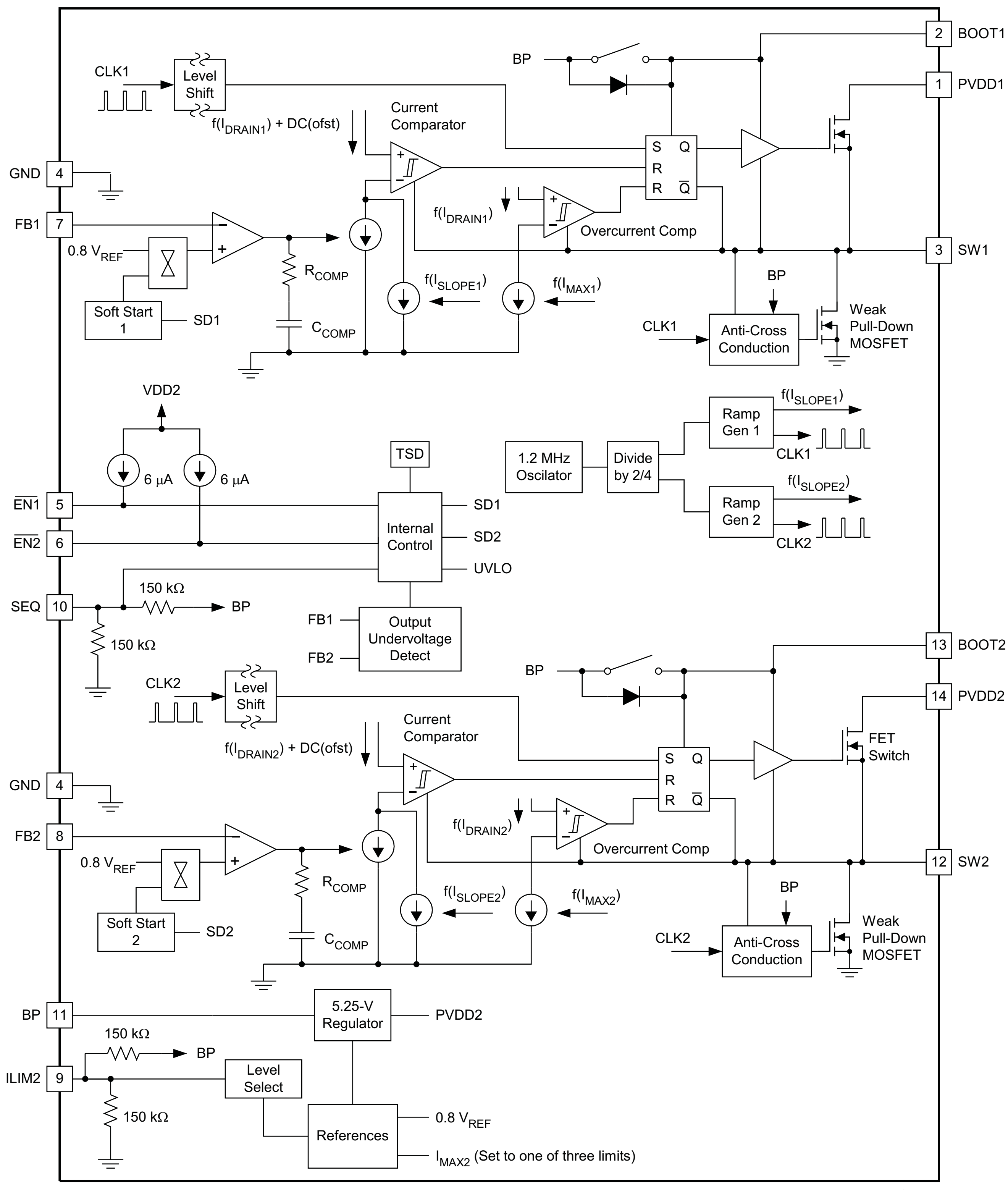
## TERMINAL FUNCTIONS (continued)

## TERMINAL FUNCTIONS (continued)

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| SEQ | 10 | I | This pin configures the output start-up mode. If the SEQ pin is connected to BP, then when output 2 is enabled, output 1 is allowed to start after output 2 has reached regulation; that is, sequential startup where output 1 is slave to output 2. If EN2 is allowed to go high after the outputs have been operating, then both outputs are disabled immediately, and the output voltages decay according to the load that is present. For this sequence configuration, tie EN1 to ground.<br>If the SEQ pin is connected to GND, then when output 1 is enabled, output 2 is allowed to start after output 1 has reached regulation; that is, sequential start-up where output 2 is slave to output 1. If EN1 is allowed to go high after the outputs have been operating, then both outputs are disabled immediately, and the output voltages decay according to the load that is present. For this sequence configuration, tie EN2 to ground.<br>If left floating, output 1 and output 2 start ratiometrically when both outputs are enabled at the same time. They soft-start at a rate determined by their final output voltage and enter regulation at the same time. If the EN1 and EN2 pins are allowed to operate independently, then the two outputs also operate independently.<br>NOTE: An internal two-resistor (150-kΩ each) divider connects BP to SEQ and to GND. See the Sequence States table. |
| SW1 | 3 | O | Source (switching) output for output 1 PWM. A snubber is recommended to reduce ringing on this node. See SW Node Ringing for further information. |
| SW2 | 12 | O | Source (switching) output for output 2 PWM. A snubber is recommended to reduce ringing on this node. See SW Node Ringing for further information. |
| Thermal pad | – | – | This pad must be tied externally to a ground plane and the GND pin. |

## BLOCK DIAGRAM



# APPLICATION INFORMATION

## FUNCTIONAL DESCRIPTION

The TPS54386-Q1 is a dual-output, non-synchronous converter. Each PWM channel contains an internally compensated error amplifier, current-mode pulse-width modulator (PWM), switch MOSFET, enable, and fault-protection circuitry. Common to the two channels are the internal voltage regulator, voltage reference, clock oscillator, and output-voltage sequencing functions.

**DESIGN HINT**

The TPS54386-Q1 contains internal slope compensation and loop compensation components; therefore, the external L-C filter must be selected appropriately so that the resulting control loop meets criteria for stability. This approach differs from an externally-compensated controller, where the L-C filter is generally selected first, and the compensation network is found afterwards. (See the *Feedback Loop and L-C Filter Selection* section.)

**NOTE**

Unless otherwise noted, a label with a lowercase *x* appended implies the term applies to both outputs of the two modulator channels. For example, the term *ENx* implies both $\overline{EN1}$ and $\overline{EN2}$. Unless otherwise noted, all parametric values given are typical. See the *Electrical Characteristics* for minimum and maximum values. Calculations should be performed with tolerance values taken into consideration.

### Voltage Reference

The band-gap cell common to both outputs, trimmed to 800 mV.

### Oscillator

The oscillator frequency is internally fixed at two times the SWx node switching frequency. The two outputs are internally configured to operate on alternating switch cycles (that is, 180° out of phase).

### Input Undervoltage Lockout (UVLO) and Startup

When the voltage at the PVDD2 pin is less than 4.1 V, a portion of the internal bias circuitry is operational, and all other functions are held OFF. All of the internal MOSFETs are also held OFF. When the PVDD2 voltage rises above the UVLO turnon threshold, the state of the enable pins determines the remainder of the internal start-up sequence. If either output is enabled ($\overline{ENx}$ pulled low), the BP regulator turns on, charging the BP capacitor with a 20-mA current. When the BP pin is greater than 4 V, PWM is enabled and soft-start begins, depending on the SEQ mode of operation and the $\overline{EN1}$ and $\overline{EN2}$ settings.

Note that the internal regulator and control circuitry are powered from PVDD2. The voltage on PVDD1 may be higher or lower than PVDD2. (See the *Dual Supply Operation* section.)

### Enable and Timed Turnon of the Outputs

Each output has a dedicated (active-low) enable pin. If left floating, an internal current source pulls the pin to PVDD2. By grounding, or by pulling the $\overline{ENx}$ pin to below approximately 1.2 V with an external circuit, the associated output is enabled and soft-start is initiated.

If both enable pins are left in the *high* state, the device operates in a shutdown mode, where the BP regulator is shut down and minimal functions are active. The total standby current from both PVDD pins is approximately 70 µA at the 12-V input supply.

An R-C circuit connected to an $\overline{ENx}$ pin may be used to delay the turnon of the associated output after power is applied to PVDDx (see Figure 16). After power is applied to PVDD2, the voltage on the $\overline{ENx}$ pin slowly decays towards ground. Once the voltage decays to approximately 1.2 V, then the output is enabled and the startup sequence begins. If it is desired to enable the outputs of the device immediately upon the application of power to PVDD2, then omit these two components and tie the $\overline{ENx}$ pin to GND directly.

If an R-C circuit is used to delay the turnon of the output, the resistor value must be much less than 1.2 V / 6 µA or 200 kΩ. A suggested value is 51 kΩ. This resistor value allows the $\overline{ENx}$ voltage to decay below the 1.2-V threshold while the 6-µA bias current flows.

The capacitor value required to delay the start-up time (after the application of PVDD2) is shown in Equation 1.

$$C = \frac{t_{DELAY}}{R \times \ell n\left(\frac{V_{IN} - 2 \times I_{ENx} \times R}{V_{TH} - I_{ENx} \times R}\right)} \text{ farads} \quad (1)$$

where:

- R and C are the timing components.
- $V_{TH}$ is the 1.2-V enable threshold voltage.
- $I_{\overline{ENx}}$ is the 6-µA enable-pin biasing current.

Other enable-pin functionality is dictated by the state of the SEQ pin. (See the *Output Voltage Sequencing* section.)

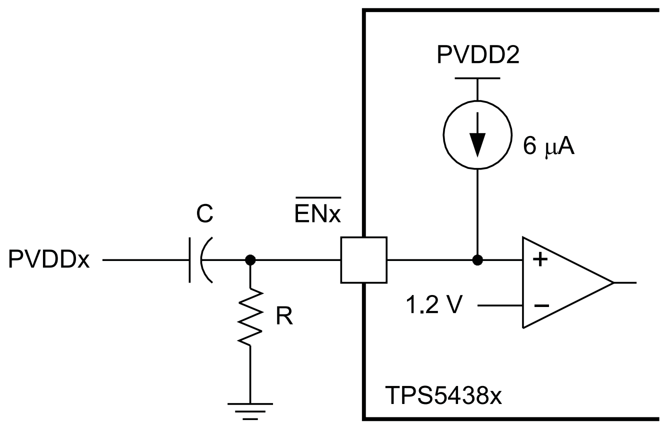



**Figure 16. Start-Up Delay Schematic**

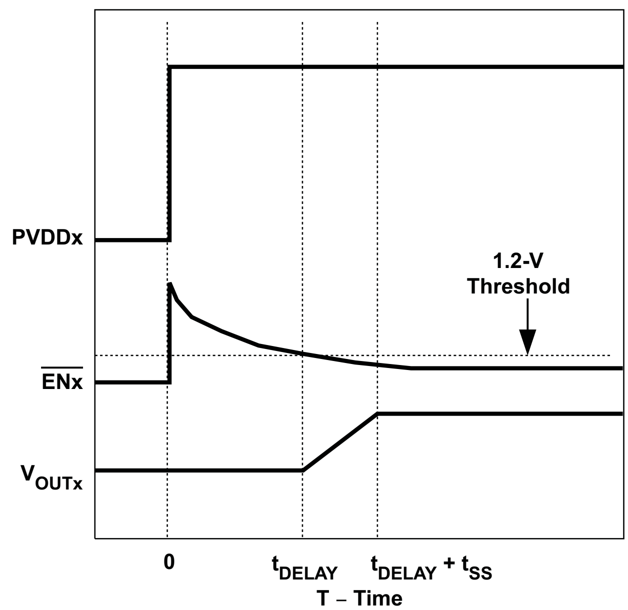



**Figure 17. Start-Up Delay With R-C on Enable**

---

**DESIGN HINT**

If delayed output-voltage start-up is not necessary, simply connect $\overline{EN1}$ and $\overline{EN2}$ to GND. This configuration allows the outputs to start immediately on valid application of PVDD2.

---

If $\overline{ENx}$ is allowed to go *high* after output x has been in regulation, the upper MOSFET shuts off, and the output decays at a rate determined by the output capacitor and the load. The internal pulldown MOSFET remains in the OFF state. (See the *Bootstrap for N-Channel MOSFET* section.)

## Output-Voltage Sequencing

The TPS54386-Q1 allows single-pin programming of output-voltage start-up sequencing. During power on, the state of the SEQ pin is detected. Based on whether the pin is tied to BP, to GND, or left floating, the outputs behave as described in Table 2.

**Table 2. Sequence States**

| SEQ PIN STATE | MODE | $\overline{EN1}$ | $\overline{EN2}$ |
|---|---|---|---|
| BP | Sequential, output 2 then output 1 | Ignored by the device.when $V_{\overline{EN2}}$ < enable threshold voltage<br>Tie $\overline{EN1}$ to < enable threshold voltage for BP to be active when $V_{\overline{EN2}}$ > enable threshold voltage<br>Tie $\overline{EN1}$ to > enable threshold voltage for low quiescent current (BP inactive) when $V_{\overline{EN2}}$ > enable threshold voltage | Active |
| GND | Sequential, output 1 then output 2 | Active | Ignored by the device.when $V_{\overline{EN1}}$ < enable threshold voltage<br>Tie $\overline{EN2}$ to < enable threshold voltage for BP to be active when $V_{\overline{EN1}}$ > enable threshold voltage<br>Tie $\overline{EN2}$ to > enable threshold voltage for low quiescent current (BP inactive) when $V_{\overline{EN1}}$ > enable threshold voltage |
| (floating) | Independent or ratiometric, output 1 and output 2 | Active. $\overline{EN1}$ and $\overline{EN2}$ must be tied together for Ratio-metric startup. | Active. $\overline{EN1}$ and $\overline{EN2}$ must be tied together for ratiometric start-up. |

If the SEQ pin is connected to BP, then when output 2 is enabled, output 1 is allowed to start approximately 400 µs after output 2 has reached regulation; that is, sequential start-up where output 1 is slave to output 2. If $\overline{EN2}$ is allowed to go high after the outputs have been operating, then both outputs are disabled immediately, and the output voltages decay according to the load that is present.

If the SEQ pin is connected to GND, then when output 1 is enabled, output 2 is allowed to start approximately 400 µs after output 1 has reached regulation; that is, sequential start-up where output 2 is slave to output 1. If $\overline{EN1}$ is allowed to go high after the outputs have been operating, then both outputs are disabled immediately, and the output voltages decay according to the load that is present.

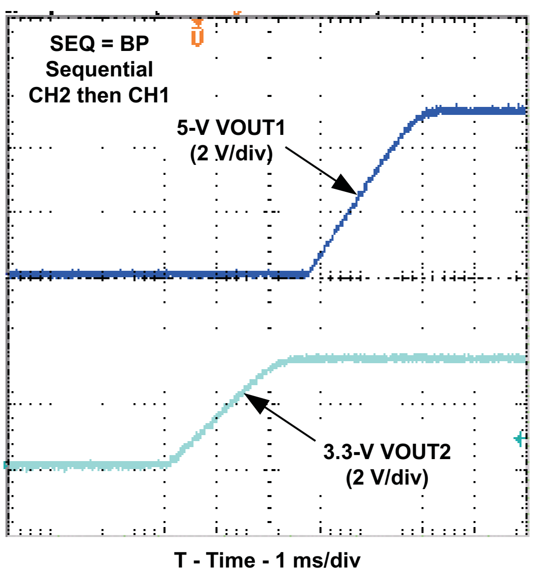



**Figure 18. SEQ Pin Tied to BP**

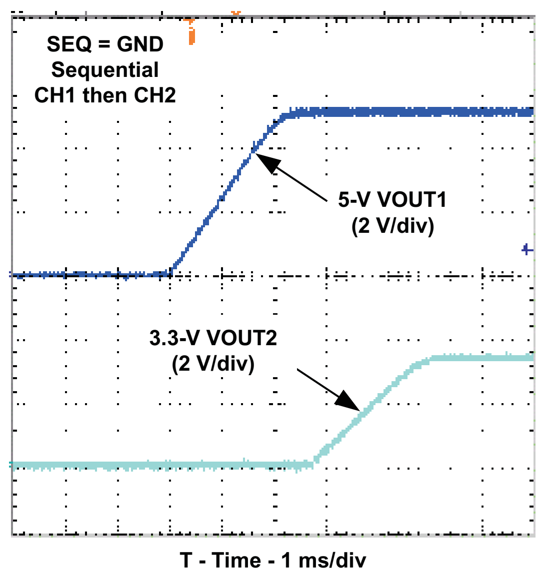



**Figure 19. SEQ Pin Tied to GND**

**NOTE**

An R-C network connected to the $\overline{ENx}$ pin may be used in addition to the SEQ pin in sequential mode to delay the start-up of the first output voltage. This approach may be necessary in systems with a large number of output voltages and elaborate voltage-sequencing requirements. See *Enable and Timed Turn On of the Outputs*.

If the SEQ pin is left floating, output 1 and output 2 each start ratiometrically when both outputs are enabled at the same time. Output 1 and output 2 soft-start at a rate that is determined by the respective final output voltages and enter regulation at the same time. If the $\overline{EN1}$ and $\overline{EN2}$ pins are allowed to operate independently, then the two outputs also operate independently.

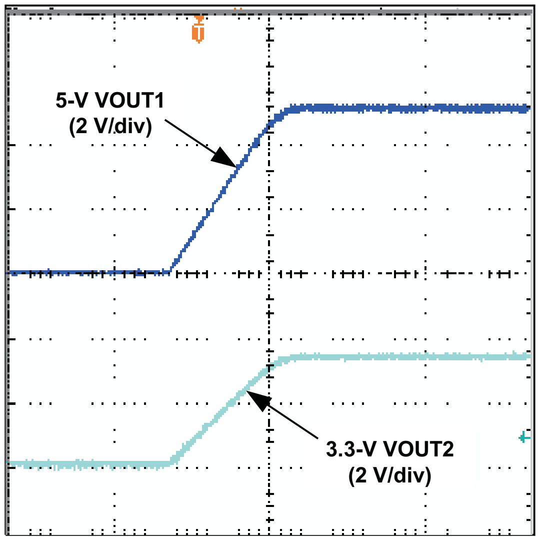



**Figure 20. SEQ Pin Floating**

### Soft Start

Each output has a dedicated soft-start circuit. The soft-start voltage is an internal digital reference ramp to one of two noninverting inputs of the error amplifier. The other input is the (internal) precision 0.8-V reference. The total ramp time for the FB voltage to charge from 0 V to 0.8 V is about 2.1 ms. During a soft-start interval, the TPS54386-Q1 output slowly increases the voltage to the noninverting input of the error amplifier. In this way, the output voltage ramps up slowly until the voltage on the noninverting input to the error amplifier reaches the internal 0.8-V reference voltage. At that time, the voltage at the noninverting input to the error amplifier remains at the reference voltage.

**NOTE**

To avoid a disturbance in the output voltage during the stepping of the digital soft-start, a minimum output capacitance of 50 μF is recommended. See *Feedback Loop and Inductor-Capacitor (L-C) Filter Selection*. Once the filter and compensation components have been established, laboratory measurements of the physical design should be performed to confirm converter stability.

During the soft-start interval, pulse-by-pulse current limiting is in effect. If an overcurrent pulse is detected, six PWM pulses are skipped to allow the inductor current to decay before another PWM pulse is applied. (See the *Output Overload Protection* section.) There is no pulse-skipping if a current-limit pulse is not detected.

**DESIGN HINT**

If the rate of rise of the input voltage (PVDDx) is such that the input voltage is too low to support the desired regulation voltage by the time soft-start has completed, then the output UV circuit may trip and cause a *hiccup* in the output voltage. In this case, use a timed-delay start-up from the $\overline{ENx}$ pin to delay the start-up of the output until the PVDDx voltage has the capability of supporting the desired regulation voltage. See *Operating Near Maximum Duty Cycle* and *Maximum Output Capacitance* for related information.

### Output Voltage Regulation

Each output has a dedicated feedback loop comprising a voltage-setting divider, an error amplifier, a pulse-width modulator, and a switching MOSFET. The regulation output voltage is determined by a resistor divider connecting the output node, the FBx pin, and GND (see Figure 21). Assuming the value of the upper resistor of the voltage-setting divider is known, the value of the lower divider resistor for a desired output voltage is calculated by Equation 2.

$$R2 = R1 \times \left( \frac{V_{REF}}{V_{OUT} - V_{REF}} \right) \quad (2)$$

where

- $V_{REF}$ is the internal 0.8-V reference voltage.

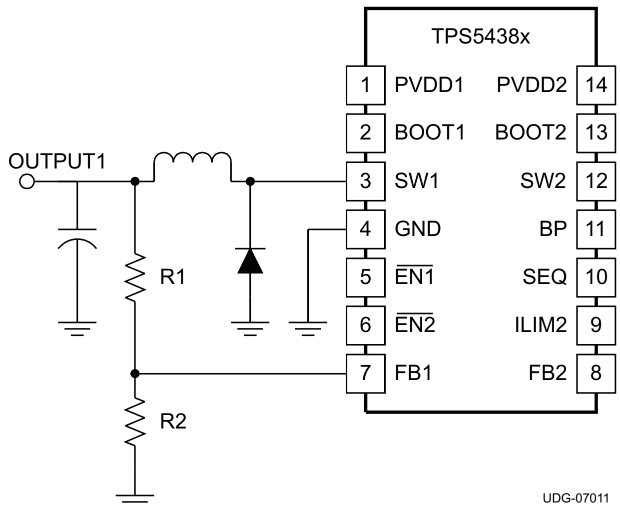



**Figure 21. Feedback Network for Channel 1**

---

**DESIGN HINT**

There is a leakage current of up to 12 µA out of the SW pin when a single output of the TPS54386-Q1 is disabled. Keeping the series impedance of R1 + R2 less than 50 kΩ prevents the output from floating above the reference voltage while the controller output is in the OFF state.

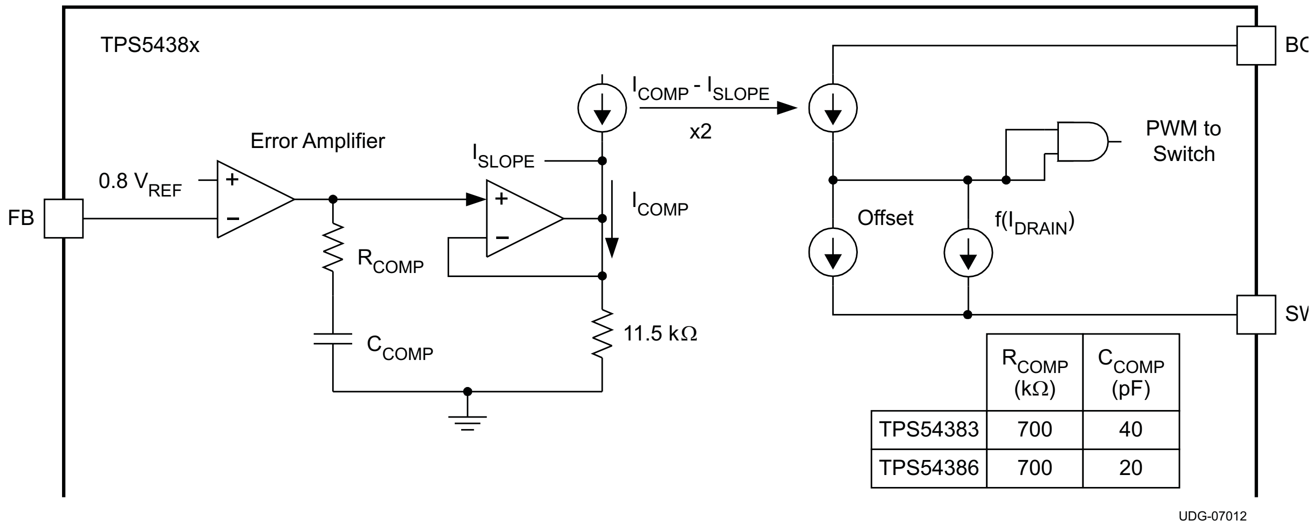
---

### Feedback Loop and Inductor-Capacitor (L-C) Filter Selection

In the feedback signal path, the output voltage-setting divider is followed by an internal $g_M$-type error amplifier with a typical transconductance of 30 μs. An internal series-connected R-C circuit from the $g_M$ amplifier output to ground serves as the compensation network for the converter. The signal from the error amplifier output is then buffered and combined with a slope compensation signal before it is mirrored to be referenced to the SW node. Here, it is compared with the current feedback signal to create a pulse-width-modulated (PWM) signal to drive the upper MOSFET switch. A simplified equivalent circuit of the signal control path is depicted in Figure 22.

**NOTE**

Noise coupling from the SWx node to internal circuitry of BOOTx may impact narrow pulse-width operation, especially at load currents less than 1 A. See SW Node Ringing for further information on reducing noise on the SWx node.




| | $R_{COMP}$ (kΩ) | $C_{COMP}$ (pF) |
|---|---|---|
| TPS54383 | 700 | 40 |
| TPS54386 | 700 | 20 |

**Figure 22. Feedback-Loop Equivalent Circuit**

A more conventional small-signal equivalent block diagram is shown in Figure 23. Here, the full closed-loop signal path is shown. Because the TPS54386-Q1 contains internal slope-compensation and loop-compensation components, the external L-C filter must be selected appropriately so that the resulting control loop meets criteria for stability. This approach differs from an externally-compensated controller, where the L-C filter is generally selected first, and the compensation network is found afterwards. To find the appropriate L and C filter combination, the output-to-Vc signal path plots (see the next section) of gain and phase are used along with other design criteria to aid in finding the combination that best results in a stable feedback loop.

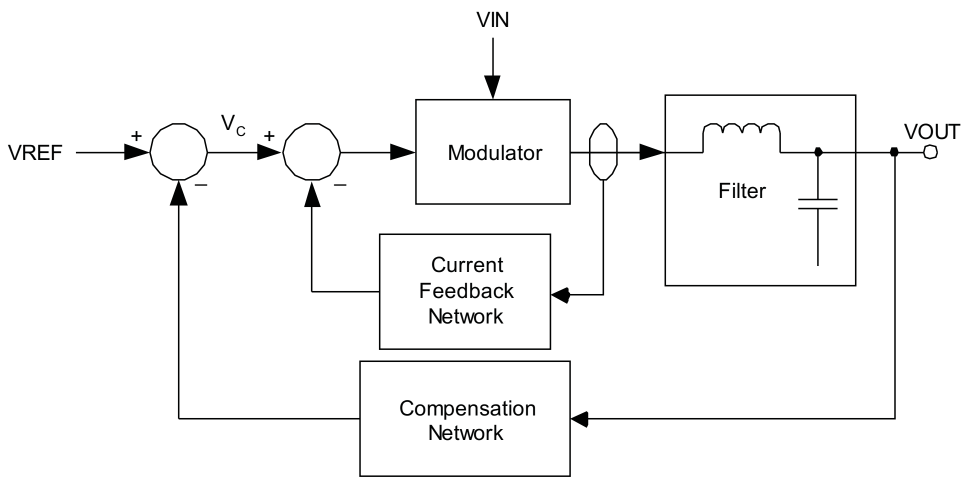



**Figure 23. Small-Signal Equivalent Block Diagram**

## Inductor-Capacitor (L-C) Selection

The following figures plot the TPS54386-Q1 output-to-Vc gain and phase versus frequency for various duty cycles (10%, 30%, 50%, 70%, 90%) at three (200 mA, 400 mA, 600 mA) peak-to-peak ripple-current levels. The loop response curve selected to compensate the loop is based on the duty cycle of the application and the ripple current in the inductor. Once the curve has been selected and the inductor value has been calculated, the output capacitor is found by calculating the L-C resonant frequency required to compensate the feedback loop. A brief example follows the curves.

Note that the internal error-amplifier compensation is optimized for output capacitors with an ESR zero frequency between 20 kHz and 60 kHz. See the following sections for further details.

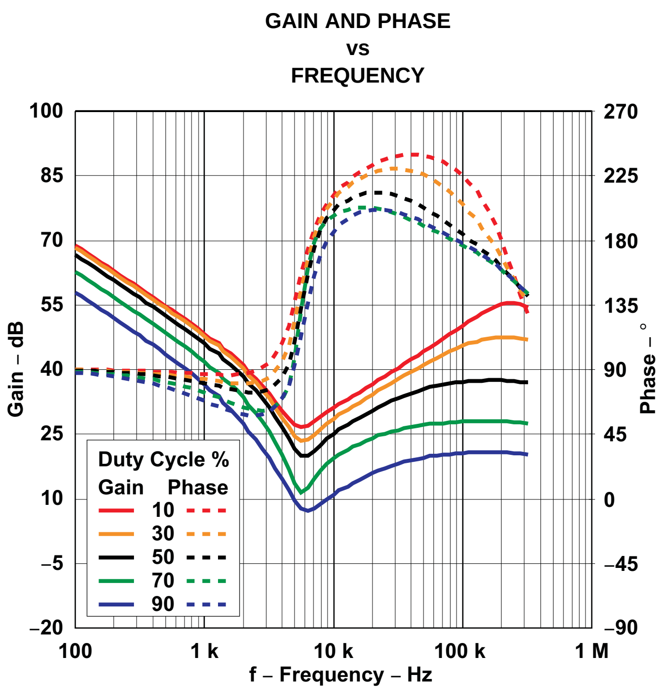



**Figure 24. TPS54386-Q1 at 200-mApp Ripple Current**

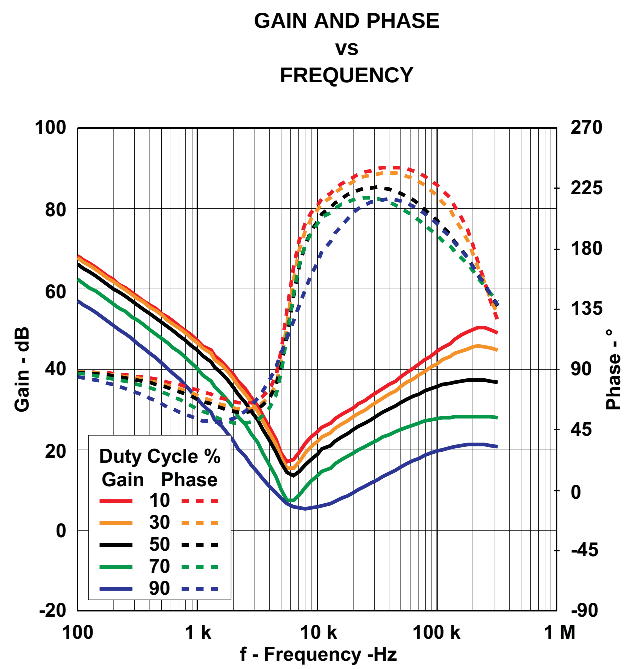



**Figure 25. TPS54386-Q1 at 400-mApp Ripple Current**

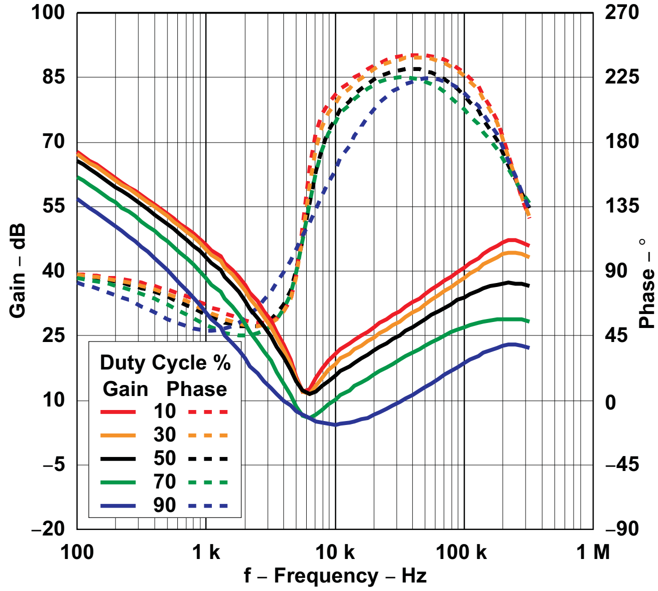



**Figure 26. TPS54386-Q1 at 600-mApp Ripple Current**

### Maximum Output Capacitance

With internal pulse-by-pulse current limiting and a fixed soft-start time, there is a maximum output capacitance which may be used before start-up problems begin to occur. If the output capacitance is large enough so that the device enters a current-limit protection mode during startup, then there is a possibility that the output will never reach regulation. Instead, the TPS54386-Q1 simply shuts down and attempts a restart as if the output were short-circuited to ground. The maximum output capacitance (including bypass capacitance distributed at the load) is given by Equation 3:

$$C_{OUTmax} = \frac{t_{SS}}{V_{REF}}\left[I_{CLx} - V_{REF}\left(1 + \frac{R1}{R2}\right)\left(1 - \frac{V_{REF}\left(1 + \frac{R1}{R2}\right) \times T_S}{2 \times V_{IN} \times L} + \frac{1}{R_{LOAD}}\right)\right] \quad (3)$$

### Minimum Output Capacitance

Ensure the value of capacitance selected for closed-loop stability is compatible with the requirements of *Soft Start*.

### Modifying The Feedback Loop

Within the limits of the internal compensation, there is flexibility in the selection of the inductor and output-capacitor values. A smaller inductor increases ripple current, and raises the resonant frequency, thereby incerasing the required amount of output capacitance. A smaller capacitor could also be used, increasing the resonant frequency, and increasing the overall loop bandwidth—perhaps at the expense of adequate phase margin.

The internal compensation of the TPS54x8x is designed for capacitors with an ESR zero frequency between 20 kHz and 60 kHz. It is possible, with additional feedback compensation components, to use capacitors with higher or lower ESR zero frequencies. For either case, the components C1 and R3 (see Figure 30) are added to re-compensate the feedback loop for stability. In this configuration, a low frequency pole is followed by a higher-frequency zero. The placement of this pole-zero pair is dependent on the type of output capacitor used and the desired closed-loop frequency response.

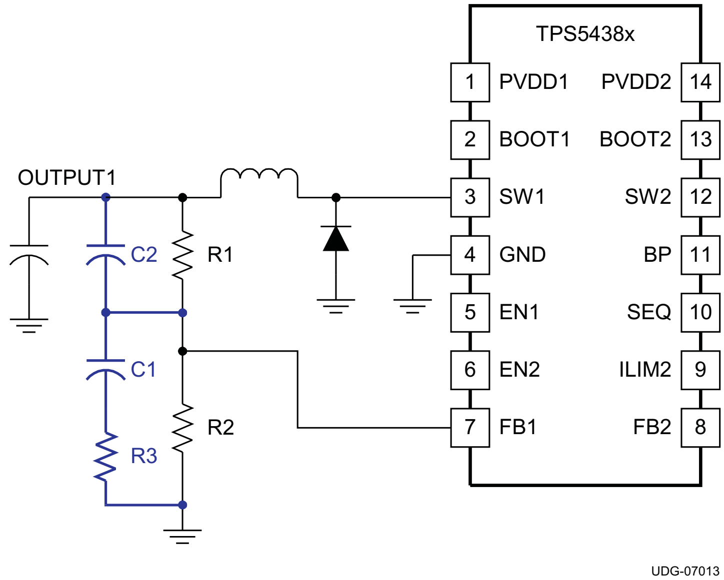



**Figure 27. Optional Loop Compensation Components**

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**NOTE**

Once the filter and compensation components have been established, laboratory measurements of the physical design should be performed to confirm converter stability.

---

### *Using High-ESR Output Capacitors*

If a high-ESR capacitor is used in the output filter, a zero appears in the loop response that could lead to instability. To compensate, a small R-C series connected network is placed in parallel with the lower voltage-setting divider resistor (see Figure 27). The values of the components are determined such that a pole is placed at the same frequency as the ESR zero and a new zero is placed at a frequency location conducive to good loop stability.

The value of the resistor is calculated using a ratio of impedances to match the ratio of ESR zero frequency to the desired zero frequency.

$$R3 = \frac{R2}{\left(\left(\frac{f_{ZERO(desired)}}{f_{ESR(zero)}}\right) - 1\right)}$$

where:

- $f_{ESR(zero)}$ is the ESR zero frequency of the output capacitor.
- $f_{ZERO(desired)}$ is the desired frequency of the zero added to the feedback. This frequency should be placed between 20 kHz and 60 kHz to ensure good loop stability. (4)

The value of the capacitor is calculated in Equation 5.

$$C1 = \frac{1}{2\pi \times R_{EQ} \times f_{ESR(zero)}}$$

where:

- $R_{EQ}$ is an equivalent impedance created by the parallel combination of the voltage-setting divider resistors (R1 and R2) in series with R3. (5)

$$R_{EQ} = R3 + \frac{1}{\left(\left(\frac{1}{R1}\right) + \left(\frac{1}{R2}\right)\right)} \tag{6}$$

### Using All Ceramic Output Capacitors

With low-ESR ceramic capacitors, there may not be enough phase margin at the crossover frequency. In this case (see Figure 27), resistor R3 is set equal to 1/2 R2. This lowers the gain by 6 dB, reduces the crossover frequency, and improves phase margin.

The value of C1 is found by determining the frequency at which to place the low-frequency pole. The minimum frequency at which to place the pole is 1 kHz. Any lower, and the time constant will be too slow and interfere with the internal soft-start (see Soft Start). The upper bound for the pole frequency is determined by the operating frequency of the converter. It is 3 kHz for the TPS54x83, and 6 kHz for the TPS54x86. C1 is then found from Equation 7. Keep component tolerances in mind when selecting the desired pole frequency.

$$C1 = \frac{1}{2\pi \times R_{EQ} \times f_{POLE(desired)}}$$

where:

- $f_{POLE(desired)}$ is the desired pole frequency between 1 kHz and 3 kHz (TPS54x83) or 1 kHz and 6 kHz (TPS54x86).
- $R_{EQ}$ is an equivalent impedance created by the parallel combination of the voltage-setting divider resistors (R1 and R2) in series with R3. (7)

$$R_{EQ} = R3 + \frac{1}{\left(\left(\frac{1}{R1}\right) + \left(\frac{1}{R2}\right)\right)} \tag{8}$$

If it is necessary to increase phase margin, place a capacitor in parallel with the upper voltage-setting divider resistor (C2 in Equation 9).

$$C2 = \frac{1}{2\pi \times f_C \times R1} \times \sqrt{1 + \frac{R1}{\left(\frac{(R2 \times R3)}{(R2 + R3)}\right)}}$$

where

- $f_C$ is the unity-gain crossover frequency, (approximately 50 kHz for most designs following these guidelines). (9)

### Example: TPS54386-Q1 Buck Converter Operating at 12-V Input, 3.3-V Output and 400-mA$_{(P-P)}$ Ripple Current

First, the steady-state duty cycle is calculated. Assuming the rectifier diode has a voltage drop of 0.5 V, the duty cycle is approximated using Equation 10.

$$\delta = \frac{V_{OUT} + V_{DIODE}}{V_{IN} + V_{DIODE}} = \frac{3.3 + 0.5}{12 + 0.5} = 30\% \tag{10}$$

The filter inductor is then calculated; see Equation 11.

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I_L} \times \delta \times T_S = \frac{12 - 3.3}{0.4} \times 0.3 \times \frac{1}{600000} = 10.9\,\mu H \tag{11}$$

A custom-designed inductor may be used for the application, or a standard value close to the calculated value may be used. For this example, a standard 10-µH inductor is used. Using Figure 25, find the 30% duty cycle curve. The 30% duty cycle curve has a down slope from low frequency and rises at approximately 6 kHz. This curve is the resonant frequency that must be compensated. Any frequency within an octave of the peak may be used in calculating the capacitor value. In this example, 6 kHz is used.

$$C = \frac{1}{L \times (2 \times \pi \times f_{RES})^2} = \frac{1}{10 \times 10^{-6} \times (2 \times 3.14 \times 6000)^2} = 70\,\mu F \tag{12}$$

A 68-µF capacitor should be used as a bulk capacitor, with up to 10 µF of ceramic bypass capacitance. To ensure the ESR zero does not significantly impact the loop response, the ESR of the bulk capacitor should be placed a decade above the resonant frequency.

$$R_{ESR} < \frac{1}{2 \times \pi \times 10 \times f_{RES} \times C} = \frac{1}{2 \times 3.14 \times 10 \times 6000 \times 68 \times (10)^{-6}} \approx 40\ m\Omega \tag{13}$$

The resulting loop gain and phase are shown in Figure 28. Based on measurement, loop crossover is 45 kHz with a phase margin of 60 degrees.

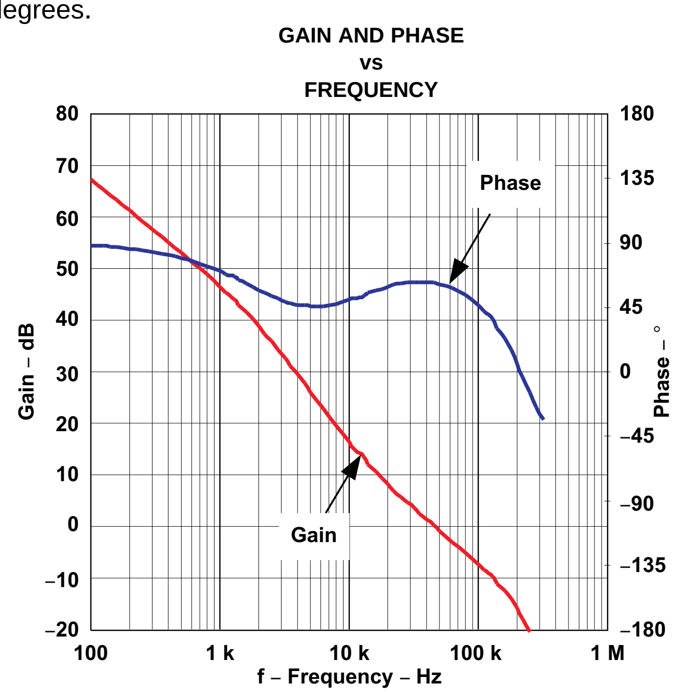


**Figure 28. Example Loop Result**

 

### Bootstrap for the N-Channel MOSFET

A bootstrap circuit provides a voltage source higher than the input voltage and of sufficient energy to fully enhance the switching MOSFET each switching cycle. The PWM duty cycle is limited to a maximum of 90%, allowing an external bootstrap capacitor to charge through an internal synchronous switch (between BP and BOOTx) during every cycle. When the PWM switch is commanded to turn ON, the energy used to drive the MOSFET gate is derived from the voltage on this capacitor.

To allow the bootstrap capacitor to charge each switching cycle, an internal pulldown MOSFET (from SW to GND) is turned ON for approximately 140 ns at the beginning of each switching cycle. In this way, if, during light load operation, there is insufficient energy for the SW node to drive to ground naturally, this MOSFET forces the SW node toward ground and allows the bootstrap capacitor to charge.

Because this is a charge transfer circuit, care must be taken in selecting the value of the bootstrap capacitor. It must be sized such that the energy stored in the capacitor on a per-cycle basis is greater than the gate charge requirement of the MOSFET being used.

---

**DESIGN HINT**

For the bootstrap capacitor, use a ceramic capacitor with a value between 22 nF and 82 nF.

---

**NOTE**

For 5-V input applications, connect PVDDx to BP directly. This connection bypasses the internal control-circuit regulator and provides maximum voltage to the gate-drive circuitry. In this configuration, shutdown mode $IDD_{SDN}$ is the same as quiescent $IDD_Q$.

---

### Light Load Operation

There is no special circuitry for pulse skipping at light loads. The normal characteristic of a nonsynchronous converter is to operate in the *discontinuous-conduction mode* (DCM) at an average load current less than one-half of the inductor peak-to-peak ripple current. Note that the amplitude of the ripple current is a function of input voltage, output voltage, inductor value, and operating frequency, as shown in Equation 14.

$$I_{DCM} = \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L} \times \delta \times T_S \tag{14}$$

Further, during discontinuous-mode operation the commanded pulse duration may become narrower than the capability of the converter to resolve. To maintain the output voltage within regulation, skipping switching pulses at light load conditions is a natural byproduct of that mode. This condition may occur if the output capacitor is charged to a value greater than the output regulation voltage and there is insufficient load to discharge the capacitor. A byproduct of pulse skipping is an increase in the peak-to-peak output ripple voltage.

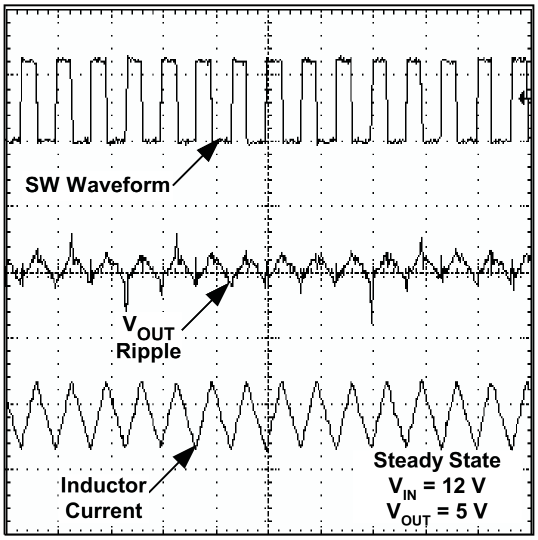


**Figure 29. Steady State**

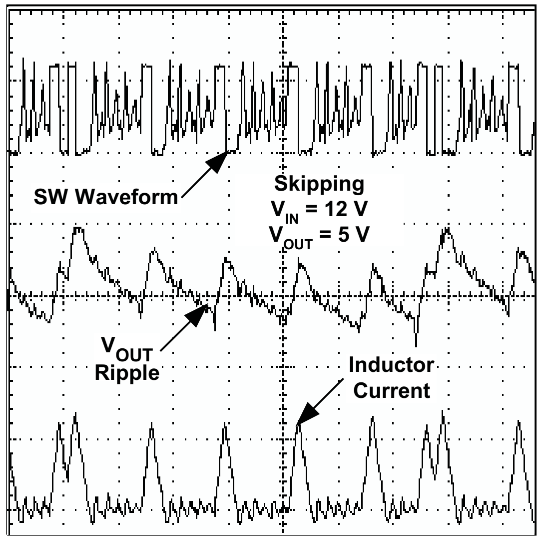


**Figure 30. Skipping**

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**DESIGN HINT**

If additional output capacitance is required to reduce the output-voltage ripple during DCM operation, be sure to recheck the *Feedback Loop and Inductor-Capacitor (L-C) Filter Selection* and *Maximum Output Capacitance* sections.

---

### SW Node Ringing

A portion of the control circuitry is referenced to the SW node. To ensure jitter-free operation, it is necessary to decrease the voltage waveform ringing at the SW node to less than 5 volts peak and of a duration of less than 30-ns. In addition to following good printed-circuit board (PCB) layout practices, there are a couple of design techniques for reducing ringing and noise.

#### *SW Node Snubber*

Voltage ringing observable at the SW node is caused by fast switching edges and parasitic inductance and capacitance. If the ringing results in excessive voltage on the SW node, or erratic operation of the converter, an R-C snubber may be used to dampen the ringing and ensure proper operation over the full load range.

---

**DESIGN HINT**

A series-connected R-C snubber (C = between 330 pF and 1 nF, R = 10 Ω) connected from SW to GND reduces the ringing on the SW node.

---

#### *Bootstrap Resistor*

A small resistor in series with the bootstrap capacitor reduces the turnon time of the internal MOSFET, thereby reducing the rising-edge ringing of the SW node.

---

**DESIGN HINT**

A resistor with a value between 1 Ω and 3 Ω may be placed in series with the bootstrap capacitor to reduce ringing on the SW node.

---

**DESIGN HINT**

Placeholders for these components should be placed on the initial prototype PCBs in case they are needed.

---

### Output Overload Protection

In the event of an overcurrent during soft-start on either output (such as starting into an output short), pulse-by-pulse current limiting and PWM frequency division are in effect for that output until the internal soft-start timer ends. At the end of the soft-start time, a UV condition is declared and a fault is declared. During this fault condition, both PWM outputs are disabled and the small pulldown MOSFETs (from SWx to GND) are turned ON. This process ensures that both outputs discharge to GND in the event that overcurrent is on one output while the other is not loaded. The converter then enters a *hiccup*-mode time-out before attempting to restart. *Frequency division* means if an overcurrent pulse is detected, six clock cycles are skipped before the next PWM pulse is initiated, effectively dividing the operating frequency by six and preventing excessive current buildup in the inductor.

In the event of an overcurrent on either output after the output reaches regulation, pulse-by-pulse current limit is in effect for that output. In addition, an output undervoltage (UV) comparator monitors the FBx voltage (that follows the output voltage) to declare a fault if the output drops below 85% of regulation. During this fault condition, both PWM outputs are disabled and the small pulldown MOSFETs (from SWx to GND) are turned ON. This design ensures that both outputs discharge to GND, in the event that overcurrent is on one output while the other is not loaded. The converter then enters a *hiccup*-mode timeout before attempting to restart.

The overcurrent threshold for output 1 is set nominally at 4.5 A. The overcurrent level of output 2 is determined by the state of the ILIM2 pin. The ILIM setting of output 2 is not latched in place and may be changed during operation of the converter.

**Table 3. Current Limit Threshold Adjustment for Output 2**

| ILIM2 Connection | OCP Threshold for Output 2 |
|---|---|
| BP | 4.5-A nominal setting |
| (floating) | 3-A nominal setting |
| GND | 1.5-A nominal setting |

**DESIGN HINT**

The OCP threshold refers to the peak current in the internal switch. Be sure to add one-half of the peak inductor ripple current to the dc load current in determining how close the actual operating point is to the OCP threshold.

### Operating Near Maximum Duty Cycle

If the TPS54386-Q1 operates at maximum duty cycle, and if the input voltage is insufficient to support the output voltage (at full load or during a load-current transient), then there is a possibility that the output voltage will fall from regulation and trip the output UV comparator. If this should occur, the TPS54386-Q1 protection circuitry declares a fault and enters a shut-down-and-restart cycle.

**DESIGN HINT**

Ensure that under ALL conditions of line and load regulation, there is sufficient duty cycle to maintain output-voltage regulation.

To calculate the operating duty cycle, use Equation 15.

$$\delta = \frac{V_{OUT} + V_{DIODE}}{V_{IN} + V_{DIODE}} \qquad (15)$$

where

- $V_{DIODE}$ is the voltage drop of the rectifier diode.

### Dual-Supply Operation

It is possible to operate a TPS54386-Q1 from two supply voltages. If this application is desired, then the sequencing of the supplies must be such that PVDD2 is above the UVLO voltage before PVDD1 begins to rise. This level requirement ensures that the internal regulator and the control circuitry are in operation before PVDD1 supplies energy to the output. In addition, output 1 must be held in the disabled state ($\overline{\text{EN1}}$ high) until there is sufficient voltage on PVDD1 to support output 1 in regulation. (See the *Operating Near Maximum Duty Cycle* section.)

The preferred sequence of events is:

1. PVDD2 rises above the input UVLO voltage.
2. PVDD1 rises with output 1 disabled until PVDD1 rises above the level to support output 1 regulation.

   With these two conditions satisfied, there is no restriction on PVDD2 to be greater than or less than PVDD1.

---

**DESIGN HINT**

An R-C delay on $\overline{\text{EN1}}$ may be used to delay the start-up of output 1 for a long-enough period of time to ensure that PVDD1 can support the output 1 load.

---

### Cascading Supply Operation

It is possible to source PVDD1 from output 2 as depicted in Figure 31 and Figure 32. This configuration may be preferred if the input voltage is high, relative to the voltage on output 1.

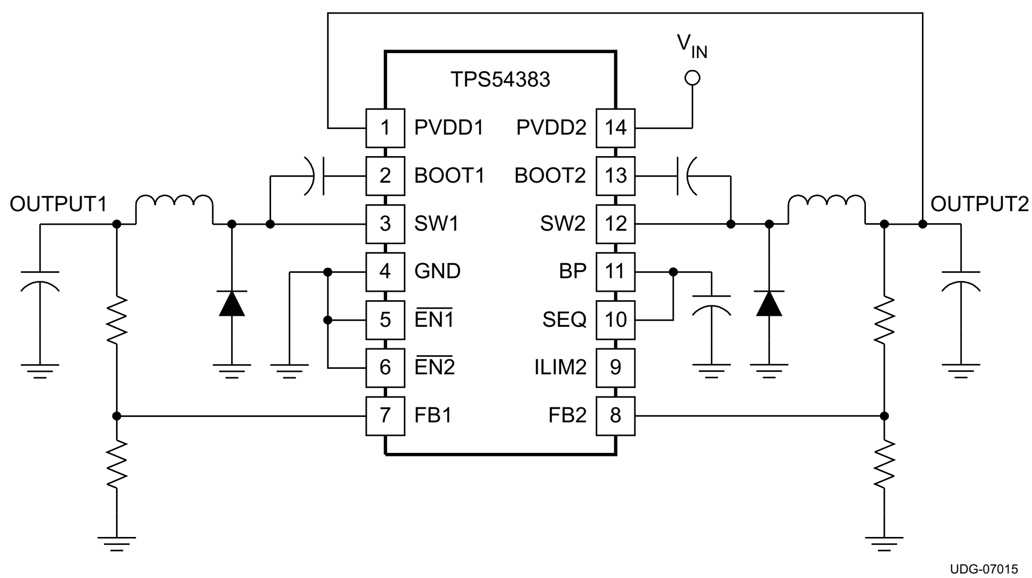


**Figure 31. Schematic Showing Cascading PVDD1 From Output 2**

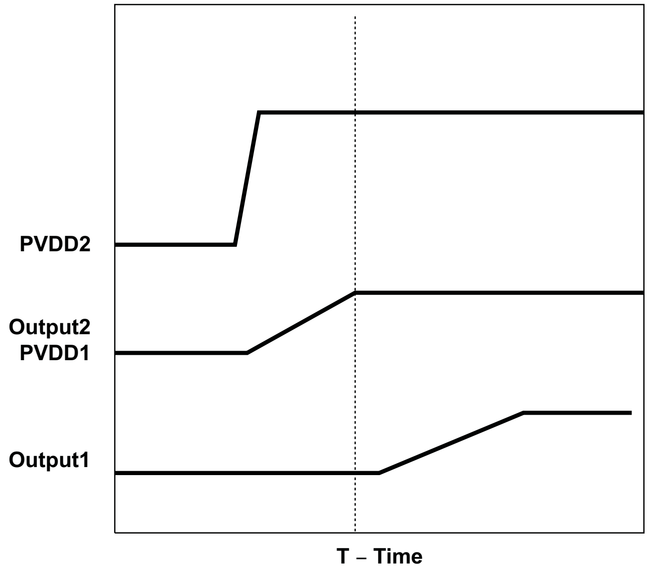


**Figure 32. Waveforms Resulting From Cascading PVDD1 From Output 2**

In this configuration, the following conditions must be maintained:

1. Output 2 must be of a voltage high enough to maintain regulation of output 1 under all load conditions.
2. The sum of the current drawn by output 2 load plus the current into PVDD1 must be less than the overload protection current level of output 2.
3. The method of output sequencing must be such that the voltage on output 2 is sufficient to support output 1 before output 1 is enabled. This requrement may be accomplished by:
   (a) a delay of the enable function
   (b) selecting sequential sequencing of output 1 starting after output 2 is in regulation

### Multiphase Operation

The TPS54386-Q1 is not designed to operate as a two-channel multiphase converter. See http://www.power.ti.com for appropriate device selection.

### Bypass and FIltering

As with any integrated circuit, supply bypassing is important for jitter-free operation. To improve the noise immunity of the converter, ceramic bypass capacitors must be placed as close to the package as possible.

1. PVDD1 to GND: Use a 10-μF ceramic capacitor.
2. PVDD2 to GND: Use a 10-μF ceramic capacitor.
3. BP to GND: Use a 4.7-μF to 10-μF ceramic capacitor.

### Overtemperature Protection and Junction Temperature Rise

The overtemperature thermal protection limits the maximum power to be dissipated at a given operating ambient temperature. In other words, at a given device power dissipation, the maximum ambient operating temperature is limited by the maximum allowable junction operating temperature. The device junction temperature is a function of power dissipation and the thermal impedance from the junction to ambient. If the internal die temperature should reach the thermal shutdown level, the TPS54386-Q1 shuts off both PWMs and remains in this state until the die temperature drops below the hysteresis value, at which time the device restarts.

The first step to determine the device junction temperature is to calculate the power dissipation. The power dissipation is dominated by the two switching MOSFETs and the BP internal regulator. The power dissipated by each MOSFET is composed of conduction losses and output (switching) losses incurred while driving the external rectifier diode. To find the conduction loss, first find the rms current through the upper switch MOSFET.

$$I_{RMS(outputx)} = \sqrt{D \times \left( \left(I_{OUTPUTx}\right)^2 + \left( \frac{\left(\Delta I_{OUTPUTx}\right)^2}{12} \right) \right)}$$

where

- D is the duty cycle.
- $I_{OUTPUTx}$ is the dc output current.
- $\Delta I_{OUTPUTx}$ is the peak ripple current in the inductor for output x. (16)

Notice the impact of the operating duty cycle on the result.

Multiplying the result by the $R_{DS(on)}$ of the MOSFET gives the conduction loss.

$$P_{D(cond)} = I_{RMS(outputx)}^{\ 2} \times R_{DS(on)} \tag{17}$$

The switching loss is approximated by:

$$P_{D(SW)} = \left[ \frac{(V_{IN})^2 \times C_J \times f_S}{2} \right]$$

where

- where $C_J$ is the parallel capacitance of the rectifier diode and snubber (if any).
- $f_S$ is the switching frequency. (18)

The total power dissipation is found by summing the power loss for both MOSFETs plus the loss in the internal regulator.

$$P_D = P_{D(cond)output1} + P_{D(SW)output1} + P_{D(cond)output2} + P_{D(SW)output2} + V_{IN} \times Iq \tag{19}$$

The temperature rise of the device junction depends on the thermal impedance from the junction to the mounting pad (see the *Package Dissipation Ratings* table), plus the thermal impedance from the thermal pad to ambient. The thermal impedance from the thermal pad to ambient depends on the PCB layout (thermal-pad interface to the PCB, the exposed pad area) and airflow (if any). See the *PCB Layout Guidelines, Additional References* section.

The operating junction temperature is shown in Equation 20.

$$T_J = T_A + P_D \times \left(\theta_{TH(pkg)} + \theta_{TH(pad-amb)}\right) \tag{20}$$

### Power Derating

The TPS54386-Q1 delivers full current at ambient temperatures up to 85°C if the thermal impedance from the thermal pad maintains the junction temperature below the thermal shutdown level. At higher ambient temperatures, the device power dissipation must be reduced to maintain the junction temperature at or below the thermal shutdown level. Figure 33 illustrates the power derating for elevated ambient temperature under various airflow conditions. Note that these curves assume that the thermal pad is properly soldered to the recommended board. (See the *References* section for further information.)

 

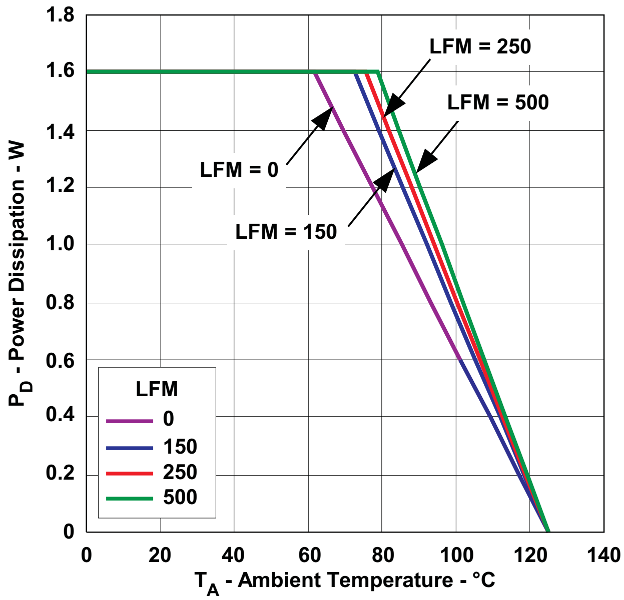


**Figure 33. Power-Derating Curves**

### PowerPAD Package

The PowerPAD package provides low thermal impedance for heat removal from the device. The thermal pad derives its name and low thermal impedance from the large bonding pad on the bottom of the device. The circuit board must have an area of solder-tinned-copper underneath the package. The dimensions of this area depend on the size of the PowerPAD package. Thermal vias connect this area to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the solder-tinned area under the device during solder reflow. Drill diameters of 0.33 mm (13 mils) work well when 1-oz. copper is plated at the surface of the board while simultaneously plating the barrel of the via. If the thermal vias are not plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a diameter equal to the via diameter of 0.1 mm minimum. This capping prevents the solder from being wicked through the thermal vias and potentially creating a solder void under the package. (See the *Additional References* section.)

### PCB Layout Guidelines

The layout guidelines presented here are illustrated in the PCB layout examples given in Figure 34 and Figure 35.

- The thermal pad must be connected to a low-current (signal) ground plane having a large copper surface area to dissipate heat. Extend the copper surface well beyond the IC package area to maximize thermal transfer of heat away from the IC.
- Connect the GND pin to the thermal pad through a 10-mil (0.010-in, or 0.254-mm) wide trace.
- Place the ceramic input capacitors close to PVDD1 and PVDD2; connect using short, wide traces.
- Maintain a tight loop of wide traces from SW1 or SW2 through the switch node, inductor, output capacitor, and rectifier diode. Avoid using vias in this loop.
- Use a wide ground connection from the input capacitor to the rectifier diode, placed as close to the power path as possible. Placement directly under the diode and the switch node is recommended.
- Locate the bootstrap capacitor close to the BOOT pin to minimize the gate-drive loop.
- Locate voltage-setting resistors and any feedback components over the ground plane and away from the switch node and the rectifier diode to the input-capacitor ground connection.
- Locate snubber components (if used) close to the rectifier diode with minimal loop area.

- Locate the BP bypass capacitor very close to the IC; a minimal loop area is recommended.
- Locate the output ceramic capacitor close to the inductor output terminal between the inductor and any electrolytic capacitors, if used.

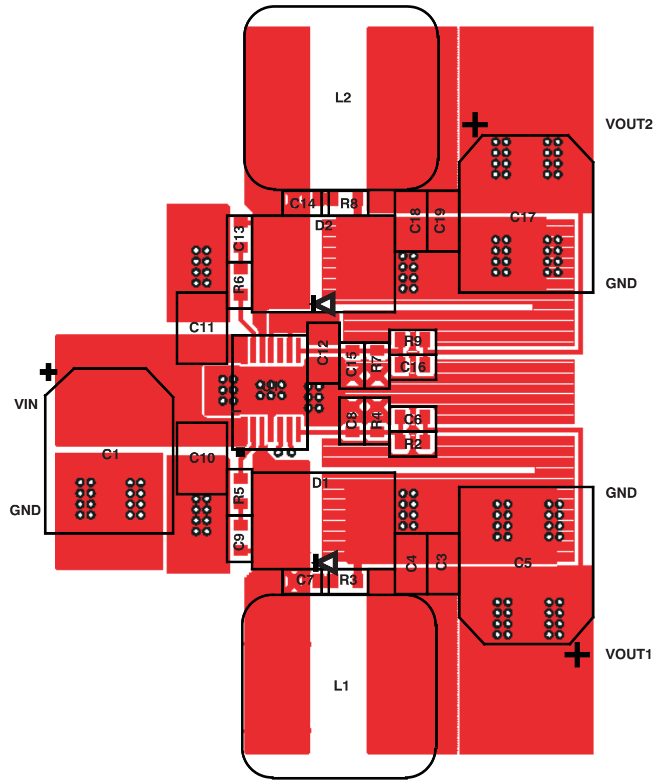


**Figure 34. Top Layer Copper Layout and Component Placement**

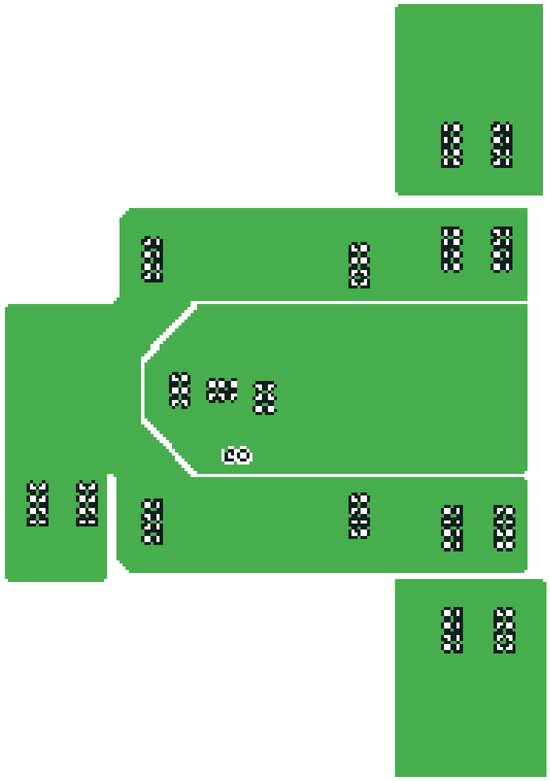

**Figure 35. Bottom Layer Copper Layout**

# DESIGN EXAMPLES

## Example 1: Detailed Design of a 12-V to 5-V and 3.3-V Converter

The following example illustrates a design process and component selection for a 12-V to 5-V and 3.3-V dual non-synchronous buck regulator using the TPS54386-Q1 converter. Design Example List of Materials and Table 5, Definition of Symbols is found at the end of this section.

| PARAMETER | | NOTES AND CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | |
| $V_{IN}$ | Input voltage | | 6.9 | 12 | 13.2 | V |
| $I_{IN}$ | Input current | $V_{IN}$ = nom, $I_{OUT}$ = max | | 1.6 | 2 | A |
| | No load input current | $V_{IN}$ = nom, $I_{OUT}$ = 0 A | | 12 | 20 | mA |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| $V_{OUT1}$ | Output voltage 1 | $V_{IN}$ = nom, $I_{OUT}$ = nom | 4.8 | 5 | 5.2 | V |
| $V_{OUT2}$ | Output voltage 2 | $V_{IN}$ = nom, $I_{OUT}$ = nom | 3.2 | 3.3 | 3.4 | |
| | Line regulation | $V_{IN}$ = min to max | | | 1% | |
| | Load regulation | $I_{OUT}$ = min to max | | | 1% | |
| $V_{OUT(ripple)}$ | Output voltage ripple | $V_{IN}$ = nom, $I_{OUT}$ = max | | | 50 | $mV_{PP}$ |
| $I_{OUT1}$ | Output current 1 | $V_{IN}$ = min to max | 0 | | 2 | A |
| $I_{OUT2}$ | Output current 2 | $V_{IN}$ = min to max | 0 | | 2 | |
| $I_{OCP1}$ | Output overcurrent channel 1 | $V_{IN}$ = nom, $V_{OUT}$ = $V_{OUT1}$ = 5% | 2.4 | 3 | 3.5 | |
| $I_{OCP2}$ | Output overcurrent channel 2 | $V_{IN}$ = nom, $V_{OUT}$ = $V_{OUT2}$ = 5% | 2.4 | 3 | 3.5 | |
| | Transient response $\Delta V_{OUT}$ from load transient | $\Delta I_{OUT}$ = 1 A at 3 A/µs | | 200 | | mV |
| | Transient response settling time | | | 1 | | ms |
| **SYSTEM CHARACTERISTICS** | | | | | | |
| $f_{SW}$ | Switching frequency | | 250 | 310 | 370 | kHz |
| η | Full-load efficiency | | | 85% | | |
| $T_J$ | Operating temperature range | | 0 | 25 | 60 | °C |

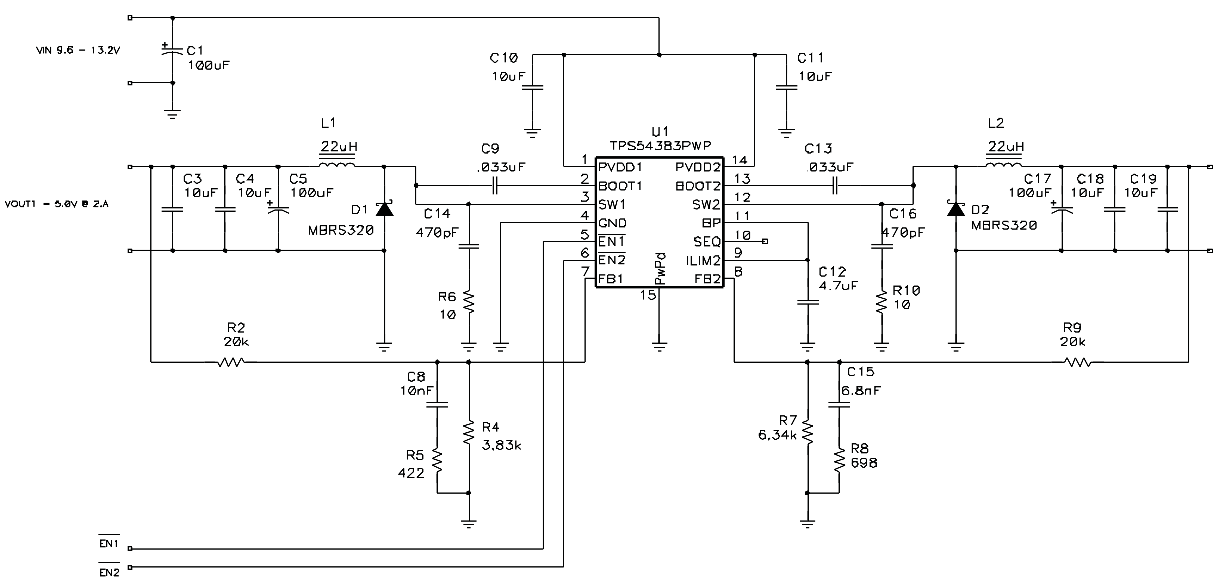


**Figure 36. Design Example Schematic**

## Design Procedure

### Duty Cycle Estimation

The first step is to estimate the duty cycle of each switching FET.

$$D_{max} \approx \frac{V_{OUT} + V_{FD}}{V_{IN(min)} + V_{FD}} \tag{21}$$

$$D_{min} \approx \frac{V_{OUT} + V_{FD}}{V_{IN(max)} + V_{FD}} \tag{22}$$

Using an assumed forward drop of 0.5 V for a Schottky rectifier diode, the channel 1 duty cycle is approximately 40.1% (minimum) to 48.7% (maximum), while the channel 2 duty cycle is approximately 27.7% (minimum) to 32.2% (maximum).

### Inductor Selection

The peak-to-peak ripple is limited to 30% of the maximum output current. This places the peak current far enough from the minimum overcurrent trip level to ensure reliable operation.

For both channel 1 and channel 2, the maximum inductor ripple current is 600 mA. The inductor size is estimated in Equation 23.

$$L_{min} \approx \frac{V_{IN(max)} - V_{OUT}}{I_{LRIP(max)}} \times D_{min} \times \frac{1}{f_{SW}} \tag{23}$$

The inductor values are

- L1 = 18.3 μH
- L2 = 15.3 μH

The next-higher standard inductor value of 22 μH is used for both inductors.

The resulting ripple currents are :

$$I_{RIPPLE} \approx \frac{V_{IN(max)} - V_{OUT}}{L} \times D_{min} \times \frac{1}{f_{SW}} \tag{24}$$

Peak-to-peak ripple currents of 0.498 A and 0.416 A are estimated for channel 1 and channel 2, respectively.

The rms current through an inductor is approximated by Equation 25.

$$I_{L(rms)} = \sqrt{\left(I_{L(avg)}\right)^2 + \frac{1}{12}\left(I_{RIPPLE}\right)^2} \tag{25}$$

and is approximately 2 A for both channels.

The peak inductor current is found using:

$$I_{L(peak)} \approx I_{OUT(max)} + \frac{1}{2} I_{RIPPLE} \tag{26}$$

An inductor with a minimum rms current rating of 2 A and minimum saturation current rating of 2.25 A is required. A Coilcraft MSS1278-223ML 22-μH, 6.8-A inductor is selected.

### Rectifier Diode Selection

A Schottky diode is selected as a rectifier diode for its low forward-voltage drop. Allowing 20% over VIN for ringing on the switch node, the required minimum reverse-breakdown voltage of the rectifier diode is:

$$V_{(BR)R(min)} \geq 1.2 \times V_{IN} \tag{27}$$

The diode must have reverse breakdown voltage greater than 15.8 V, therefore a 20-V device is used.

The average current in the rectifier diode is estimated by Equation 28.

$$I_{D(avg)} \approx I_{OUT(max)} \times (1 - D) \quad (28)$$

For this design, 1.2-A (average) and 2.25 A (peak) is estimated for channel 1 and 1.5-A (average) and 2.21-A (peak) for channel 2.

An MBRS320, 20-V, 3-A diode in an SMC package is selected for both channels. This diode has a forward voltage drop of 0.4 V at 2 A.

The power dissipation in the diode is estimated by Equation 29.

$$P_{D(max)} \approx V_{FM} \times I_{D(avg)} \quad (29)$$

For this design, the full-load power dissipation is estimated to be 480 mW in D1, and 580 mW in D2.

### Output Capacitor Selection

The TPS54386-Q1 internal compensation limits the selection of the output capacitors. From , the internal compensation has a double zero resonance at about 3 kHz. The output capacitor is selected by Equation 30.

$$C_{OUT} = \frac{1}{4 \times \pi^2 \times (f_{RES})^2 \times L} \quad (30)$$

Solving for $C_{OUT}$ using

- $f_{RES}$ = 3 kHz
- L = 22 µH

The resulting is $C_{OUT}$ = 128 µF. The output ripple voltage of the converter is composed of the ripple voltage across the output capacitance and the ripple voltage across the ESR of the output capacitor. To find the maximum ESR allowable to meet the output ripple requirements, the total ripple is partitioned and the equation solved to find the ESR.

$$ESR_{(max)} = \frac{V_{RIPPLE(tot)} - V_{RIPPLE(cap)}}{I_{RIPPLE}} = \frac{V_{RIPPLE(tot)}}{I_{RIPPLE}} - \frac{D}{f_S \times C_{OUT}} \quad (31)$$

Based on 128 µF of capacitance, 300-kHz switching frequency, and 50-mV ripple voltage, plus rounding up the ripple current to 0.5 A and the duty cycle to 50%, the capacitive portion of the ripple voltage is 6.5 mV, leaving a maximum allowable ESR of 87 mΩ.

To meet the ripple-voltage requirements, a low-cost 100-µF electrolytic capacitor with 400 mΩ ESR (C5, C17) and two 10-µF ceramic capacitors (C3 and C4; and C18 and C19) with 2.5-mΩ ESR are selected. From the data sheets for the ceramic capacitors, the parallel combination provides an impedance of 28 mΩ at 300 kHz for 14 mV of ripple.

### Voltage Setting

The primary feedback divider resistors (R2, R9) from VOUT to FB should be between 10 kΩ and 50 kΩ to maintain a balance between power dissipation and noise sensitivity. For this design, 20 kΩ is selected.

The lower resistors, R4 and R7 are found using the following equations.

$$R4 = \frac{V_{FB} \times R2}{V_{OUT1} - V_{FB}} \quad (32)$$

$$R7 = \frac{V_{FB} \times R9}{V_{OUT2} - V_{FB}} \quad (33)$$

- R2 = R9 = 20 kΩ
- $V_{FB}$ = 0.8 V

- R4 = 3.8 kΩ (3.83 kΩ standard value is used)
- R7 = 6.4 kΩ (6.34 kΩ standard value is used)

### Compensation Capacitors

Checking the ESR zero of the output capacitors:

$$f_{ESR(zero)} = \frac{1}{2 \times \pi \times C \times ESR}$$

- C = 100 µF
- ESR = 400 mΩ
- ESR(zero) = 3980 Hz (34)

Because the ESR zero of the main output capacitor is less than 20 kHz, an R-C filter is added in parallel with R4 and R7 to compensate for the ESR of the electrolytic capacitor and add a zero of approximately 40 kHz.

$$R5 = \frac{R4}{\left(\left(\frac{f_{ZERO(desired)}}{f_{ESR(zero)}}\right) - 1\right)}$$

- $f_{ESR(zero)}$ = 4 kHz
- $f_{ESR(desired)}$ = 40 kHz
- R4 = 3.83 kΩ
- R5 = 424 Ω (422 Ω selected)
- R7 = 6.34 kΩ
- R8 = 702 Ω (698 Ω selected) (35)

$$R_{EQ} = R5 + \frac{1}{\left(\left(\frac{1}{R2}\right) + \left(\frac{1}{R4}\right)\right)}$$

- R2 = R9 = 20 kΩ
- $R_{EQ1}$ = 3.63 kΩ
- $R_{EQ2}$ = 5.51 kΩ (36)

$$C8 = \frac{1}{2 \times \pi \times R_{EQ} \times f_{ESR(zero)}}$$

- C8 = 10.9 nF (10 nF selected)
- C15 = 7.22 nF (6800 pF selected) (37)

### Input Capacitor Selection

The TPS54386-Q1 data sheet recommends a minimum 10-µF ceramic input capacitor on each PVDD pin. These capacitors must be capable of handling the rms ripple current of the converter. The rms current in the input capacitors is estimated by Equation 38.

$$I_{RMS(outputx)} = \sqrt{D \times \left( \left(I_{OUTPUTx}\right)^2 + \left( \frac{\left(\Delta I_{OUTPUTx}\right)^2}{12} \right) \right)} \quad (38)$$

- $I_{RMS(CIN)}$ = 0.43 A

One 1210 10-µF, 25-V, X5R ceramic capacitor with 2-mΩ ESR and a 2-A rms current rating is selected for each PVDD input. Higher-voltage capacitors are selected to minimize capacitance loss at the dc bias voltage to ensure the capacitors maintain sufficient capacitance at the working voltage.

### Bootstrap Capacitor

To ensure proper charging of the high-side FET gate and limit the ripple voltage on the boost capacitor, a 33-nF bootstrap capacitor is used.

### ILIM

Current limit must be set above the peak inductor current $I_{L(peak)}$. Comparing $I_{L(peak)}$ to the available minimum current limits, ILIM is connected to BP for the highest current-limit level.

### SEQ

The SEQ pin is left floating, leaving the enable pins to function independently. If the enable pins are tied together, the two supplies start up ratiometrically. Alternatively, SEQ could be connected to BP or GND to provide sequential start-up.

### Power Dissipation

The power dissipation in the TPS54386-Q1 is composed of FET conduction losses, switching losses, and internal regulator losses. The rms FET current is found using Equation 39.

$$I_{RMS(outputx)} = \sqrt{D \times \left( \left(I_{OUTPUTx}\right)^2 + \left( \frac{\left(\Delta I_{OUTPUTx}\right)^2}{12} \right) \right)} \quad (39)$$

This results in 1.05 -A rms for channel 1 and 0.87 A rms for channel 2.

Conduction losses are estimated by:

$$P_{CON} = R_{DS(on)} \times \left(I_{QSW(rms)}\right)^2 \quad (40)$$

Conduction losses of 198 mW and 136 mW are estimated for channel 1 and channel 2 respectively.

The switching losses are estimated in Equation 41.

$$P_{SW} \approx \frac{\left(V_{IN(max)}\right)^2 \times \left(C_{DJ} + C_{OSS}\right) \times f_{SW}}{2} \quad (41)$$

From the data sheet of the MBRS320, the junction capacitance is 658 pF. Because this is large compared to the output capacitance of the TPS54x8x, the FET capacitance is neglected, leaving switching losses of 17 mW for each channel.

The regulator losses are estimated in Equation 42.

$$P_{REG} \approx I_{DD} \times V_{IN(max)} + I_{BP} \times \left(V_{IN(max)} - V_{BP}\right) \quad (42)$$

With no external load on BP ($I_{BP}$ = 0), the power dissipation of the regulator is 66 mW.

Total power dissipation in the device is the sum of conduction and switching for both channels, plus regulator losses.

The total power dissipation is $P_{DISS}$ = 0.198 + 0.136 + 0.017 + 0.017 + 0.066 = 434 mW.

## Design Example Test Results

The following results are from the TPS54386-Q1-001 EVM.

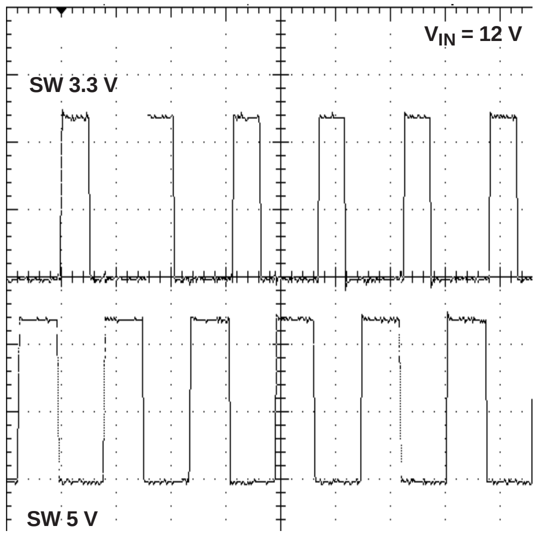


**Figure 37. Switching-Node Waveforms**

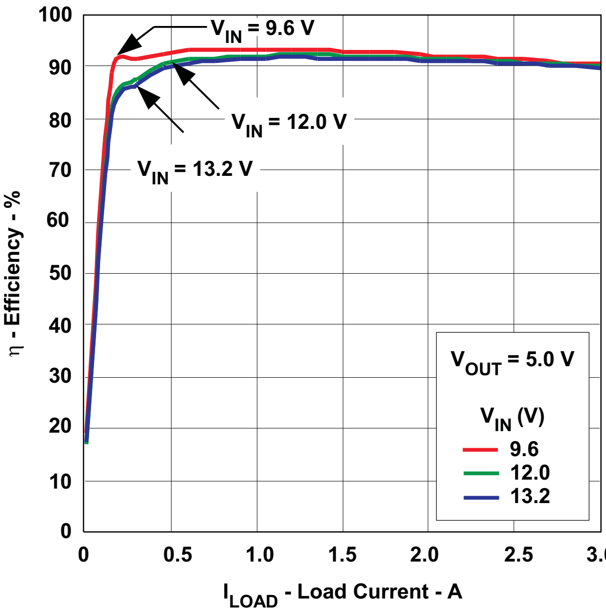


**Figure 38. 5-V Output Efficiency vs Load Current**

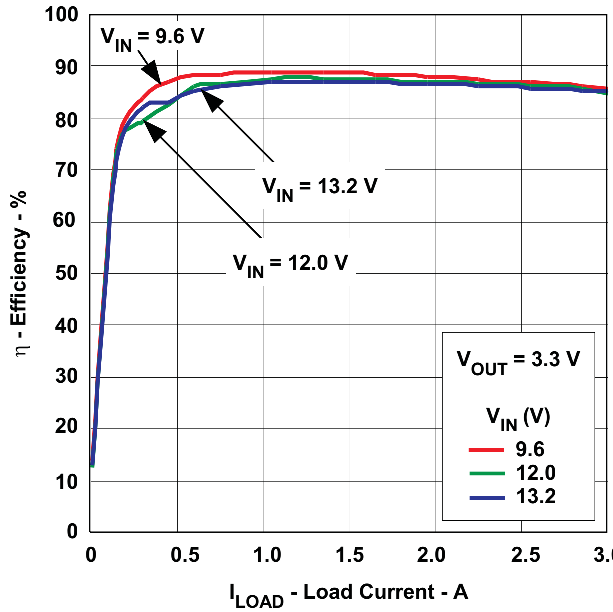


**Figure 39. 3.3-V Output Efficiency vs Load Current**

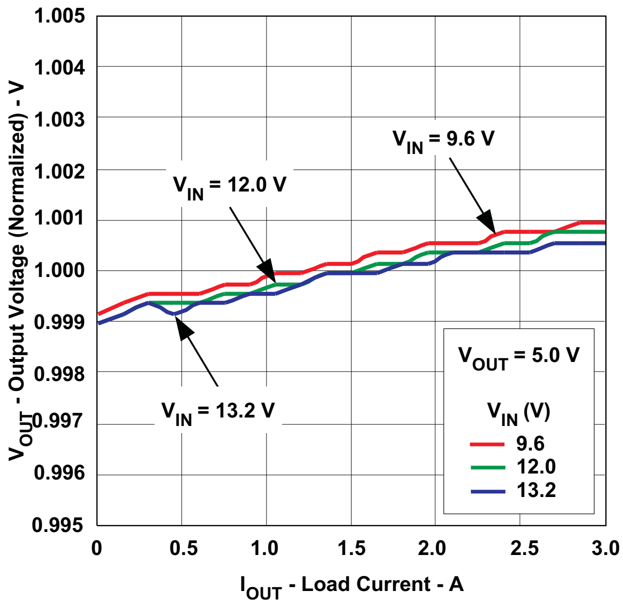


Figure 40. 5-V Output Voltage vs Load Current

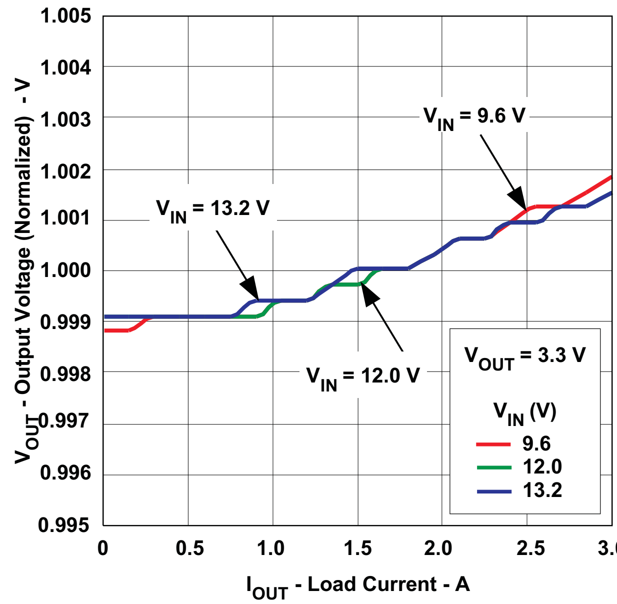


Figure 41. 3.3-V Output Voltage vs Load Current

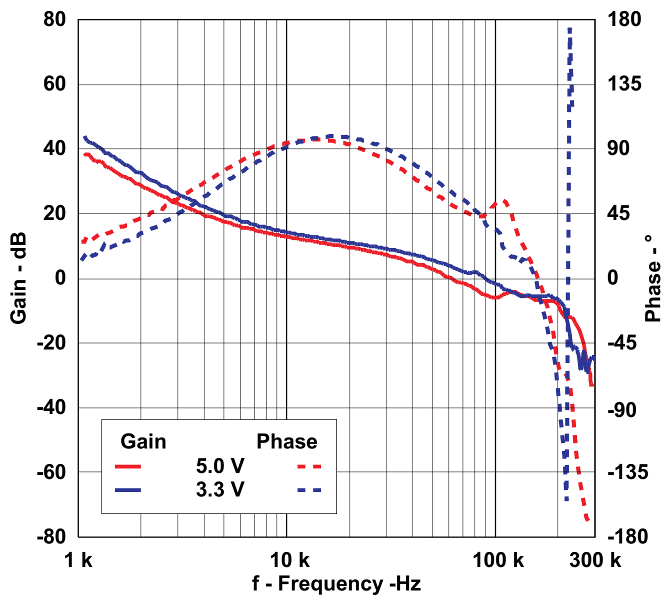


Figure 42. Example 1 Loop Response

### Table 4. Design Example List of Materials

| QTY | REFERENCE DESIGNATOR | VALUE | DESCRIPTION | SIZE | PART NUMBER | MANUFACTURER |
|---|---|---|---|---|---|---|
| 1 | C1 | 100 µF | Capacitor, Aluminum, 25V, 20% | E-can | EEEFC1E101P | Panasonic |
| 2 | C10, C11 | 10 µF | Capacitor, Ceramic, 25V, X5R 20% | 1210 | C3216X5R1E106M | TDK |
| 1 | C12 | 4.7 µF | Capacitor, Ceramic, 10V, X5R 20% | 0805 | Std | Std |
| 2 | C14, C16 | 470 pF | Capacitor, Ceramic, 25V, X7R, 20% | 0603 | Std | Std |
| 1 | C15 | 6.8 nF | Capacitor, Ceramic, 25V, X7R, 20% | 0603 | Std | Std |
| 1 | C17, C5 | 100 µF | Capacitor, Aluminum, 10V, 20%, FC Series | F-can | EEEFC1A101P | Panasonic |
| 4 | C3, C4, C18, C19 | 10 µF | Capacitor, Ceramic, 6.3V, X5R 20% | 0805 | C2012X5R0J106M | TDK |
| 1 | C8 | 10 nF | Capacitor, Ceramic, 25V, X7R, 20% | 0603 | Std | Std |
| 2 | C9, C13 | 0.033 µF | Capacitor, Ceramic, 25V, X7R, 20% | 0603 | Std | Std |
| 2 | D1, D2 | MBRS320 | Diode, Schottky, 3-A, 30-V | SMC | MBRS330T3 | On Semi |
| 2 | L1, L2 | 22 µH | Inductor, Power, 6.8A, 0.038 Ω | 0.484 x 0.484 | MSS1278-153ML | Coilcraft |
| 2 | R2, R9 | 20 kΩ | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std |
| 1 | R5 | 422 Ω | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std |
| 2 | R6, R10 | 10 Ω | Resistor, Chip, 1/16W, 5% | 0603 | Std | Std |
| 1 | R8 | 698 Ω | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std |
| 1 | R4 | 3.83 kΩ | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std |
| 1 | R7 | 6.34 kΩ | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std |
| 1 | U1 | | TPS54386-Q1 DC-DC Switching Converter w/ FET | HTSSOP -14 | TPS54386-Q1PWP | TI |

**Table 5. Definition of Symbols**

| | |
|---|---|
| $C_{DJ}$ | Average junction capacitance of the rectifier diode from 0 V to VIN(max) |
| $C_{OSS}$ | Average output capacitance of the switching MOSFET from 0 V to VIN(max) |
| $C_{OUT}$ | Output capacitor |
| $D_{(max)}$ | Maximum steady-state operating duty cycle |
| $D_{(min)}$ | Minimum steady-state operating duty cycle |
| $ESR_{(max)}$ | Maximum allowable output-capacitor ESR |
| $f_{SW}$ | Switching frequency |
| $I_{BP}$ | Output current of BP regulator due to external loads |
| $I_{DD}$ | Switching quiescent current with no load on BP |
| $I_{D(avg)}$ | Average diode conduction current |
| $I_{D(peak)}$ | Peak diode conduction current |
| $I_{IN(avg)}$ | Average input current |
| $I_{IN(rms)}$ | Root mean squared (RMS) input current |
| $I_{L(avg)}$ | Average inductor current |
| $I_{L(rms)}$ | Root mean squared (RMS) inductor current |
| $I_{L(peak)}$ | Peak current in inductor |
| $I_{LRIP(max)}$ | Maximum allowable inductor ripple current |
| $L_{(min)}$ | Minimum inductor value to maintain desired ripple current |
| $I_{OUT(max)}$ | Maximum designed output current |
| $I_{RMS(cin)}$ | Root mean squared (RMS) current through the input capacitor |
| $I_{RIPPLE}$ | Inductor peak-to-peak ripple current |
| $I_{QSW(rms)}$ | Root mean squared current through the switching MOSFET |
| $P_{CON}$ | Power loss due to conduction through switching MOSFET |
| $P_{D(max)}$ | Maximum power dissipation in diode |
| $R_{DS(on)}$ | Drain-to-source resistance of the switching MOSFET when ON |
| $P_{SW}$ | Power loss due to switching |
| $P_{REG}$ | Power loss due to the internal regulator |
| $V_{BP}$ | Output voltage of BP regulator |
| $V_{(BR)R(min)}$ | Minimum reverse-breakdown voltage rating for rectifier diode |
| $V_{FB}$ | Regulated feedback voltage |
| $V_{FD}$ | Forward voltage drop across rectifier diode |
| $V_{IN}$ | Power-stage input voltage |
| $V_{OUT}$ | Regulated output voltage |
| $V_{RIPPLE(cap)}$ | Peak-to-peak ripple voltage due to ideal capacitor (ESR = 0 Ω) |
| $V_{RIPPLE(tot)}$ | Maximum allowable peak-to-peak output ripple voltage |

### Example 2: 24 V to 12 V and 24 V to 5 V

For a higher input voltage, both a snubber and bootstrap resistors are added to reduce ringing on the switch node and a 30-V Schottky diode is selected. A higher-resistance feedback network is chosen for the 12-V output to reduce the feedback current.

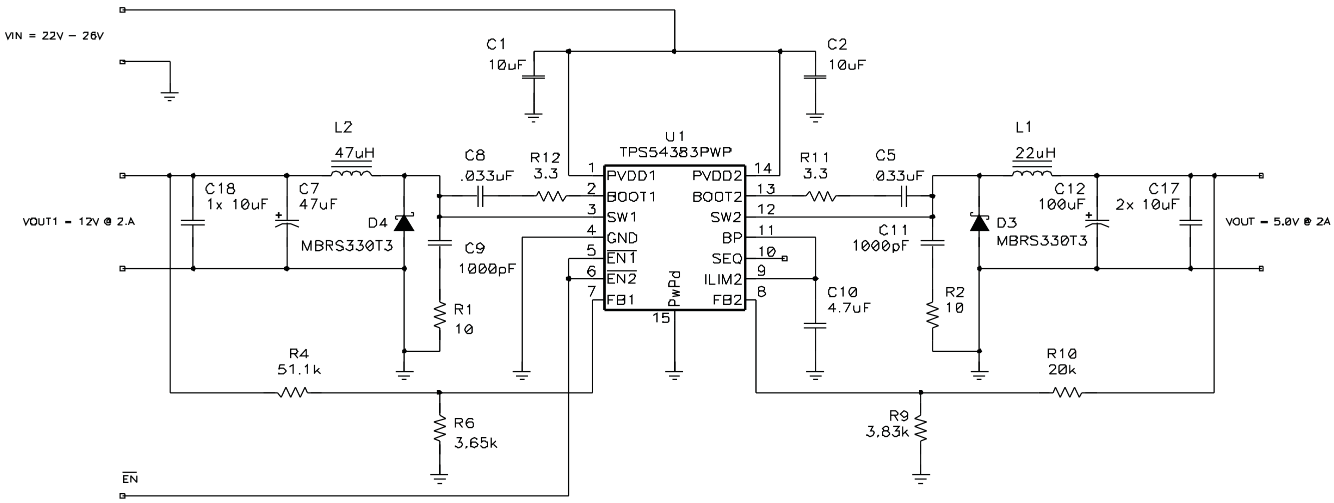


**Figure 43. 24 V to 12 V and 24 V to 5 V Using the TPS54386-Q1**

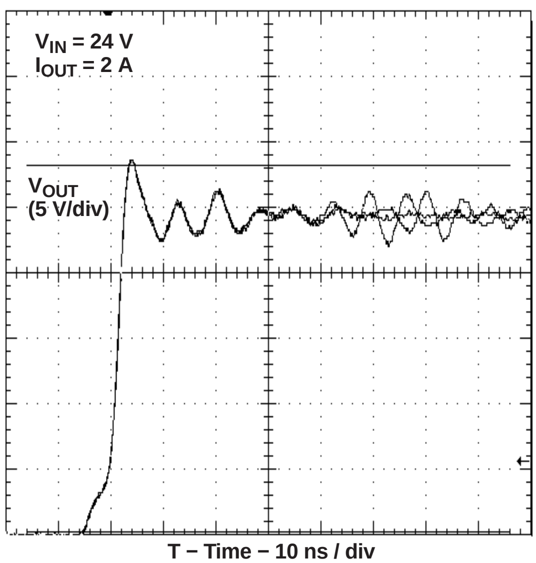


**Figure 44. Switch Node Ringing Without Snubber and Boost Resistor**

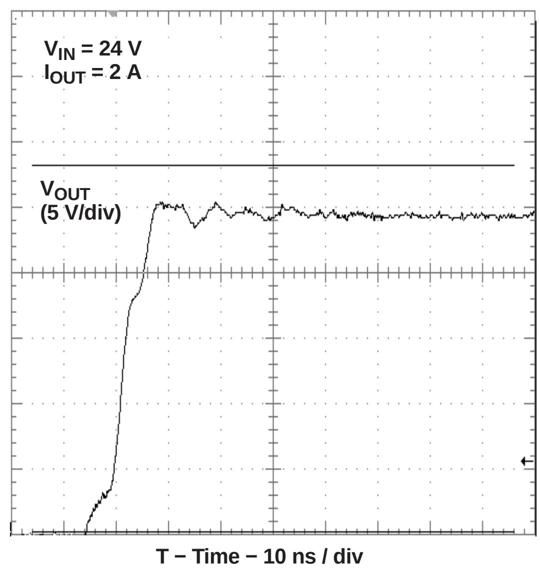


**Figure 45. Switch Node Ringing With Snubber and Boost Resistor**

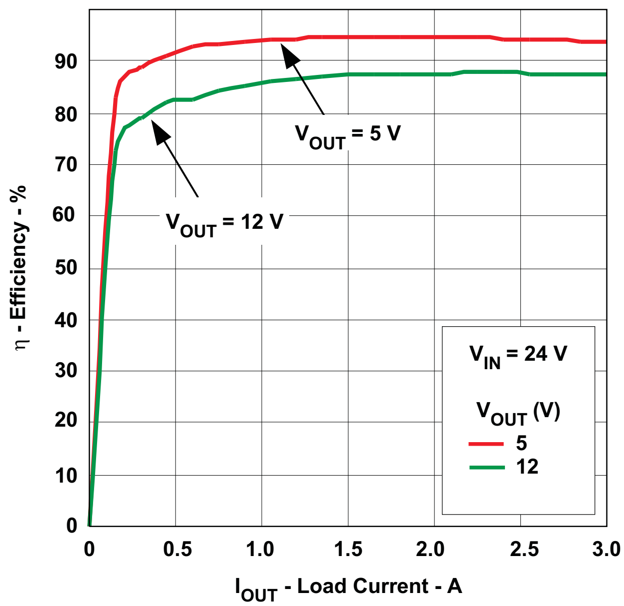


**Figure 46. Efficiency vs Load Current**

 

### Example 3: 5 V to 3.3 V and 5 V to 1.2 V

For a low-input-voltage application, the TPS54386-Q1 is selected for reduced size, and all ceramic output capacitors are used. 22-μF input capacitors are selected to reduce input ripple and lead capacitors are placed in the feedback to boost phase margin.

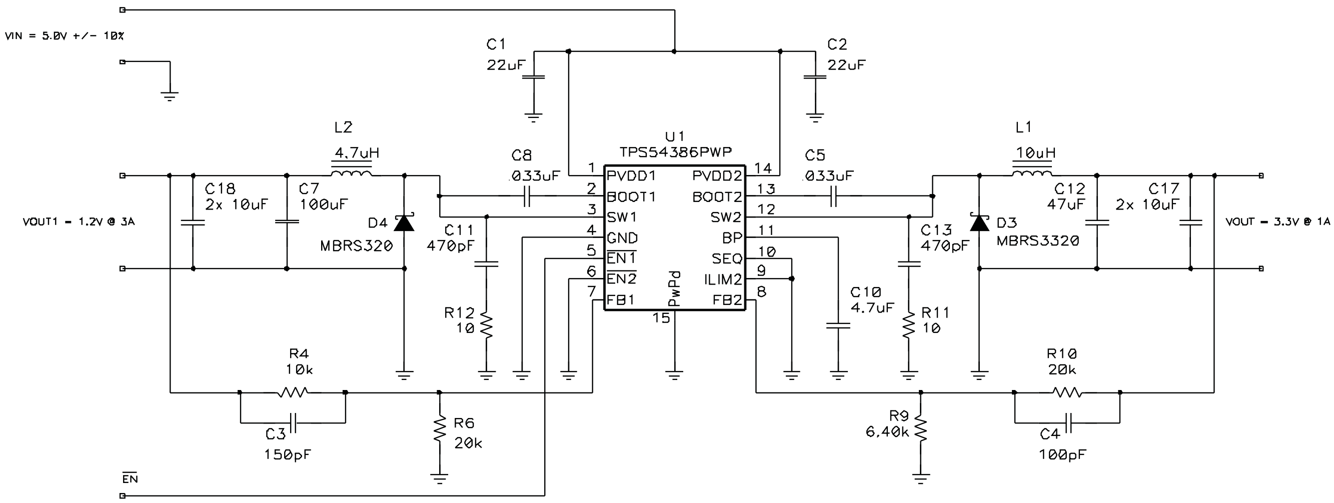


**Figure 47. 5 V to 3.3 V and 5 V to 1.2 V**

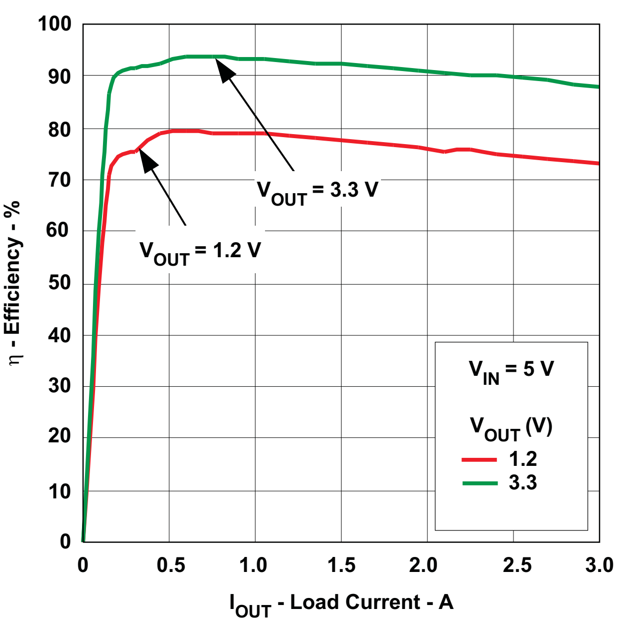


**Figure 48. Efficiency vs Load Current**

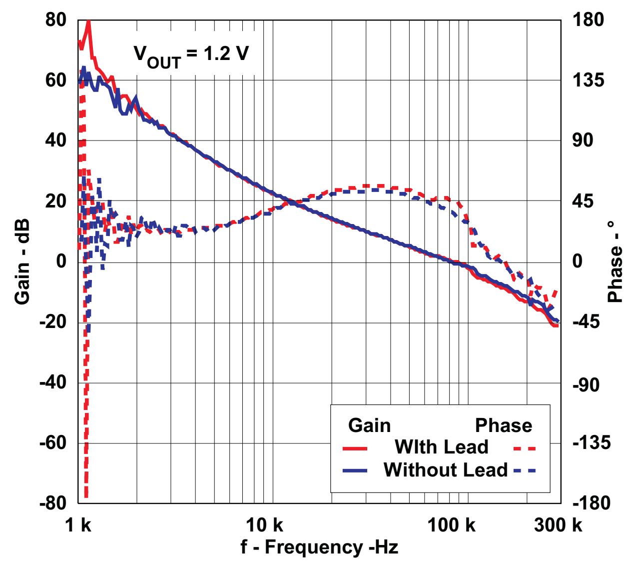


**Figure 49. Example 3 Loop Response**

# ADDITIONAL REFERENCES

## Related Devices

The following parts have characteristics similar to the TPS54386-Q1 and may be of interest.

**Table 6. Devices Related to the TPS54386-Q1**

| TI LITERATURE NUMBER | DEVICE | DESCRIPTION |
|---|---|---|
| SLUS642 | TPS40222 | 5-V input, 1.6-A non-synchronous buck converter |
| SLUS749 | TPS54283 / TPS54286 | 2-A dual non-synchronous converter with integrated high-side MOSFET |

## References

These references, design tools, and links to additional references, including design software, may be found at http:www.power.ti.com

**Table 7. References**

| TI LITERATURE NUMBER | DESCRIPTION |
|---|---|
| SLMA002 | PowerPAD Thermally Enhanced Package Application Report |
| SLMA004 | PowerPAD™ Made Easy |
| SLUP206 | Under the Hood Of Low Voltage DC/DC Converters. SEM1500 Topic 5, 2002 Seminar Series |
| SLVA057 | Understanding Buck Power Stages in Switchmode Power Supplies |
| SLUP173 | Designing Stable Control Loops. SEM 1400, 2001 Seminar Series |

## Package Outline and Recommended PCB Footprint

The following pages outline the mechanical dimensions of the 14-Pin PWP package and provide recommendations for PCB layout.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS54386TPWPRQ1 | ACTIVE | HTSSOP | PWP | 14 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 105 | 54386T | Samples |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

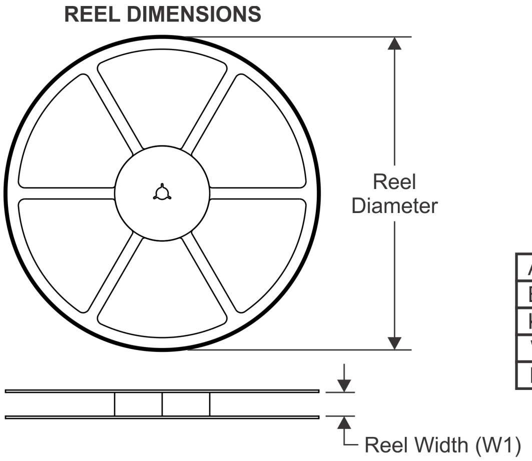
**OTHER QUALIFIED VERSIONS OF TPS54386-Q1 :**

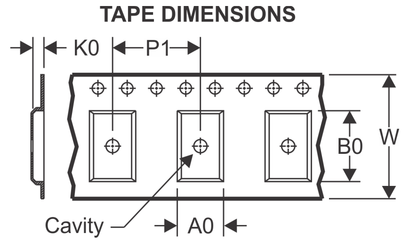
- Catalog: TPS54386

NOTE: Qualified Version Definitions:

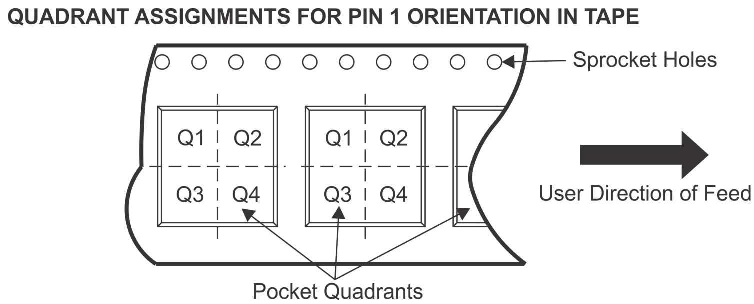
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



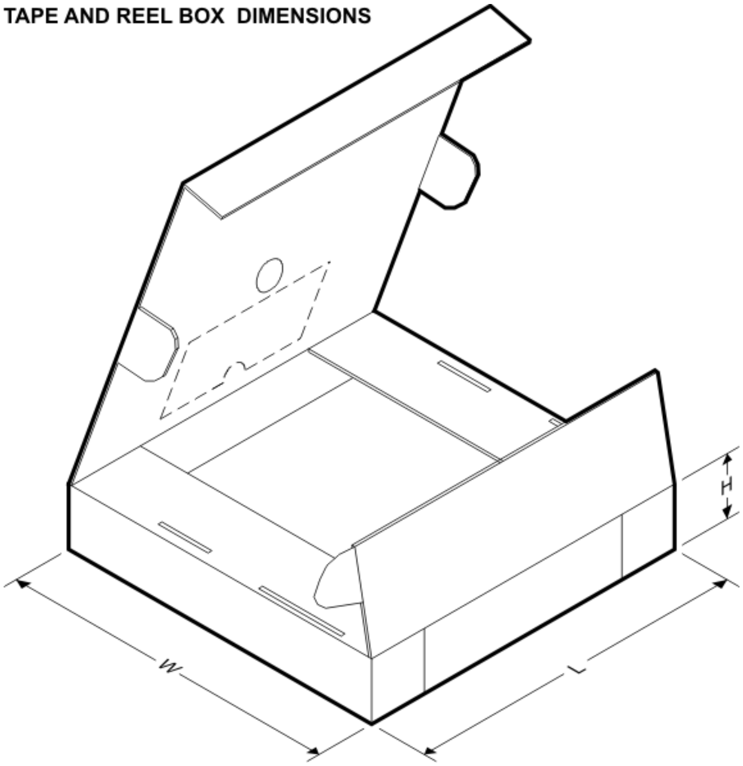

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS54386TPWPRQ1 | HTSSOP | PWP | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

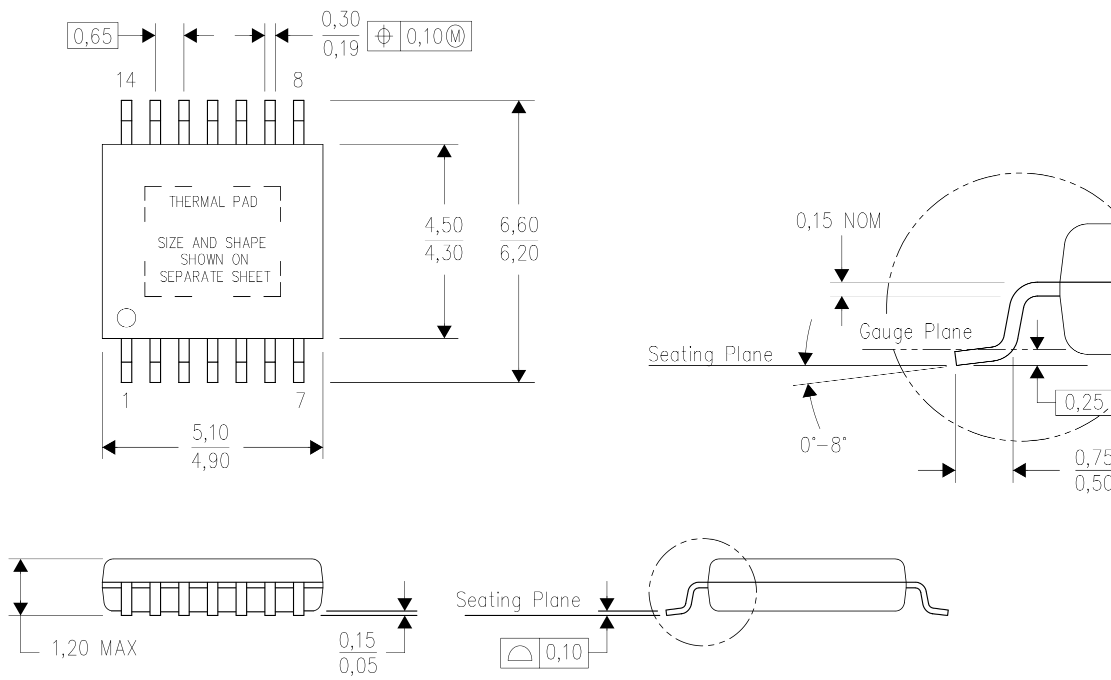
## TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS54386TPWPRQ1 | HTSSOP | PWP | 14 | 2000 | 350.0 | 350.0 | 43.0 |

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE




4073225–2/I 05/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

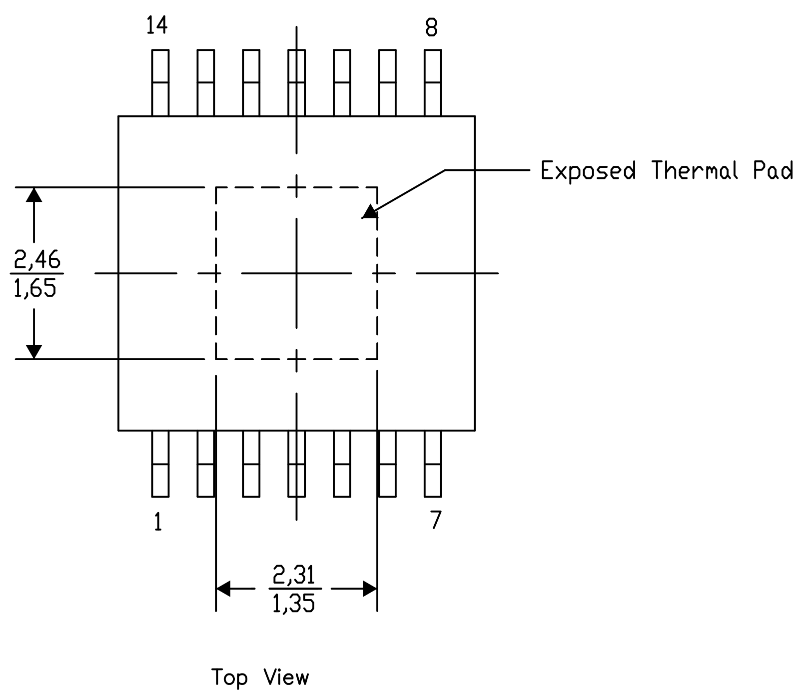
## PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



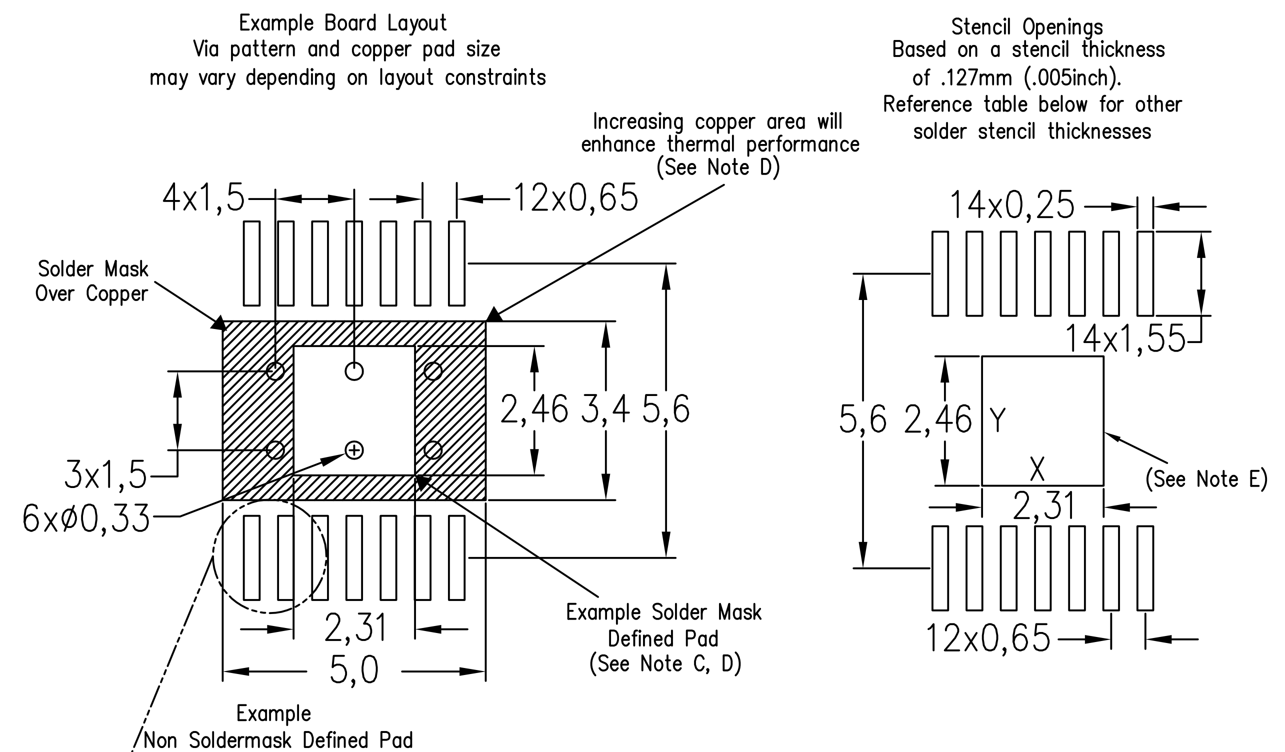

Exposed Thermal Pad Dimensions

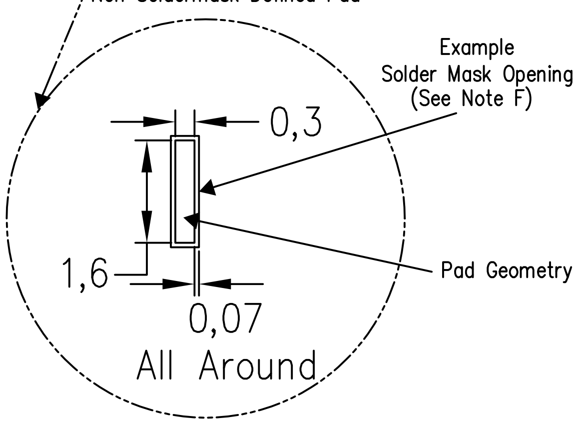
4206332–2/A0 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

## PWP (R-PDSO-G14) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 2.5 | 2.65 |
| 0.127mm | 2.31 | 2.46 |
| 0.152mm | 2.15 | 2.3 |
| 0.178mm | 2.05 | 2.15 |

4207609-2/W 09/15

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.