



### High Efficiency, Sine Amplitude Converter™

#### FEATURES

- 48 Vdc to 1.5 Vdc 50 A current multiplier
  - Operating from standard 48 V or 24 V PRM modules
- High efficiency (>89%) reduces system power consumption
- High density (334 A/in<sup>3</sup>)
- “Half Chip” VI Chip<sup>®</sup> package enables surface mount, low impedance interconnect to system board
- Contains built-in protection features against:
  - Overvoltage
  - Overcurrent
  - Short Circuit
  - Overtemperature
- Provides enable/disable control, internal temperature monitoring, current monitoring
- ZVS/ZCS resonant Sine Amplitude Converter topology
- Less than 50°C temperature rise at full load in typical applications

#### TYPICAL APPLICATIONS

- High End Computing Systems
- Automated Test Equipment
- High Density Power Supplies
- Communications Systems

#### DESCRIPTION

The VI Chip current multiplier is a high efficiency (>89%) Sine Amplitude Converter™ (SAC™) operating from a 26 to 55 Vdc primary bus to deliver an isolated output. The Sine Amplitude Converter offers a low AC impedance beyond the bandwidth of most downstream regulators, which means that capacitance normally at the load can be located at the input to the Sine Amplitude Converter. Since the K factor of the VTM48EH015T050A00 is 1/32, that capacitance value can be reduced by a factor of 1024, resulting in savings of board area, materials and total system cost.

The VTM48EH015T050A00 is provided in a VI Chip package compatible with standard pick-and-place and surface mount assembly processes. The co-molded VI Chip package provides enhanced thermal management due to large thermal interface area and superior thermal conductivity. With high conversion efficiency the VTM48EH015T050A00 increases overall system efficiency and lowers operating costs compared to conventional approaches.

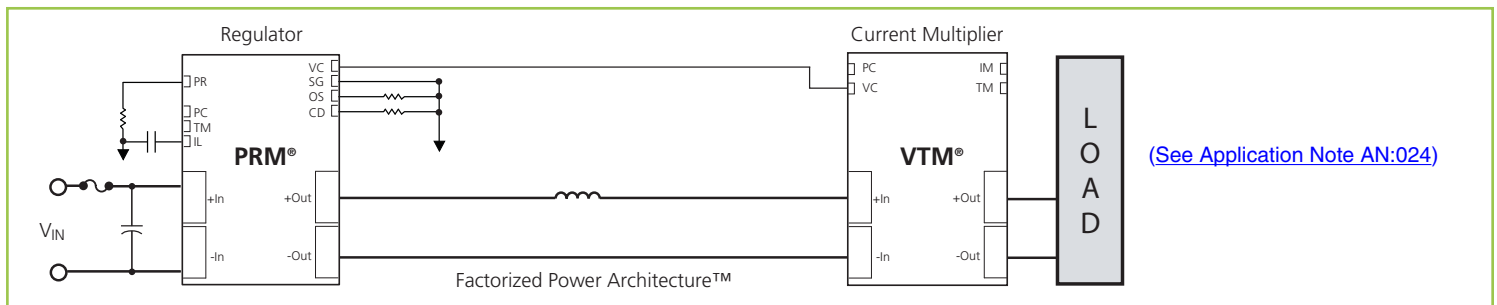
The VTM48EH015T050A00 enables the utilization of Factorized Power Architecture providing efficiency and size benefits by lowering conversion and distribution losses and promoting high density point of load conversion.

$V_{IN} = 26 \text{ to } 55 \text{ V}$	$I_{OUT} = 50 \text{ A}_{(NOM)}$
$V_{OUT} = 0.8 \text{ to } 1.7 \text{ V}_{(NO \text{ LOAD})}$	$K = 1/32$

#### PART NUMBERING

PART NUMBER	PRODUCT GRADE
VTM48EH015 x 050A00	T = -40° to 125°C
	M = -55° to 125°C

*For Storage and Operating Temperatures see Section 6.0 General Characteristics*



## 1.0 ABSOLUTE MAXIMUM VOLTAGE RATINGS

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

	MIN	MAX	UNIT		MIN	MAX	UNIT
+ IN to - IN	-1.0	60	V <sub>DC</sub>	IM to - IN	0	3.15	V <sub>DC</sub>
PC to - IN	-0.3	20	V <sub>DC</sub>	+ IN / - IN to + OUT / - OUT (hipot)		2250	V <sub>DC</sub>
TM to -IN	-0.3	7	V <sub>DC</sub>	+ OUT to - OUT	-1.0	4	V <sub>DC</sub>
VC to - IN	-0.3	20	V <sub>DC</sub>				

## 2.0 ELECTRICAL CHARACTERISTICS

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of **-40°C < T<sub>J</sub> < 125°C (T-Grade)**; All other specifications are at **T<sub>J</sub> = 25°C** unless otherwise noted.

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
Input Voltage Range	V <sub>IN</sub>	No external VC applied	<b>26</b>		<b>55</b>	V <sub>DC</sub>
		VC applied	<b>0</b>		<b>55</b>	
V <sub>IN</sub> Slew Rate	dV <sub>IN</sub> /dt				<b>1</b>	V/μs
V <sub>IN</sub> UV Turn Off	V <sub>IN_UV</sub>	Module latched shutdown, No external VC applied, I <sub>OUT</sub> = 50A		16.2	<b>26.0</b>	V
No Load power dissipation	P <sub>NL</sub>	V <sub>IN</sub> = 42 V	<b>1.2</b>		<b>5.0</b>	W
		V <sub>IN</sub> = 26 V to 55 V			<b>7.1</b>	
		V <sub>IN</sub> = 42 V, T <sub>C</sub> = 25°C		2.6	3.5	
		V <sub>IN</sub> = 26 V to 55 V, T <sub>C</sub> = 25°C			4.8	
Inrush current peak	I <sub>INRP</sub>	VC enable, V <sub>IN</sub> = 42 V C <sub>OUT</sub> = 5000 μF, R <sub>LOAD</sub> = 28 mΩ		2.5	<b>10</b>	A
DC input current	I <sub>IN_DC</sub>				<b>1.8</b>	A
Transfer ratio	K	K = V <sub>OUT</sub> /V <sub>IN</sub> , I <sub>OUT</sub> = 0 A		1/32		V/V
Output voltage	V <sub>OUT</sub>	V <sub>OUT</sub> = V <sub>IN</sub> • K - I <sub>OUT</sub> • R <sub>OUT</sub> , Section 11				V
Output current (average)	I <sub>OUT_AVG</sub>				<b>50</b>	A
Output current (peak)	I <sub>OUT_PK</sub>	T <sub>PEAK</sub> < 10 ms, I <sub>OUT_AVG</sub> ≤ 50 A			<b>75</b>	A
Output power (average)	P <sub>OUT_AVG</sub>	I <sub>OUT_AVG</sub> ≤ 50 A			<b>80</b>	W
Efficiency (ambient)	η <sub>AMB</sub>	V <sub>IN</sub> = 42 V, I <sub>OUT</sub> = 50 A	87.2	88.6		%
		V <sub>IN</sub> = 26 V to 55 V, I <sub>OUT</sub> = 50 A	83.0			
		V <sub>IN</sub> = 42 V, I <sub>OUT</sub> = 25 A	86.3	88.0		
Efficiency (hot)	η <sub>HOT</sub>	V <sub>IN</sub> = 42 V, T <sub>C</sub> = 100°C, I <sub>OUT</sub> = 50 A	87.0	88.3		%
Efficiency (Over load range)	η <sub>20%</sub>	10 A < I <sub>OUT</sub> < 50 A	<b>70.0</b>			%
Output resistance (Cold)	R <sub>OUT_COLD</sub>	T <sub>C</sub> = -40°C, I <sub>OUT</sub> = 50 A	1.2	1.5	1.8	mΩ
Output resistance (Ambient)	R <sub>OUT_AMB</sub>	T <sub>C</sub> = 25°C, I <sub>OUT</sub> = 50 A	1.5	1.8	2.2	mΩ
Output resistance (Hot)	R <sub>OUT_HOT</sub>	T <sub>C</sub> = 100°C, I <sub>OUT</sub> = 50 A	1.9	2.2	2.5	mΩ
Switching frequency	F <sub>SW</sub>		<b>1.30</b>	1.45	<b>1.60</b>	MHz
Output ripple frequency	F <sub>SW_RP</sub>		<b>2.60</b>	2.90	<b>3.20</b>	MHz
Output voltage ripple	V <sub>OUT_PP</sub>	C <sub>OUT</sub> = 0 F, I <sub>OUT</sub> = 50 A, V <sub>IN</sub> = 42 V, 20 MHz BW, Section 12		155	<b>300</b>	mV
Output inductance (parasitic)	L <sub>OUT_PAR</sub>	Frequency up to 30 MHz, Simulated J-lead model		600		pH
Output capacitance (internal)	C <sub>OUT_INT</sub>	V <sub>OUT</sub> = 1.5 V		130		μF
Output capacitance (external)	C <sub>OUT_EXT</sub>	VTM Standalone Operation V <sub>IN</sub> pre-applied, VC enable			<b>5000</b>	μF
<b>PROTECTION</b>						
OVLO	V <sub>IN_OVLO+</sub>	Module latched shutdown	<b>55.5</b>	57.7	<b>59.8</b>	V
Overvoltage lockout response time	T <sub>OVLO</sub>	Effective internal RC filter		2.4		μs
Output overcurrent trip	I <sub>OCP</sub>		<b>60</b>	75	<b>100</b>	A
Short circuit protection trip current	I <sub>SCP</sub>		75			A
Output overcurrent response time constant	T <sub>OCP</sub>	Effective internal RC filter (Integrative).		8		ms
Short circuit protection response time	T <sub>SCP</sub>	From detection to cessation of switching (Instantaneous)		1		μs
Thermal shutdown setpoint	T <sub>J_OTP</sub>		125	130	135	°C

### 3.0 SIGNAL CHARACTERISTICS

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of  $-40^{\circ}\text{C} < T_j < 125^{\circ}\text{C}$  (T-Grade); All other specifications are at  $T_j = 25^{\circ}\text{C}$  unless otherwise noted.

#### VTM CONTROL : VC

- Used to wake up powertrain circuit.
- A minimum of 12 V must be applied indefinitely for  $V_{IN} < 26\text{ V}$  to ensure normal operation.
- VC slew rate must be within range for a successful start.
- PRM<sup>®</sup> VC can be used as valid wake-up signal source.
- VC voltage may be continuously applied; there will be minimal VC current drawn when  $V_{IN} > 26\text{ V}$  and  $VC < 13$ .
- Internal resistance used in adaptive loop compensation

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG INPUT	Steady	External VC voltage	$V_{VC\_EXT}$	Required for startup, and operation below 26 V. See Section 7.	<b>12</b>		<b>16.5</b>	V
		VC current draw threshold	$V_{VC\_TH}$	Low VC current draw for $V_{IN} > 26\text{ V}$		13		V
		VC current draw	$I_{VC}$	VC = 13 V, $V_{IN} = 0\text{ V}$ VC = 13 V, $V_{IN} > 26\text{ V}$ VC = 16.5 V, $V_{IN} > 26\text{ V}$		90	<b>150</b>	mA
		VC internal resistor	$R_{VC\_INT}$			6		
	Start Up	VC slew rate	$dVC/dt$	Required for proper startup;	<b>0.02</b>		<b>0.25</b>	V/ $\mu\text{s}$
		VC inrush current	$I_{INR\_VC}$	VC = 16.5 V, $dVC/dt = 0.25\text{ V}/\mu\text{s}$			<b>750</b>	mA
	Transitional	VC output turn-on delay	$T_{ON}$	$V_{IN}$ pre-applied, PC floating, VC enable $C_{PC} = 0\ \mu\text{F}$ , $C_{OUT} = 5000\ \mu\text{F}$			<b>500</b>	$\mu\text{s}$
		VC to PC delay	$T_{VC\_PC}$	VC = 12 V to PC high, $V_{IN} = 0\text{ V}$ , $dVC/dt = 0.25\text{ V}/\mu\text{s}$		10	<b>25</b>	$\mu\text{s}$
Internal VC capacitance		$C_{VC\_INT}$	VC = 0 V		2.2		$\mu\text{F}$	

#### PRIMARY CONTROL : PC

- The PC pin enables and disables the VTM. When held below 2 V, the VTM will be disabled.
- PC pin outputs 5 V during normal operation. PC pin is equal to 2.5 V during fault mode given  $V_{IN} > 26\text{ V}$  and  $VC > 12\text{ V}$ .
- After successful start-up and under no fault condition, PC can be used as a 5 V regulated voltage source with a 2 mA maximum current.
- Module will shutdown when pulled low with an impedance less than 400  $\Omega$ .
- In an array of VTMs, connect PC pin to synchronize startup.
- PC pin cannot sink current and will not disable other module during fault mode.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG OUTPUT	Steady	PC voltage	$V_{PC}$		<b>4.7</b>	5.0	<b>5.3</b>	V
		PC source current	$I_{PC\_OP}$				2	mA
		PC resistance (internal)	$R_{PC\_INT}$	Internal pull down resistor	<b>50</b>	150	<b>400</b>	$k\Omega$
	Start Up	PC source current	$I_{PC\_EN}$		<b>50</b>	100	<b>300</b>	$\mu\text{A}$
		PC capacitance (internal)	$C_{PC\_INT}$	Section 7			<b>50</b>	pF
DIGITAL INPUT / OUTPUT	Enable	PC resistance (external)	$R_{PC\_EXT}$		<b>60</b>			$k\Omega$
		PC voltage (enable)	$V_{PC\_EN}$		<b>2</b>	2.5	<b>3</b>	V
	Disable	PC voltage (disable)	$V_{PC\_DIS}$				<b>2</b>	V
		PC pull down current	$I_{PC\_PD}$		<b>5.1</b>			mA
	Transitional	PC disable time	$T_{PC\_DIS\_T}$			4		$\mu\text{s}$
		PC fault response time	$T_{FR\_PC}$	From fault to PC = 2 V		100		$\mu\text{s}$

#### TEMPERATURE MONITOR : TM

- The TM pin monitors the internal temperature of the VTM controller IC within an accuracy of  $\pm 5^{\circ}\text{C}$ .
- Can be used as a "Power Good" flag to verify that the VTM is operating.
- The TM pin has a room temperature setpoint of 3 V (@27°C) and approximate gain of 10 mV/°C.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG OUTPUT	Steady	TM voltage	$V_{TM\_AMB}$	$T_j$ controller = 27°C	2.95	3.00	3.05	V
		TM source current	$I_{TM}$				<b>100</b>	$\mu\text{A}$
		TM gain	$A_{TM}$			10		mV/°C
		TM voltage ripple	$V_{TM\_PP}$	$C_{TM} = 0\text{ F}$ , $V_{IN} = 42\text{ V}$ , $I_{OUT} = 50\text{ A}$			120	<b>200</b>
DIGITAL OUTPUT (FAULT FLAG)	Disable	TM voltage	$V_{TM\_DIS}$			0		V
		TM resistance (internal)	$R_{TM\_INT}$	Internal pull down resistor	<b>25</b>	40	<b>50</b>	$k\Omega$
	Transitional	TM capacitance (external)	$C_{TM\_EXT}$				<b>50</b>	pF
		TM fault response time	$T_{FR\_TM}$	From fault to TM = 1.5 V		10		$\mu\text{s}$

### 3.0 SIGNAL CHARACTERISTICS (CONT.)

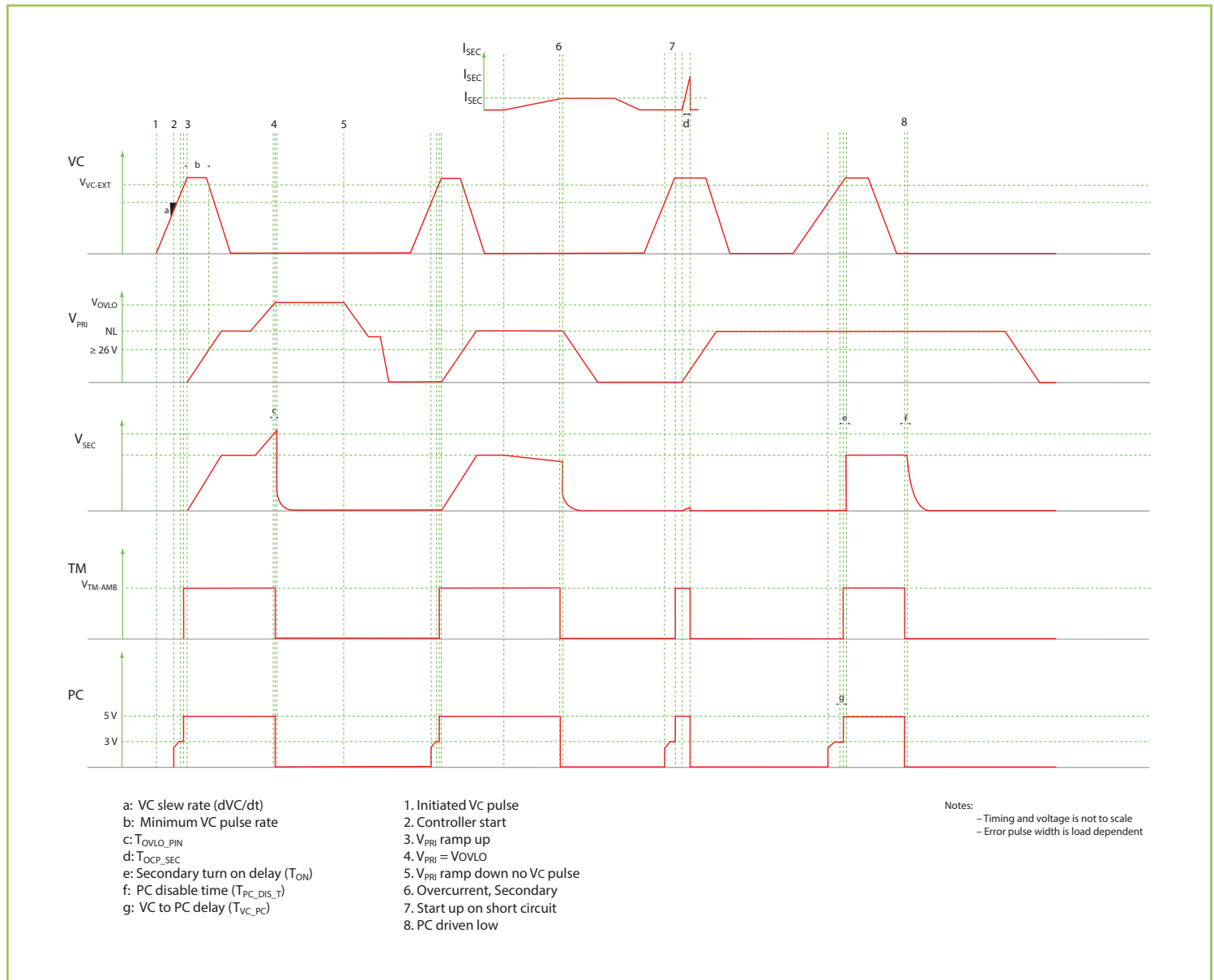
Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of  $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$  (T-Grade); All other specifications are at  $T_J = 25^{\circ}\text{C}$  unless otherwise noted.

#### CURRENT MONITOR : IM

- The nominal IM pin voltage varies between 0.39 V and 1.86 V representing the output current within  $\pm 25\%$  under all operating line temperature conditions between 50% and 100%.
- The IM pin provides a DC analog voltage proportional to the output current of the VTM.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG OUTPUT	Steady	IM voltage (no load)	$V_{IM\_NL}$	$T_C = 25^{\circ}\text{C}, V_{IN} = 42\text{ V}, I_{OUT} = 0\text{ A}$	0.25	0.39	0.49	V
		IM voltage (50%)	$V_{IM\_50\%}$	$T_C = 25^{\circ}\text{C}, V_{IN} = 42\text{ V}, I_{OUT} = 25\text{ A}$		0.98		V
		IM voltage (full load)	$V_{IM\_FL}$	$T_C = 25^{\circ}\text{C}, V_{IN} = 42\text{ V}, I_{OUT} = 50\text{ A}$		1.86		V
		IM gain	$A_{IM}$	$T_C = 25^{\circ}\text{C}, V_{IN} = 42\text{ V}, I_{OUT} > 25\text{ A}$		35.2		mV/A
		IM resistance (external)	$R_{IM\_EXT}$			<b>2.5</b>		

### 4.0 TIMING DIAGRAM



5.0 APPLICATION CHARACTERISTICS

The following values, typical of an application environment, are collected at  $T_C = 25^\circ\text{C}$  unless otherwise noted. See associated figures for general trend data.

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	TYP	UNIT
No load power dissipation	$P_{NL}$	$V_{IN} = 42\text{ V}$	3.1	W
Efficiency (ambient)	$\eta_{AMB}$	$V_{IN} = 42\text{ V}, I_{OUT} = 50\text{ A}$	88.6	%
Efficiency (hot)	$\eta_{HOT}$	$V_{IN} = 42\text{ V}, I_{OUT} = 50\text{ A}, T_C = 100^\circ\text{C}$	88.0	%
Output resistance (ambient)	$R_{OUT\_AMB}$	$V_{IN} = 42\text{ V}, I_{OUT} = 50\text{ A}$	1.8	$\text{m}\Omega$
Output resistance (hot)	$R_{OUT\_HOT}$	$V_{IN} = 42\text{ V}, I_{OUT} = 50\text{ A}, T_C = 100^\circ\text{C}$	2.2	$\text{m}\Omega$
Output resistance (cold)	$R_{OUT\_COLD}$	$V_{IN} = 42\text{ V}, I_{OUT} = 50\text{ A}, T_C = -40^\circ\text{C}$	1.5	$\text{m}\Omega$
Output voltage ripple	$V_{OUT\_PP}$	$C_{OUT} = 0\text{ F}, I_{OUT} = 50\text{ A}, V_{IN} = 42\text{ V}, 20\text{ MHz BW, Section 12}$	235	mV
$V_{OUT}$ Transient (positive)	$V_{OUT\_TRAN+}$	$I_{OUT\_STEP} = 0\text{ A to } 50\text{ A}, V_{IN} = 42\text{ V}, I_{SLEW} > 10\text{ A/us}$	20	mV
$V_{OUT}$ Transient (negative)	$V_{OUT\_TRAN-}$	$I_{OUT\_STEP} = 50\text{ A to } 0\text{ A}, V_{IN} = 42\text{ V}, I_{SLEW} > 10\text{ A/us}$	20	mV

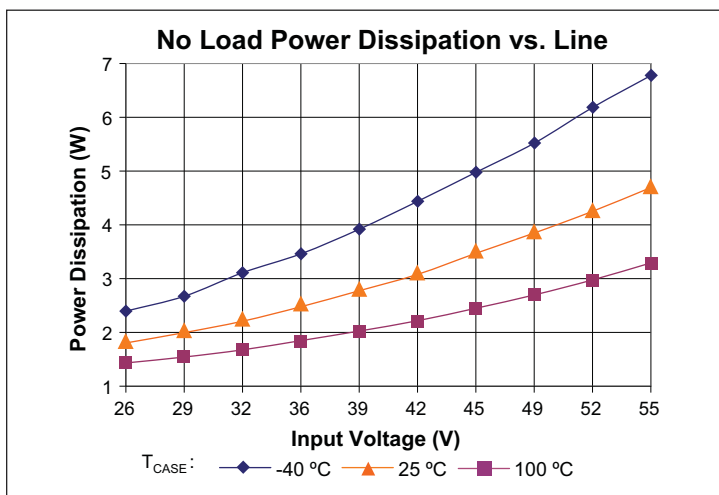


Figure 1 — No load power dissipation vs.  $V_{IN}$

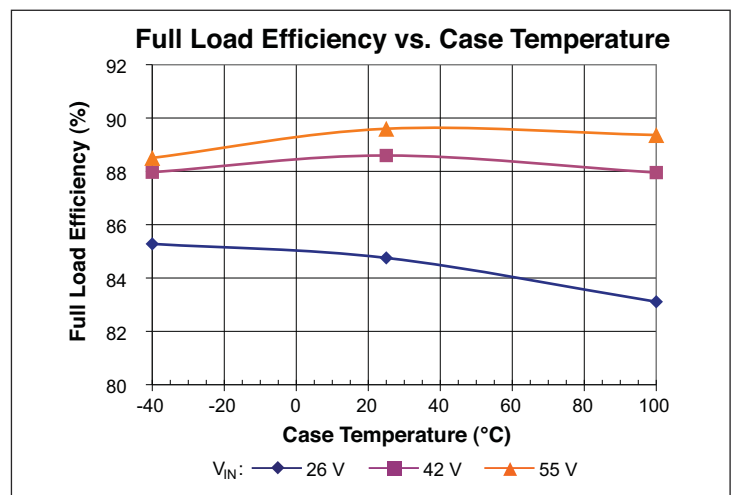


Figure 2 — Full load efficiency vs. temperature

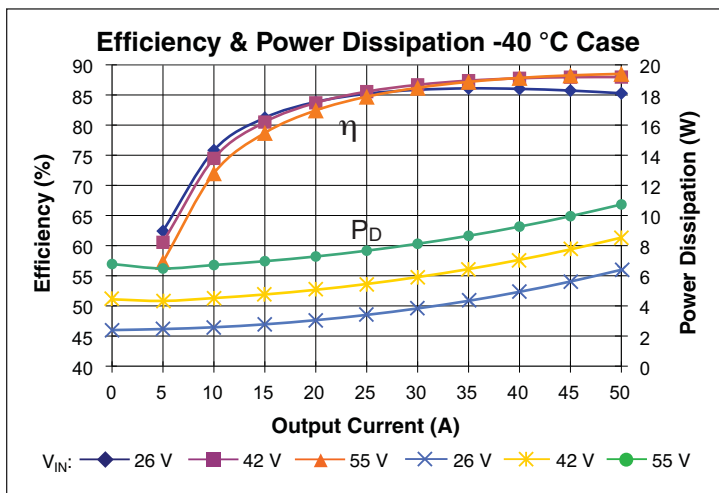


Figure 3 — Efficiency and power dissipation at  $-40^\circ\text{C}$

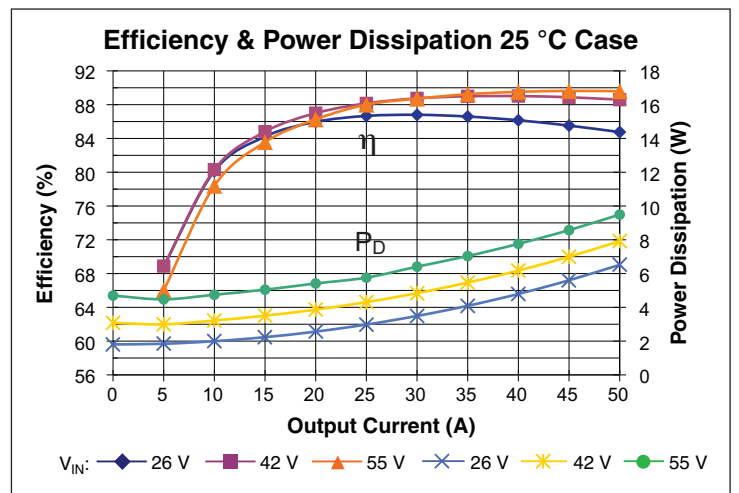


Figure 4 — Efficiency and power dissipation at  $25^\circ\text{C}$

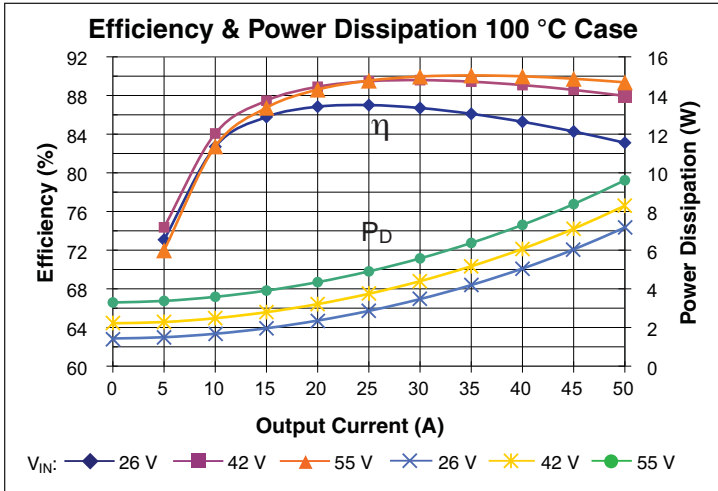


Figure 5 — Efficiency and power dissipation at 100°C

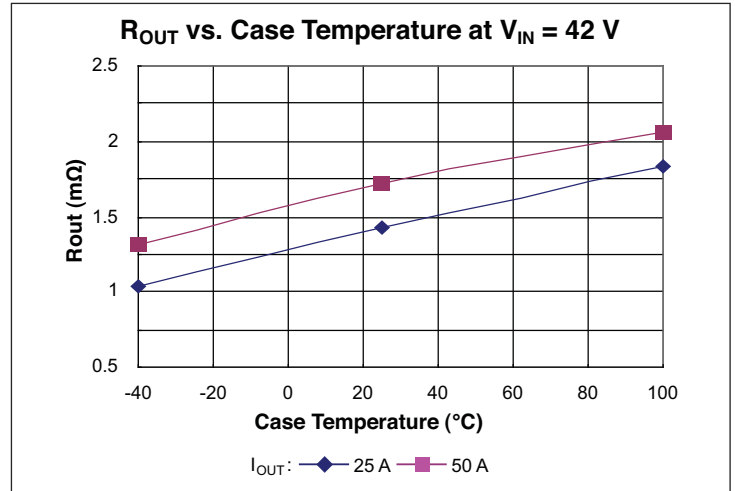


Figure 6 —  $R_{OUT}$  vs. temperature

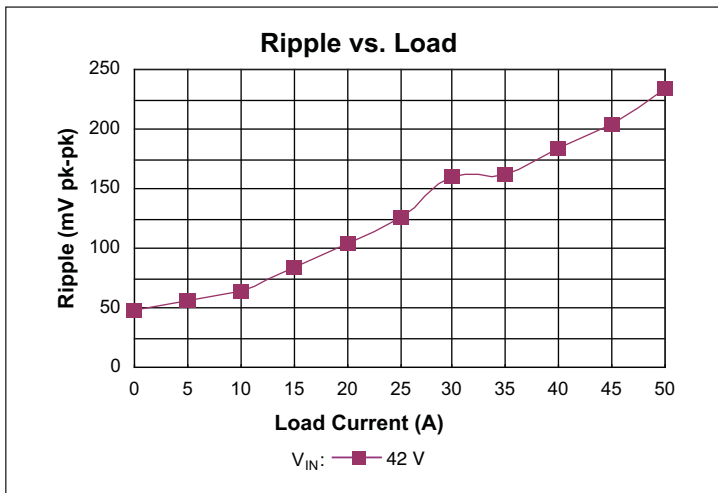


Figure 7 —  $V_{RIPPLE}$  vs.  $I_{OUT}$ ; No external  $C_{OUT}$ . Board mounted module, scope setting: 20 MHz analog BW

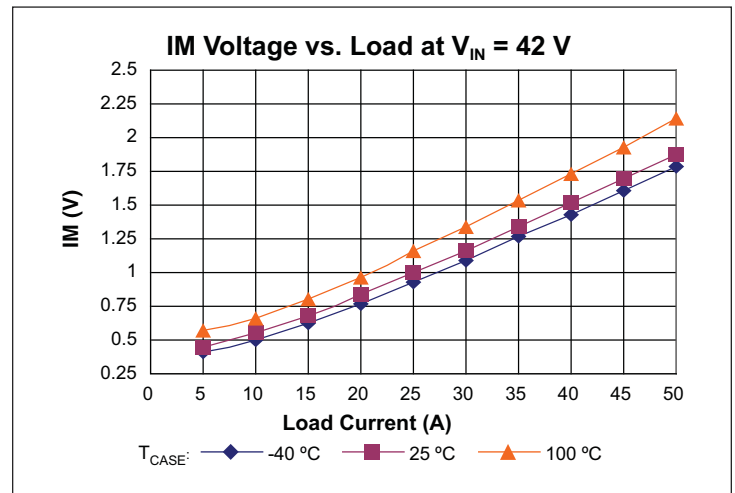


Figure 8 — IM voltage vs. load

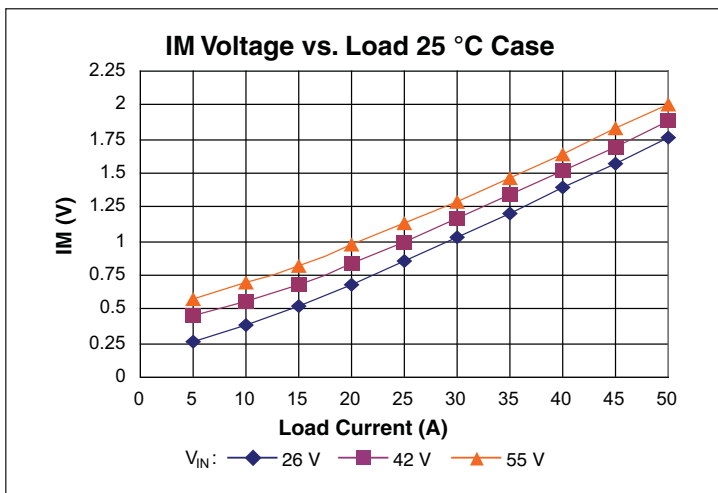


Figure 9 — IM voltage vs. load

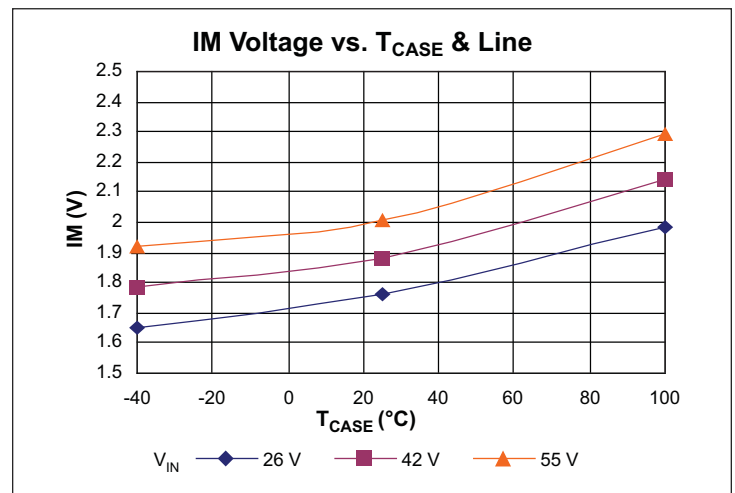


Figure 10 — Full load IM voltage vs.  $T_{CASE}$

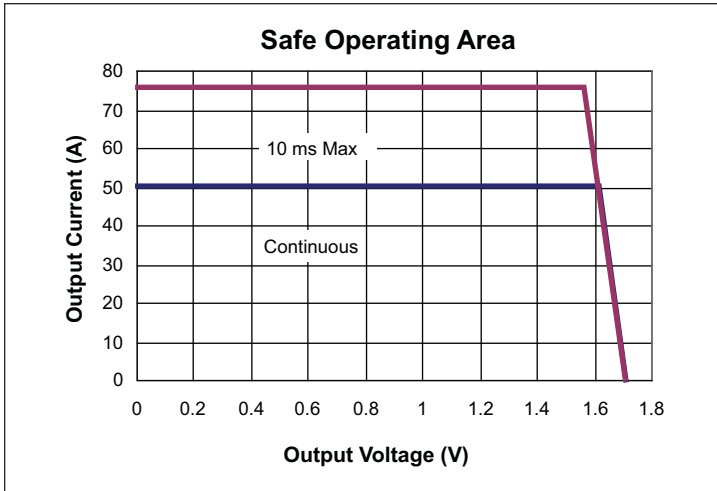


Figure 11 — Safe operating area

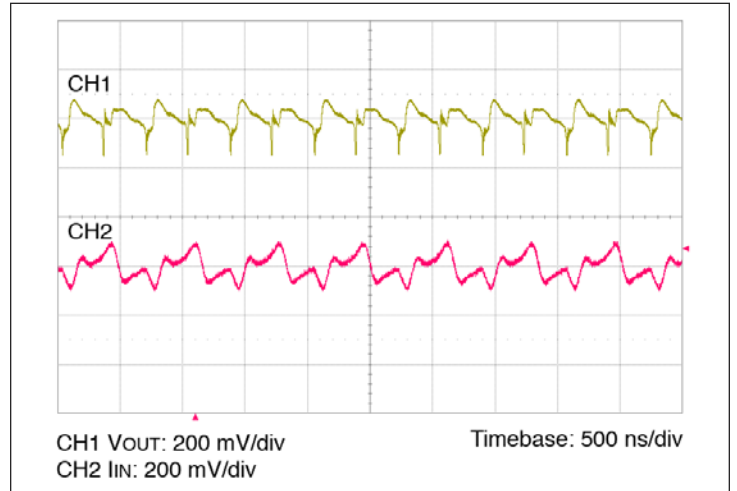


Figure 12 — Full load ripple, 100  $\mu$ F  $C_{IN}$ ; No external  $C_{OUT}$ . Board mounted module, scope setting : 20 MHz analog BW

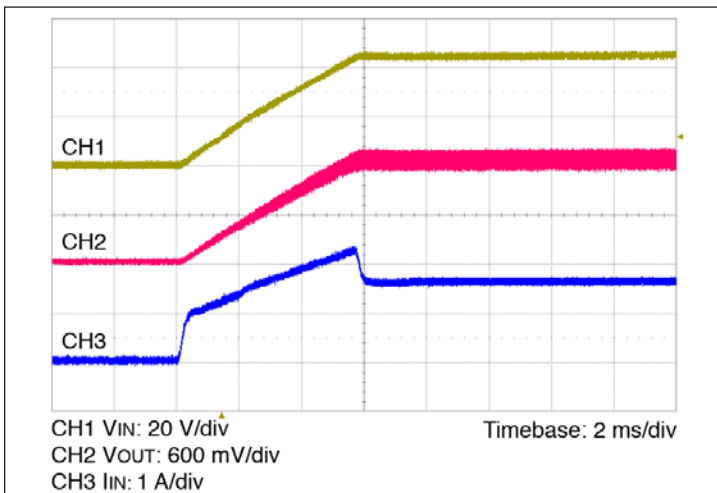


Figure 13 — Start up from application of  $V_{IN}$ ; VC pre-applied  $C_{OUT} = 0 \mu$ F

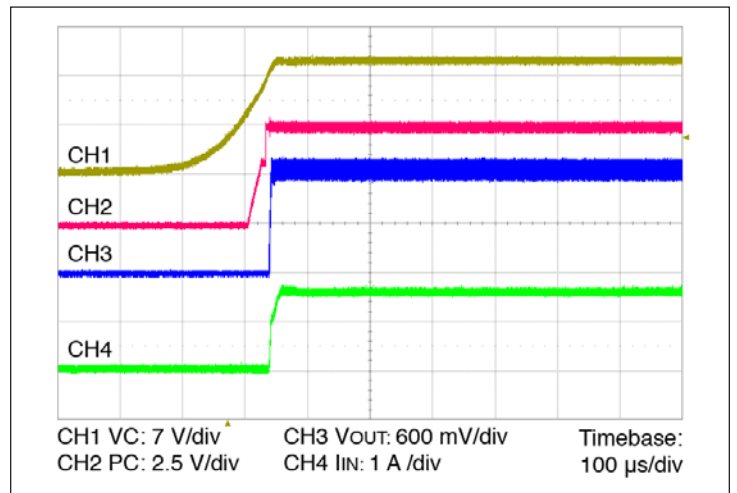


Figure 14 — Start up from application of VC;  $V_{IN}$  pre-applied  $C_{OUT} = 0 \mu$ F

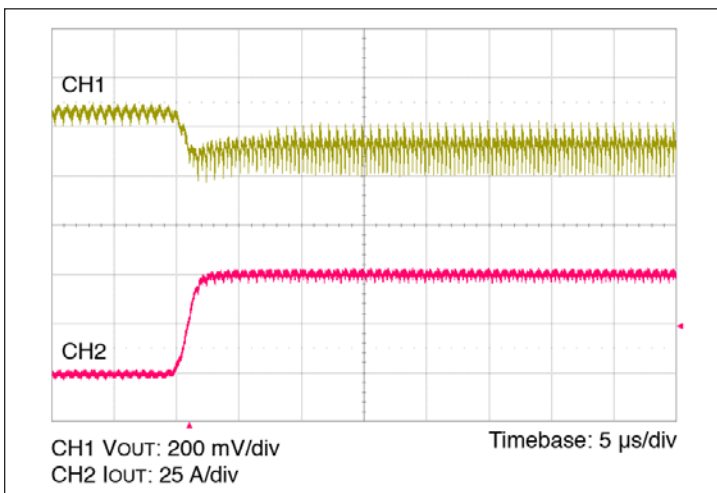


Figure 15 — 0 A – 50 A transient response:  $C_{IN} = 100 \mu$ F, no external  $C_{OUT}$

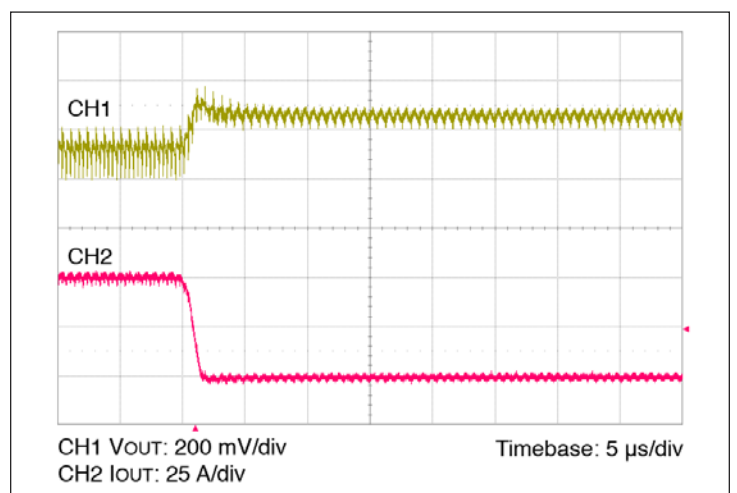


Figure 16 — 50 A – 0 A transient response:  $C_{IN} = 100 \mu$ F, no external  $C_{OUT}$

## 6.0 GENERAL CHARACTERISTICS

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of  $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$  (T-Grade); All Other specifications are at  $T_J = 25^{\circ}\text{C}$  unless otherwise noted.

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
<b>MECHANICAL</b>						
Length	L		21.7 / [0.85]	22.0 / [0.87]	22.3 / [0.88]	mm/[in]
Width	W		16.4 / [0.64]	16.5 / [0.65]	16.6 / [0.66]	mm/[in]
Height	H		6.48 / [0.255]	6.73 / [0.265]	6.98 / [0.275]	mm/[in]
Volume	Vol	No heat sink		2.44 / [0.150]		cm <sup>3</sup> /[in <sup>3</sup> ]
Weight	W			8.0 / 0.28		g/[oz]
Lead finish		Nickel	0.51		2.03	$\mu\text{m}$
		Palladium	0.02		0.15	
		Gold	0.003		0.051	
<b>THERMAL</b>						
Operating temperature	$T_J$	VTM48EH015T050A00 (T-Grade)	-40		125	$^{\circ}\text{C}$
		VTM48EH015M050A00 (M-Grade)	-55		125	$^{\circ}\text{C}$
Thermal capacity				5		Ws/ $^{\circ}\text{C}$
<b>ASSEMBLY</b>						
Peak compressive force Applied to case (Z-axis)		Supported by J-lead only		2.5	3	lbs
Storage temperature	$T_{ST}$	VTM48EH015T050A00 (T-Grade)	-40		125	$^{\circ}\text{C}$
		VTM48EH015M050A00 (M-Grade)	-65		125	$^{\circ}\text{C}$
ESD withstand	ESD <sub>HBM</sub>	Human Body Model, "JEDEC JESD 22-A114C.01 "	1500			$V_{DC}$
	ESD <sub>MM</sub>	Machine Model, "JEDEC JESD 22-A115-A"	400			
<b>SOLDERING</b>						
Peak temperature during reflow		MSL 4 (Datecode 1528 and later)			245	$^{\circ}\text{C}$
Peak time above 217 $^{\circ}\text{C}$					150	s
Peak heating rate during reflow				1.5	3	$^{\circ}\text{C}/\text{s}$
Peak cooling rate post reflow				1.5	6	$^{\circ}\text{C}/\text{s}$
<b>SAFETY</b>						
Isolation voltage (hipot)	$V_{HIPOT}$		<b>2250</b>			V <sub>bc</sub>
Isolation capacitance	$C_{IN\_OUT}$	Unpowered Unit	<b>1350</b>	1750	<b>2150</b>	pF
Isolation resistance	$R_{IN\_OUT}$		<b>10</b>			M $\Omega$
MTBF		MIL HDBK 217, 25 $^{\circ}\text{C}$ , Ground Benign		4.5		MHrs
Agency approvals/standards		cTUVus				
		cURus				
		CE Marked for low voltage directive and RoHS recast directive, as applicable				



## 7.0 USING THE CONTROL SIGNALS VC, PC, TM, IM

The **VTM Control (VC)** pin is an input pin which powers the internal VCC circuitry when within the specified voltage range of 12 V to 16.5 V. This voltage is required in order for the VTM module to start, and must be applied as long as the input is below 26 V. In order to ensure a proper start, the slew rate of the applied voltage must be within the specified range.

Some additional notes on the using the VC pin:

- In most applications, the VTM module will be powered by an upstream PRM® which provides a 10 ms VC pulse during startup. In these applications the VC pins of the PRM and VTM should be tied together.
- The VC voltage can be applied indefinitely allowing for continuous operation down to 0 V<sub>IN</sub>.
- The fault response of the VTM module is latching. A positive edge on VC is required in order to restart the unit. If VC is continuously applied the PC pin may be toggled to restart the module.

**Primary Control (PC)** pin can be used to accomplish the following functions:

- **Delayed start:** Upon the application of VC, the PC pin will source a constant 100 µA current to the internal RC network. Adding an external capacitor will allow further delay in reaching the 2.5 V threshold for module start.
- **Auxiliary voltage source:** Once enabled in regular operational conditions (no fault), each VTM PC provides a regulated 5 V, 2 mA voltage source.
- **Output disable:** PC pin can be actively pulled down in order to disable the module. Pull down impedance shall be lower than 400 Ω.
- **Fault detection flag:** The PC 5 V voltage source is internally turned off as soon as a fault is detected. It is important to notice that PC doesn't have current sink capability. Therefore, in an array, PC line will not be capable of disabling neighboring modules if a fault is detected.
- **Fault reset:** PC may be toggled to restart the unit if VC is continuously applied.

**Temperature Monitor (TM)** pin provides a voltage proportional to the absolute temperature of the converter control IC.

It can be used to accomplish the following functions:

- **Monitor the control IC temperature:** The temperature in Kelvin is equal to the voltage on the TM pin scaled by 100. (i.e. 3.0 V = 300 K = 27°C). If a heat sink is applied, TM can be used to thermally protect the system.
- **Fault detection flag:** The TM voltage source is internally turned off as soon as a fault is detected. For system monitoring purposes (microcontroller interface) faults are detected on falling edges of TM signal.

**Current Monitor (IM)** pin provides a voltage proportional to the output current of the VTM module. The nominal voltage will vary between 0.39 V and 1.86 V over the output current range of the module (See Figures 8–10). The accuracy of the IM pin will be within 25% under all line and temperature conditions between 50% and 100% load.

## 8.0 STARTUP BEHAVIOR

Depending on the sequencing of the VC with respect to the input voltage, the behavior during startup will vary as follows:

- **Normal Operation (VC applied prior to V<sub>IN</sub>):** In this case the controller is active prior to ramping the input. When the input voltage is applied, the VTM output voltage will track the input (See Figure 13). The inrush current is determined by the input voltage rate of rise and output capacitance. If the VC voltage is removed prior to the input reaching 26 V, the VTM module may shut down.
- **Stand Alone Operation (VC applied after V<sub>IN</sub>):** In this case the module output will begin to rise upon the application of the VC voltage (See Figure 14). The Adaptive Soft Start circuit (See Section 10) may vary the output rate of rise in order to limit the inrush current to its maximum level. When starting into high capacitance, or a short, the output current will be limited for a maximum of 900 µsec. After this period, the adaptive soft start circuit will time out and the module may shut down. No restart will be attempted until VC is re-applied, or PC is toggled. The maximum output capacitance is limited to 5000 µF in this mode of operation to ensure a successful start.

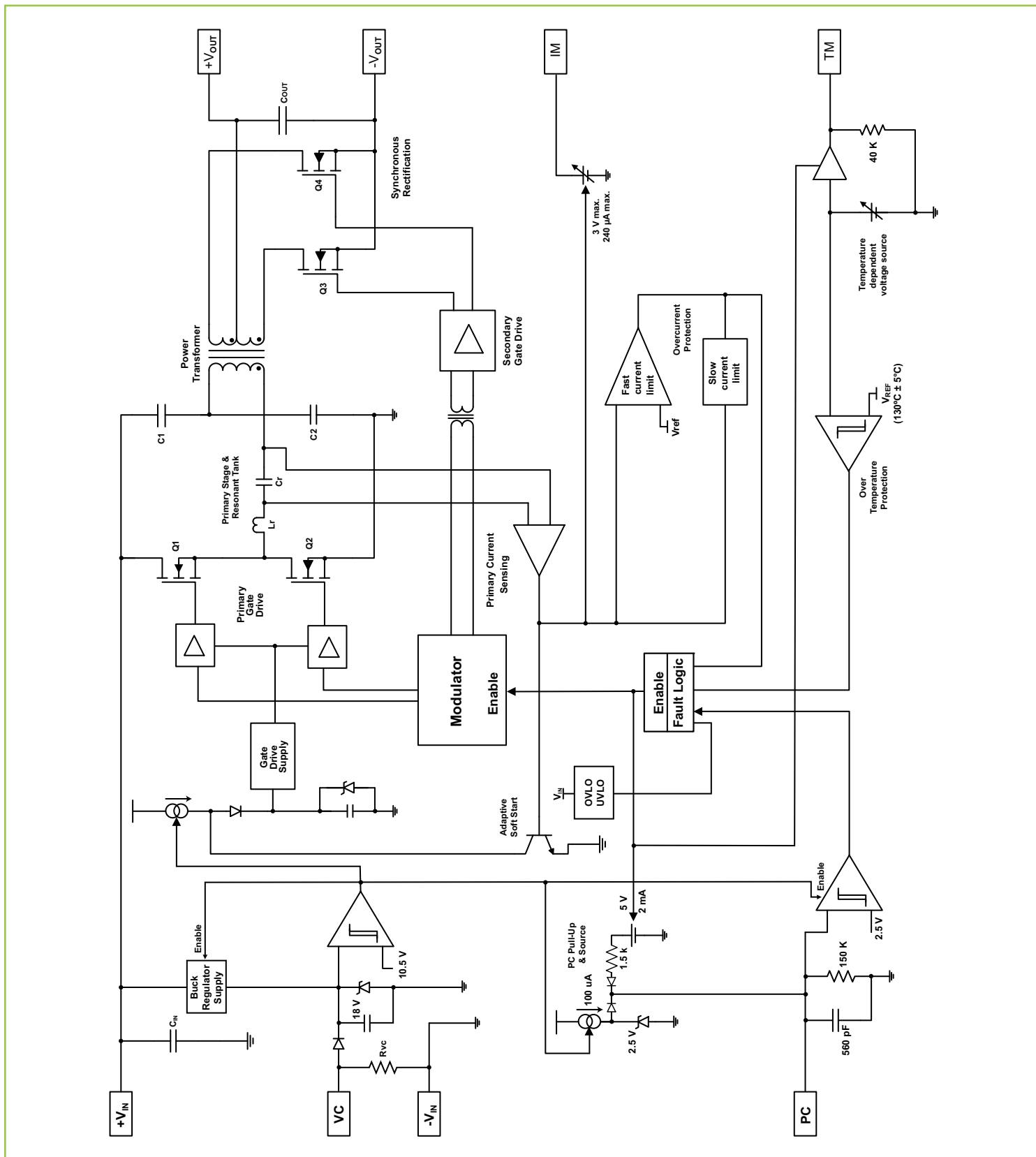
## 9.0 THERMAL CONSIDERATIONS

VI Chip® products are multi-chip modules whose temperature distribution varies greatly for each part number as well as with the input / output conditions, thermal management and environmental conditions. Maintaining the top of the VTM48EH015T050A00 case to less than 100°C will keep all junctions within the VI Chip below 125°C for most applications.

The percent of total heat dissipated through the top surface versus through the J-lead is entirely dependent on the particular mechanical and thermal environment. The heat dissipated through the top surface is typically 60%. The heat dissipated through the J-lead onto the PCB board surface is typically 40%. Use 100% top surface dissipation when designing for a conservative cooling solution.

It is not recommended to use a VI Chip module for an extended period of time at full load without proper heat sinking.

10.0 VTM MODULE BLOCK DIAGRAM



## 11.0 SINE AMPLITUDE CONVERTER™ POINT OF LOAD CONVERSION

The Sine Amplitude Converter (SAC™) uses a high frequency resonant tank to move energy from input to output. (The resonant tank is formed by Cr and leakage inductance Lr in the power transformer windings as shown in the VTM™ Module Block Diagram. See Section 10). The resonant LC tank, operated at high frequency, is amplitude modulated as

function of input voltage and output current. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieving power density.

The VTM48EH015T050A00 SAC can be simplified into the following model:

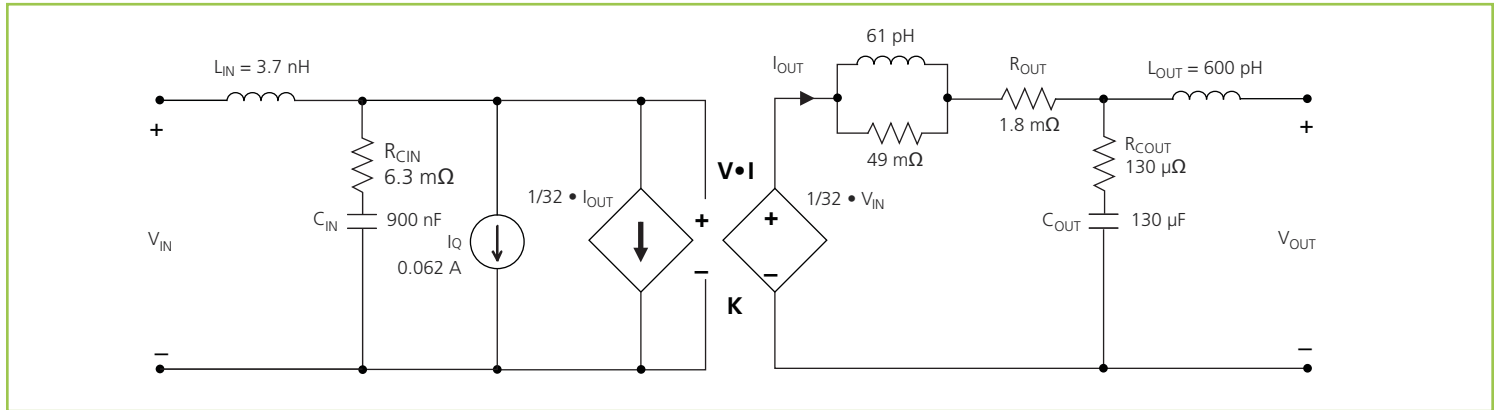


Figure 17 — VI Chip® module AC model

At no load:

$$V_{OUT} = V_{IN} \cdot K \quad (1)$$

K represents the “turns ratio” of the SAC.  
Rearranging Eq (1):

$$K = \frac{V_{OUT}}{V_{IN}} \quad (2)$$

In the presence of load,  $V_{OUT}$  is represented by:

$$V_{OUT} = V_{IN} \cdot K - I_{OUT} \cdot R_{OUT} \quad (3)$$

and  $I_{OUT}$  is represented by:

$$I_{OUT} = \frac{I_{IN} - I_Q}{K} \quad (4)$$

$R_{OUT}$  represents the impedance of the SAC, and is a function of the  $R_{DS(ON)}$  of the input and output MOSFETs and the winding resistance of the power transformer.  $I_Q$  represents the quiescent current of the SAC control and gate drive circuitry. The use of DC voltage transformation provides additional interesting attributes. Assuming for the moment that

$R_{OUT} = 0 \Omega$  and  $I_Q = 0 A$ , Eq. (3) now becomes Eq. (1) and is essentially load independent. A resistor R is now placed in series with  $V_{IN}$  as shown in Figure 18.

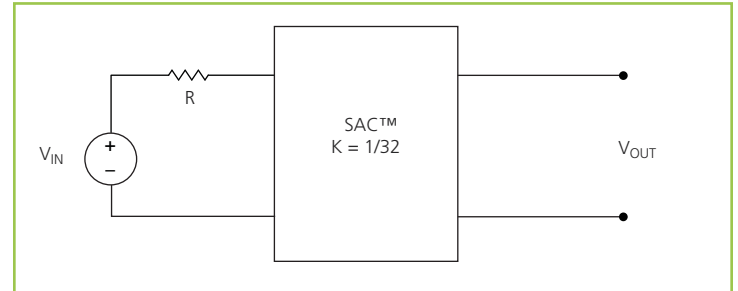


Figure 18 —  $K = 1/32$  Sine Amplitude Converter™ with series input resistor

The relationship between  $V_{IN}$  and  $V_{OUT}$  becomes:

$$V_{OUT} = (V_{IN} - I_{IN} \cdot R) \cdot K \quad (5)$$

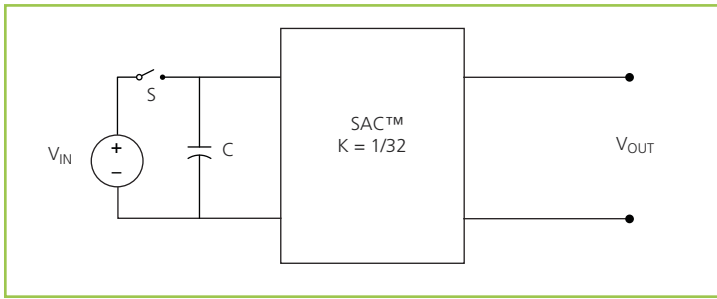
Substituting the simplified version of Eq. (4) ( $I_Q$  is assumed = 0 A) into Eq. (5) yields:

$$V_{OUT} = V_{IN} \cdot K - I_{OUT} \cdot R \cdot K^2 \quad (6)$$

This is similar in form to Eq. (3), where  $R_{OUT}$  is used to represent the characteristic impedance of the SAC™. However, in this case a real  $R$  on the input side of the SAC is effectively scaled by  $K^2$  with respect to the output.

Assuming that  $R = 1 \Omega$ , the effective  $R$  as seen from the secondary side is  $0.98 \text{ m}\Omega$ , with  $K = 1/32$  as shown in Figure 18.

A similar exercise should be performed with the addition of a capacitor, or shunt impedance, at the input to the SAC. A switch in series with  $V_{IN}$  is added to the circuit. This is depicted in Figure 19.



**Figure 19** — Sine Amplitude Converter™ with input capacitor

A change in  $V_{IN}$  with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C \frac{dV_{IN}}{dt} \quad (7)$$

Assume that with the capacitor charged to  $V_{IN}$ , the switch is opened and the capacitor is discharged through the idealized SAC. In this case,

$$I_C = I_{OUT} \cdot K \quad (8)$$

Substituting Eq. (1) and (8) into Eq. (7) reveals:

$$I_{OUT} = \frac{C}{K^2} \cdot \frac{dV_{OUT}}{dt} \quad (9)$$

Writing the equation in terms of the output has yielded a  $K^2$  scaling factor for  $C$ , this time in the denominator of the equation. For a  $K$  factor less than unity, this results in an effectively larger capacitance on the output when expressed in terms of the input. With a  $K=1/32$  as shown in Figure 19,  $C=1 \mu\text{F}$  would effectively appear as  $C=1024 \mu\text{F}$  when viewed from the output.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance, while simultaneously providing appropriate filtering for any switched current. The use of a SAC between the regulation stage and the point of load provides a dual benefit, scaling down series impedance leading back to the source and scaling up shunt capacitance (or energy storage) as a function of its  $K$  factor squared. However, these benefits are not useful if the series impedance of the SAC is too high. The impedance of the SAC must be low well beyond the crossover frequency of the system.

A solution for keeping the impedance of the SAC low involves switching at a high frequency. This enables magnetic components to be small since magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies reduces core losses as well.

The two main terms of power loss in the VTM® module are:

- No load power dissipation ( $P_{NL}$ ): defined as the power used to power up the module with an enabled power train at no load.
- Resistive loss ( $R_{OUT}$ ): refers to the power loss across the VTM current multiplier modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{NL} + P_{ROUT} \quad (10)$$

Therefore,

$$P_{OUT} = P_{IN} - P_{DISSIPATED} = P_{IN} - P_{NL} - P_{ROUT} \quad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{IN} - P_{NL} - P_{ROUT}}{P_{IN}} \quad (12)$$

$$= \frac{V_{IN} \cdot I_{IN} - P_{NL} - (I_{OUT})^2 \cdot R_{OUT}}{V_{IN} \cdot I_{IN}}$$

$$= 1 - \left( \frac{P_{NL} + (I_{OUT})^2 \cdot R_{OUT}}{V_{IN} \cdot I_{IN}} \right)$$

## 12.0 INPUT AND OUTPUT FILTER DESIGN

A major advantage of a SAC™ system versus a conventional PWM converter is that the former does not require large functional filters. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of input voltage and output current and efficiently transfers charge through the isolation transformer. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieving high power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

1. Guarantee low source impedance.

To take full advantage of the VTM module dynamic response, the impedance presented to its input terminals must be low from DC to approximately 5 MHz. Input capacitance may be added to improve transient performance or compensate for high source impedance.

2. Further reduce input and/or output voltage ripple without sacrificing dynamic response.

Given the wide bandwidth of the VTM module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the source will appear at the output of the module multiplied by its K factor.

3. Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and cause failures.

The VI Chip® module input/output voltage ranges must not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating input range. Even during this condition, the powertrain is exposed to the applied voltage and power MOSFETs must withstand it.

## 13.0 CAPACITIVE FILTERING CONSIDERATIONS FOR A SINE AMPLITUDE CONVERTER

It is important to consider the impact of adding input and output capacitance to a Sine Amplitude Converter™ on the system as a whole. Both the capacitance value, and the effective impedance of the capacitor must be considered.

A Sine Amplitude Converter has a DC  $R_{OUT}$  value which has already been discussed in section 11. The AC  $R_{OUT}$  of the SAC contains several terms:

- Resonant tank impedance
- Input lead inductance and internal capacitance
- Output lead inductance and internal capacitance

The values of these terms are shown in the behavioral model in section 11. It is important to note on which side of the transformer these impedances appear and how they reflect across the transformer given the K factor.

The overall AC impedance varies from model to model but for most models it is dominated by DC  $R_{OUT}$  value from DC to beyond 500 KHz. The behavioral model in section 11 should be used to approximate the AC impedance of the specific model.

Any capacitors placed at the output of the VTM module reflect back to the input of the module by the square of the K factor (Eq. 9) with the impedance of the module appearing in series. It is very important to keep this in mind when using a PRM™ regulator to power the VTM. Most PRM® regulators have a limit on the maximum amount of capacitance that can be applied to the output. This capacitance includes both the regulator output capacitance and the current multiplier output capacitance reflected back to the input. In PRM regulator remote sense applications, it is important to consider the reflected value of VTM current multiplier output capacitance when designing and compensating the PRM regulator control loop.

Capacitance placed at the input of the VTM module appear to the load reflected by the K factor, with the impedance of the VTM module in series. In step-down VTM ratios, the effective capacitance is increased by the K factor. The effective ESR of the capacitor is decreased by the square of the K factor, but the impedance of the VTM module appears in series. Still, in most step-down VTM modules an electrolytic capacitor placed at the input of the module will have a lower effective impedance compared to an electrolytic capacitor placed at the output. This is important to consider when placing capacitors at the output of the current multiplier. Even though the capacitor may be placed at the output, the majority of the AC current will be sourced from the lower impedance, which in most cases will be the VTM current multiplier. This should be studied carefully in any system design using a VTM current multiplier. In most cases, it should be clear that electrolytic output capacitors are not necessary to design a stable, well-bypassed system.

## 14.0 CURRENT SHARING

The SAC™ topology bases its performance on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with some resistive drop and positive temperature coefficient.

This type of characteristic is close to the impedance characteristic of a DC power distribution system, both in behavior (AC dynamic) and absolute value (DC dynamic).

When connected in an array with the same K factor, the VTM module will inherently share the load current with parallel units, according to the equivalent impedance divider that the system implements from the power source to the point of load.

Some general recommendations to achieve matched array impedances:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide the PCB layout as symmetric as possible.
- Apply same input / output filters (if present) to each unit.

For further details see [AN:016 Using BCM® Bus Converters in High Power Arrays](#).

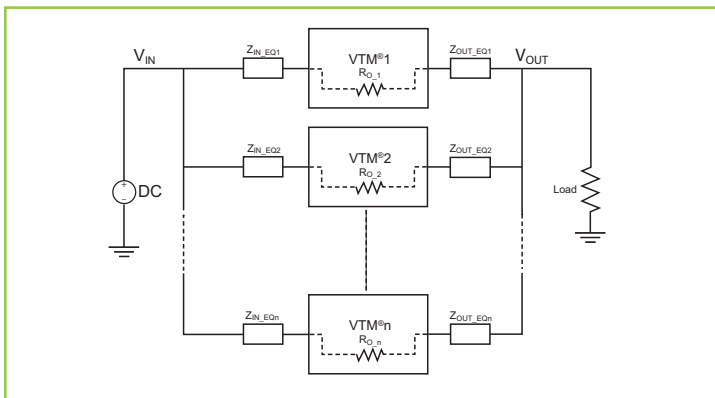


Figure 20 — VTM module array

## 15.0 FUSE SELECTION

In order to provide flexibility in configuring power systems VI Chip® products are not internally fused. Input line fusing of VI Chip products is recommended at system level to provide thermal protection in case of catastrophic failure.

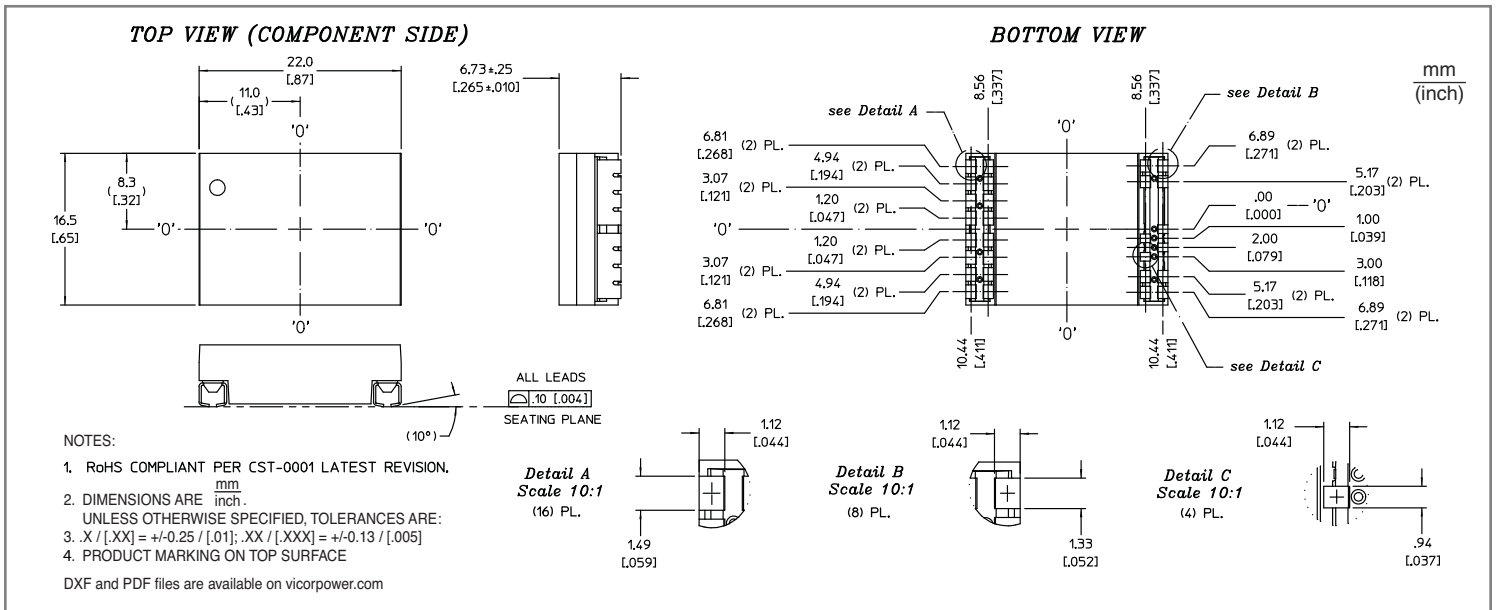
The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating (usually greater than maximum VTM module current)
- Maximum voltage rating (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting  $I^2t$

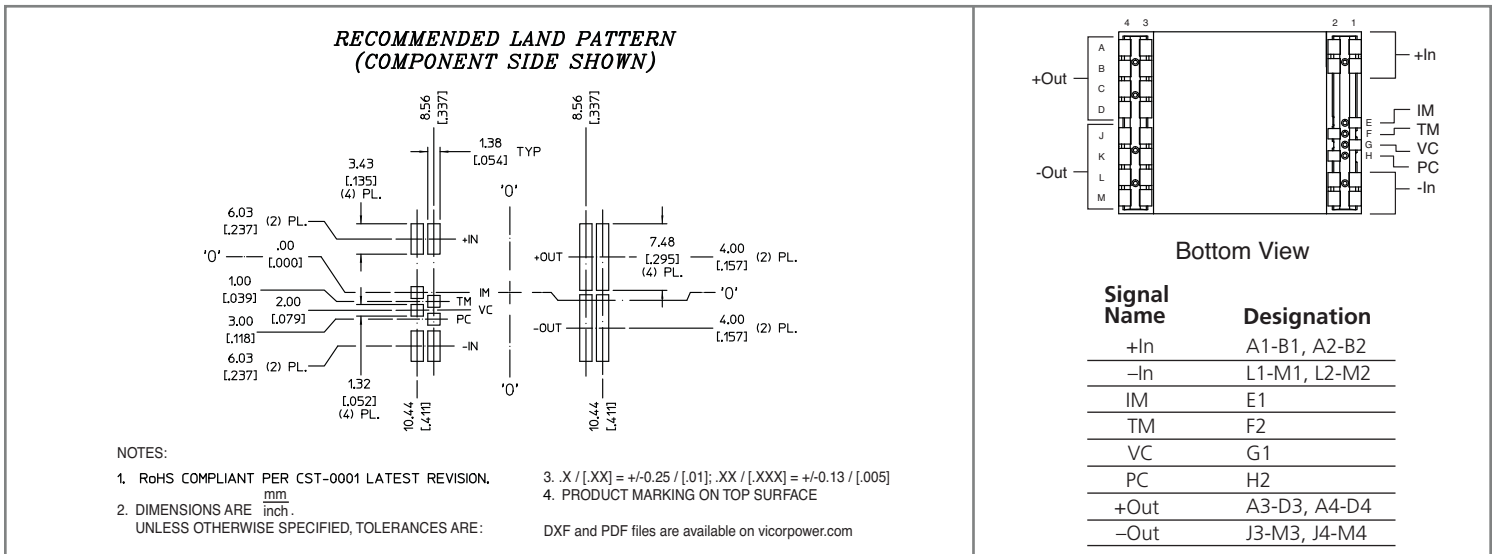
## 16.0 REVERSE OPERATION

The VTM48EH015T050A00 is capable of reverse operation. If a voltage is present at the output which satisfies the condition  $V_{OUT} > V_{IN} \cdot K$  at the time the VC voltage is applied, or after the unit has started, then energy will be transferred from secondary to primary. The input to output ratio will be maintained. The VTM48EH015T050A00 will continue to operate in reverse as long as the input and output are within the specified limits. The VTM48EH015T050A00 has not been qualified for continuous operation (>10 ms) in the reverse direction.

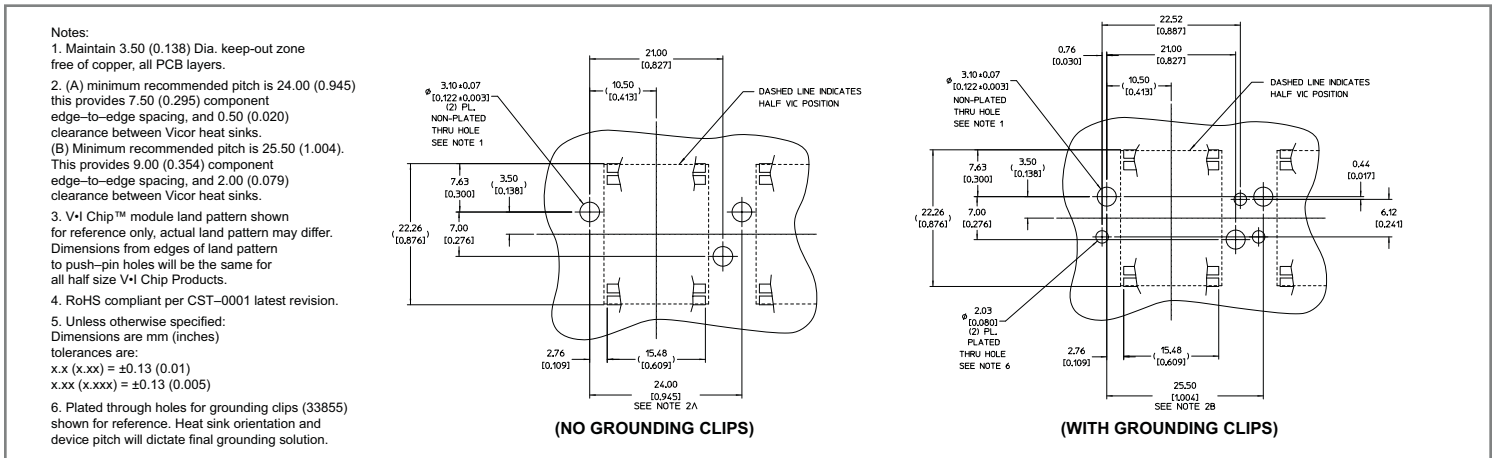
17.1 MECHANICAL DRAWING



17.2 RECOMMENDED LAND PATTERN



17.3 RECOMMENDED HEAT SINK PUSH PIN LOCATION



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