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November 2013

# FDP5N60NZ / FDPF5N60NZ N-Channel UniFET<sup>TM</sup> II MOSFET 600 V, 4.5 A, 2.0 $\Omega$

#### **Features**

- $R_{DS(on)}$  = 1.65  $\Omega$  (Typ.) @  $V_{GS}$  = 10 V,  $I_D$  = 2.25 A
- Low Gate Charge (Typ. 10 nC)
- Low C<sub>rss</sub> (Typ. 5 pF)
- · 100% Avalanche Tested
- · Improved dv/dt Capability
- · ESD Improved Capability
- RoHS Compliant

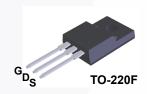
## **Applications**

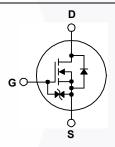
- · LCD / LED / PDP TV
- · Lighting
- Uninterruptible Power Supply
- · AC-DC Power Supply

## Description

UniFET<sup>TM</sup> II MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.







## MOSFET Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol		Parameter		FDP5N60NZ	FDPF5N60NZ	Unit
$V_{DSS}$	Drain to Source Voltage			6	V	
$V_{GSS}$	Gate to Source Voltage		±	25	V	
	Drain Current	- Continuous (T <sub>C</sub> = 25°C)		4.5	4.5*	۸
ID	Drain Current	- Continuous (T <sub>C</sub> = 100°C)		2.7	2.7*	Α
I <sub>DM</sub>	Drain Current	- Pulsed	(Note 1)	18	18*	Α
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)		(Note 2)	175		mJ
I <sub>AR</sub>	Avalanche Current		(Note 1)	4.5		Α
E <sub>AR</sub>	Repetitive Avalanche Energy		(Note 1)	10		mJ
dv/dt	MOSFET dv/dt			20		V/ns
uv/ut	Peak Diode Recovery dv/dt		(Note 3)	10		V/ns
D	Dower Dissipation	(T <sub>C</sub> = 25°C)		100	33	W
$P_D$	Power Dissipation  - Derate above 25°C		0.8	0.27	W/°C	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range			-55 to +150		°C
T <sub>L</sub>	Maximum Lead Temperature	for Soldering, 1/8" from Case for	5 Seconds	3	00	°C

<sup>\*</sup>Dran current limited by maximum junction temperature

#### **Thermal Characteristics**

Symbol	Parameter	FDP5N60NZ	FDPF5N60NZ	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.25	3.75	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	62.5	C/VV

## **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP5N60NZ	FDP5N60NZ	TO-220	Tube	N/A	N/A	50 units
FDPF5N60NZ	FDPF5N60NZ	TO-220F	Tube	N/A	N/A	50 units

## **Electrical Characteristics** T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A},  V_{GS} = 0 \text{V}$	600	-	-	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C	-	0.6	-	V/°C
ı	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	-	-	1	μА
DSS	Zero Gate Voltage Drain Current	$V_{DS} = 480 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	-	10	μΑ
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>GS</sub> = ±25 V, V <sub>DS</sub> = 0 V	-	-	±10	μΑ

#### **On Characteristics**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu\text{A}$	3.0	-	5.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.25 A	-	1.65	2.0	Ω
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_{D} = 2.25 \text{ A}$	-	5	ı	S

## **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V = 25 V V = 0 V		-	450	600	pF
Coss	Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz		-	50	65	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 = 1 101112		-	5	7.5	pF
$Q_g$	Total Gate Charge at 10V	V <sub>DS</sub> = 480 V, I <sub>D</sub> = 4.5 A,		-	10	13	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	V <sub>GS</sub> = 10 V		-	2.5	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		(Note 4)	1	4	-	nC

## **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 4.5 A,		-	15	40	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 10 \text{ V}, R_{G} = 25 \Omega$		-	20	50	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			-	35	80	ns
t <sub>f</sub>	Turn-Off Fall Time	(Not	e 4)	-/	20	50	ns

#### **Drain-Source Diode Characteristics**

I <sub>S</sub>	Maximum Continuous Drain to Source Dioc	Maximum Continuous Drain to Source Diode Forward Current		-	4.5	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Fo	orward Current	-	-	18	Α
$V_{SD}$	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 4.5 A	-	-	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 4.5 A,	-	230	/ -	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> /dt = 100 A/μs	-	0.9	-	μС

#### Notes

- 1. Repetitive rating: pulse-width limited by maximum junction temperature.
- 2. L = 17.3 mH, I  $_{AS}$  = 4.5 A, V  $_{DD}$  = 50 V, R  $_{G}$  = 25  $\Omega,$  starting T  $_{J}$  = 25°C.
- 3.  $I_{SD} \le 4.5$  A, di/dt  $\le 200$  A/ $\mu$ s,  $V_{DD} \le BV_{DSS}$ , starting  $T_J$  = 25°C.
- 4. Essentially independent of operating temperature typical characteristics.

## **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

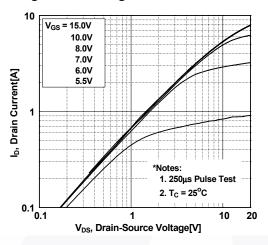


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

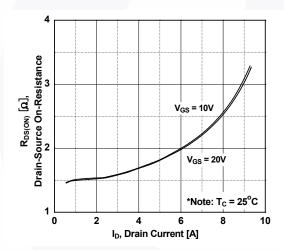


Figure 5. Capacitance Characteristics

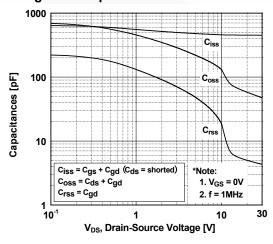


Figure 2. Transfer Characteristics

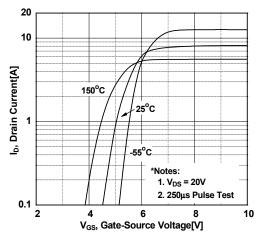


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

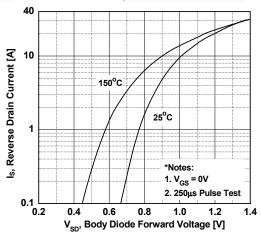
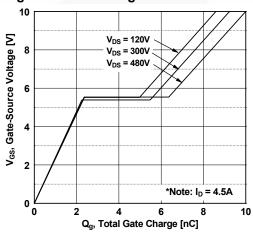


Figure 6. Gate Charge Characteristics



## **Typical Performance Characteristics** (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

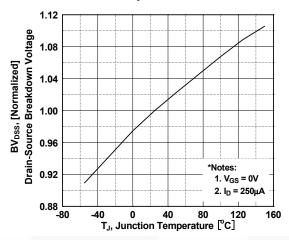


Figure 9. Maximum Safe Operating Area - FDP5N60NZ

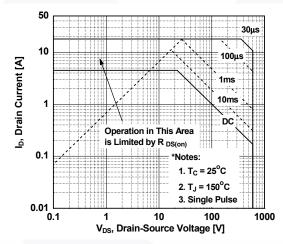


Figure 11. Maximum Drain Current vs.

Case Temperature

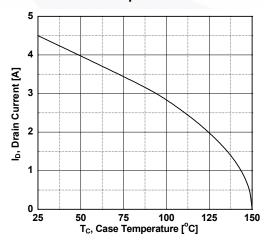


Figure 8. On-Resistance Variation vs. Temperature

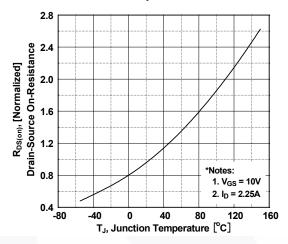


Figure 10. Maximum Safe Operating Area - FDPF5N60NZ

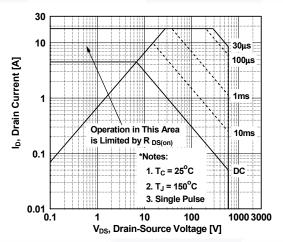
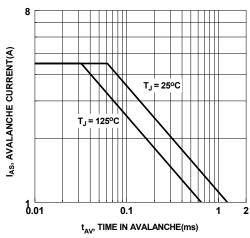


Figure 12. Unclamped Inductive Switching Capability



## **Typical Performance Characteristics** (Continued)

Figure 13. Transient Thermal Response Curve - FDP5N60NZ

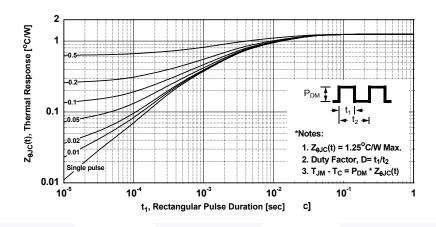
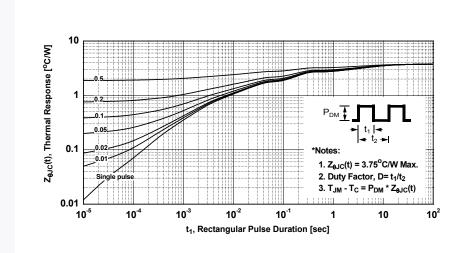


Figure 14. Transient Thermal Response Curve - FDPF5N60NZ



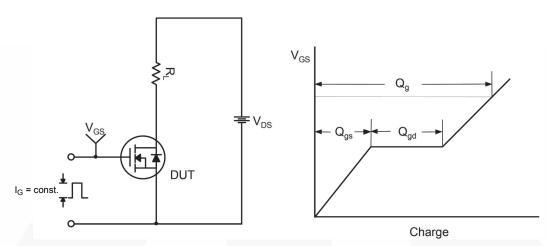


Figure 15. Gate Charge Test Circuit & Waveform

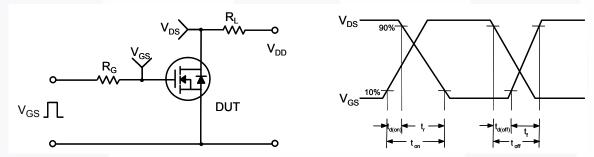


Figure 16. Resistive Switching Test Circuit & Waveforms

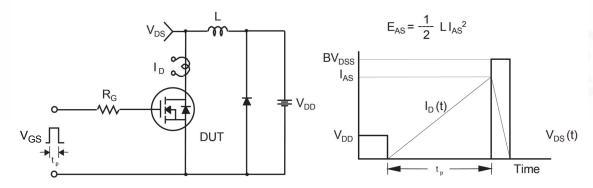


Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms

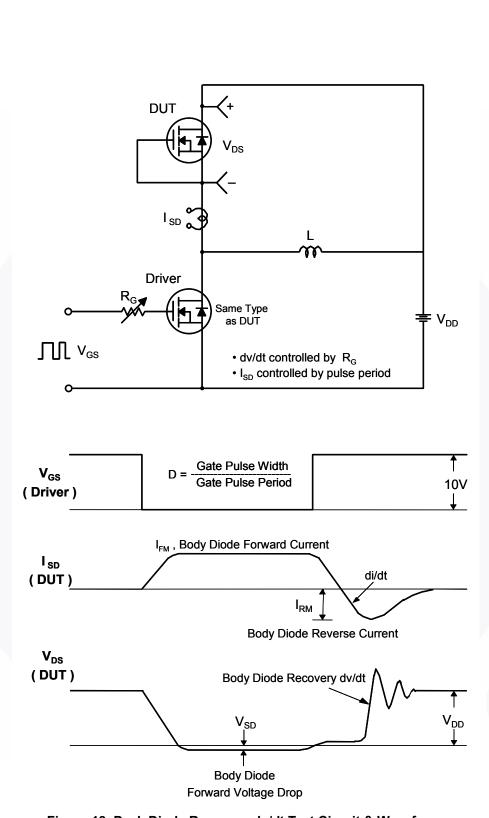


Figure 18. Peak Diode Recovery dv/dt Test Circuit & Waveforms

## **Mechanical Dimensions**

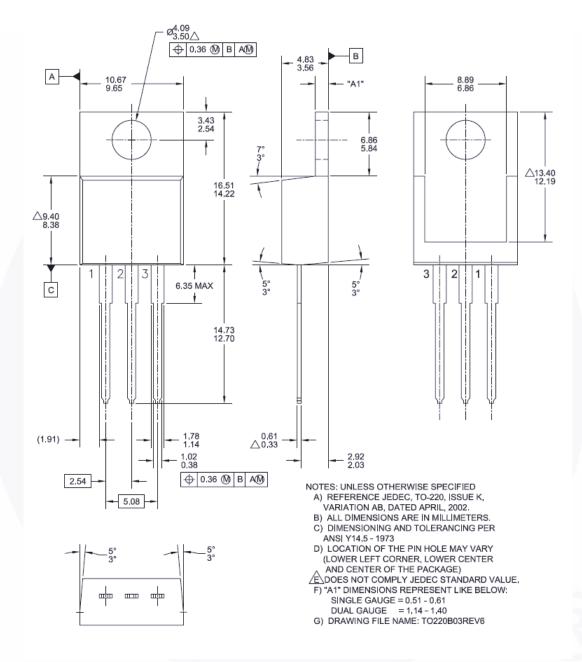


Figure 19. TO-220, Molded, 3-Lead, Jedec Variation AB

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## **Mechanical Dimensions**

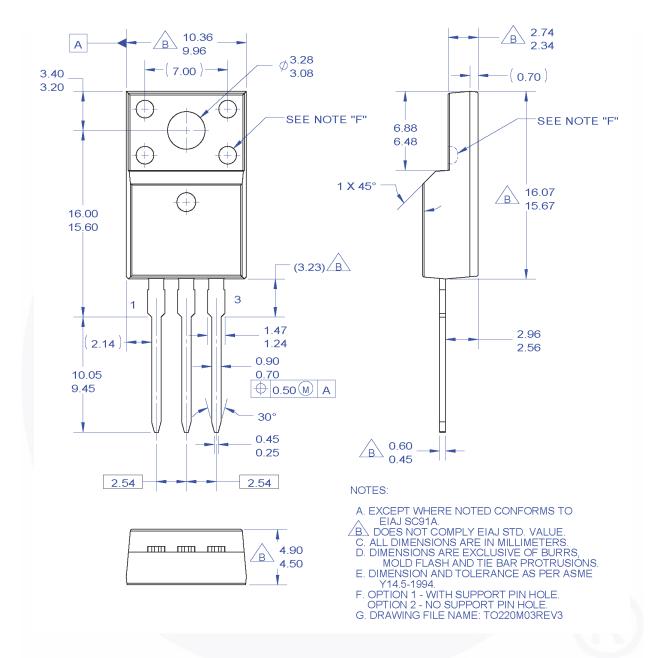


Figure 20. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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