50 Hz to 6 GHz, 50 dB TruPwr™ Detector

Data Sheet **AD8363**

FEATURES

- Accurate rms-to-dc conversion from 50 Hz to 6 GHz
- Single-ended input dynamic range of >50 dB
- No balun or external input tuning required
- Waveform and modulation independent RF power detection
- Linear-in-decibels output, scaled: 52 mV/dB
- Log conformance error: <±0.15 dB
- Temperature stability: <±0.5 dB
- Voltage supply range: 4.5 V to 5.5 V
- Operating temperature range: −40°C to +125°C
- Power-down capability to 1.5 mW
- Small footprint, 4 mm × 4 mm, LFCSP

APPLICATIONS

- Power amplifier linearization/control loops
- Multi-Standard, Multi-Carrier Wireless Infrastructure (MCGSM, CDMA, WCDMA, TD-SCDMA, WiMAX, LTE)
- Transmitter power control
- Transmitter signal strength indication (TSSI)
- RF instrumentation

FUNCTIONAL BLOCK DIAGRAM

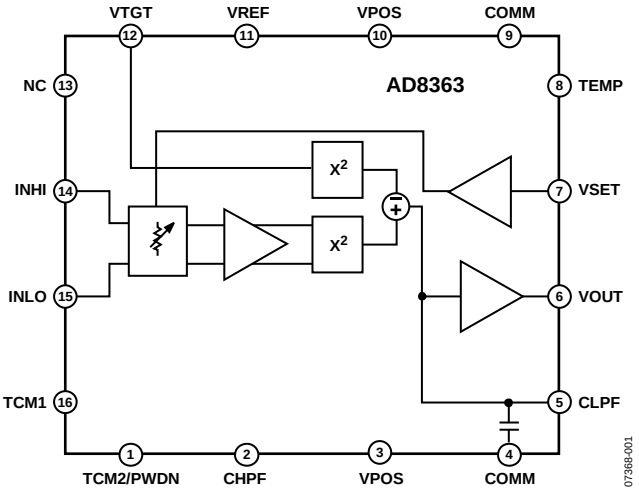

Figure 1. AD8363 Block Diagram

GENERAL DESCRIPTION

The AD8363 is a true rms responding power detector that can be directly driven with a single-ended 50 Ω source. This feature makes the AD8363 frequency versatile by eliminating the need for a balun or any other form of external input tuning for operation up to 6 GHz.

The AD8363 provides an accurate power measurement, independent of waveform, for a variety of high frequency communication and instrumentation systems. Requiring only a single supply of 5 V and a few capacitors, it is easy to use and provides high measurement accuracy. The AD8363 can operate from arbitrarily low frequencies to 6 GHz and can accept inputs that have rms values from less than −50 dBm to at least 0 dBm, with large crest factors exceeding the requirements for accurate measurement of WiMAX, CDMA, W-CDMA, TD-SCDMA, multicarrier GSM, and LTE signals.

The AD8363 can determine the true power of a high frequency signal having a complex low frequency modulation envelope, or it can be used as a simple low frequency rms voltmeter. The high-pass corner generated by its internal offset-nulling loop can be lowered by a capacitor added on the CHPF pin.

Used as a power measurement device, VOUT is connected to VSET. The output is then proportional to the logarithm of the rms value of the input. The reading is presented directly in decibels and is conveniently scaled to 52 mV/dB, or approximately 1 V per decade; however, other slopes are easily arranged. In controller mode, the voltage applied to VSET determines the power level required at the input to null the deviation from the setpoint. The output buffer can provide high load currents.

The AD8363 has 1.5 mW power consumption when powered down by a logic high applied to the TCM2/PWDN pin. It powers up within about 30 µs to its nominal operating current of 60 mA at 25°C. The AD8363 is available in a 4 mm × 4 mm 16-lead LFCSP for operation over the −40°C to +125°C temperature range.

A fully populated RoHS compliant evaluation board is also available.

Rev. B

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5/09—Revision 0: Initial Version

SPECIFICATIONS

V_{POS} = 5 V, T_A = 25°C, Z_O = 50 Ω, single-ended input drive, VOUT connected to VSET, V_{TGT} = 1.4 V, C_{LPF} = 3.9 nF, C_{HPF} = 2.7 nF, error referred to best-fit line (linear regression) from −20 dBm to −40 dBm, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Maximum Input Frequency				6	GHz
RF INPUT INTERFACE	INHI (Pin 14), INLO (Pin 15), ac-coupled				
Input Resistance	Single-ended drive		50		Ω
Common-Mode DC Voltage			2.6		V
100 MHz	TCM1 (Pin 16) = 0.47 V, TCM2 (Pin 1) = 1.0 V, INHI input				
Output Voltage: High Power In	P_{IN} = −10 dBm		2.47		V
Output Voltage: Low Power In	P_{IN} = −40 dBm		0.92		V
±1.0 dB Dynamic Range	CW input, T_A = 25°C				
	3-point calibration at 0 dBm, −10 dBm, and −40 dBm		64		dB
	Best-fit (linear regression) at −20 dBm and −40 dBm		65		dB
Maximum Input Level, ±1.0 dB			9		dBm
Minimum Input Level, ±1.0 dB			−56		dBm
Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C; P_{IN} = −10 dBm		−0.2/+0.3		dB
	−40°C < T_A < +85°C; P_{IN} = −40 dBm		−0.5/+0.6		dB
Logarithmic Slope			51.7		mV/dB
Logarithmic Intercept			−58		dBm
Deviation from CW Response	13 dB peak-to-rms ratio (W-CDMA), over 40 dB dynamic range		<±0.1		dB
	12 dB peak-to-rms ratio (WiMAX), over 40 dB dynamic range		<±0.1		dB
	14.0 dB peak-to-rms ratio (16C CDMA2K), over 40 dB dynamic range		<±0.1		dB
	256 QAM, CF = 8 dB, over 40 dB dynamic range		<±0.1		dB
Input Impedance	Single-ended drive		49 – j0.09		Ω
900 MHz	TCM1 (Pin 16) = 0.5 V, TCM2 (Pin 1) = 1.2 V, INHI input				
Output Voltage: High Power In	P_{IN} = −15 dBm		2.2		V
Output Voltage: Low Power In	P_{IN} = −40 dBm		0.91		V
±1.0 dB Dynamic Range	CW input, T_A = 25°C				
	3-point calibration at 0 dBm, −10 dBm, and −40 dBm		60		dB
	Best-fit (linear regression) at −20 dBm and −40 dBm		54		dB
Maximum Input Level, ±1.0 dB			−2		dBm
Minimum Input Level, ±1.0 dB			−56		dBm
Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C; P_{IN} = −15 dBm		+0.6/−0.4		dB
	−40°C < T_A < +85°C; P_{IN} = −40 dBm		+0.8/−0.6		dB
Logarithmic Slope			51.8		mV/dB
Logarithmic Intercept			−58		dBm
Deviation from CW Response	13 dB peak-to-rms ratio (W-CDMA), over 40 dB dynamic range		<±0.1		dB
	12 dB peak-to-rms ratio (WiMAX), over 40 dB dynamic range		<±0.1		dB
	14.0 dB peak-to-rms ratio (16C CDMA2K), over 40 dB dynamic range		<±0.1		dB
	256 QAM, CF = 8 dB, over 40 dB dynamic range		<±0.1		dB
Input Impedance	Single-ended drive		60 – j3.3		Ω

Parameter	Conditions	Min	Typ	Max	Unit
1.9 GHz	TCM1 (Pin 16) = 0.52 V, TCM2 (Pin 1) = 0.51 V, INHI input				
Output Voltage: High Power In	P_{IN} = −15 dBm		2.10		V
Output Voltage: Low Power In	P_{IN} = −40 dBm		0.8		V
±1.0 dB Dynamic Range	CW input, T_A = 25°C				
	3-point calibration at 0 dBm, −10 dBm, and −40 dBm		56		dB
	Best-fit (linear regression) at −20 dBm and −40 dBm		48		dB
Maximum Input Level, ±1.0 dB			−6		dBm
Minimum Input Level, ±1.0 dB			−53		dBm
Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C; P_{IN} = −15 dBm		+0.3/−0.5		dB
	−40°C < T_A < +85°C; P_{IN} = −40 dBm		+0.4/−0.4		dB
Logarithmic Slope			52		mV/dB
Logarithmic Intercept			−55		dBm
Deviation from CW Response	13 dB peak-to-rms ratio (W-CDMA), over 37 dB dynamic range		±0.1		dB
	12 dB peak-to-rms ratio (WiMAX), over 37 dB dynamic range		±0.1		dB
	14.0 dB peak-to-rms ratio (16C CDMA2K), over 37 dB dynamic range		±0.1		dB
	256 QAM, CF = 8 dB, over 37 dB dynamic range		±0.1		dB
Input Impedance	Single-ended drive		118 – j26		Ω
2.14 GHz	TCM1 (Pin 16) = 0.52 V, TCM2 (Pin 1) = 0.6 V, INHI input				
Output Voltage: High Power In	P_{IN} = −15 dBm		2.0		V
Output Voltage: Low Power In	P_{IN} = −40 dBm		0.71		V
±1.0 dB Dynamic Range	CW input, T_A = 25°C				
	3-point calibration at 0 dBm, −10 dBm and −40 dBm		55		dB
	Best-fit (linear regression) at −20 dBm and −40 dBm		44		dB
Maximum Input Level, ±1.0 dB			−8		dBm
Minimum Input Level, ±1.0 dB			−52		dBm
Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C; P_{IN} = −15 dBm		+0.1/−0.2		dB
	−40°C < T_A < +85°C; P_{IN} = −40 dBm		+0.3/−0.5		dB
Logarithmic Slope			52.2		mV/dB
Logarithmic Intercept			−54		dBm
Deviation from CW Response	13 dB peak-to-rms ratio (W-CDMA), over 35 dB dynamic range		±0.1		dB
	12 dB peak-to-rms ratio (WiMAX), over 35 dB dynamic range		±0.1		dB
	14.0 dB peak-to-rms ratio (16C CDMA2K), over 35 dB dynamic range		±0.1		dB
	256 QAM, CF = 8 dB, over 35 dB dynamic range		±0.1		dB
Rise Time	Transition from no input to 1 dB settling at RF_{IN} = −10 dBm, C_{LPF} = 390 pF, C_{HPF} = open		3		µs
Fall Time	Transition from −10 dBm to within 1 dB of final value (that is, no input level), C_{LPF} = 390 pF, C_{HPF} = open		15		µs
Input Impedance	Single-ended drive		130 – j49		Ω
2.6 GHz	TCM1 (Pin 16) = 0.54 V, TCM2 (Pin 1) = 1.1 V, INHI input				
Output Voltage: High Power In	P_{IN} = −15 dBm		1.84		V
Output Voltage: Low Power In	P_{IN} = −40 dBm		0.50		V
±1.0 dB Dynamic Range	CW input, T_A = 25°C				
	3-point calibration at 0 dBm, −10 dBm and −40 dBm		50		dB
	Best-fit (linear regression) at −20 dBm and −40 dBm		41		dB
Maximum Input Level, ±1.0 dB			−7		dBm
Minimum Input Level, ±1.0 dB			−48		dBm
Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C; P_{IN} = −15 dBm		+0.5/−0.2		dB
	−40°C < T_A < +85°C; P_{IN} = −40 dBm		+0.6/−0.2		dB

Parameter	Conditions	Min	Typ	Max	Unit
Logarithmic Slope			52.9		mV/dB
Logarithmic Intercept			−49		dBm
Deviation from CW Response	13 dB peak-to-rms ratio (W-CDMA), over 32 dB dynamic range		±0.1		dB
	12 dB peak-to-rms ratio (WiMAX), over 32 dB dynamic range		±0.1		dB
	14.0 dB peak-to-rms ratio (16C CDMA2K), over 32 dB dynamic range		±0.1		dB
	256 QAM, CF = 8 dB, over 32 dB dynamic range		±0.1		dB
Input Impedance	Single-ended drive		95 − j65		Ω
3.8 GHz	TCM1 (Pin 16) = 0.56 V, TCM2 (Pin 1) = 1.0 V, INLO input				
Output Voltage: High Power In	P_{IN} = −20 dBm		1.54		V
Output Voltage: Low Power In	P_{IN} = −40 dBm		0.54		V
±1.0 dB Dynamic Range	CW input, T_A = 25°C				
	3-point calibration at 0 dBm, −10 dBm and −40 dBm		50		dB
	Best-fit (linear regression) at −20 dBm and −40 dBm		43		dB
Maximum Input Level, ±1.0 dB			−5		dBm
Minimum Input Level, ±1.0 dB			−48		dBm
Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C; P_{IN} = −20 dBm		+0.1/−0.7		dB
	−40°C < T_A < +85°C; P_{IN} = −40 dBm		+0.4/−0.5		dB
Logarithmic Slope			50.0		mV/dB
Logarithmic Intercept			−51		dBm
Deviation from CW Response	13 dB peak-to-rms ratio (W-CDMA), over 32 dB dynamic range		±0.1		dB
	12 dB peak-to-rms ratio (WiMAX), over 32 dB dynamic range		±0.1		dB
	14.0 dB peak-to-rms ratio (16C CDMA2K), over 32 dB dynamic range		±0.1		dB
	256 QAM, CF = 8 dB, over 32 dB dynamic range		±0.1		dB
Input Impedance	Single-ended drive		42 − j4.5		Ω
5.8 GHz	TCM1 (Pin 16) = 0.88 V, TCM2 (Pin 1) = 1.0 V, INLO input				
Output Voltage: High Power In	P_{IN} = −20 dBm		1.38		V
Output Voltage: Low Power In	P_{IN} = −40 dBm		0.36		V
±1.0 dB Dynamic Range	CW input, T_A = 25°C				
	3-point calibration at 0 dBm, −10 dBm and −40 dBm		50		dB
	Best-fit (linear regression) at −20 dBm and −40 dBm		45		dB
Maximum Input Level, ±1.0 dB			−3		dBm
Minimum Input Level, ±1.0 dB			−48		dBm
Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C; P_{IN} = −20 dBm		+0.1/−0.6		dB
	−40°C < T_A < +85°C; P_{IN} = −40 dBm		+0.3/−0.8		dB
Logarithmic Slope			51.1		mV/dB
Logarithmic Intercept			−47		dBm
Deviation from CW Response	13 dB peak-to-rms ratio (W-CDMA), over 32 dB dynamic range		±0.1		dB
	12 dB peak-to-rms ratio (WiMAX), over 32 dB dynamic range		±0.1		dB
	14.0 dB peak-to-rms ratio (16C CDMA2K), over 32 dB dynamic range		±0.1		dB
	256 QAM, CF = 8 dB, over 32 dB dynamic range		±0.1		dB
Input Impedance	Single-ended drive		28 + j1.6		Ω
OUTPUT INTERFACE	VOUT (Pin 6)				
Output Swing, Controller Mode	Swing range minimum, R_L ≥ 500 Ω to ground		0.03		V
	Swing range maximum, R_L ≥ 500 Ω to ground		4.8		V
Current Source/Sink Capability	Output held at V_{POS}/2			10/10	mA
Voltage Regulation	I_{LOAD} = 8 mA, source/sink		−0.2/+0.1		%
Rise Time	Transition from no input to 1 dB settling at RF_{IN} = −10 dBm, C_{LPF} = 390 pF, C_{HPF} = open		3		µs

Parameter	Conditions	Min	Typ	Max	Unit
Fall Time	Transition from −10 dBm to within 1 dB of final value (that is, no input level), C_{LPF} = 390 pF, C_{HPF} = open		15		µs
Noise Spectral Density	Measured at 100 kHz		45		nV/√Hz
SETPOINT INPUT	VSET (Pin 7)				
Voltage Range	Log conformance error ≤ 1 dB, minimum 2.14 GHz		2.0		V
	Log conformance error ≤ 1 dB, maximum 2.14 GHz		0.7		V
Input Resistance			72		kΩ
Logarithmic Scale Factor	f = 2.14 GHz, −40°C ≤ T_A ≤ +85°C		19.2		dB/V
Logarithmic Intercept	f = 2.14 GHz, −40°C ≤ T_A ≤ +85°C, referred to 50 Ω		−54		dBm
TEMPERATURE COMPENSATION	TCM1 (Pin 16), TCM2 (Pin 1)				
Input Voltage Range		0		2.5	V
Input Bias Current, TCM1	V_{TCM1} = 0 V		−140		µA
	V_{TCM1} = 0.5 V		80		µA
Input Resistance, TCM1	V_{TCM1} > 0.7 V		5		kΩ
Input Current, TCM2	V_{TCM2} = 5 V		2		µA
	V_{TCM2} = 4.5 V		750		µA
	V_{TCM2} = 1 V		−2		µA
	V_{TCM2} = 0 V		−3		µA
Input Resistance, TCM2	0.7 V ≤ V_{TCM2} ≤ 4.0 V		500		kΩ
VOLTAGE REFERENCE	VREF (Pin 11)				
Output Voltage	RF_{IN} = −55 dBm		2.3		V
Temperature Sensitivity	25°C ≤ T_A ≤ 70°C		0.04		mV/°C
	70°C ≤ T_A ≤ 125°C		−0.06		mV/°C
	−40°C ≤ T_A ≤ +25°C		−0.18		mV/°C
Current Source/Sink Capability	25°C ≤ T_A ≤ 125°C			4/0.05	mA
	−40°C ≤ T_A < +25°C			3/0.05	mA
Voltage Regulation	T_A = 25°C, I_{LOAD} = 3 mA		−0.6		%
TEMPERATURE REFERENCE	TEMP (Pin 8)				
Output Voltage	T_A = 25°C, R_L ≥ 10 kΩ		1.4		V
Temperature Coefficient	−40°C ≤ T_A ≤ +125°C, R_L ≥ 10 kΩ		5		mV/°C
Current Source/Sink Capability	25°C ≤ T_A ≤ 125°C			4/0.05	mA
	−40°C ≤ T_A < +25°C			3/0.05	mA
Voltage Regulation	T_A = 25°C, I_{LOAD} = 3 mA		−0.1		%
RMS TARGET INTERFACE	VTGT (Pin 12)				
Input Voltage Range		1.4		2.5	V
Input Bias Current	V_{TGT} = 1.4 V		14		µA
Input Resistance			100		kΩ
POWER-DOWN INTERFACE	TCM2 (Pin1)				
Logic Level to Enable	VPWDN decreasing		4.2		V
Logic Level to Disable	VPWDN increasing		4.7		V
Input Current	V_{TCM2} = 5 V		2		µA
	V_{TCM2} = 4.5 V		750		µA
	V_{TCM2} = 1 V		−2		µA
	V_{TCM2} = 0 V		−3		µA
Enable Time	TCM2 low to V_{OUT} at 1 dB of final value, C_{LPF} = 470 pF, C_{HPF} = 220 pF, RF_{IN} = 0 dBm		35		µs
Disable Time	TCM2 high to V_{OUT} at 1 dB of final value, C_{LPF} = 470 pF, C_{HPF} = 220 pF, RF_{IN} = 0 dBm		25		µs
POWER SUPPLY INTERFACE	VPOS (Pin 3, Pin 10)				
Supply Voltage		4.5	5	5.5	V
Quiescent Current	T_A = 25°C, RF_{IN} = −55 dBm		60		mA
	T_A = 85°C		72		mA
Power-Down Current	V_{TCM2} > V_{POS} − 0.3 V		300		µA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, VPOS	5.5 V
Input Average RF Power[1]	21 dBm
Equivalent Voltage, Sine Wave Input	2.51 V rms
Internal Power Dissipation	450 mW
θ_{JC}[2]	10.6°C/W
θ_{JB}[2]	35.3°C/W
θ_{JA}[2]	57.2°C/W
Ψ_{JT}[2]	1.0°C/W
Ψ_{JB}[2]	34°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] This is for long durations. Excursions above this level, with durations much less than 1 second, are possible without damage.
[2] No airflow with the exposed pad soldered to a 4-layer JEDEC board.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

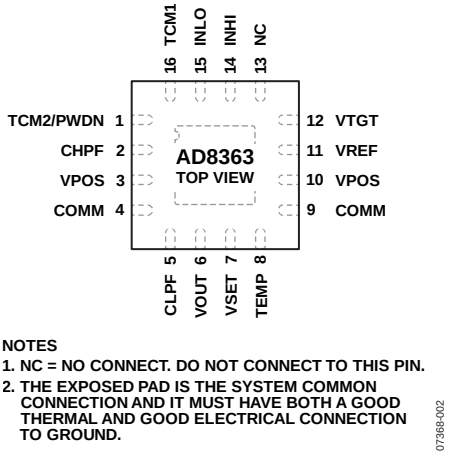

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description	Equivalent Circuit
1	TCM2/PWDN	This is a dual function pin used for controlling the amount of nonlinear intercept temperature compensation at voltages <2.5 V and/or for shutting down the device at voltages >4 V. If the shutdown function is not used, this pin can be connected to the VREF pin through a voltage divider.	See Figure 39
2	CHPF	Connect this pin to VPOS via a capacitor to determine the −3 dB point of the input signal high-pass filter. Only add a capacitor when operating at frequencies below 10 MHz.	See Figure 48
3, 10	VPOS	Supply for the Device. Connect these pins to a 5 V power supply. Pin 3 and Pin 10 are not internally connected; therefore, both must connect to the source.	Not applicable
4, 9	COMM	System Common Connection. Connect these pins via low impedance to system common.	Not applicable
5	CLPF	Connection for Loop Filter Integration (Averaging) Capacitor. Connect a ground-referenced capacitor to this pin. A resistor can be connected in series with this capacitor to improve loop stability and response time. Minimum C_{LPF} value is 390 pF.	See Figure 41
6	VOUT	Output Pin in Measurement Mode (Error Amplifier Output). In measurement mode, this pin is connected to VSET. This pin can be used to drive a gain control when the device is used in controller mode.	See Figure 41
7	VSET	The voltage applied to this pin sets the decibel value of the required RF input voltage that results in zero current flow in the loop integrating capacitor pin, CLPF. This pin controls the variable gain amplifier (VGA) gain such that a 50 mV change in VSET reduces the gain by approximately 1 dB.	See Figure 40
8	TEMP	Temperature Sensor Output.	See Figure 35
11	VREF	General-Purpose Reference Voltage Output of 2.3 V.	See Figure 36
12	VTGT	The voltage applied to this pin determines the target power at the input of the RF squaring circuit. The intercept voltage is proportional to the voltage applied to this pin. The use of a lower target voltage increases the crest factor capacity; however, this may affect the system loop response.	See Figure 42
13	NC	No Connect.	Not applicable
14	INHI	This is the RF input pin for frequencies up to and including 2.6 GHz. The RF input signal is normally ac-coupled to this pin through a coupling capacitor.	See Figure 34
15	INLO	This is the RF input pin for frequencies above 2.6 GHz. The RF input signal is normally ac-coupled to this pin through a coupling capacitor.	See Figure 34
16	TCM1	This pin is used to adjust the intercept temperature compensation. Connect this pin to VREF through a voltage divider or to an external dc source.	See Figure 38
	EPAD	Exposed Pad. The exposed pad is the system common connection and it must have both a good thermal and good electrical connection to ground.	Not applicable

TYPICAL PERFORMANCE CHARACTERISTICS

V_{POS} = 5 V, Z_O = 50 Ω, single-ended input drive, VOUT connected to VSET, V_{TGT} = 1.4 V, C_{LPF} = 3.9 nF, C_{HPF} = 2.7 nF, T_A = +25°C (black), −40°C (blue), +85°C (red), where appropriate. Error calculated using 3-point calibration at 0 dBm, −10 dBm, and −40 dBm, unless otherwise indicated. Input RF signal is a sine wave (CW), unless otherwise indicated.

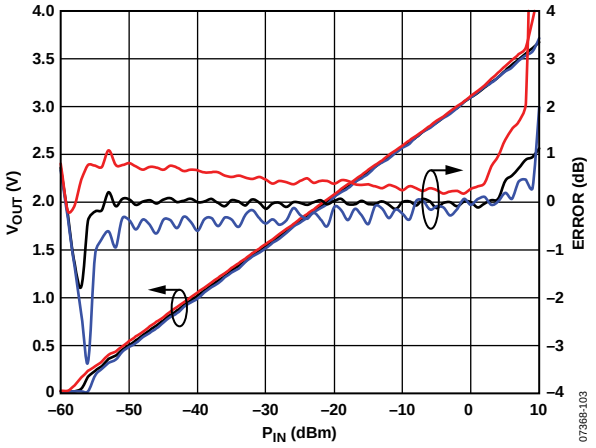

Figure 3. V_{OUT} and Log Conformance vs. Input Power and Temperature at 100 MHz

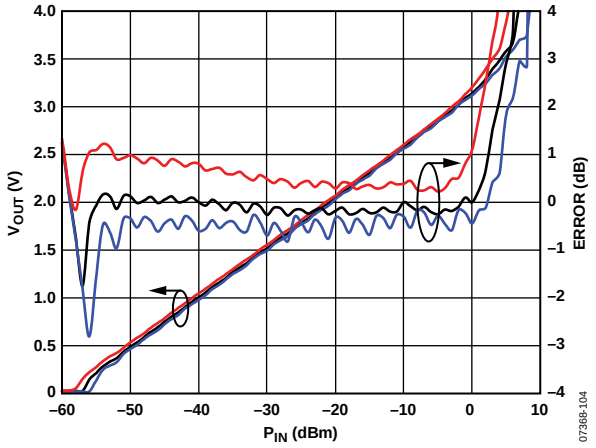

Figure 4. V_{OUT} and Log Conformance Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 900 MHz, CW, Typical Device

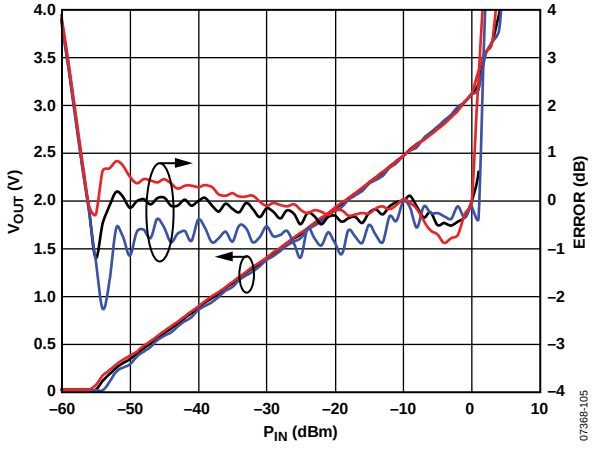

Figure 5. V_{OUT} and Log Conformance Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 1.90 GHz, CW, Typical Device

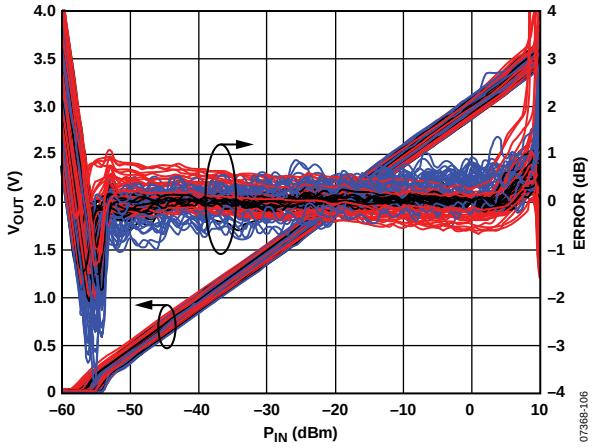

Figure 6. Distribution of V_{OUT} and Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 100 MHz, CW

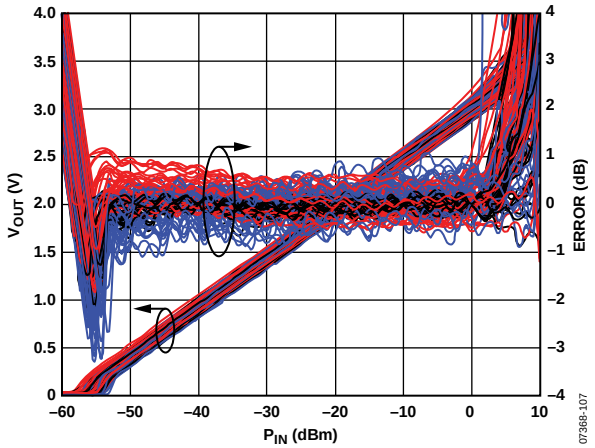

Figure 7. Distribution of V_{OUT} and Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 900 MHz, CW

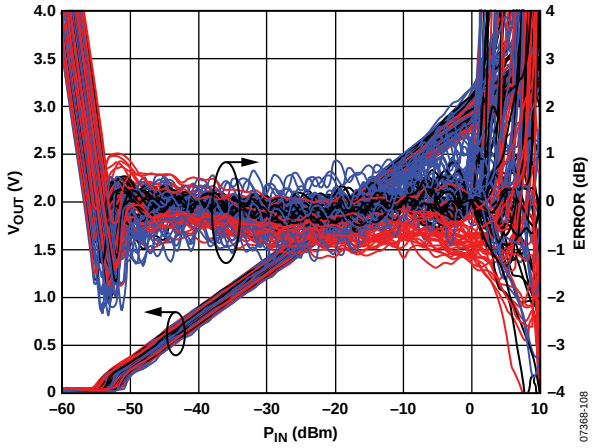

Figure 8. Distribution of V_{OUT} and Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 1.90 GHz, CW

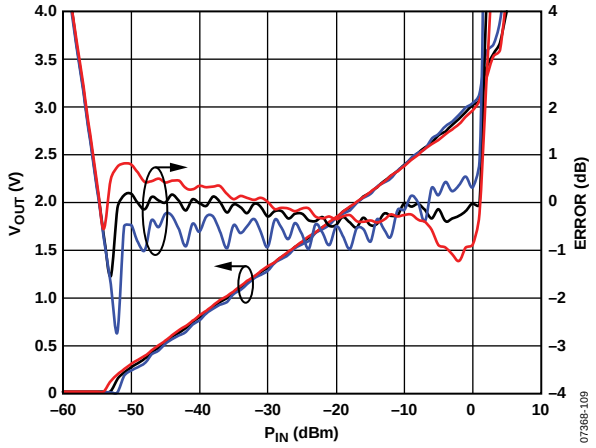

Figure 9. V_{OUT} and Log Conformance Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 2.14 GHz, CW, Typical Device

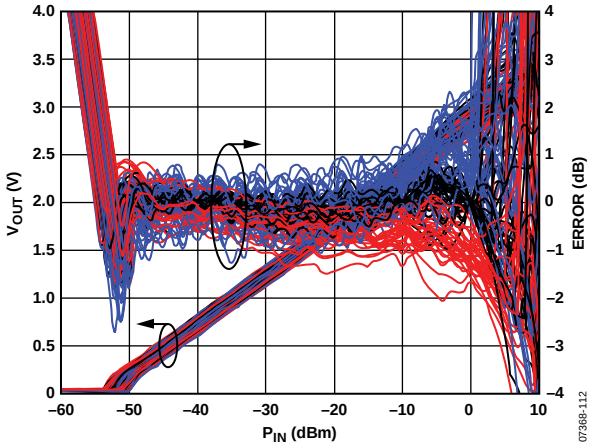

Figure 12. Distribution of V_{OUT} and Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 2.14 GHz, CW

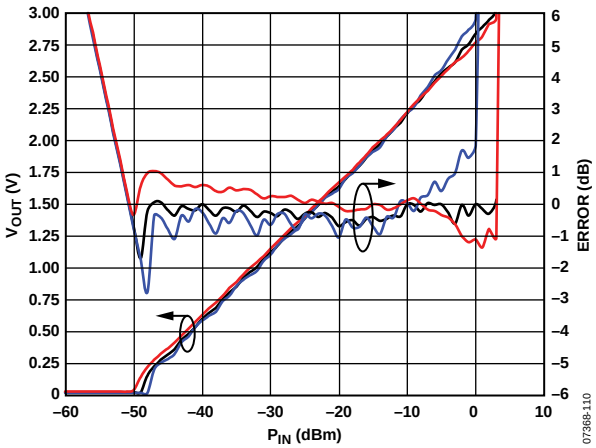

Figure 10. V_{OUT} and Log Conformance Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 2.6 GHz, CW, Typical Device

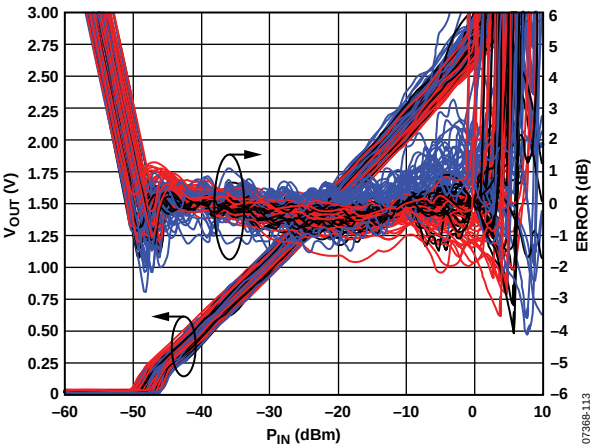

Figure 13. Distribution of V_{OUT} and Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 2.6 GHz, CW

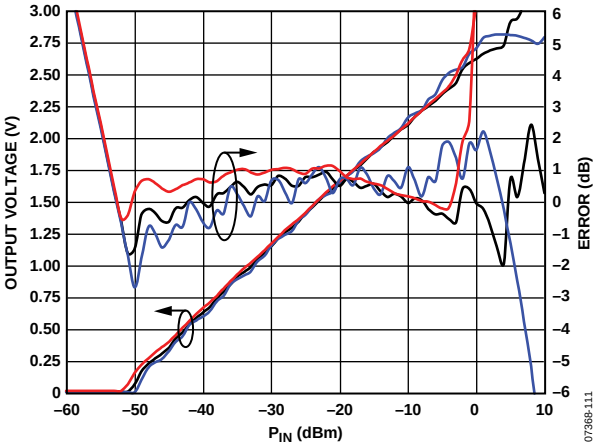

Figure 11. V_{OUT} and Log Conformance Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 3.8 GHz, CW, Typical Device

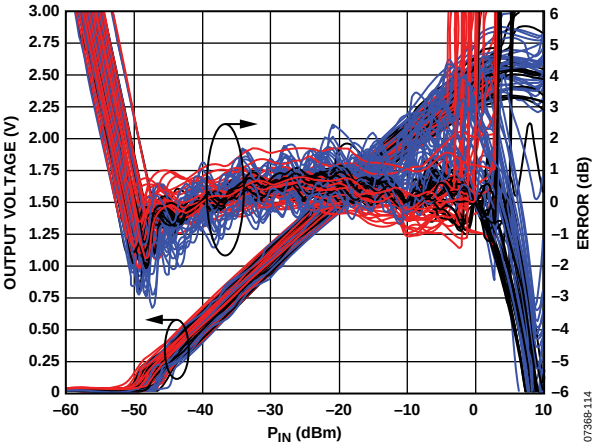

Figure 14. Distribution of V_{OUT} and Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 3.8 GHz, CW

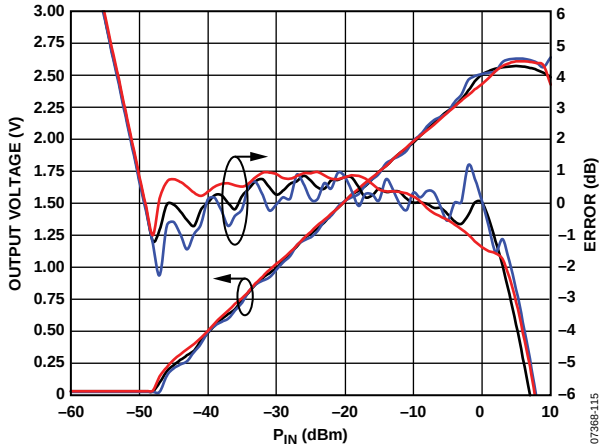

Figure 15. V_{OUT} and Log Conformance Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 5.8 GHz, Typical Device

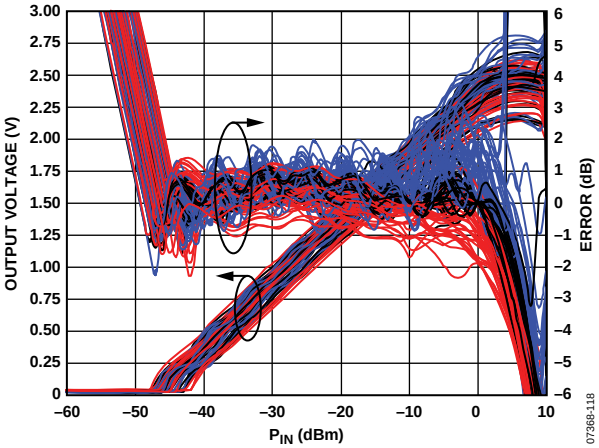

Figure 18. Distribution of V_{OUT} and Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 5.8 GHz, CW

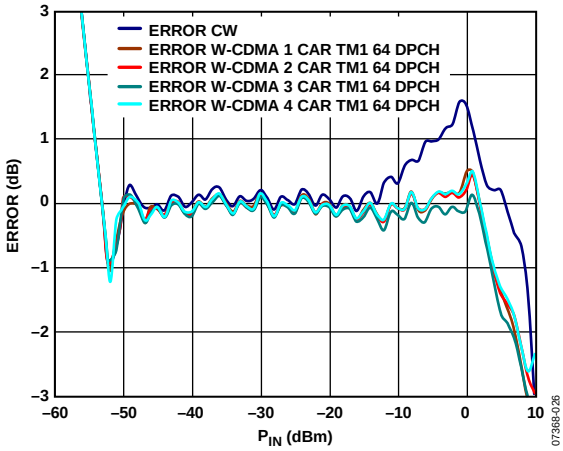

Figure 16. Error from CW Linear Reference vs. Input Amplitude with Modulation, Frequency at 2.14 GHz, C_{LPF} = 0.1 µF, INHI Input

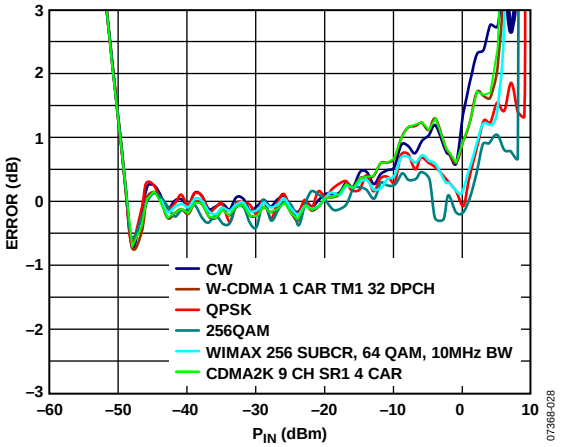

Figure 19. Error from CW Linear Reference vs. Input Amplitude with Modulation, Frequency at 2.6 GHz, C_{LPF} = 0.1 µF, INHI Input

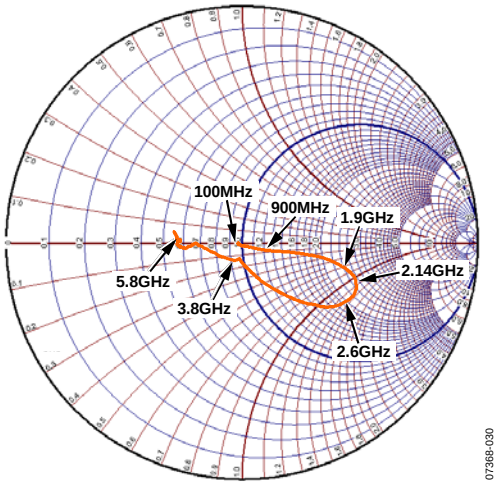

Figure 17. Single-Ended Input Impedance (S11) vs. Frequency; Z_O = 50 Ω, INHI or INLO

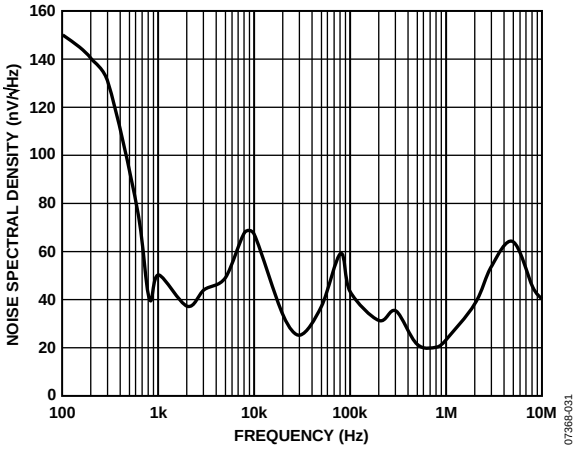

Figure 20. Typical Noise Spectral Density of V_{OUT}; All C_{LPF} Values

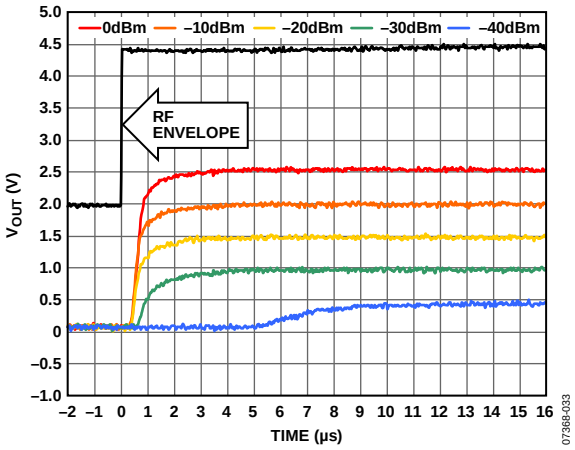

Figure 21. Output Response to RF Burst Input, Carrier Frequency at 2.14 GHz, C_{LPF} = 390 pF, C_{HPF} = Open, Rising Edge

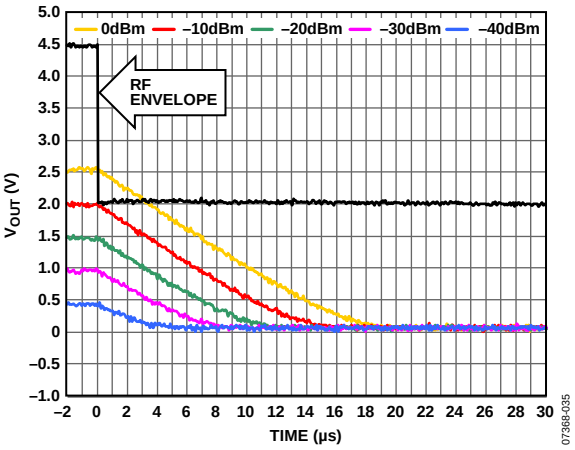

Figure 24. Output Response to RF Burst Input, Carrier Frequency at 2.14 GHz, C_{LPF} = 390 pF, C_{HPF} = Open, Falling Edge

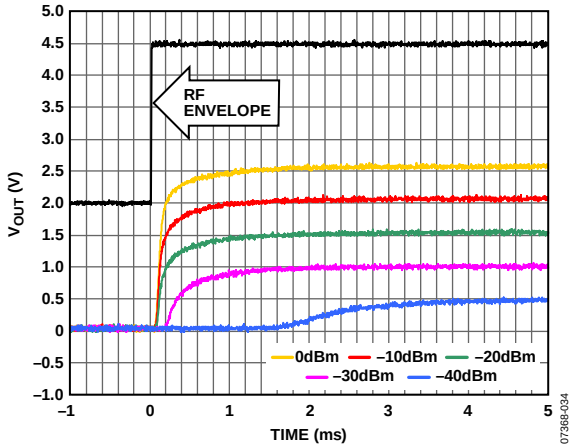

Figure 22. Output Response to RF Burst Input, Carrier Frequency at 2.14 GHz, C_{LPF} = 0.1 µF, C_{HPF} = Open, Rising Edge

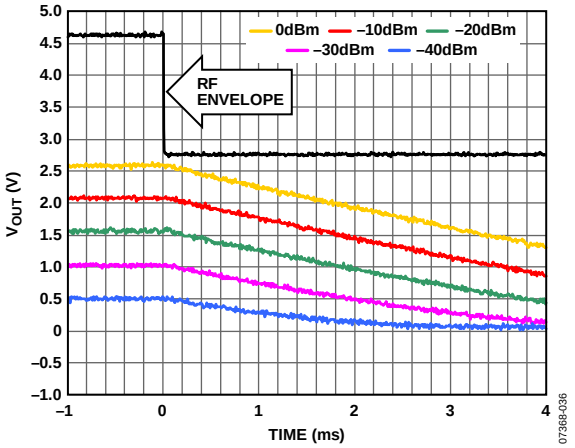

Figure 25. Output Response to RF Burst Input, Carrier Frequency at 2.14 GHz, C_{LPF} = 0.1 µF, C_{HPF} = Open, Falling Edge

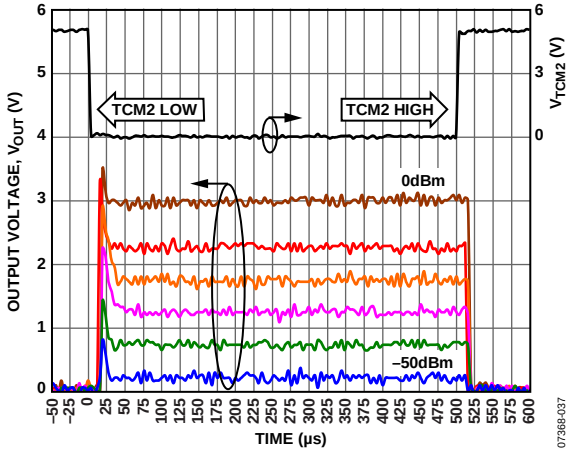

Figure 23. Output Response Using Power-Down Mode for Various RF Input Levels Carrier Frequency at 2.14 GHz, C_{LPF} = 470 pF, C_{HPF} = 220 pF

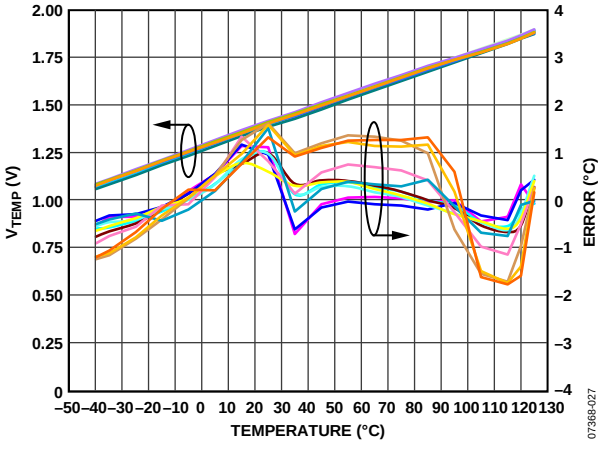

Figure 26. V_{TEMP} and Error with Respect to Straight Line vs. Temperature for Eleven Devices

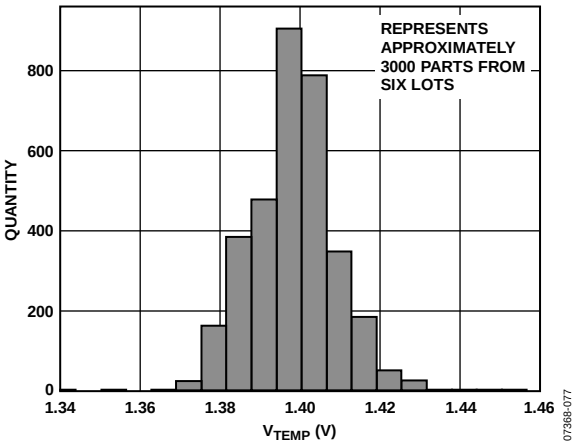

Figure 27. Distribution of V_{TEMP} Voltage at 25°C, No RF Input

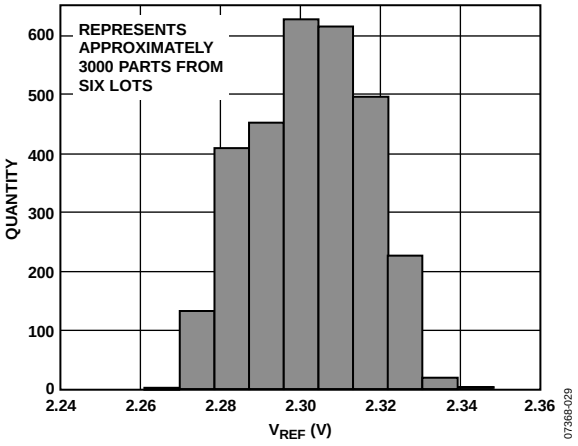

Figure 30. Distribution of V_{REF}, 25°C, No RF Input

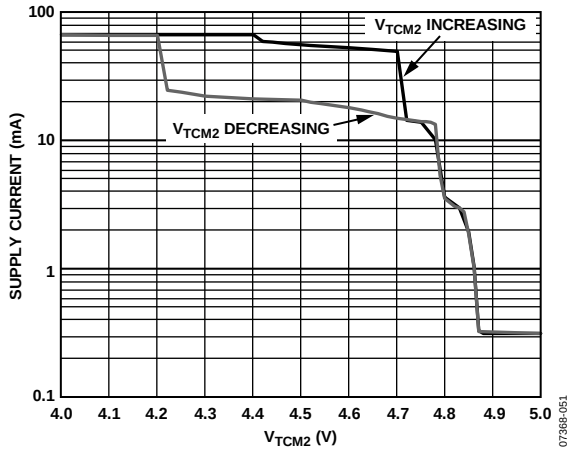

Figure 28. Supply Current vs. V_{TCM2}

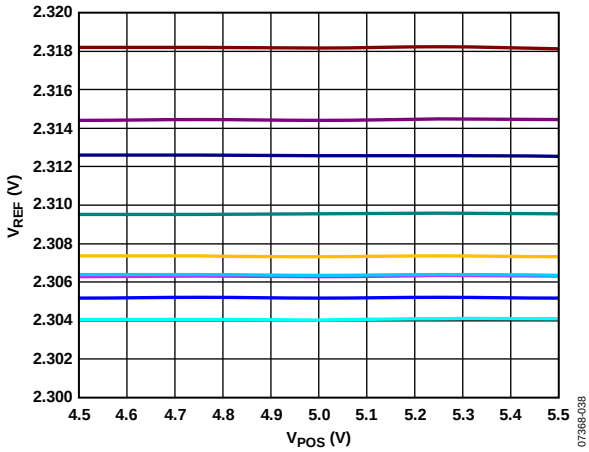

Figure 31. Change in V_{REF} with V_{POS} for Nine Devices

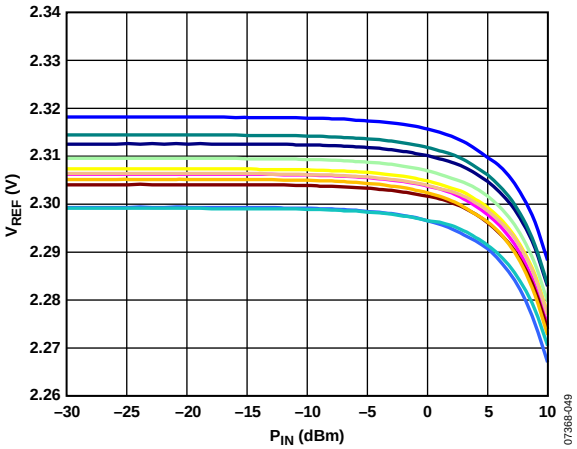

Figure 29. Change in V_{REF} with Input Amplitude for Eleven Devices

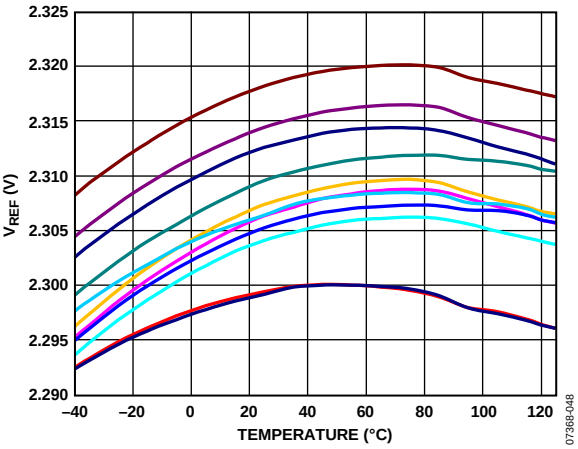

Figure 32. Change in V_{REF} with Temperature for Eleven Devices

THEORY OF OPERATION

The computational core of the AD8363 is a high performance AGC loop. As shown in Figure 33, the AGC loop comprises a wide bandwidth variable gain amplifier (VGA), square law detectors, an amplitude target circuit, and an output driver. For a more detailed description of the functional blocks, see the AD8362 data sheet.

The nomenclature used in this data sheet to distinguish between a pin name and the signal on that pin is as follows:

- The pin name is all uppercase (for example, VPOS, COMM, and VOUT).
- The signal name or a value associated with that pin is the pin mnemonic with a partial subscript (for example, C_{LPF}, C_{HPF}, and V_{OUT}).

SQUARE LAW DETECTOR AND AMPLITUDE TARGET

The VGA gain has the form

$$G_{SET} = G_O \exp(-V_{SET}/V_{GNS}) \quad (1)$$

where:
G_O is the basic fixed gain.
V_{GNS} is a scaling voltage that defines the gain slope (the decibel change per voltage). The gain decreases with increasing V_{SET}.

The VGA output is

$$V_{SIG} = G_{SET} \times RF_{IN} = G_O \times RF_{IN} \, exp(V_{SET}/V_{GNS}) \quad (2)$$

where RF_{IN} is the ac voltage applied to the input terminals of the AD8363.

The output of the VGA, V_{SIG}, is applied to a wideband square law detector. The detector provides the true rms response of the RF input signal, independent of waveform. The detector output, I_{SQR}, is a fluctuating current with positive mean value. The difference between I_{SQR} and an internally generated current, I_{TGT}, is integrated by C_F and the external capacitor attached to the CLPF pin at the summing node. C_F is an on-chip 25 pF filter capacitor, and C_{LPF}, the external capacitance connected to the CLPF pin, can be used to arbitrarily increase the averaging time while trading off with the response time. When the AGC loop is at equilibrium

$$Mean(I_{SQR}) = I_{TGT} \quad (3)$$

This equilibrium occurs only when

$$Mean(V_{SIG}^2) = V_{TGT}^2 \quad (4)$$

where V_{TGT} is the voltage presented at the VTGT pin. This pin can conveniently be connected to the VREF pin through a voltage divider to establish a target rms voltage V_{ATG} of ~70 mV rms, when V_{TGT} = 1.4 V.

Because the square law detectors are electrically identical and well matched, process and temperature dependent variations are effectively cancelled.

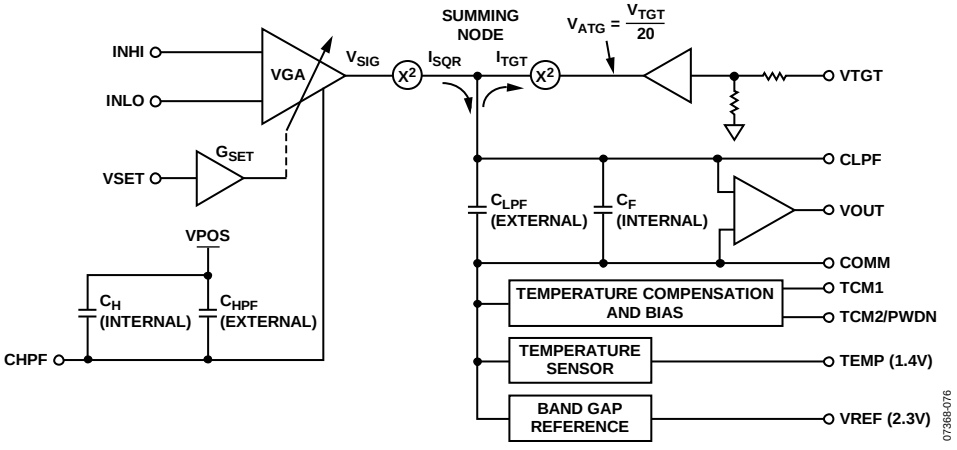

Figure 33. Simplified Architecture Details

By forcing the previous identity through varying the VGA setpoint, it is apparent that

$$RMS(V_{SIG}) = \sqrt{(Mean(V_{SIG}^2))} = \sqrt{(V_{ATG}^2)} = V_{ATG} \quad (5)$$

Substituting the value of V_{SIG} from Equation 2 results in

$$RMS(G_0 \times RF_{IN}\, exp(-V_{SET}/V_{GNS})) = V_{ATG} \quad (6)$$

When connected as a measurement device, $V_{SET} = V_{OUT}$. Solving for V_{OUT} as a function of RF_{IN}

$$V_{OUT} = V_{SLOPE} \times \log_{10}(RMS(RF_{IN})/V_Z) \quad (7)$$

where:
V_{SLOPE} is 1 V/decade (or 50 mV/dB).
V_Z is the intercept voltage.

When $RMS(RF_{IN}) = V_Z$, because $\log_{10}(1) = 0$, this implies that $V_{OUT} = 0$ V, making the intercept the input that forces $V_{OUT} = 0$ V. V_Z has been fixed to approximately 280 µV (approximately −58 dBm, referred to 50 Ω) with a CW signal at 100 MHz. In reality, the AD8363 does not respond to signals less than ~−56 dBm. This means that the intercept is an extrapolated value outside the operating range of the device.

If desired, the effective value of V_{SLOPE} can be altered by using a resistor divider between VOUT and VSET. (Refer to the Output Voltage Scaling section for more information.)

In most applications, the AGC loop is closed through the setpoint interface and the VSET pin. In measurement mode, VOUT is directly connected to VSET. (See the Measurement Mode Basic Connections section for more information.) In controller mode, a control voltage is applied to VSET and the VOUT pin typically drives the control input of an amplification or attenuation system. In this case, the voltage at the VSET pin forces a signal amplitude at the RF inputs of the AD8363 that balances the system through feedback. (See the Controller Mode Basic Connections section for more information.)

RF INPUT INTERFACE

Figure 34 shows the connections of the RF inputs within the AD8363. The input impedance is set primarily by an internal 50 Ω resistor connected between INHI and INLO. A dc level of approximately half the supply voltage on each pin is established internally. Either the INHI pin or the INLO pin can be used as the single-ended RF input pin. (See the Choice of RF Input Pin section.) If the dc levels at these pins are disturbed, performance is compromised; therefore, signal coupling capacitors must be connected from the input signal to INHI and INLO. The input signal high-pass corner formed by the coupling capacitors and the internal resistances is

$$f_{HIGH\text{-}PASS} = 1/(2 \times \pi \times 50 \times C) \quad (8)$$

where C is in farads and $f_{HIGH\text{-}PASS}$ is in hertz. The input coupling capacitors must be large enough in value to pass the input signal frequency of interest. The other input pin should be RF ac-coupled to common (ground).

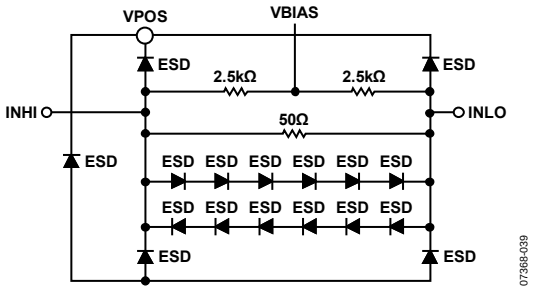

Figure 34. RF Inputs Simplified Schematic

Extensive ESD protection is employed on the RF inputs, which limits the maximum possible input amplitude to the AD8363.

CHOICE OF RF INPUT PIN

The dynamic range of the AD8363 can be optimized by choosing the correct RF input pin for the intended frequency of operation. Using INHI (Pin 14), users can obtain the best dynamic range at frequencies up to 2.6 GHz. Above 2.6 GHz, it is recommended that INLO (Pin 15) be used. At 2.6 GHz, the performance obtained at the two inputs is approximately equal.

The AD8363 was designed with a single-ended RF drive in mind. A balun can be used to drive INHI and INLO differentially, but it is not necessary, and it does not result in improved dynamic range.

SMALL SIGNAL LOOP RESPONSE

The AD8363 uses a VGA in a loop to force a squared RF signal to be equal to a squared dc voltage. This nonlinear loop can be simplified and solved for a small signal loop response. The low-pass corner pole is given by

$$Freq_{LP} \approx 1.83 \times I_{TGT}/(C_{LPF}) \quad (9)$$

where:
I_{TGT} is in amperes.
C_{LPF} is in farads.
$Freq_{LP}$ is in hertz.

I_{TGT} is derived from V_{TGT}; however, I_{TGT} is a squared value of V_{TGT} multiplied by a transresistance, namely

$$I_{TGT} = g_m \times V_{TGT}^2 \quad (10)$$

g_m is approximately 18.9 µs, so with V_{TGT} equal to the typically recommended 1.4 V, I_{TGT} is approximately 37 µA. The value of this current varies with temperature; therefore, the small signal pole varies with temperature. However, because the RF squaring circuit and dc squaring circuit track with temperature, there is no temperature variation contribution to the absolute value of V_{OUT}.

For CW signals,

$$Freq_{LP} \approx 67.7 \times 10^{-6}/(C_{LPF}) \quad (11)$$

However, signals with large crest factors include low pseudorandom frequency content that either needs to be filtered out or sampled and averaged out. See the Choosing a Value for CLPF section for more information.

TEMPERATURE SENSOR INTERFACE

The AD8363 provides a temperature sensor output with an output voltage scaling factor of approximately 5 mV/°C. The output is capable of sourcing 4 mA and sinking 50 µA maximum at temperatures at or above 25°C. If additional current sink capability is desired, an external resistor can be connected between the TEMP and COMM pins. The typical output voltage at 25°C is approximately 1.4 V.

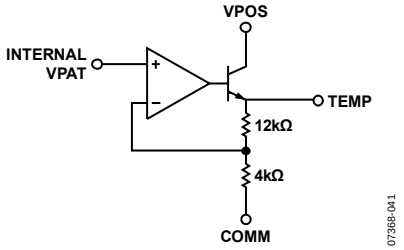

Figure 35. TEMP Interface Simplified Schematic

VREF INTERFACE

The VREF pin provides an internally generated voltage reference. The V_{REF} voltage is a temperature stable 2.3 V reference that is capable of sourcing 4 mA and sinking 50 µA maximum at temperatures at or above 25°C. An external resistor can be connected between the VREF and COMM pins to provide additional current sink capability. The voltage on this pin can be used to drive the TCM1, TCM2/PWDN, and VTGT pins, if desired.

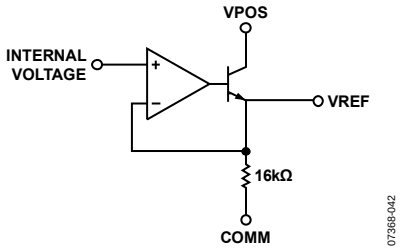

Figure 36. VREF Interface Simplified Schematic

TEMPERATURE COMPENSATION INTERFACE

Proprietary techniques are used to maximize the temperature stability of the AD8363. For optimal performance, the output temperature drift must be compensated for using the TCM1 and TCM2/PWDN pins. The absolute value of compensation varies with frequency and V_{TGT}. Table 4 shows the recommended voltages for the TCM1 and TCM2/PWDN pins to maintain the best temperature drift error over the rated temperature range (−40°C < T_A < 85°C) when driven single-ended and using a V_{TGT} = 1.4 V.

Table 4. Recommended Voltages for TCM1 and TCM2/PWDN

Frequency	TCM1 (V)	TCM2/PWDN (V)
100 MHz	0.47	1.0
900 MHz	0.5	1.2
1.9 GHz	0.52	0.51
2.14 GHz	0.52	0.6
2.6 GHz	0.54	1.1
3.8 GHz	0.56	1.0
5.8 GHz	0.88	1.0

The values in Table 4 were chosen to give the best drift performance at the high end of the usable dynamic range over the −40°C to +85°C temperature range.

Compensating the device for the temperature drift using TCM1 and TCM2/PWDN allows for great flexibility and the user may wish to modify these values to optimize for another amplitude point in the dynamic range, for a different temperature range, or for an operating frequency other than those shown in Table 4.

To find a new compensation point, V_{TCM1} and V_{TCM2} can be swept while monitoring V_{OUT} over the temperature at the frequency and amplitude of interest. The optimal voltages for V_{TCM1} and V_{TCM2} to achieve minimum temperature drift at a given power and frequency are the values of V_{TCM1} and V_{TCM2} where V_{OUT} has minimum movement. See the AD8364 and ADL5513 data sheets for more information.

Varying V_{TCM1} and V_{TCM2} has only a very slight effect on V_{OUT} at device temperatures near 25°C; however, the compensation circuit has more and more effect, and is more and more necessary for best temperature drift performance, as the temperature departs farther from 25°C.

Figure 37 shows the effect on temperature drift performance at 25°C and 85°C as V_{TCM1} is varied but V_{TCM2} is held constant at 0.6 V.

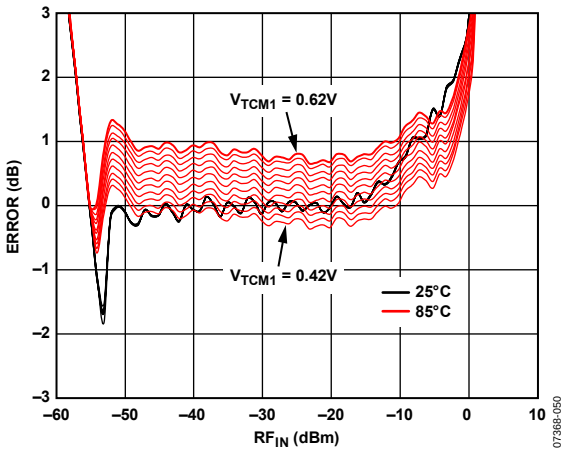

Figure 37. Error vs. Input Amplitude over Stepped V_{TCM1} Values, 25°C and 85°C, 2.14 GHz, V_{TCM2} = 0.6 V

TCM1 primarily adjusts the intercept of the AD8363 at temperature. In this way, TCM1 can be thought of as a coarse adjustment to the compensation. Conversely, TCM2 performs a fine adjustment. For this reason, it is advised that when searching for compensation with V_{TCM1} and V_{TCM2}, that V_{TCM1} be adjusted first, and when best performance is found, V_{TCM2} can then be adjusted for optimization.

It is evident from Figure 37 that the temperature compensation circuit can be used to adjust for the lowest drift at any input amplitude of choice. Though not shown in Figure 37, a similar analysis can simultaneously be performed at −40°C, or any other temperature within the operating range of the AD8363.

Performance varies slightly from device to device; therefore, optimal V_{TCM1} and V_{TCM2} values must be arrived at statistically

over a population of devices to be useful in mass production applications.

The TCM1 and TCM2 pins have high input impedances, approximately 5 kΩ and 500 kΩ, respectively, and can be conveniently driven from an external source or from a fraction of VREF by using a resistor divider. VREF does change slightly with temperature and RF input amplitude (see Figure 32 and Figure 29); however, the amount of change is unlikely to result in a significant effect on the final temperature stability of the RF measurement system.

Figure 38 shows a simplified schematic representation of TCM1. See the Power-Down Interface section for the TCM2 interface.

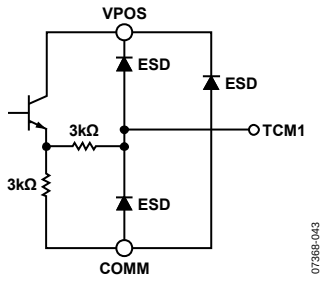

Figure 38. TCM1 Interface Simplified Schematic

POWER-DOWN INTERFACE

The quiescent and disabled currents for the AD8363 at 25°C are approximately 60 mA and 300 µA, respectively. The dual function pin, TCM2/PWDN, is connected to a temperature compensation circuit as well as a power-down circuit. Typically, when PWDN is greater than V_{POS} − 0.1 V, the device is fully powered down. Figure 28 shows this characteristic as a function of V_{PWDN}. Note that because of the design of this section of the AD8363, as V_{TCM2} passes through a narrow range at ~4.5 V (or ~V_{POS} − 0.5 V), the TCM2/PWDN pin sinks approximately 750 µA. The source used to disable the AD8363 must have a sufficiently high current capability for this reason. Figure 23 shows the typical response times for various RF input levels. The output reaches within 0.1 dB of its steady-state value in approximately 35 µs; however, the reference voltage is available to full accuracy in a much shorter time. This wake-up response varies depending on the input coupling and the capacitances, C_{HPF} and C_{LPF}.

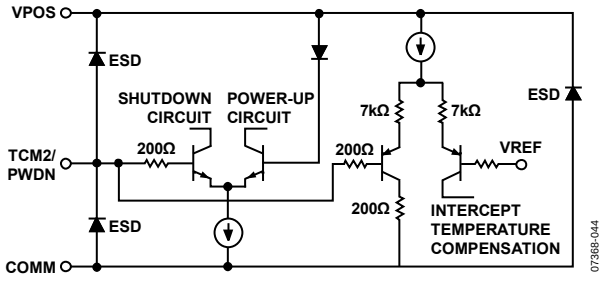

Figure 39. PWDN Interface Simplified Schematic

VSET INTERFACE

The VSET interface has a high input impedance of 72 kΩ. The voltage at VSET is converted to an internal current used to set the internal VGA gain. The VGA attenuation control is approximately 19 dB/V.

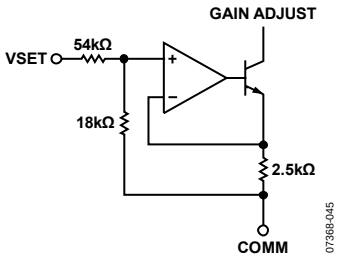

Figure 40. VSET Interface Simplified Schematic

OUTPUT INTERFACE

The output driver used in the AD8363 is different from the output stage on the AD8362. The AD8363 incorporates rail-to-rail output drivers with pull-up and pull-down capabilities. The closed-loop −3 dB bandwidth of the VOUT buffer with no load is approximately 58 MHz with a single-pole roll-off of −20 dB/dec. The output noise is approximately 45 nV/√Hz at 100 kHz, which is independent of C_{LPF} due to the architecture of the AD8363. VOUT can source and sink up to 10 mA. There is an internal load between VOUT and COMM of 2.5 kΩ.

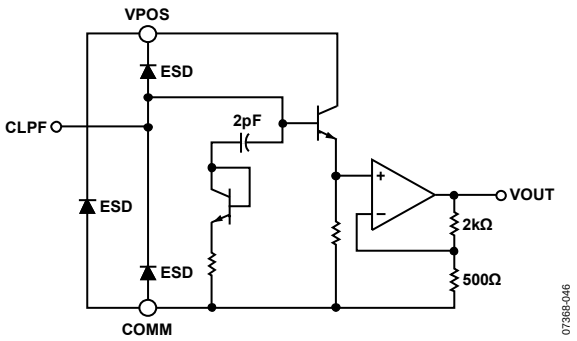

Figure 41. VOUT Interface Simplified Schematic

VTGT INTERFACE

The target voltage can be set with an external source or by connecting the VREF pin (nominally 2.3 V) to the VTGT pin through a resistive voltage divider. With 1.4 V on the VTGT pin, the rms voltage that must be provided by the VGA to balance the AGC feedback loop is 1.4 V × 0.05 = 70 mV rms. Most of the characterization information in this data sheet was collected at V_{TGT} = 1.4 V. Voltages higher and lower than this can be used; however, doing so increases or decreases the gain at the internal squaring cell, which results in a corresponding increase or decrease in intercept. This in turn affects the sensitivity and the usable measurement range. Because the gain of the squaring cell varies with temperature, oscillations or a loss in measurement range can result. For these reasons, do not reduce V_{TGT} below 1.3 V.

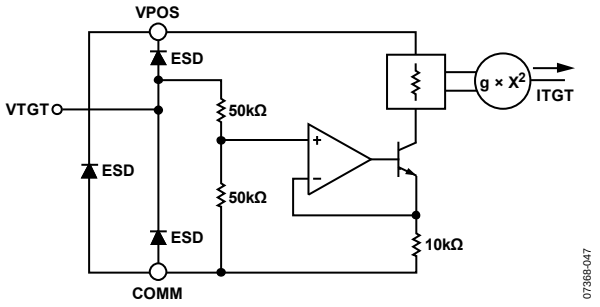

Figure 42. VTGT Interface Simplified Schematic

MEASUREMENT MODE BASIC CONNECTIONS

The AD8363 requires a single supply of nominally 5 V. The supply is connected to the two supply pins, VPOS. Decouple the pins using two capacitors with values equal or similar to those shown in Figure 43. These capacitors must provide a low impedance over the full frequency range of the input, and they should be placed as close as possible to the VPOS pins. Use two different capacitor values in parallel to provide a broadband ac short to ground.

Input signals can be applied differentially or single-ended; however, in both cases, the input impedance is 50 Ω. Most performance information in this data sheet was derived with a single-ended drive. The optimal measurement range is achieved using a single-ended drive on the INHI pin at frequencies below 2.6 GHz (as shown in Figure 43), and likewise, optimal performance is achieved using the INLO pin above 2.6 GHz (similar to Figure 43; except INLO is ac-coupled to the input and INHI is ac-coupled to ground).

The AD8363 is placed in measurement mode by connecting VOUT to VSET. This closes the AGC loop within the device with V_{OUT} representing the VGA control voltage, which is required to present the correct rms voltage at the input of the internal square law detector.

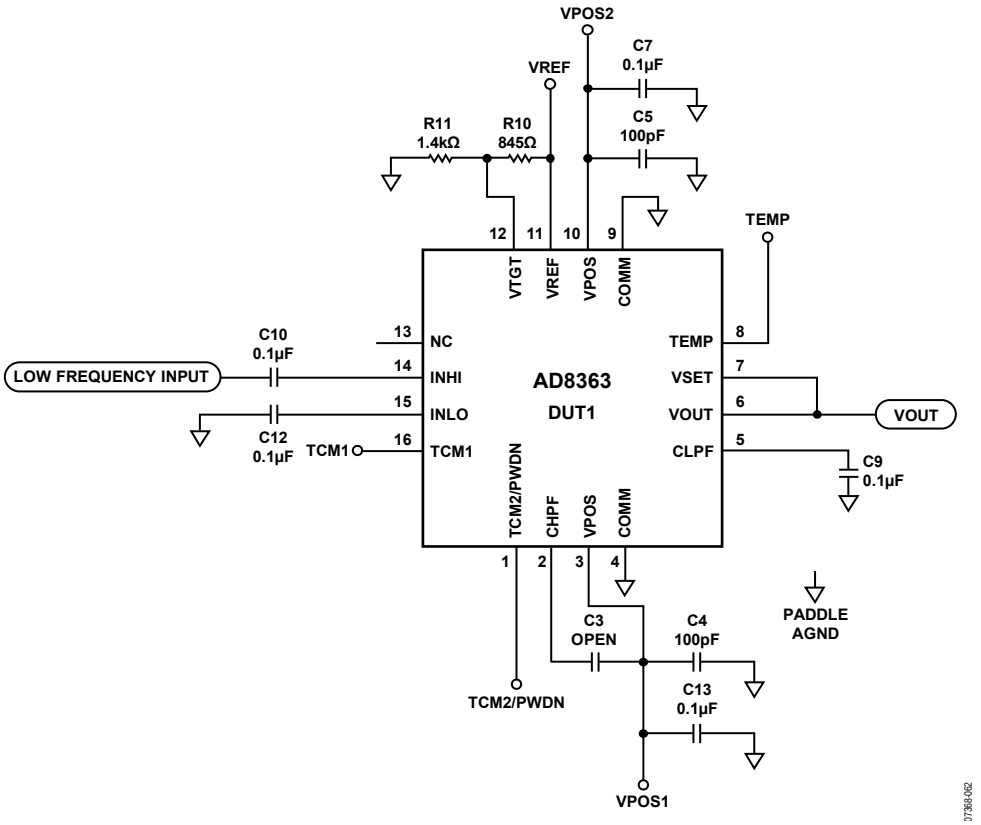

Figure 43. Measurement Mode Basic Connections

SYSTEM CALIBRATION AND ERROR CALCULATION

The measured transfer function of the AD8363 at 1.9 GHz is shown in Figure 44, which contains plots of both output voltage vs. input amplitude (power) and calculated error vs. input level. As the input level varies from −55 dBm to +0 dBm, the output voltage varies from ~0 V to ~3.1 V.

Because slope and intercept vary from device to device, board-level calibration must be performed to achieve high accuracy. The equation for the idealized output voltage can be written as

$$V_{OUT(IDEAL)} = Slope \times (P_{IN} - Intercept) \quad (12)$$

where:

Slope is the change in output voltage divided by the change in input power (dB).

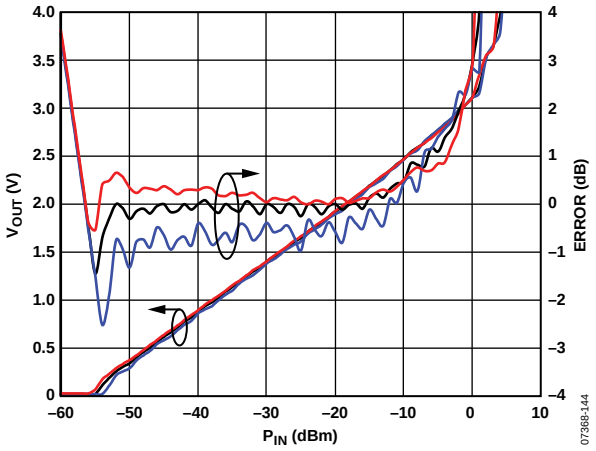

Figure 44. 1.9 GHz Transfer Function and Linearity Error using a Two-Point Calibration (Calibration Points −20 dBm and −40 dBm)

Intercept is the calculated input power level at which the output voltage would equal 0 V (note that *Intercept* is an extrapolated theoretical value not a measured value).

In general, calibration, which establishes the *Slope* and *Intercept*, is performed during equipment manufacture by applying two or more known signal levels to the input of the AD8363 and measuring the corresponding output voltages. The calibration points are generally chosen within the linear-in-dB operating range of the device.

With a two-point calibration, the slope and intercept are calculated as follows:

$$Slope = (V_{OUT1} - V_{OUT2})/(P_{IN1} - P_{IN2}) \quad (13)$$

$$Intercept = P_{IN1} - (V_{OUT1}/Slope) \quad (14)$$

After the slope and intercept are calculated and stored in non-volatile memory during equipment calibration, an equation can be used to calculate an unknown input power based on the output voltage of the detector.

$$P_{IN}\,(Unknown) = (V_{OUT1(MEASURED)}/Slope) + Intercept \quad (15)$$

The log conformance error is the difference between this straight line and the actual performance of the detector.

$$Error\,(dB) = (V_{OUT(MEASURED)} - V_{OUT(IDEAL)})/Slope \quad (16)$$

Figure 44 includes a plot of this error when using a two-point calibration (calibration points are −20 dBm and −40 dBm). The error at the calibration points is equal to 0 by definition.

The residual nonlinearity of the transfer function that is apparent in the two-point calibration error plot can be reduced by increasing the number of calibration points. Figure 45 shows the post-calibration error plots for three-point calibration. With a multipoint calibration, the transfer function is segmented, with each segment having its own slope and intercept. During calibration, multiple known power levels are applied, and multiple voltages are measured. When the equipment is in operation, the measured voltage from the detector is first used to determine which of the stored slope and intercept calibration coefficients are to be used. Then the unknown power level is calculated by inserting the appropriate slope and intercept into Equation 15.

Figure 45 shows the output voltage and error at 25°C and over temperature when a three-point calibration is used (calibration points are 0 dBm, −10 dBm and −40 dBm). When choosing calibration points, there is no requirement for, or value in equal spacing between the points. There is also no limit to the number of calibration points used.

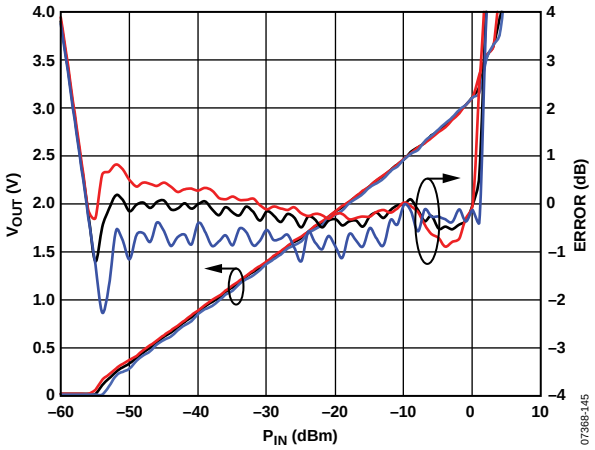

Figure 45. 1.9 GHz Transfer Function and Error at +25°C, −40°C, and +85°C Using a Three-Point Calibration (0 dBm, −10 dBm and −40 dBm)

The −40°C and +85°C error plots in Figure 44 and Figure 45 are generated using the 25°C calibration coefficients. This is consistent with equipment calibration in a mass production environment where calibration at just a single temperature is practical.

OPERATION TO 125°C

The AD8363 operates up to 125°C with slightly degraded performance. Figure 46 shows the typical operation (Errors are plotted using two-point calibration) at 125°C as compared to other temperatures using the TCM1 and TCM2 values in Table 4. Temperature compensation can be optimized for operation above 85°C by modifying the voltages on the TCM1 and TCM2 pins from those shown in Table 4.

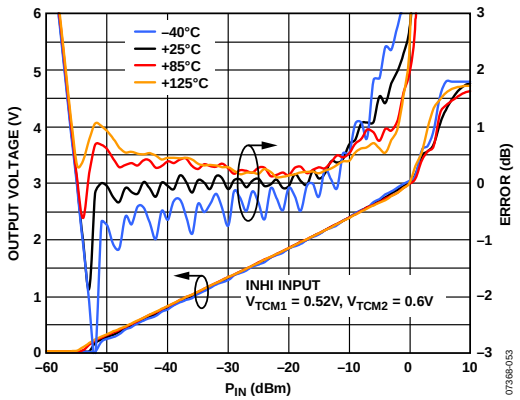

Figure 46. V_{OUT} and Log Conformance Error vs. Input Amplitude at 2.14 GHz, −40°C to +125°C

OUTPUT VOLTAGE SCALING

The output voltage range of the AD8363 (nominally 0 V to 3.5 V) can be easily increased or decreased. There are a number of situations where adjustment of the output scaling makes sense. For example, if the AD8363 is driving an analog-to-digital converter (ADC) with a 0 V to 5 V input range, it makes sense to increase the detector's nominal maximum output voltage of 3.5 V so that it is closer to 5 V. This makes better use of the input range of the ADC and maximizes the resolution of the system in terms of bits/dB.

If only a part of the RF input power range of the AD8363 is being used (for example, −10 dBm to −40 dBm), it may make sense to increase the scaling so that this reduced input range fits into the available output swing of the AD8363 (0 V to 4.8 V).

The output swing can be reduced by adding a voltage divider on the output pin, as shown in Figure 47 (with VOUT connected directly to VSET and a resistor divider on VOUT). Figure 47 also shows how the output voltage swing can be increased using a technique that is analogous to setting the gain of an op amp in noninverting mode. With the VSET pin being the equivalent of the inverting input of the op amp, a resistor divider is connected between VOUT and VSET.

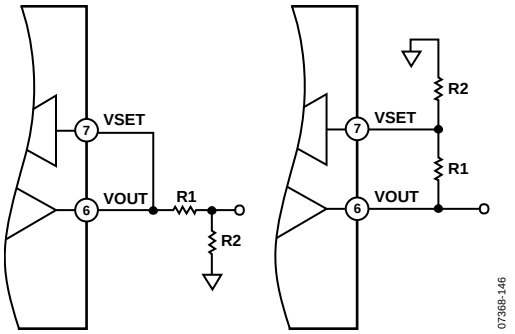

Figure 47. Decreasing and Increasing Slope

Equation 17 is the general function that governs this.

$$R1 = (R2 \parallel R_{IN})\left(\frac{V_O'}{V_O} - 1\right) \quad (17)$$

where:

V_O is the nominal maximum output voltage (see Figure 4 through Figure 18).

V'_O is the new maximum output voltage (for example, up to 4.8 V).

R_{IN} is the VSET input resistance (72 kΩ).

When choosing R1 and R2, attention must be paid to the current drive capability of the VOUT pin and the input resistance of the VSET pin. The choice of resistors should not result in excessive current draw out of VOUT. However, making R1 and R2 too large is also problematic. If the value of R2 is compatible with the 72 kΩ input resistance of the VSET input, this input resistance, which varies slightly from device to device, contributes to the resulting slope and output voltage. In general, the value of R2 should be at least ten times smaller than the input resistance of VSET. Values for R1 and R2 should, therefore, be in the 1 kΩ to 5 kΩ range.

It is also important to take into account device-to-device and frequency variation in output swing along with the AD8363 output stage's maximum output voltage of 4.8 V. The V_{OUT} distribution is well characterized at the bands of major frequencies in the Typical Performance Characteristics section (Figure 3 to Figure 18).

OFFSET COMPENSATION, MINIMUM C_{LPF}, AND MAXIMUM C_{HPF} CAPACITANCE VALUES

An offset-compensation loop is used to eliminate small dc offsets within the internal VGA as shown in Figure 48. The high-pass corner frequency of this loop is set to about 1 MHz using an on-chip 25 pF capacitor. Because input signals that are below 1 MHz are interpreted as unwanted offset voltages, this restricts the operating frequency range of the device. To operate the AD8363 at lower frequencies (than 1 MHz), the high-pass corner frequency must be reduced by connecting a capacitor between CHPF and VPOS.

Internal offset voltages vary depending on the gain at which the VGA is operating and, therefore, on the input signal amplitude. When a large C_{HPF} value is used, the offset correction process can lag the more rapid changes in the gain of the VGA, which can increase the time required for the loop to fully settle for a given steady input amplitude. This can manifest itself in a jumpy, seemingly oscillatory response of the AD8363.

Care should therefore be taken in choosing C_{HPF} and C_{LPF} because there is a potential to create oscillations. In general, make the capacitance on the CLPF pin as large as possible; there is no maximum on the amount of capacitance that can be added to this pin. At high frequencies, there is no need for an external capacitor on the CHPF pin; therefore, the pin can be left open. However, when trying to get a fast response time and/or when working at low frequencies, extra care in choosing the proper capacitance values for C_{HPF} and C_{LPF} is prudent. With the gain control pin (VSET) connected to VOUT, V_{SET} can slew at a rate determined by the on-chip squaring cell and C_{LPF}. When V_{SET} is changing with time, the dc offsets in the VGA also vary with

time. The speed at which V_{SET} slews can create a time varying offset that falls within the high-pass corner set by C_{HPF}. Therefore, in measurement mode, take care to set C_{LPF} appropriately to reduce the slew. It is also worth noting that most of the typical performance data was derived with C_{LPF} = 3.9 nF and C_{HPF} = 2.7 nF and with a CW waveform.

The minimum appropriate C_{LPF} based on slew rate limitations is as follows

$$C_{LPF} > 20 \times 10^{-3}/FREQ_{RFIN} \quad (18)$$

where:
C_{LPF} is in farads.
$FREQ_{RFIN}$ is in hertz.

This takes into account the on-chip 25 pF capacitor, C_F, in parallel with C_{LPF}. However, because there are other internal device time delays that affect loop stability, use a minimum C_{LPF} of 390 pF.

The minimum appropriate C_{HPF} for a given high-pass pole frequency is

$$C_{HPF} = 29.2 \times 10^{-6}/FHP_{POLE} - 25 \text{ pF} \quad (19)$$

where FHP_{POLE} is in hertz.

The subtraction of 25 pF is a result of the on-chip 25 pF capacitor in parallel with the external C_{HPF}. Typically, choose C_{HPF} to give a pole (3 dB corner) at least 1 decade below the desired signal frequency. Note that the high pass corner of the offset compensation system is approximately 1 MHz without an external C_{HPF}; therefore, adding an external capacitor lowers the corner frequency.

The following example illustrates the proper selection of the input coupling capacitors, minimum C_{LPF}, and maximum C_{HPF} when using the AD8363 in measurement mode for a 1 GHz input signal.

1. Choose the input coupling capacitors that have a 3 dB corner at least one decade below the input signal frequency. From Equation 8, $C > 10/(2 \times \pi \times RF_{IN} \times 50) = 32$ pF minimum. According to this calculation, 32 pF is sufficient; however, the input coupling capacitors should be a much larger value, typically 0.1 µF. The offset compensation circuit, which is connected to CHPF, should be the true determinant of the system high-pass corner frequency and not the input coupling capacitors. With 0.1 µF coupling capacitors, signals as low as 32 kHz can couple to the input, which is well below the system high-pass frequency.
2. Choose C_{LPF} to reduce instabilities due to VSET slew rate. See Equation 18, where FRQ_{RFIN} = 1 GHz, and this results in C_{LPF} > 20 pF. However, as previously mentioned, values below 390 pF are not recommended. For this reason, a 470 pF capacitor was chosen. In addition, if fast response times are not required, an even larger C_{LPF} value than given here should be chosen.
3. Choose C_{HPF} to set a 3 dB corner to the offset compensation system. See Equation 19, where FHP_{POLE} is in this case 100 MHz, one decade below the desired signal. This results in a negative number and, obviously, a negative value is not practical. Because the high-pass corner frequency is already 1 MHz, this result simply illustrates that the appropriate solution is to use no external C_{HPF} capacitor.

Note that per Equation 9

$$Freq_{LP} \approx 1.83 \times I_{TGT}/(C_{LPF})$$

A C_{LPF} of 470 pF results in a small signal low-pass corner frequency of approximately 144 kHz. This reflects the bandwidth of the measurement system, and how fast the user can expect changes on the output. It does not imply any limitations on the input RF carrier frequency.

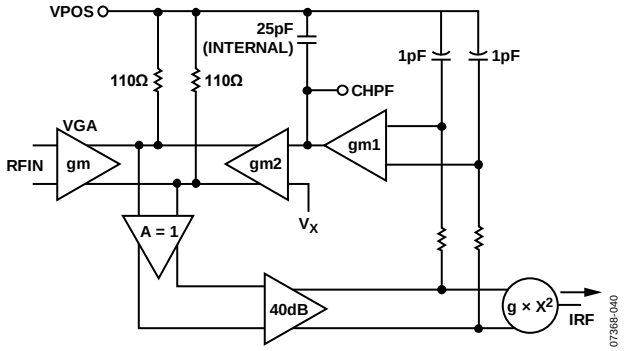

Figure 48. Offset Compensation Circuit

CHOOSING A VALUE FOR C_{LPF}

The Small Signal Loop Response section and the Offset Compensation, Minimum CLPF, and Maximum CHPF Capacitance Values section discussed how to choose the minimum value capacitance for C_{LPF} based on a minimum capacitance of 390 pF, slew rate limitation, and frequency of operation. Using the minimum value for C_{LPF} allows the quickest response time for pulsed type waveforms (such as WiMAX) but also allows the most residual ripple on the output caused by the pseudorandom modulation waveform. There is not a maximum for the capacitance that can be applied to the CLPF pin, and in most situations, a large enough capacitor can be added to remove the residual ripple caused by the modulation and yet allow a fast enough response to changes in input power.

Figure 49 shows how residual ripple, rise time, and fall time vary with filter capacitance when the AD8363 is driven by a single carrier CDMA2000 9CH SR1 signal at 2.14 GHz. The rise time and fall time is based on a signal that is pulsed between no signal and 10 dBm but is faster if the input power change is less.

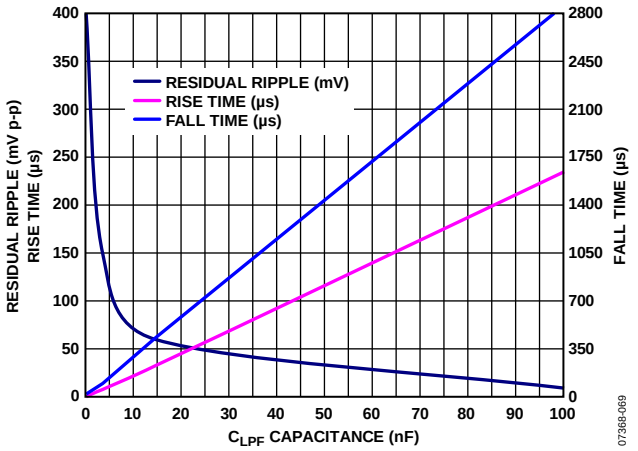

Figure 49. Residual Ripple, Rise Time, and Fall Time vs. C_{LPF} Capacitance, Single Carrier CDMA2000 9CH SR1 Signal at 2.14 GHz with 10 dBm Pulse

Table 5 shows the recommended values of C_{LPF} for popular modulation schemes. For nonpulsed waveforms, increase C_{LPF} until the residual output noise falls below 50 mV (±0.5 dB). In each case, the capacitor can be increased to further reduce the noise. A 10% to 90% step response to an input step is also listed. Where the increased response time is unacceptably high, reduce C_{LPF}, which increases the noise on the output. Due to the random nature of the output ripple, if it is sampled by an ADC, averaging in the digital domain further reduces the residual noise.

Table 5 gives C_{LPF} values to minimize noise while trying to keep a reasonable response time. For non-pulsed type waveforms, averaging is not required on the output. For pulsed waveforms, the smaller the noise, the less averaging is needed on the output.

System specifications determine the necessary rise time and fall time. For example, the suggested C_{LPF} value for WiMAX assumes that it is not necessary to measure the power in the preamble.

Figure 50 shows how the rise time cuts off the preamble. Note that the power in the preamble can be easily measured; however, the C_{LPF} value would have to be reduced slightly, and the noise in the main signal would increase.

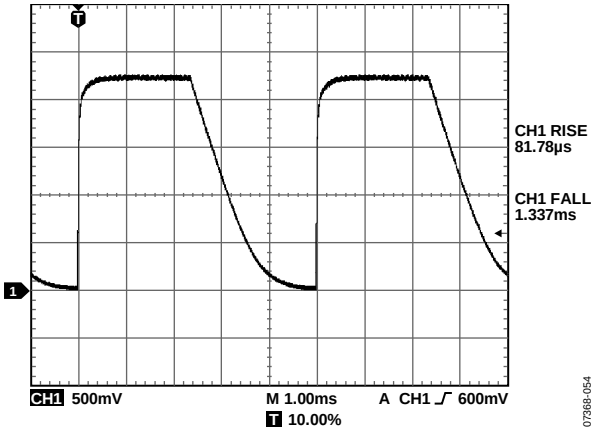

Figure 50. AD8363 Output Response to a WiMAX 802.16, 64 QAM, 256 Subcarriers, 10 MHz Bandwidth Signal with C_{LPF} = 0.027 µF

As shown in Figure 49, the fall time for the AD8363 increases faster than the rise time with an increase in C_{LPF} capacitance. Some pulse-type modulation standards require a fast fall time as well as a fast rise time, and in all cases, less output ripple is desired. Placing an RC filter on the output reduces the ripple, according to the frequency content of the ripple and the poles and zeros of the filter. Using an RC output filter also changes the rise and fall time vs. the output ripple response as compared to increasing the C_{LPF} capacitance.

Table 5. Recommended C_{LPF} Values for Various Modulation Schemes

Modulation/Standard	Crest Factor (dB)	C_{LPF}	Residual Ripple (mV p-p)	Response Time (Rise/Fall) 10% to 90%
W-CDMA, 1Carrier, TM1-64	12	0.1 µF	15	236 µs/2.9 ms
W-CDMA, 1Carrier, TM1-64 (EVDO)	12	3900 pF	150	8.5 µs/100 µs
W-CDMA 4Carrier, TM1-64	11	0.1 µF	8	240 µs/2.99 ms
CDMA2000, 1Carrier, 9CH	9.1	0.1 µF	10	210 µs/3.1 ms
CDMA2000, 3Carrier, 9CH	11	0.1 µF	13	215 µs/3.14 ms
WiMAX 802.16 , 64 QAM, 256 Subcarriers, 10 MHz Bandwidth	14	0.027 µF	10	83 µs/1.35 ms
6C TD-SCDMA	14	0.01 µF	69	24 µs/207 µs
1C TD-SCDMA	11.4	0.01 µF	75	24 µs /198 µs

Figure 51 shows the response for a 2.14 GHz pulsed signal, with C_{LPF} = 3900 pF. The residual ripple from a single carrier CDMA2000 9CH SR1 signal is 150 mV p-p. (The ripple is not shown in Figure 51. The ripple was measured separately.) Figure 52 shows the response for a 2.14 GHz pulse signal with a C_{LPF} of 390 pF and an output filter that consists of a series 75 Ω resistor (closest to the output) followed by a 0.15 µF capacitor to ground. The residual ripple for this configuration is also 150 mV p-p. Note that the rise time is faster and the fall time is slower when the larger C_{LPF} is used to obtain a 150 mV p-p ripple.

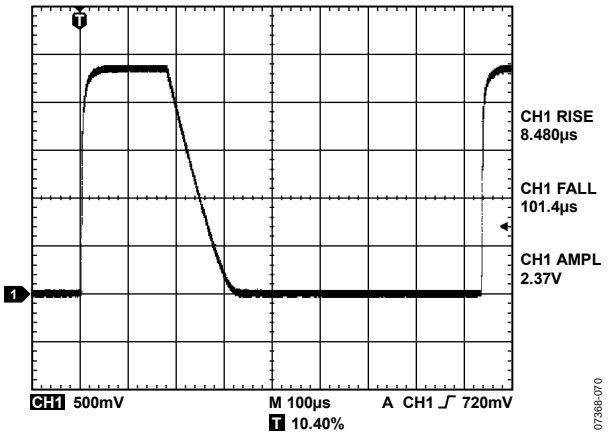

Figure 51. Pulse Response with C_{LPF} = 3900 pF Resulting in a 150 mV p-p Ripple for a Single Carrier CDMA2000 9CH SR1 Signal at 2.14 GHz

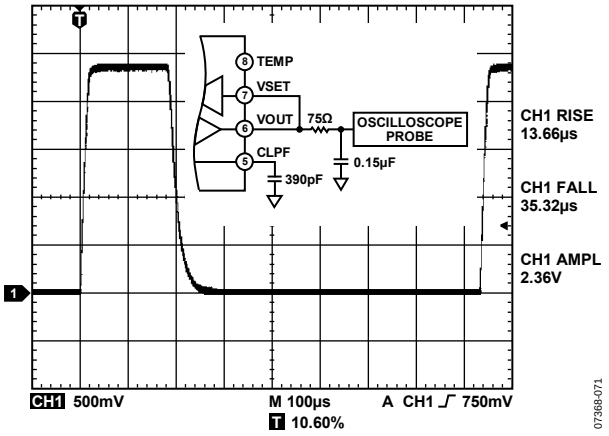

Figure 52. Pulse Response with C_{LPF} = 390 pF and Series 75 Ω Resistor Followed by a 0.15 µF Capacitor to Ground, Resulting in a 150 mV p-p Ripple for a Single Carrier CDMA2000 9CH SR1 Signal at 2.14 GHz

RF PULSE RESPONSE AND VTGT

The response of the AD8363 to pulsed RF waveforms is affected by V_{TGT}. Referring to Figure 21 and Figure 22, there is a period of inactivity between the start of the RF waveform and the time at which V_{OUT} begins to show a reaction. This happens as a result of the implementation of the balancing of the squarer currents within the AD8363. This delay can be reduced by decreasing V_{TGT}; however, as previously noted in the VTGT Interface section, this has implications on the sensitivity, intercept, and dynamic range. While the delay is reduced, reducing V_{TGT} increases the rise and fall time of V_{OUT}.

CONTROLLER MODE BASIC CONNECTIONS

In addition to being a measurement device, the AD8363 can also be configured to control rms signal levels, as shown in Figure 53.

The RF input to the device is configured as it was in measurement mode and either input can be used. A directional coupler taps off some of the power being generated by the VGA. If loss in the main signal path is not a concern, and there are no issues with reflected energy from the next stage in the signal chain, a power splitter can be used instead of a directional coupler. Some additional attenuation may be required to set the maximum input signal at the AD8363 to be equal to the recommended maximum input level for optimum linearity and temperature stability at the frequency of operation.

The VSET and VOUT pins are no longer shorted together. VOUT now provides a bias or gain control voltage to the VGA. The gain control sense of the VGA must be negative and monotonic, that is, increasing voltage tends to decrease gain. However, the gain control transfer function of the device does not need to be well controlled or particularly linear. If the gain control sense of the VGA is positive, an inverting op amp circuit with a dc offset shift can be used between the AD8363 and the VGA to keep the gain control voltage in the 0.03 V to 4.8 V range.

VSET becomes the set-point input to the system. This can be driven by a DAC, as shown in Figure 53, if the output power is expected to vary, or it can simply be driven by a stable reference voltage, if constant output power is required. This DAC should have an output swing that covers the 0.15 V to 3.5 V range.

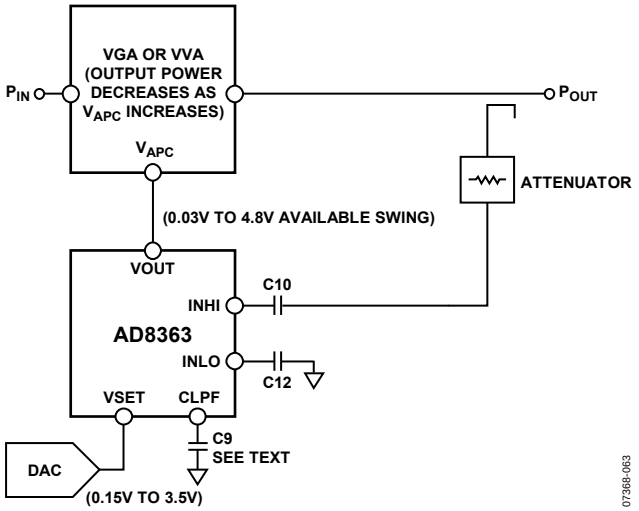

Figure 53. Controller Mode Operation for Automatic Power Control

When V_{SET} is set to a particular value, the AD8363 compares this value to the equivalent input power present at the RF input. If these two values do not match, V_{OUT} increases or decreases in an effort to balance the system. The dominant pole of the error amplifier/integrator circuit that drives V_{OUT} is set by the capacitance on the CLPF pin; some experimentation may be necessary to choose the right value for this capacitor.

In general, C_{LPF} should be chosen to provide stable loop operation for the complete output power control range. If the slope (in dB/V) of the gain control transfer function of the VGA is not constant, C_{LPF} must be chosen to guarantee a stable loop when the gain control slope is at its maximum. In addition, C_{LPF} must provide adequate averaging to the internal low range squaring detector so that the rms computation is valid. Larger values of C_{LPF} tend to make the loop less responsive.

The relationship between V_{SET} and the RF input follows the measurement mode behavior of the device. For example, Figure 4 shows the measurement mode transfer function at 900 MHz and that an input power of −10 dBm yields an output voltage of approximately 2.5 V. Therefore, in controller mode, if V_{SET} is 2.5 V, the AD8363 output would go to whatever voltage is necessary to set the AD8363 input power to −10 dBm.

CONSTANT OUTPUT POWER OPERATION

In controller mode, the AD8363 can be used to hold the output power of a VGA stable over a broad temperature/input power range. This is useful in topologies where a transmit card is driving an HPA, or when connecting any two power sensitive modules together.

Figure 54 shows a schematic of a circuit setup that holds the output power to approximately −26 dBm at 2.14 GHz, when the input power is varied over a 40 dB dynamic range. Figure 55 shows the results. A portion of the output power is coupled off using a 10 dB directional coupler, and it is then fed into the AD8363. V_{SET} is fixed at 0.95 V, which forces to AD8363 output voltage to control the ADL5330 so that the input to the AD8363 is approximately −36 dBm.

If the AD8363 was in measurement mode and a −36 dBm input power is applied, the output voltage would be 0.95 V. A general-purpose, rail-to-rail op amp (AD8062) is used to invert the slope of the AD8363 so that the gain of the ADL5330 decreases as the AD8363 control voltage increases. The output power is controlled to a 10 dB higher power level than that seen by the AD8363 due to the coupler. The high-end power is limited by the linearity of the VGA (ADL5330) with high attenuation and can be increased by using a higher linearity VGA.

The low end power is limited by the maximum gain of the VGA (ADL5330) and can be increased by using a VGA with more gain. The temperature performance is directly related to the temperature performance of the AD8363 at 2.14 GHz and −26 dBm, using TCM1 = 0.52 V and TCM2 = 0.6 V. All other temperature variations are removed by the AD8363.

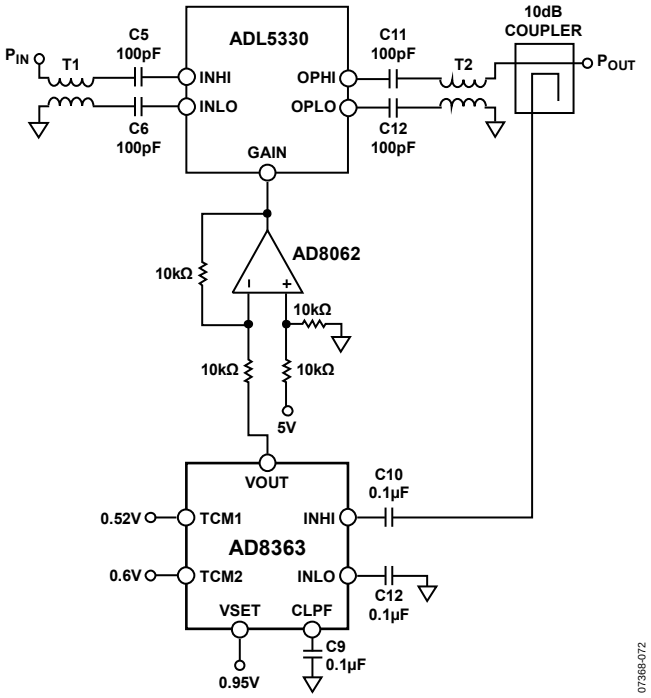

Figure 54. Constant Power Circuit

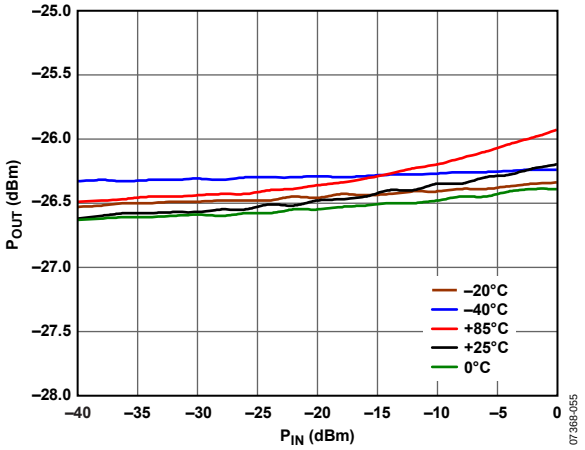

Figure 55. Performance of the Circuit Shown in Figure 54

DESCRIPTION OF RF CHARACTERIZATION

The general hardware configuration used for most of the AD8363 characterization is shown in Figure 56. The AD8363 was driven in a single-ended configuration for all characterization.

Characterization of the AD8363 employed a multisite test strategy. Several AD8363 devices mounted on circuit boards constructed with Rogers 3006 material was simultaneously inserted into a remotely-controlled thermal test chamber. A Keithley S46 RF switching network connected an Agilent E8251A signal source to the appropriate device under test. An Agilent 34980A switch matrix provided switching of dc power and metering for the test sites. A PC running Agilent VEE Pro controlled the signal source, switching, and chamber temperature.

A voltmeter measured the subsequent response to the stimulus, and the results were stored in a database for later analysis. In this way, multiple AD8363 devices were characterized over amplitude, frequency, and temperature in a minimum amount of time.

The RF stimulus amplitude was calibrated up to the connector of the circuit board that carries the AD8363. However, the calibration does not account for the slight losses due to the connector and the traces from the connector to the device under test. For this reason, there is a small absolute amplitude error (<0.5 dB) not accounted for in the characterization data.

This implies a slight error in the reported intercept; however, this is generally not important because the slope and the relative accuracy of the AD8363 are not affected.

The typical performance data was derived with C_{LPF} = 3.9 nF and C_{HPF} = 2.7 nF with a CW waveform.

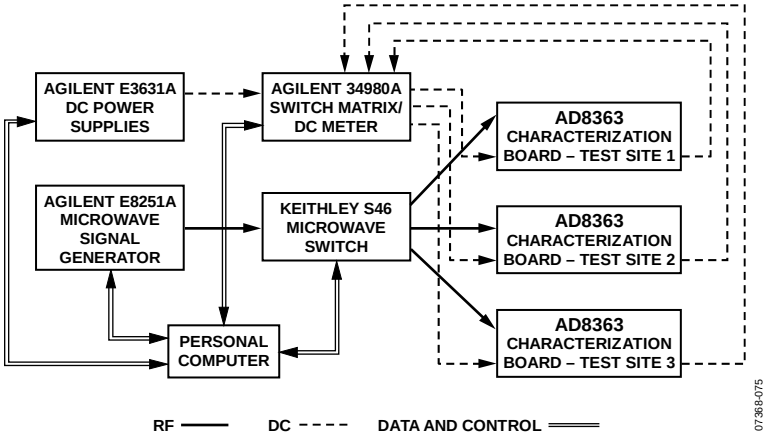

Figure 56. General RF Characterization Configuration

EVALUATION AND CHARACTERIZATION CIRCUIT BOARD LAYOUTS

Figure 57 to Figure 61 show the evaluation board for the AD8363.

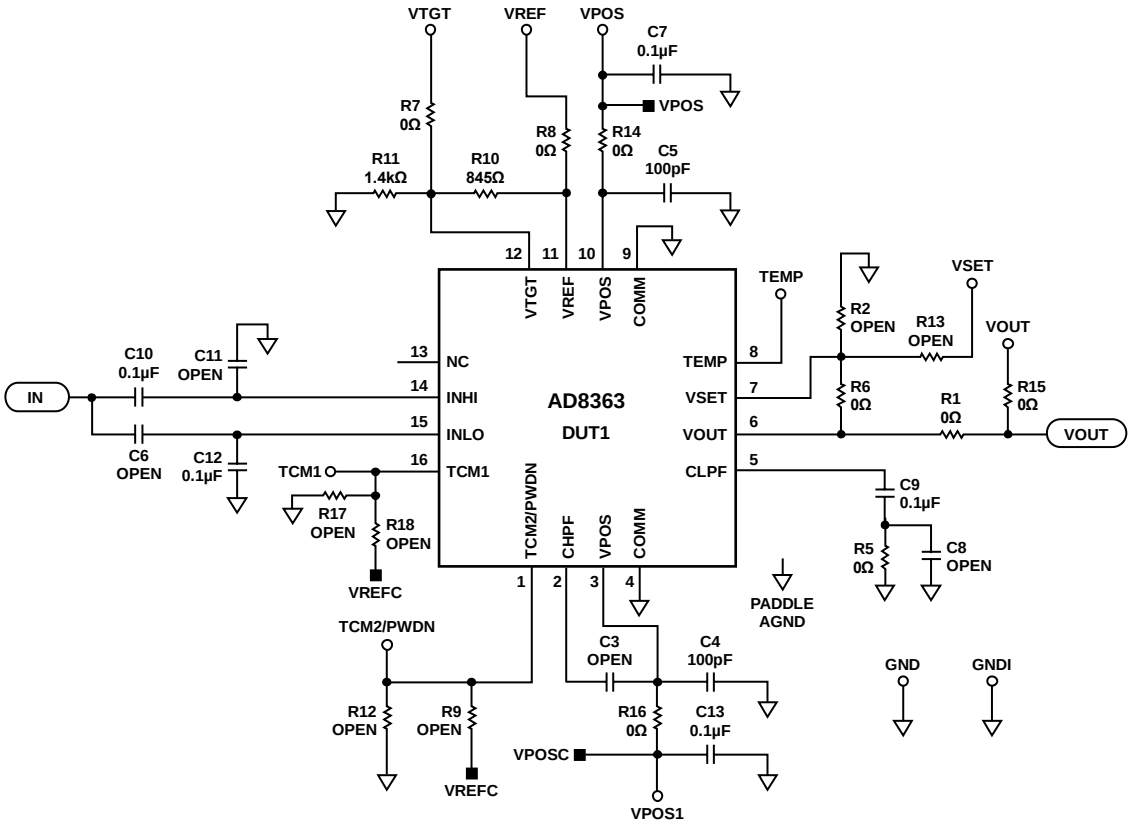

Figure 57. Evaluation Board Schematic

Table 6. Evaluation Board Configuration Options

Component	Function/Notes	Default Value
C6, C10, C11, C12	Input. The AD8363 is single-ended driven. At frequencies ≤2.6 GHz, the best dynamic range is achieved by driving Pin 14 (INHI). When driving INHI, populate C10 and C12 with an appropriate capacitor value for the frequency of operation and leave C6 and C11 open. For frequencies >2.6 GHz, additional dynamic range can be achieved by driving Pin 15 (INLO). When driving INLO, populate C6 and C11 with an appropriate capacitor value for the frequency of operation and leave C10 and C12 open.	C6 = open, C10 = 0.1 µF, C11 = open C12 = 0.1 µF
R7, R8, R10, R11	VTGT. R10 and R11 are set up to provide 1.4 V to VTGT from VREF. If R10 and R11 are removed, an external voltage can be used. Alternatively, R7 and R11 can be used to form a voltage divider for an external reference.	R7 = 0 Ω, R8 = 0 Ω, R10 = 845 Ω, R11 = 1.4 kΩ
C4, C5, C7, C13, R14, R16	Power Supply Decoupling. The nominal supply decoupling consists of a 100 pF filter capacitor placed physically close to the AD8363, a 0 Ω series resistor, and a 0.1 µF capacitor placed close to the power supply input pin. The 0 Ω resistor can be replaced with a larger resistor to add more filtering; however, it is at the expense of a voltage drop.	C4 = 100 pF, C5 = 100 pF, C7 = 0.1µF, C13 = 0.1µF, R14 = 0 Ω, R16 = 0 Ω
R1, R2, R6, R13, R15	Output Interface (Default Configuration) in Measurement Mode. In this mode, a portion of the output voltage is fed back to the VSET pin via R6. Using the voltage divider created by R2 and R6, the magnitude of the slope at VOUT is increased by reducing the portion of VOUT that is fed back to VSET. If a fast responding output is expected, the 0 Ω resistor (R15) can be removed to reduce parasitics on the output. Output Interface in Controller Mode. In this mode, R6 must be open and R13 must have a 0 Ω resistor. In controller mode, the AD8363 can control the gain of an external component. A setpoint voltage is applied to the VSET pin, the value of which corresponds to the desired RF input signal level applied to the AD8363. If a fast responding output is expected, the 0 Ω resistor (R15) can be removed to reduce parasitics on the output.	R1 = 0 Ω, R2 = open, R6 = 0 Ω, R13 = open, R15 = 0 Ω
C8, C9, R5	Low-Pass Filter Capacitors, C_{LPF}. The low-pass filter capacitors reduce the noise on the output and affect the pulse response time of the AD8363. This capacitor should be as large as possible. The smallest C_{LPF} capacitance should be 390 pF. R5, when set to a value other than 0 Ω, is used in conjunction with C8 and C9 to modify the loop transfer function and change the loop dynamics in controller mode.	C8 = open, C9 = 0.1 µF, R5 = 0 Ω
C3	C_{HPF} Capacitor. The C_{HPF} capacitor introduces a high-pass filter affect into the AD8363 transfer function and can also affect the response time. The C_{HPF} capacitor should be as small as possible and connect to VPOS when used. No capacitor is needed for input frequencies greater than 10 MHz.	C3 = open
R9, R12	TCM2/PWDN. The TCM2/PWDN pin controls the amount of nonlinear intercept temperature compensation and/or shuts down the device. The evaluation board is configured to control this from a test loop, but VREF can also be used by the voltage divider created by R9 and R12.	R9 = open, R12 = open
R17, R18	TCM1. TCM1 controls the temperature compensation (5 kΩ impedance). The evaluation board is configured to control this from a test loop, but VREF can also be used by the voltage divider created by R17 and R18. Due to the relatively low impedance of the TCM1 pin and the limited current of the VREF pin, care should be taken when choosing the R17 and R18 values.	R17 = open, R18 = open
Paddle	Connect the paddle to both a thermal and electrical ground.	

ASSEMBLY DRAWINGS

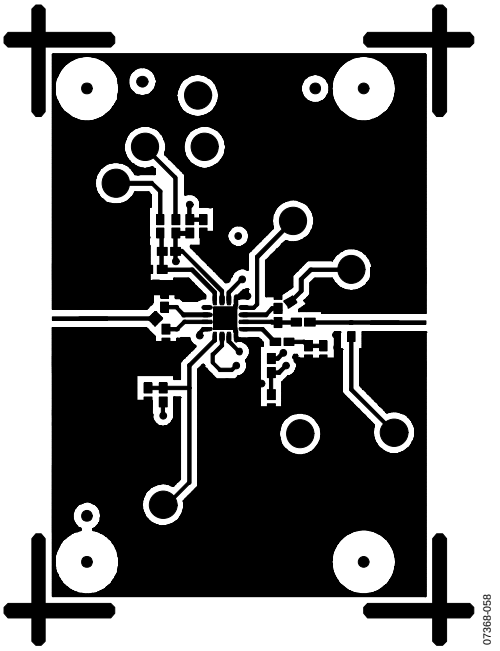

Figure 58. Evaluation Board Layout, Top Side

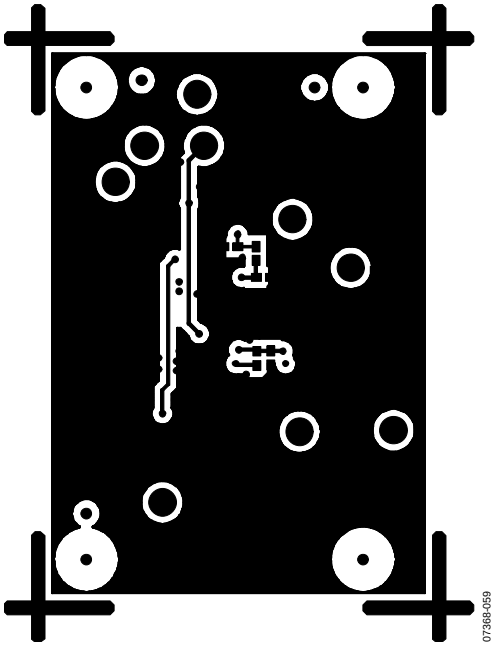

Figure 59. Evaluation Board Layout, Bottom Side

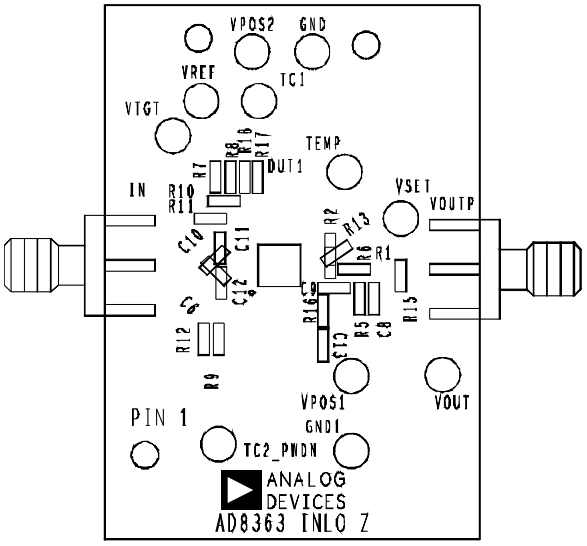

Figure 60. Evaluation Board Assembly, Top Side

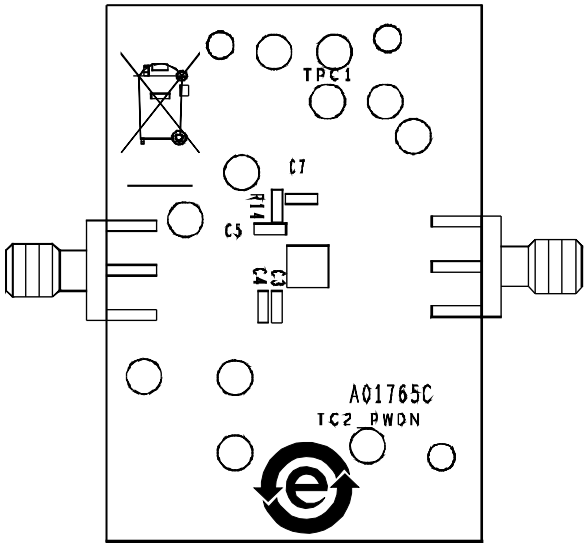

Figure 61. Evaluation Board Assembly, Bottom Side

OUTLINE DIMENSIONS

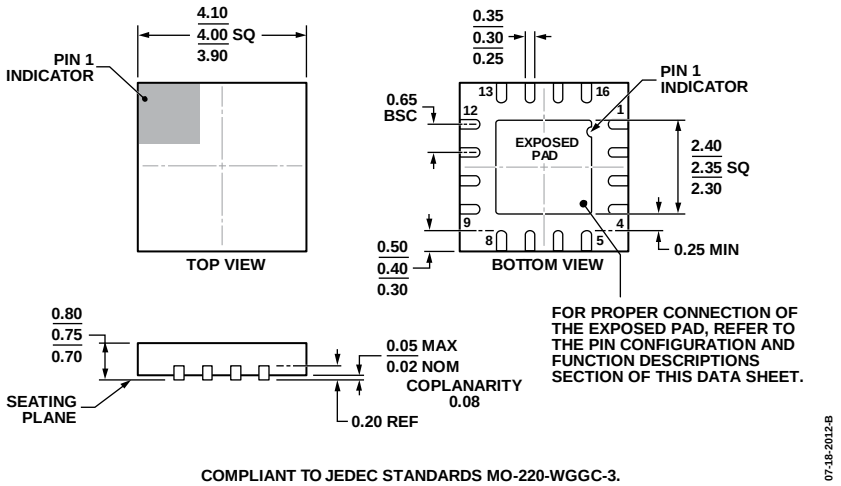

Figure 62. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-16-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
AD8363ACPZ-R2	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-20	250
AD8363ACPZ-R7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-20	1,500
AD8363ACPZ-WP	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-20	64
AD8363-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

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Analog Devices Inc.:

AD8363ACPZ-R7 AD8363-EVALZ