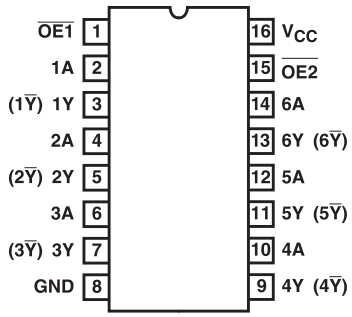
HIGH-SPEED CMOS LOGIC HEX BUFFER/LINE DRIVER, THREE-STATE NON-INVERTING AND INVERTING

Check for Samples: CD74HC365-Q1, CD74HC366-Q1, CD74HCT365-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Buffered Inputs**
- **High Current Bus Driver Outputs**
- **Typical Propagation Delay t_{PLH}, t_{PHL} = 8ns at V_{CC} = 5V, C_L = 15pF, T_A = 25°C**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . –40°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, Il ≤ 1μA at V_{OL}, V_{OH}**

D PACKAGE
(TOP VIEW)



DESCRIPTION

The CD74HC365-Q1, CD74HC366-Q1, and CD74HCT365-Q1 silicon gate CMOS three state buffers are general purpose high-speed non-inverting and inverting buffers. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. Both circuits are capable of driving up to 15 low power Schottky inputs.

The CD74HC365-Q1 and CD74HCT365-Q1 are non-inverting buffers, whereas the CD74HC366-Q1 is an inverting buffer. These devices have two three-state control inputs ($\overline{OE1}$ and $\overline{OE2}$) which are NORed together to control all six gates.

The 'HCT365-Q1 logic families are speed, function and pin compatible with the standard LS logic family.

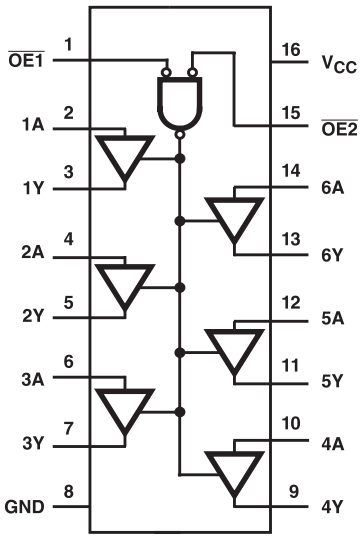
ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Reel of 2500	CD74HC366QDRQ1	HC366Q
			CD74HC365QDRQ1	Product Preview
			CD74HCT365QDRQ1	Product Preview

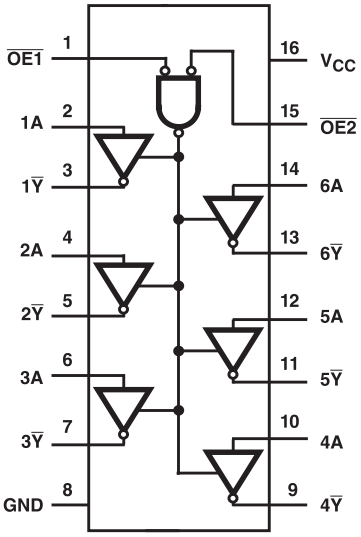
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTIONAL DIAGRAMS

CD74HC365-Q1, CD74HCT365-Q1



CD74HC366-Q1

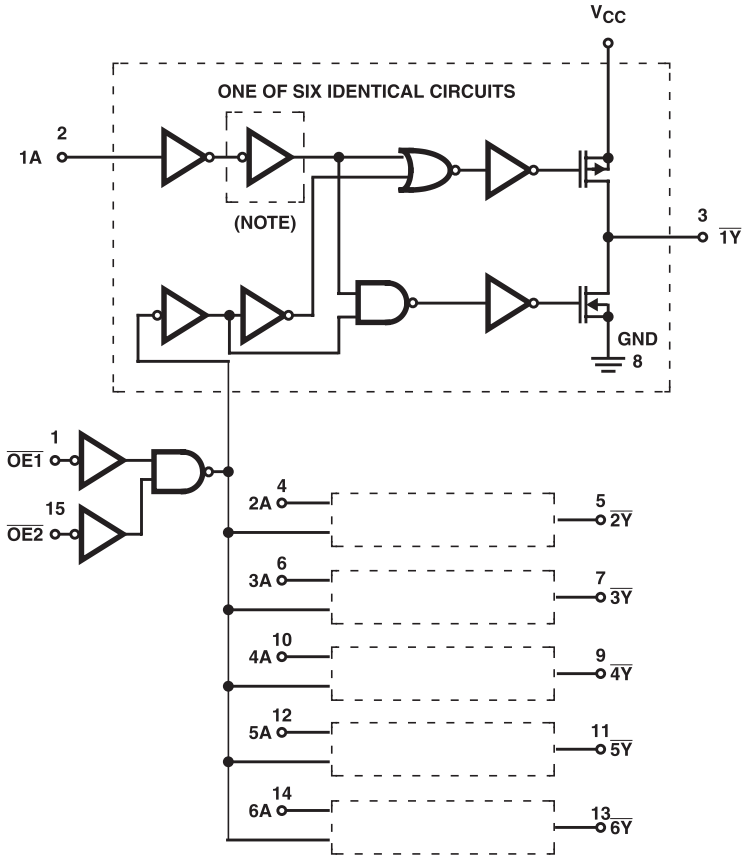


TRUTH TABLE(1)

INPUTS			OUTPUTS (Y)	
OE1	OE2	A	HC/HCT365	HC366
L	L	L	L	H
L	L	H	H	L
X	H	X	Z	Z
H	X	X	Z	Z

(1) H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance (OFF) State

LOGIC DIAGRAM



NOTE: Inverter not included in CD74HC365-Q1, CD74HCT365-Q1

Figure 1. LOGIC DIAGRAM FOR THE HC/HCT365 AND HC366 (outputs for HC/HCT365 are complements of those shown, i.e., 1Y, 2Y, etc.)

ABSOLUTE MAXIMUM RATINGS(1)

PARAMETER			CONDITIONS	VALUE
V_{CC}	DC supply voltage			-0.5V to +7V
I_{IK}	DC input diode current,		V_I < -0.5V or V_I > V_{CC} + 0.5V	±20mA
I_{OK}	DC output diode current		V_O < -0.5V or V_O > V_{CC} + 0.5V	±20mA
I_O	DC drain current per output		V_O > -0.5V or V_O < V_{CC} + 0.5V	±35mA
	DC output source or sink current per output pin			±25mA
I_{CC}	DC V_{CC} or ground current			±50mA
ESD	Electrostatic discharge	Human-Body Model		1.5kV
		Machine Model		200V
		Field_Induced_Charged Device Model		250V
	Latch up			Class I

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
θ_{JA}	Thermal resistance (typical)(1)	D (SOIC) package		73	°C/W
J_T	Maximum junction temperature			150	°C
T_{stg}	Maximum storage temperature range		–65	150	°C
	Maximum lead temperature (soldering 10s)	(SOIC - lead tips only)		300	°C

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CC}	Supply voltage	HC Types	2	6	V
		HCT Types	4.5	5.5	
V_I	DC Input voltage		0	V_{CC}	V
V_O	DC Output voltage		0	V_{CC}	V
T_A	Operating free-air temperature		–40	125	°C
	Input Rise and Fall Time	2 V		1000	ns
		4.5 V		500	
		6 V		400	

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 125°C		UNITS
			V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	
HC Types											
V_{IH}	High-level input voltage		-	-	2	1.5	-	-	1.5	-	V
					4.5	3.15	-	-	3.15	-	
					6	4.2	-	-	4.2	-	
V_{IL}	Low-level input voltage		-	-	2	-	-	0.5	-	0.5	V
					4.5	-	-	1.35	-	1.35	
					6	-	-	1.8	-	1.8	
V_{OH}	High-level output voltage loads	CMOS	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	V
					4.5	4.4	-	-	4.4	-	
					6	5.9	-	-	5.9	-	
		TTL		-6	4.5	3.98	-	-	3.7	-	
				-7.8	6	5.48	-	-	5.2	-	
V_{OL}	Low-level output voltage loads	CMOS	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	V
					4.5	-	-	0.1	-	0.1	
					6	-	-	0.1	-	0.1	
		TTL		6	4.5	-	-	0.26	-	0.4	
				7.8	6	-	-	0.26	-	0.4	
I_I	Input leakage current		V_{CC} or GND	-	6	-	-	±0.1	-	±1	µA
I_{CC}	Quiescent device current		V_{CC} or GND	0	6	-	-	8	-	160	µA
I_{OZ}	Three-state leakage current		V_{IH} or V_{IL}	V_O = V_{CC} or GND	6	-	-	±0.5	-	±10	µA
HCT Types											
V_{IH}	High-level input voltage		-	-	4.5 to 5.5	2	-	-	2	-	V
V_{IL}	Low-level input voltage		-	-	4.5 to 5.5	-	-	0.8	-	0.8	V
V_{OH}	High-level output voltage loads	CMOS	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	V
		TTL		-4	4.5	3.98	-	-	3.7	-	
V_{OL}	Low-level output voltage loads	CMOS	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	V
		TTL		4	4.5	-	-	0.26	-	0.4	
I_I	Input leakage current		V_{CC} or GND	-	5.5	-	-	±0.1	-	±1	µA
I_{CC}	Quiescent device current		V_{CC} or GND	0	5.5	-	-	8	-	160	µA
ΔI_{CC}	Additional quiescent device current per input pin: 1 unit load(1)		V_{CC} - 2.1	-	4.5 to 5.5	-	100	360	-	490	µA
I_{OZ}	Three-state leakage current		V_{IH} or V_{IL}	V_O = V_{CC} or GND	5.5	-	-	±0.5	-	±10	µA

(1) For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading

INPUT	UNIT LOADS
$\overline{OE1}$	0.6
All Others	0.55

SWITCHING CHARACTERISTICS

Input t_r, t_f = 6ns

PARAMETER			TEST CONDITIONS	V_{CC} (V)	25°C		-40°C TO 125°C	UNITS
					TYP	MAX	MAX	
HC Types								
t_{PLH}, t_{PHL}	Propagation delay, data to outputs	HC365	C_L = 50pF	2	-	110	165	ns
				4.5	-	22	33	
				6	-	19	28	
			C_L = 15pF	5	9	-	-	
		HC366	C_L = 50pF	2	-	150	225	
				4.5	-	31	45	
				6	-	26	38	
			C_L = 15pF	5	12	-	-	
t_{TLH}, t_{THL}	Output transition time		C_L = 50pF	2	-	60	90	ns
				4.5	-	12	18	
				6	-	10	15	
C_I	Input capacitance		-	-	-	10	10	pF
C_O	Three-state output capacitance		-	-	-	20	20	pF
C_{PD}	Power dissipation capacitance(1)(2)		-	5	40	-	-	pF
HCT Types								
t_{PLH}, t_{PHL}	Propagation delay, data to outputs	HCT365	C_L = 50pF	4.5	-	25	38	ns
			CL = 15pF	5	9	-	-	
		HCT366	C_L = 50pF	4.5	-	27	41	
			CL = 15pF	5	11	-	-	
t_{PLH}, t_{PHL}	Propagation delay, output enable and disable to outputs		C_L = 50pF	4.5	-	35	53	ns
			C_L = 15pF	5	14	-	-	
t_{TLH}, t_{THL}	Output transition time		C_L = 50pF	4.5	-	12	18	ns
C_I	Input capacitance		-	-	-	10	10	pF
C_O	Three-state output capacitance		-	-	-	20	20	pF
C_{PD}	Power dissipation capacitance(1)(2)		-	5	42	-	-	pF

(1) C_{PD} is used to determine the dynamic power consumption, per inverter.
(2) $P_D = V_{CC2} \times f_i (C_{PD} + C_L)$, where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage

TEST CIRCUIT AND WAVEFORMS

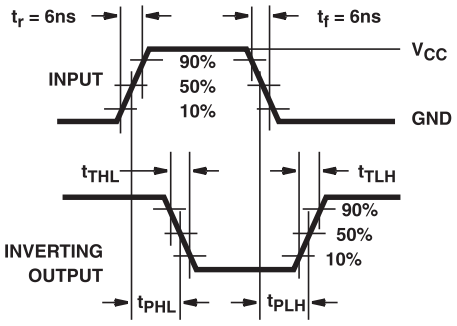


Figure 2. HC and HCU Transition Times and Propagation Delay Times, Combination Logic

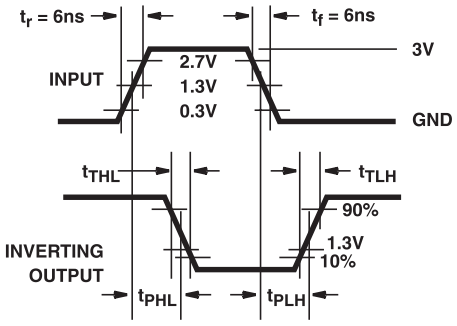


Figure 3. HCT Transition Times and Propagation Delay Times, Combination Logic

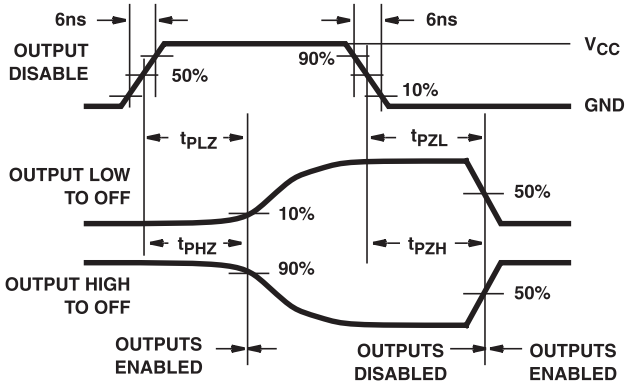


Figure 4. HC Three-State Propagation Delay Waveform

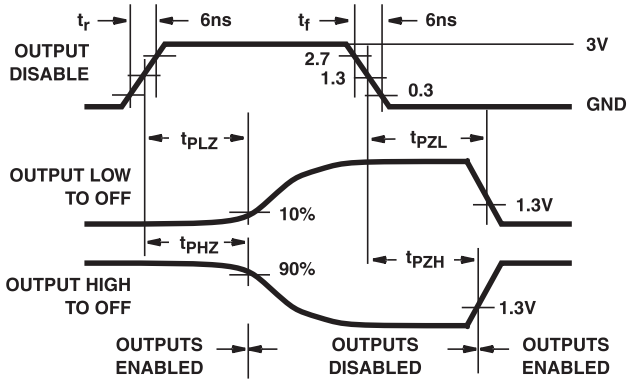
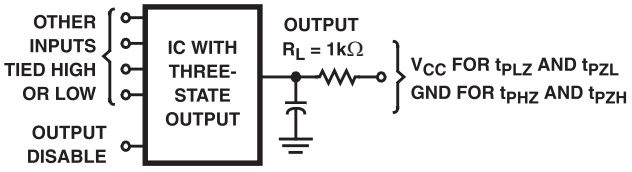


Figure 5. HCT Three-State Propagation Delay Waveform



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output R_L = 1kΩ to V_{CC}, C_L = 50pF.

Figure 6. HC and HCT Three-State Propagation Delay Test Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC366QDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC366Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

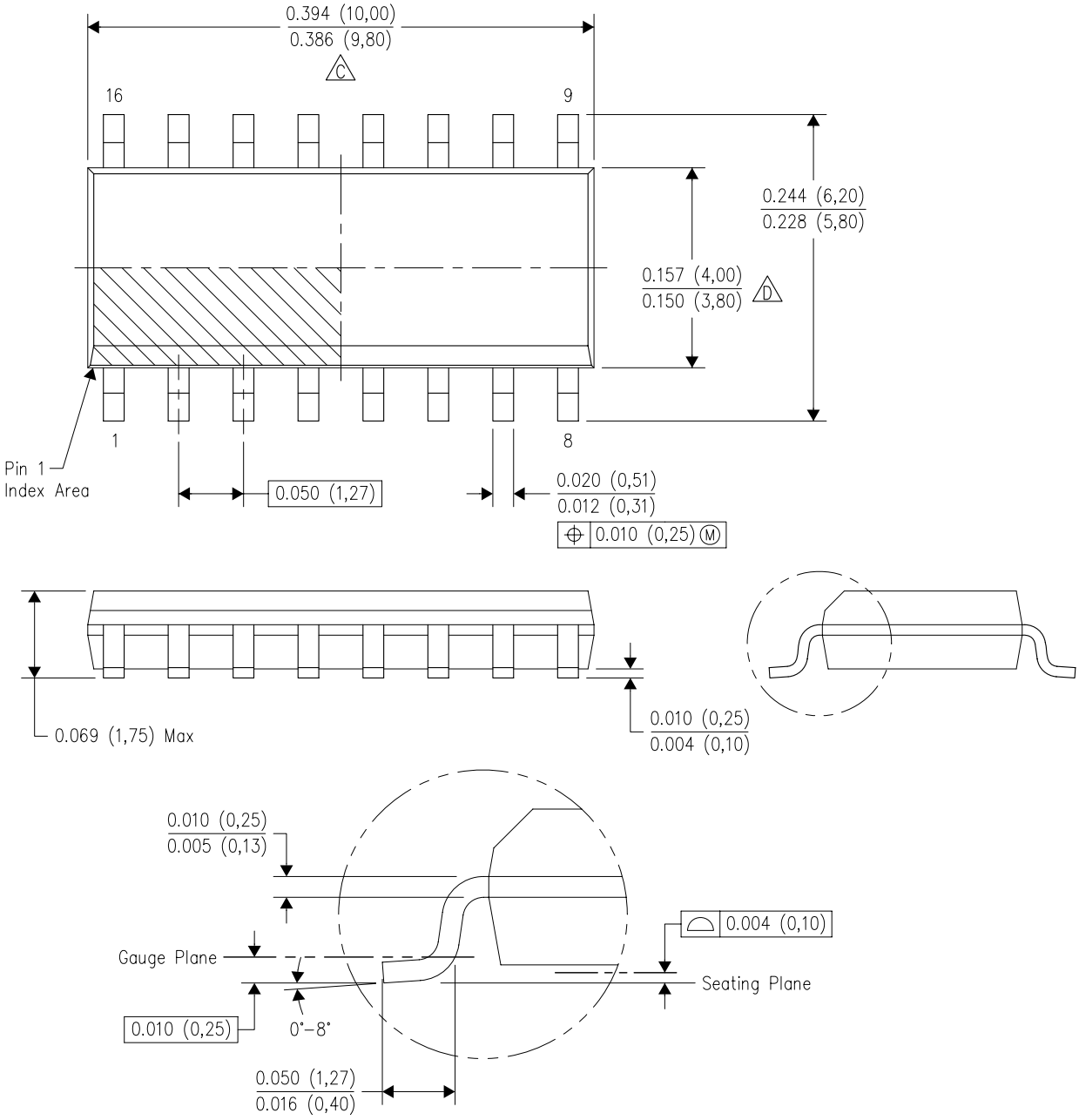
OTHER QUALIFIED VERSIONS OF CD74HC366-Q1 :

- Catalog: CD74HC366
- Military: CD54HC366

NOTE: Qualified Version Definitions:

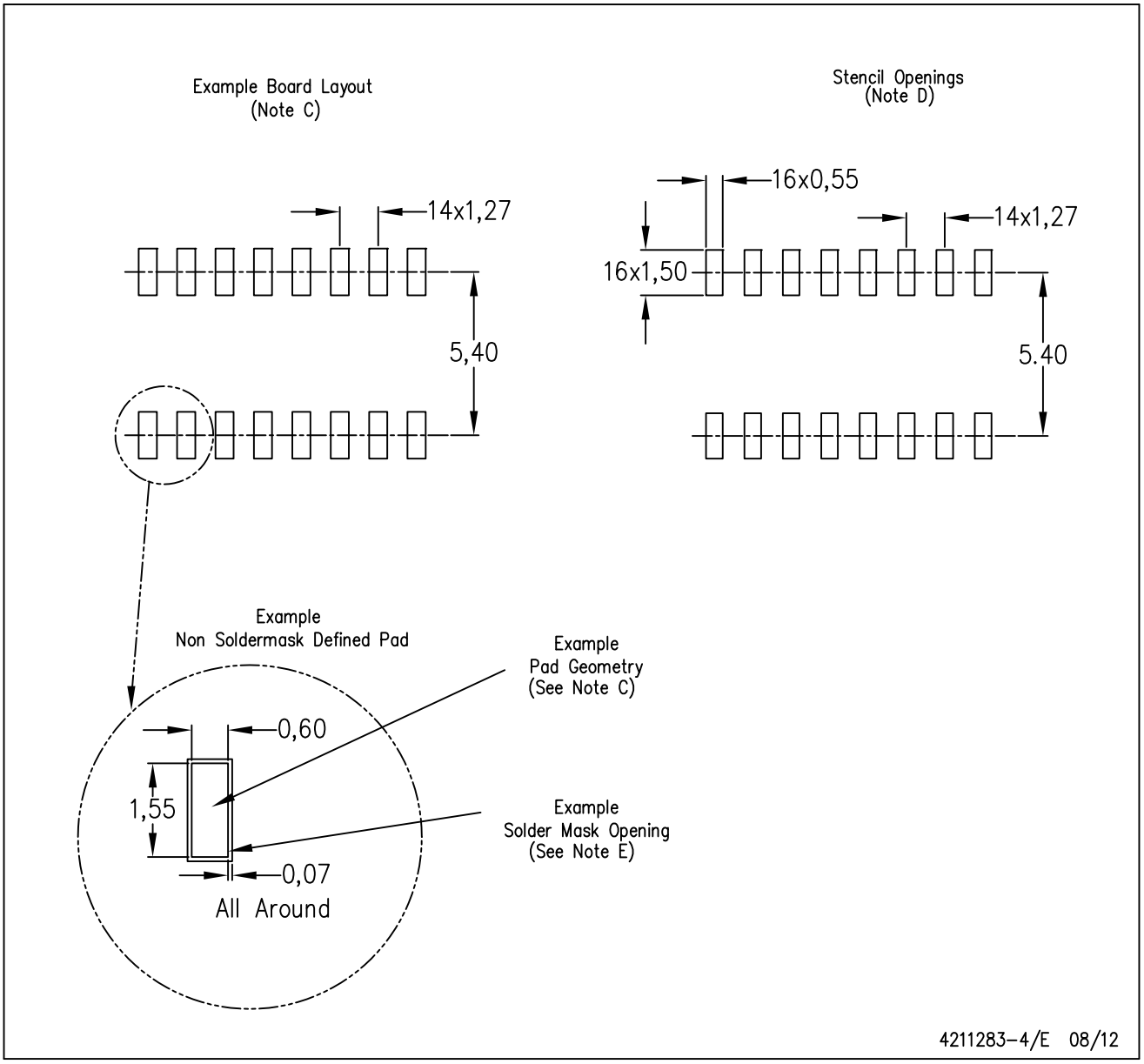
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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