Low Noise, 1 GHz *FastFET* Op Amps

Data Sheet

ADA4817-1/ADA4817-2

FEATURES

- High speed
  - −3 dB bandwidth (G = 1, R_L = 100 Ω): 1050 MHz
  - Slew rate: 870 V/µs
  - 0.1% settling time: 9 ns
- Input bias current: 2 pA typical
- Input capacitance
  - Common-mode capacitance: 1.3 pF typical
  - Differential mode capacitance: 0.1 pF typical
- Low input noise
  - Voltage noise: 4 nV/√Hz at 100 kHz
  - Current noise: 2.5 fA/√Hz at 100 kHz
- Low distortion: −90 dBc at 10 MHz (G = 1, R_L = 1 kΩ)
- orms a pole in the lo: 40 mA
- Supply quiescent current per amplifier: 19 mA typical
- Powered down supply quiescent current per amplifier:
  - 1.5 mA typical

APPLICATIONS

- Photodiode amplifiers
- Data acquisition front ends
- Instrumentation
- Filters
- ADC drivers
- Output buffers

CONNECTION DIAGRAMS

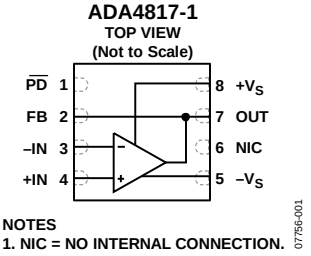

Figure 1. 8-Lead LFCSP (CP-8-13)

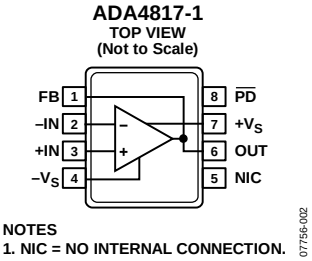

Figure 2. 8-Lead SOIC (RD-8-1)

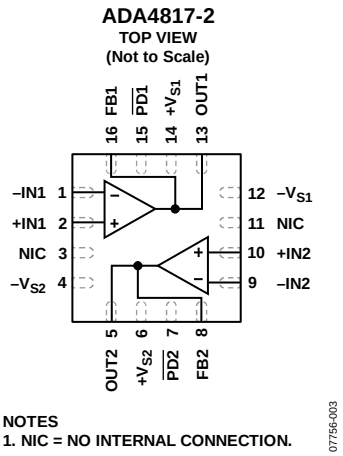

Figure 3. 16-Lead LFCSP (CP-16-20)

Rev. F

Document Feedback

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11/2008—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADA4817-1 (single) and ADA4817-2 (dual) *FastFET*™ amplifiers are unity-gain stable, ultrahigh speed, voltage feedback amplifiers with FET inputs. These amplifiers were developed with the Analog Devices, Inc., proprietary eXtra fast complementary bipolar (XFCB) process, which allows the amplifiers to achieve ultralow noise (4 nV/√Hz; 2.5 fA/√Hz) as well as very high input impedances.

With 1.3 pF of input capacitance, low noise (4 nV/√Hz), low offset voltage (2 mV maximum), and 1050 MHz −3 dB bandwidth, the ADA4817-1/ADA4817-2 are ideal for data acquisition front ends as well as wideband transimpedance applications, such as photodiode preamps.

With a wide supply voltage range from 5 V to 10 V and the ability to operate on either single or dual supplies, the ADA4817-1/ADA4817-2 are designed to work in a variety of applications including active filtering and analog-to-digital converter (ADC) driving. The ADA4817-1 is available in a 3 mm × 3 mm, 8-lead LFCSP and 8-lead SOIC, and the ADA4817-2 is available in a 4 mm × 4 mm, 16-lead LFCSP. These packages feature a low distortion pinout that improves second harmonic distortion and simplifies circuit board layout. They also feature an exposed pad that provides a low thermal resistance path to the printed circuit board (PCB). The EPAD enables more efficient heat transfer and increases reliability. These products are rated to work over the extended industrial temperature range (−40°C to +105°C).

SPECIFICATIONS

±5 V OPERATION

T_A = 25°C, $+V_S$ = 5 V, $-V_S$ = −5 V, G = 1, R_F = 348 Ω for G > 1, R_L = 100 Ω to ground, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.1 V p-p		1050		MHz
	V_{OUT} = 2 V p-p		200		MHz
	V_{OUT} = 0.1 V p-p, G = 2		390		MHz
Gain Bandwidth Product	V_{OUT} = 0.1 V p-p		≥410		MHz
Full Power Bandwidth	V_{IN} = 3.3 V p-p, G = 2		60		MHz
0.1 dB Flatness	V_{OUT} = 2 V p-p, R_L = 100 Ω, G = 2		60		MHz
Slew Rate	V_{OUT} = 4 V step		870		V/µs
Settling Time to 0.1%	V_{OUT} = 2 V step, G = 2		9		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion					
f = 1 MHz	V_{OUT} = 2 V p-p, R_L = 1 kΩ				
HD2			−113		dBc
HD3			−117		dBc
f = 10 MHz	V_{OUT} = 2 V p-p, R_L = 1 kΩ				
HD2			−90		dBc
HD3			−94		dBc
f = 50 MHz	V_{OUT} = 2 V p-p, R_L = 1 kΩ				
HD2			−64		dBc
HD3			−66		dBc
Input Voltage Noise	f = 100 kHz		4		nV/√Hz
Input Current Noise	f = 100 kHz		2.5		fA/√Hz
DC PERFORMANCE					
Input Offset Voltage			0.4	2	mV
	T_{MIN} to T_{MAX}, SOIC			6	mV
	T_{MIN} to T_{MAX}, LFCSP			4	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}, SOIC		25	80	µV/°C
	T_{MIN} to T_{MAX}, LFCSP		10	50	µV/°C
Input Bias Current			2	20	pA
	T_{MIN} to T_{MAX}		75	135	pA
Input Bias Offset Current			1	10	pA
	T_{MIN} to T_{MAX}			110	pA
Open-Loop Gain		62	65		dB
INPUT CHARACTERISTICS					
Input Resistance	Common mode		500		GΩ
Input Capacitance	Common mode		1.3		pF
	Differential mode		0.1		pF
Input Common-Mode Voltage Range			$-V_S$ to $(+V_S - 2.8)$		V
Common-Mode Rejection	V_{CM} = ±0.5 V	−77	−90		dB
	V_{CM} = ±0.5 V, T_{MIN} to T_{MAX}	−73			dB
	V_{CM} = −4.2 V to 2.2 V, T_{MIN} to T_{MAX}	−65			dB
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time	V_{IN} = ±2.5 V, G = 2		8		ns
Output Voltage Swing					
High	R_L = 100 Ω	$+V_S - 1.5$	$+V_S - 1.3$		V
	R_L = 100 Ω, T_{MIN} to T_{MAX}	$+V_S - 1.65$			V
	R_L = 1 kΩ	$+V_S - 1.1$	$+V_S - 1$		V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	R_L = 1 kΩ, T_{MIN} to T_{MAX}	$+V_S$ − 1.4			V
Low	R_L = 100 Ω		$-V_S$ + 1.4	$-V_S$ + 1.5	V
	R_L = 100 Ω, T_{MIN} to T_{MAX}			$-V_S$ + 1.65	V
	R_L = 1 kΩ		$-V_S$ + 1	$-V_S$ + 1.1	V
	R_L = 1 kΩ, T_{MIN} to T_{MAX}			$-V_S$ + 1.2	V
Linear Output Current	1% output error		40		mA
Short-Circuit Current	Sinking		100		mA
	Sourcing		170		mA
POWER-DOWN					
$\overline{PD}$ Pin Voltage	Enabled, T_{MIN} to T_{MAX}	>$+V_S$ − 0.9			V
	Powered down, T_{MIN} to T_{MAX}			<$+V_S$ − 3.5	V
Turn On Time			0.3		µs
Turn Off Time			1		µs
Input Leakage Current	$\overline{PD}$ = $+V_S$		0.3	3	µA
	$\overline{PD}$ = $-V_S$		34	61	µA
POWER SUPPLY					
Operating Range		5		10	V
Quiescent Current per Amplifier			19	21	mA
Powered Down Quiescent Current			1.5	3	mA
Positive Power Supply Rejection	$+V_S$ = 4.5 V to 5.5 V, $-V_S$ = −5 V	−67	−72		dB
Negative Power Supply Rejection	$+V_S$ = 5 V, $-V_S$ = −4.5 V to −5.5 V	−67	−72		dB

5 V OPERATION

T_A = 25°C, $+V_S$ = 3 V, $-V_S$ = −2 V, G = 1, R_F = 348 Ω for G > 1, R_L = 100 Ω to ground, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.1 V p-p		500		MHz
	V_{OUT} = 1 V p-p		160		MHz
	V_{OUT} = 0.1 V p-p, G = 2		280		MHz
Full Power Bandwidth	V_{IN} = 1 V p-p, G = 2		95		MHz
0.1 dB Flatness	V_{OUT} = 1 V p-p, G = 2		32		MHz
Slew Rate	V_{OUT} = 2 V step		320		V/µs
Settling Time to 0.1%	V_{OUT} = 1 V step, G = 2		11		Ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion					
f = 1 MHz	V_{OUT} = 1 V p-p, R_L = 1 kΩ				dBc
HD2			−87		dBc
HD3			−88		
f = 10 MHz	V_{OUT} = 1 V p-p, R_L = 1 kΩ				
HD2			−68		dBc
HD3			−66		dBc
f = 50 MHz	V_{OUT} = 1 V p-p, R_L = 1 kΩ				
HD2			−57		dBc
HD3			−55		dBc
Input Voltage Noise	f = 100 kHz		4		nV/√Hz
Input Current Noise	f = 100 kHz		2.5		fA/√Hz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DC PERFORMANCE					
Input Offset Voltage			0.5	2.3	mV
	T_{MIN} to T_{MAX}, SOIC			6.5	mV
	T_{MIN} to T_{MAX}, LFCSP			5	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}, SOIC		25	75	µV/°C
	T_{MIN} to T_{MAX}, LFCSP		10	45	µV/°C
Input Bias Current			2	20	pA
	T_{MIN} to T_{MAX}		50	70	pA
Input Bias Offset Current			1	10	pA
	T_{MIN} to T_{MAX}			65	pA
Open-Loop Gain		61	63		dB
INPUT CHARACTERISTICS					
Input Resistance	Common mode		500		GΩ
Input Capacitance	Common mode		1.3		pF
	Differential mode		0.1		pF
Input Common-Mode Voltage Range			$-V_S$ to $(+V_S - 2.9)$		V
Common-Mode Rejection	V_{CM} = ±0.25 V	−72	−83		dB
	V_{CM} = ±0.3 V, T_{MIN} to T_{MAX}	−70			dB
	V_{CM} = ±0.8 V, T_{MIN} to T_{MAX}	−59			dB
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time	V_{IN} = ±1.25 V, G = 2		13		ns
Output Voltage Swing					
High	R_L = 100 Ω	$+V_S - 1.3$	$+V_S - 1.2$		V
	R_L = 100 Ω, T_{MIN} to T_{MAX}	$+V_S - 1.4$			V
	R_L = 1 kΩ	$+V_S - 1.1$	$+V_S - 1$		V
	R_L = 1 kΩ, T_{MIN} to T_{MAX}	$+V_S - 1.2$			V
Low	R_L = 100 Ω		$-V_S + 1$	$-V_S + 1.1$	V
	R_L = 100 Ω, T_{MIN} to T_{MAX}			$-V_S + 1.2$	V
	R_L = 1 kΩ		$-V_S + 0.9$	$-V_S + 1$	V
	R_L = 1 kΩ, T_{MIN} to T_{MAX}			$-V_S + 1.1$	V
Linear Output Current	1% output error		20		mA
Short-Circuit Current	Sinking		40		mA
	sourcing		130		mA
POWER-DOWN					
$\overline{PD}$ Pin Voltage	Enabled, T_{MIN} to T_{MAX}	$>+V_S - 0.9$			V
	Powered down, T_{MIN} to T_{MAX}			$<+V_S - 3.5$	V
Turn On Time			0.2		µs
Turn Off Time			0.7		µs
Input Leakage Current	$\overline{PD} = +V_S$		0.2	3	µA
	$\overline{PD} = -V_S$		31	53	µA
POWER SUPPLY					
Operating Range		5		10	V
Quiescent Current per Amplifier			14	16	mA
Powered Down Quiescent Current			1.5	2.8	mA
Positive Power Supply Rejection	$+V_S$ = 4.75 V to 5.25 V, $-V_S$ = 0 V	−66	−71		dB
Negative Power Supply Rejection	$+V_S$ = 5 V, $-V_S$ = −0.25 V to +0.25 V	−63	−69		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	10.6 V
Power Dissipation	See Figure 4
Common-Mode Input Voltage Range	$-V_S - 0.5$ V to $+V_S + 0.5$ V
Differential Input Voltage	$\pm V_S$
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +105°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
CP-8-13	94	29	°C/W
RD-8-1	79	29	°C/W
CP-16-20	64	14	°C/W

MAXIMUM SAFE POWER DISSIPATION

The maximum safe power dissipation for the ADA4817-1/ADA4817-2 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C (which is the glass transition temperature), the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4817-1/ADA4817-2. Exceeding a junction temperature of 150°C for an extended period can result in changes in silicon devices, potentially causing degradation or loss of functionality.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the die due to the ADA4817-1/ADA4817-2 drive at the output. The quiescent power is the voltage between the supply pins (V_S) multiplied by the quiescent current (I_S).

PD = Quiescent Power + (Total Drive Power − Load Power) (1)

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L} \quad (2)$$

Consider root mean square (rms) output voltages. If R_L is referenced to $-V_S$, as in single-supply operation, the total drive power is $V_S \times I_{OUT}$. If the rms signal levels are indeterminate, consider the worst-case scenario, when $V_{OUT} = V_S/4$ for R_L to midsupply.

$$P_D = (V_S \times I_S) + \frac{(V_S/4)^2}{R_L} \quad (3)$$

In single-supply operation with R_L referenced to $-V_S$, the worst-case situation is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. More metal directly in contact with the package leads and exposed pad from metal traces, through holes, ground, and power planes also reduces θ_{JA}.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature for the exposed paddle 8-lead LFCSP (single 94°C/W), 8-lead SOIC (single 79°C/W), and 16-lead LFCSP (dual 64°C/W) packages on JEDEC standard 4-layer boards. θ_{JA} values are approximations.

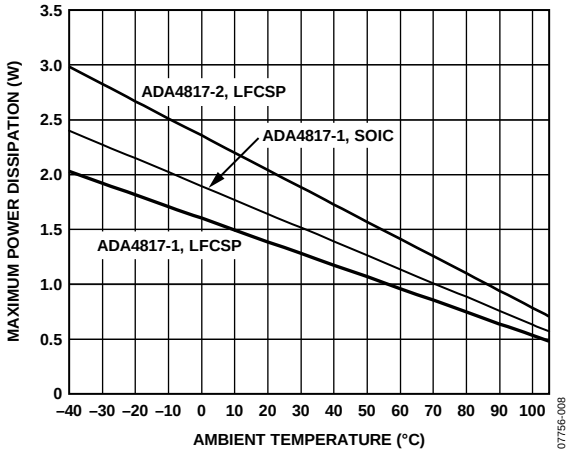

Figure 4. Maximum Safe Power Dissipation vs. Ambient Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

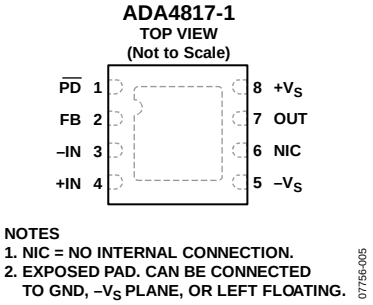

Figure 5. ADA4817-1 Pin Configuration (8-Lead LFCSP)

Table 5. ADA4817-1 Pin Function Descriptions (8-Lead LFCSP)

Pin No.	Mnemonic	Description
1	$\overline{PD}$	Power-Down. Do not leave floating.
2	FB	Feedback Pin.
3	−IN	Inverting Input.
4	+IN	Noninverting Input.
5	$-V_S$	Negative Supply.
6	NIC	No Internal Connection.
7	OUT	Output.
8	$+V_S$	Positive Supply.
	EPAD	Exposed Pad. Can be connected to GND, $-V_S$ plane, or left floating.

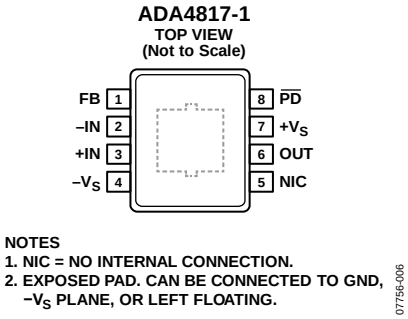

Figure 6. ADA4817-1 Pin Configuration (8-Lead SOIC)

Table 6. ADA4817-1 Pin Function Descriptions (8-Lead SOIC)

Pin No.	Mnemonic	Description
1	FB	Feedback Pin.
2	−IN	Inverting Input.
3	+IN	Noninverting Input.
4	$-V_S$	Negative Supply.
5	NIC	No Internal Connection.
6	OUT	Output.
7	$+V_S$	Positive Supply.
8	$\overline{PD}$	Power-Down. Do not leave floating.
	EPAD	Exposed Pad. Can be connected to GND, $-V_S$ plane, or left floating.

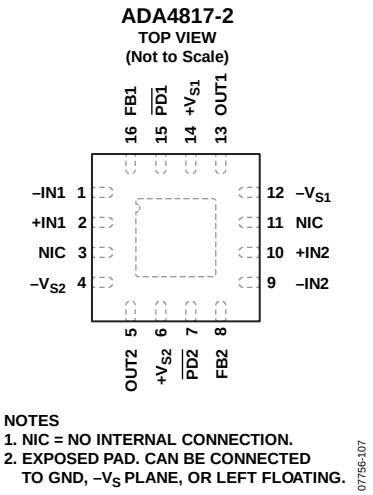

Figure 7. ADA4817-2 Pin Configuration (16-Lead LFCSP)

Table 7. ADA4817-2 Pin Function Descriptions (16-Lead LFCSP)

Pin No.	Mnemonic	Description
1	–IN1	Inverting Input 1.
2	+IN1	Noninverting Input 1.
3, 11	NIC	No Internal Connection.
4	$-V_{S2}$	Negative Supply 2.
5	OUT2	Output 2.
6	$+V_{S2}$	Positive Supply 2.
7	$\overline{PD2}$	Power-Down 2. Do not leave floating.
8	FB2	Feedback Pin 2.
9	–IN2	Inverting Input 2.
10	+IN2	Noninverting Input 2.
12	$-V_{S1}$	Negative Supply 1.
13	OUT1	Output 1.
14	$+V_{S1}$	Positive Supply 1.
15	$\overline{PD1}$	Power-Down 1. Do not leave floating.
16	FB1	Feedback Pin 1.
	EPAD	Exposed Pad. Can be connected to GND, $-V_S$ plane, or left floating.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±5 V, G = 1, (R_F = 348 Ω for G > 1), R_L = 100 Ω to ground, small signal V_{OUT} = 100 mV p-p, large signal V_{OUT} = 2 V p-p, unless otherwise noted.

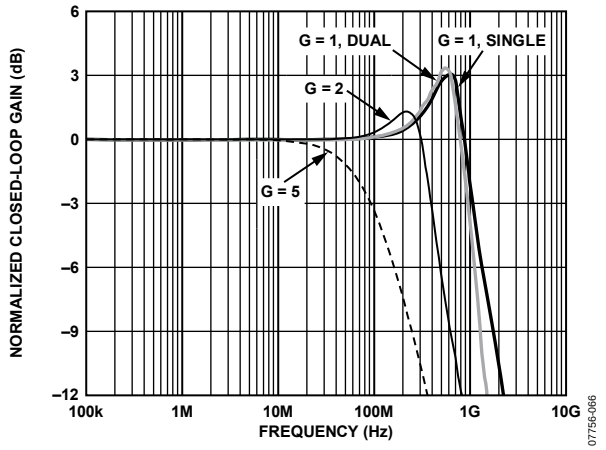

Figure 8. Small Signal Frequency Response for Various Gains (LFCSP)

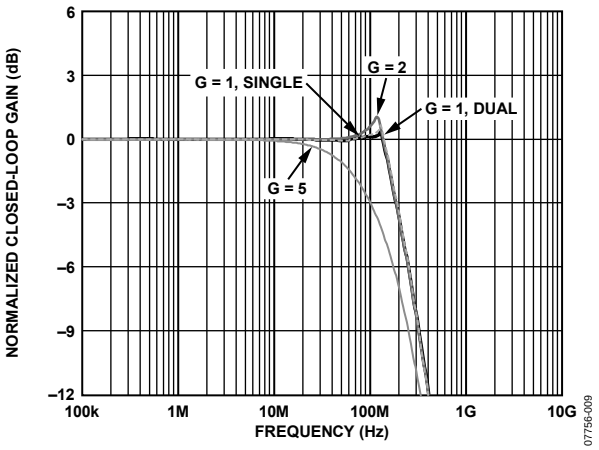

Figure 11. Large Signal Frequency Response for Various Gains

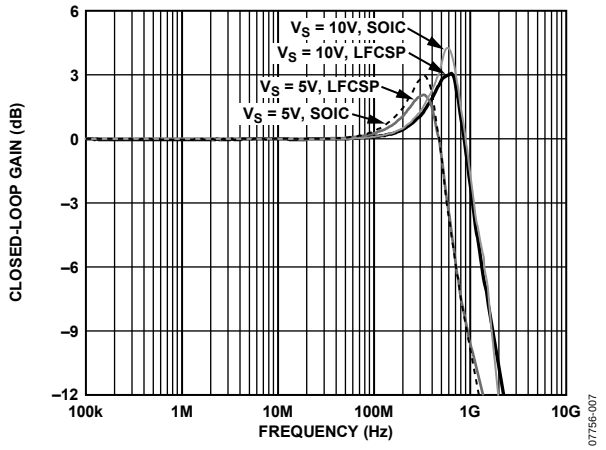

Figure 9. Small Signal Frequency Response for Various Supplies

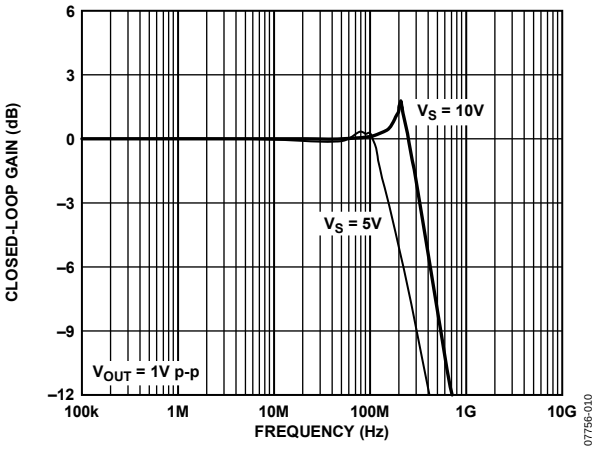

Figure 12. Large Signal Frequency Response for Various Supplies

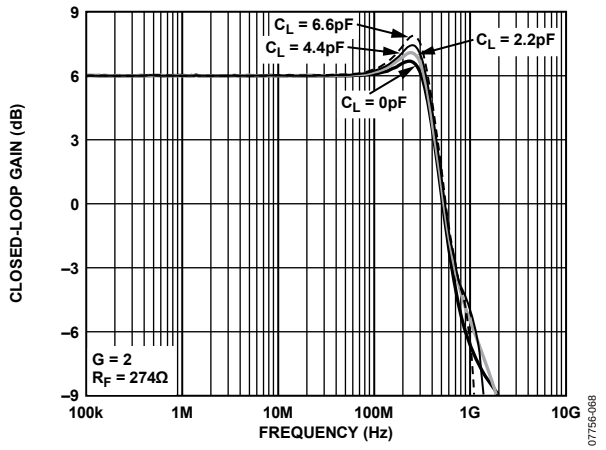

Figure 10. Small Signal Frequency Response for Various C_L

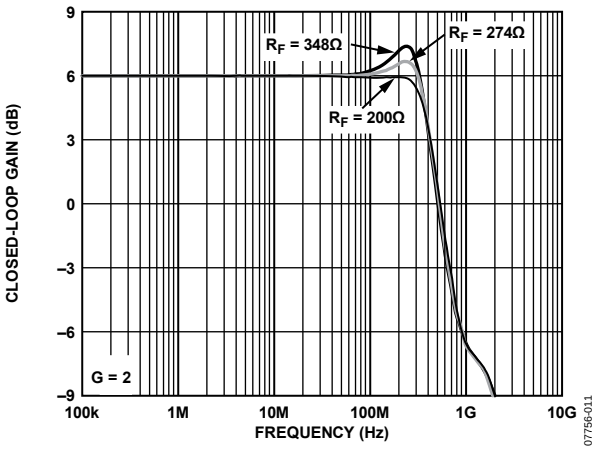

Figure 13. Small Signal Frequency Response for Various R_F

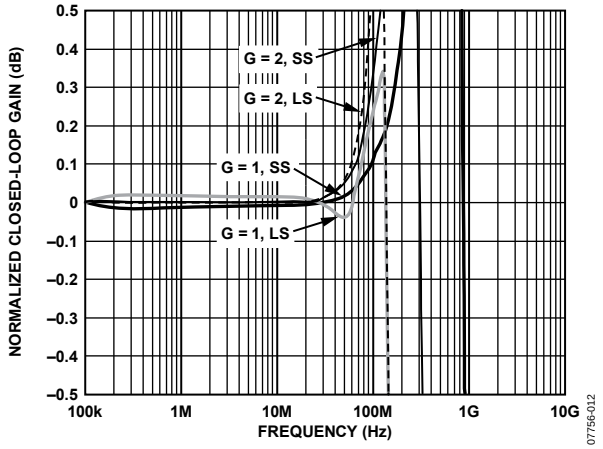

Figure 14. 0.1 dB Flatness Frequency Response vs. Gain and Output Voltage

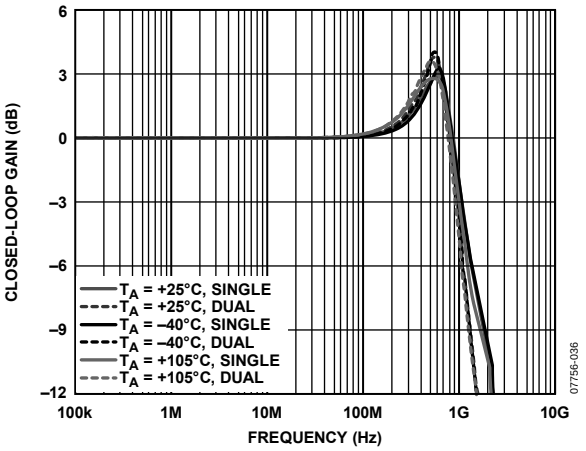

Figure 17. Small Signal Frequency Response vs. Temperature

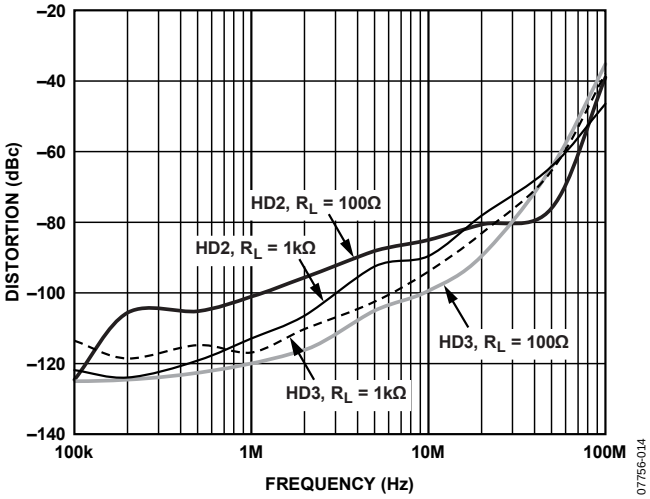

Figure 15. Distortion vs. Frequency for Various Loads, V_{OUT} = 2 V p-p

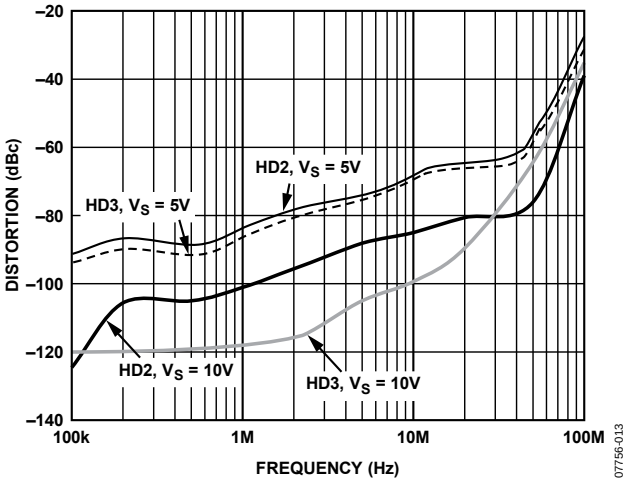

Figure 18. Distortion vs. Frequency for Various Supplies, V_{OUT} = 2 V p-p

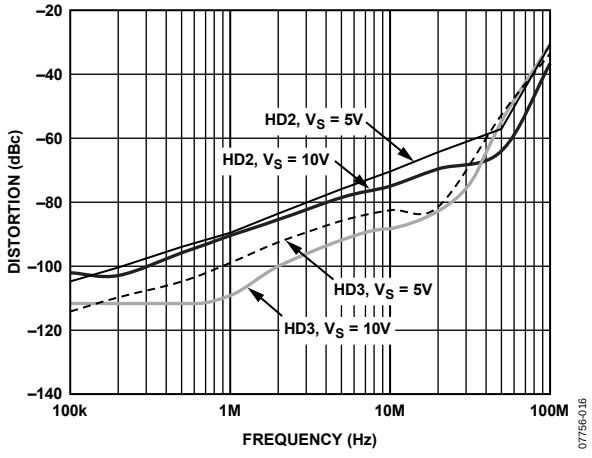

Figure 16. Distortion vs. Frequency for Various Supplies, G = 2, V_{OUT} = 2 V p-p

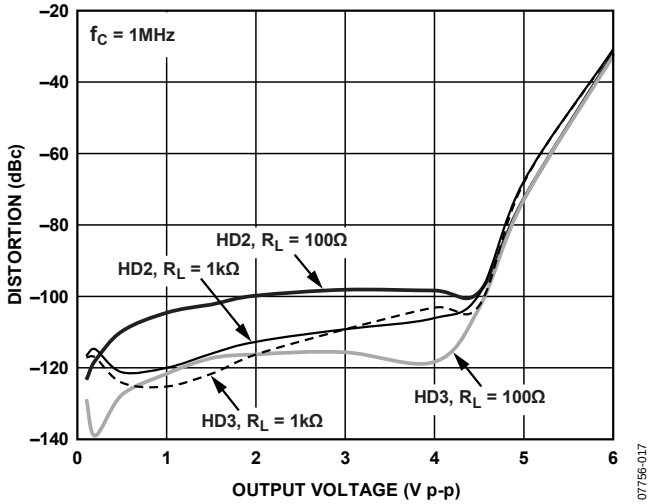

Figure 19. Distortion vs. Output Voltage for Various Loads

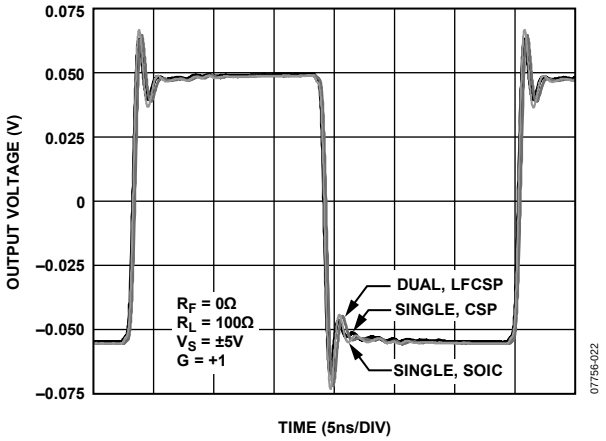

Figure 20. Small Signal Transient Response vs. Package

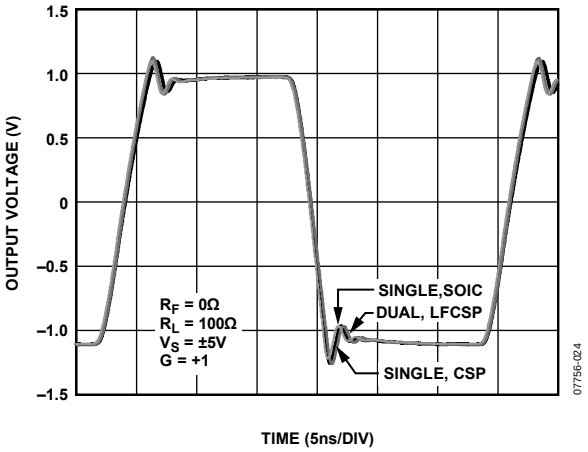

Figure 23. Large Signal Transient Response vs. Package

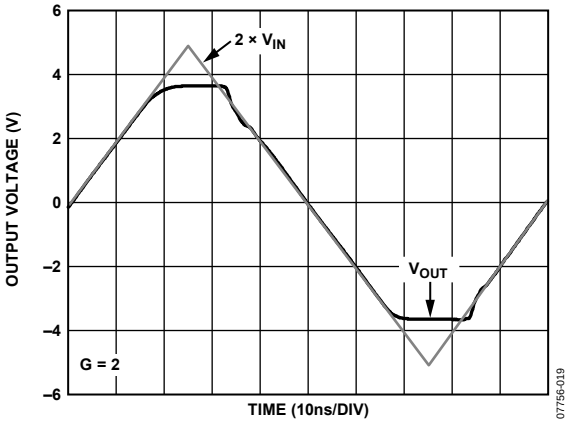

Figure 21. Output Overdrive Recovery

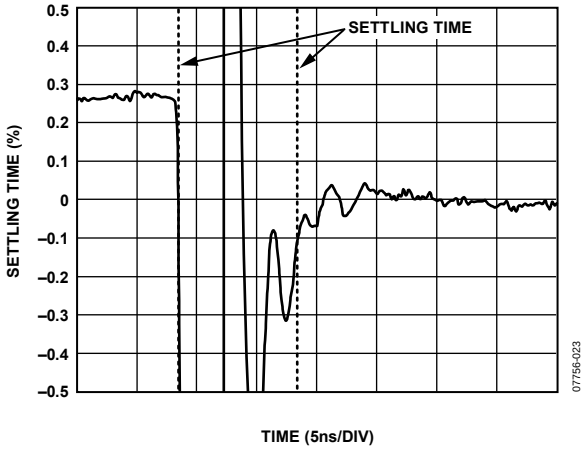

Figure 24. 0.1% Short-Term Settling Time

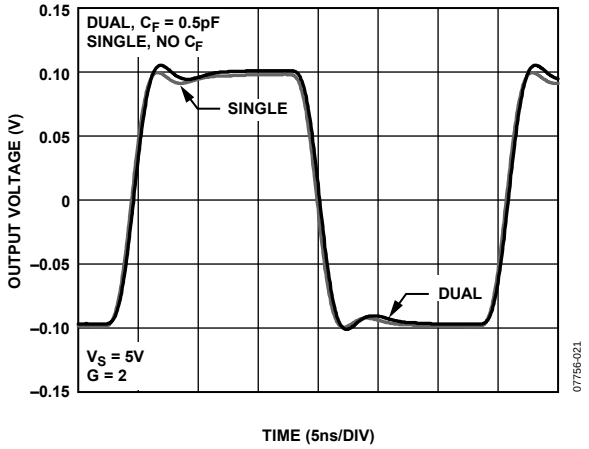

Figure 22. Small Signal Transient Response

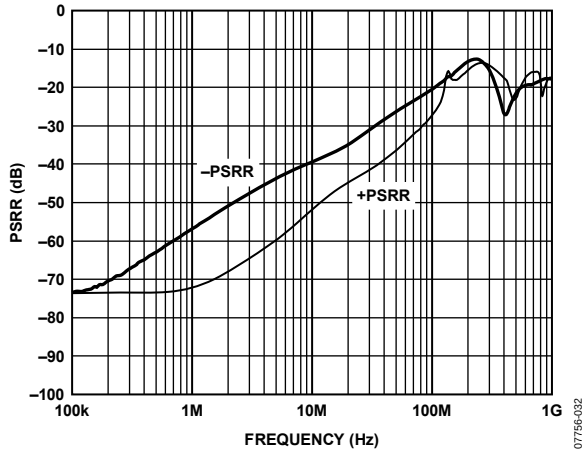

Figure 25. Power Supply Rejection Ratio (PSRR) vs. Frequency

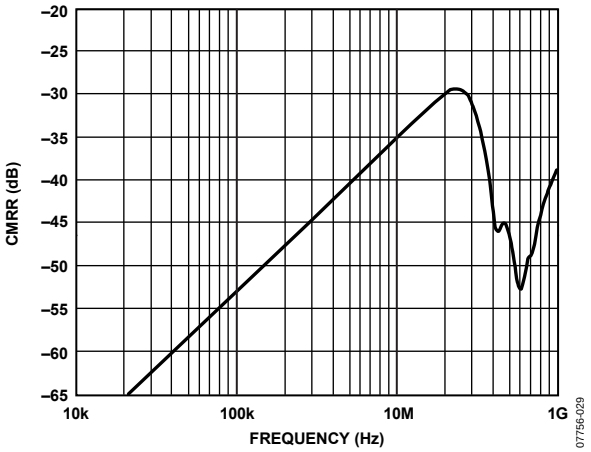

Figure 26. Common-Mode Rejection Ratio (CMRR) vs. Frequency

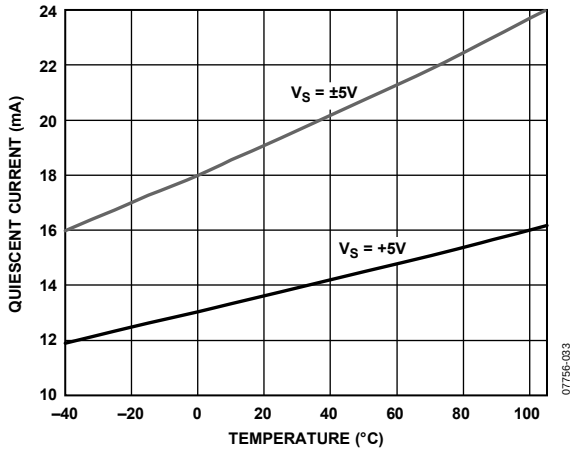

Figure 29. Quiescent Current vs. Temperature for Various Supply Voltages

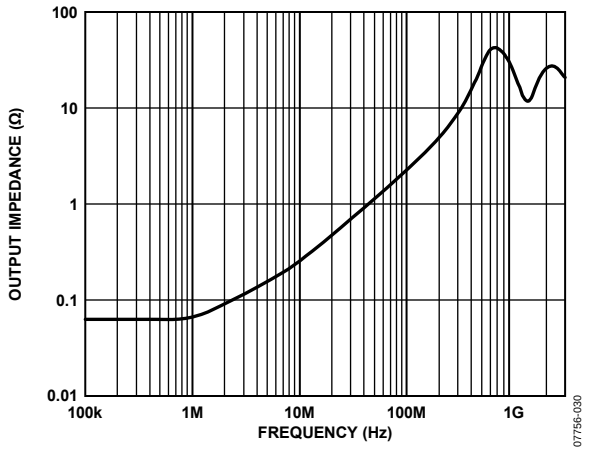

Figure 27. Output Impedance vs. Frequency

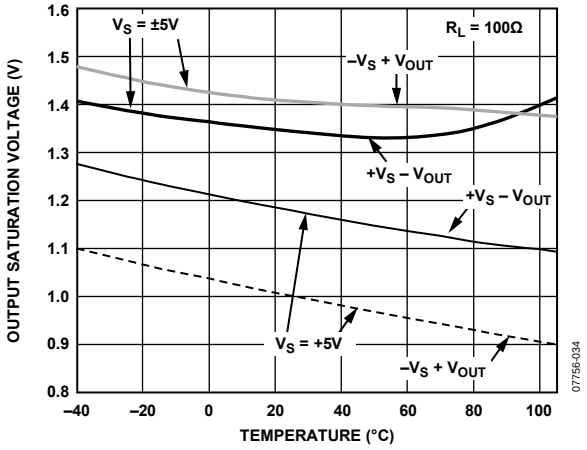

Figure 30. Output Saturation Voltage vs. Temperature

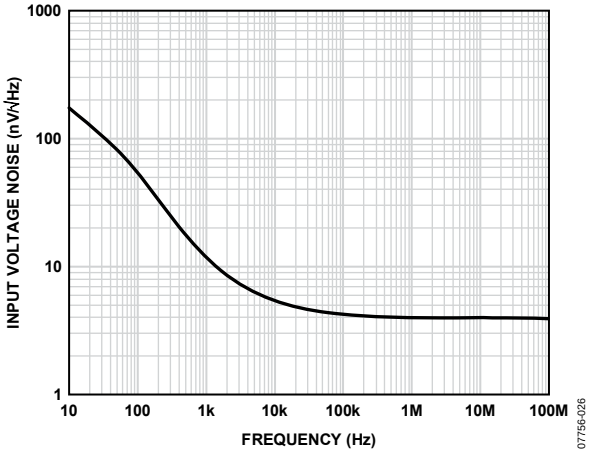

Figure 28. Input Voltage Noise vs. Frequency

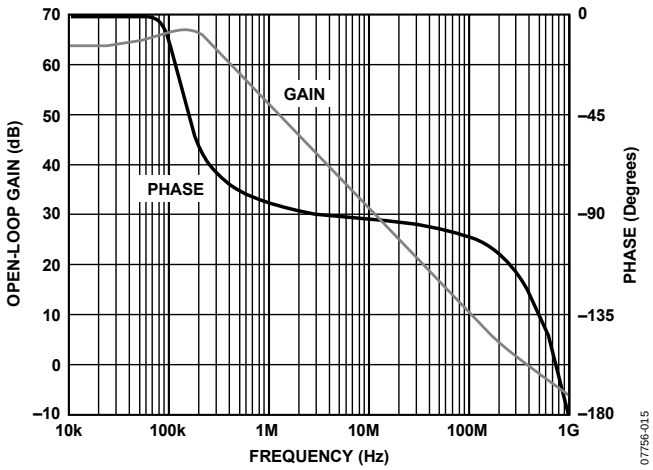

Figure 31. Open-Loop Gain and Phase vs. Frequency

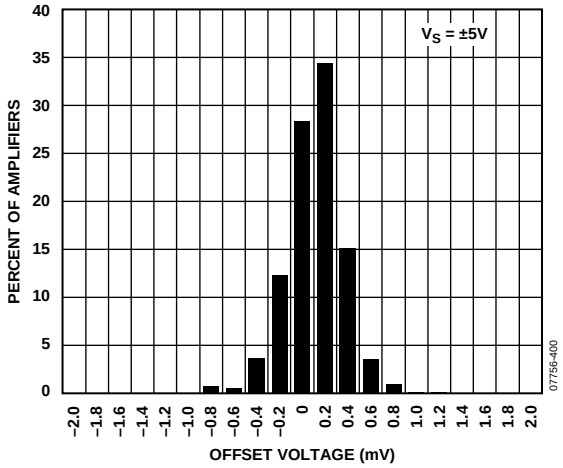

Figure 32. Input Offset Voltage Histogram (V_S = ±5 V), LFCSP Only

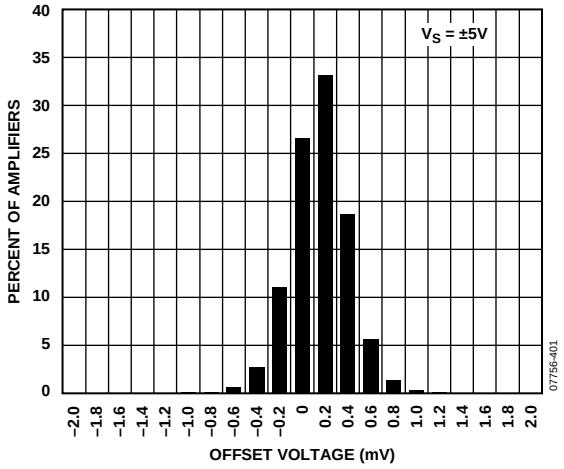

Figure 35. Input Offset Voltage Histogram (V_S = ±5 V), SOIC Only

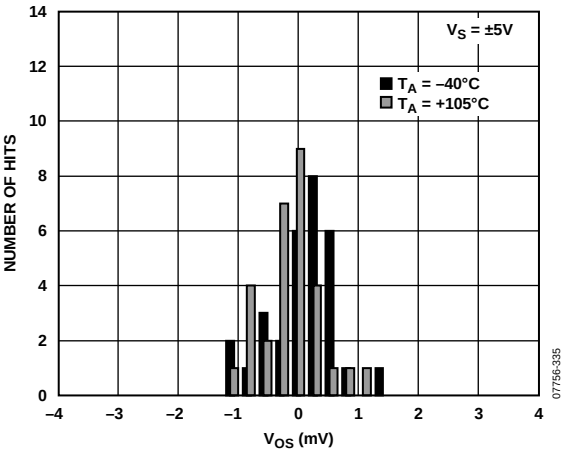

Figure 33. Input Offset Voltage Histogram over Temperature (V_S = ±5 V), LFCSP Only

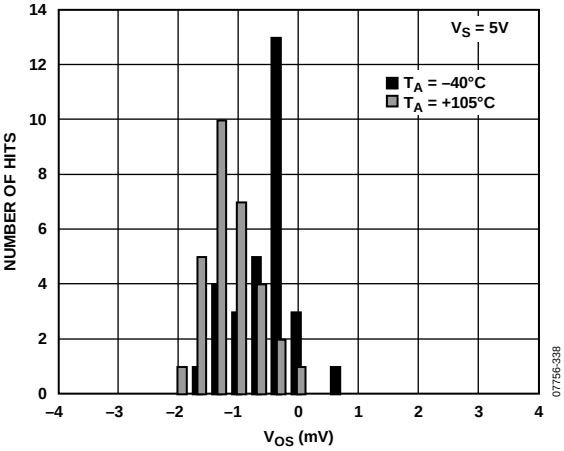

Figure 36. Input Offset Voltage Histogram over Temperature (V_S = 5 V), LFCSP Only

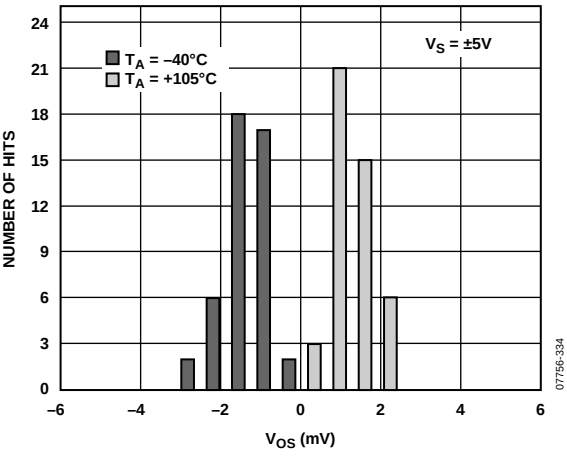

Figure 34. Input Offset Voltage Histogram over Temperature (V_S = ±5 V), SOIC Only

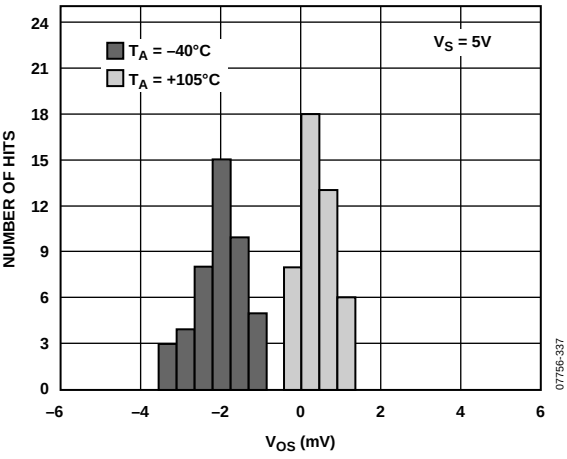

Figure 37. Input Offset Voltage Histogram over Temperature (V_S = 5 V), SOIC Only

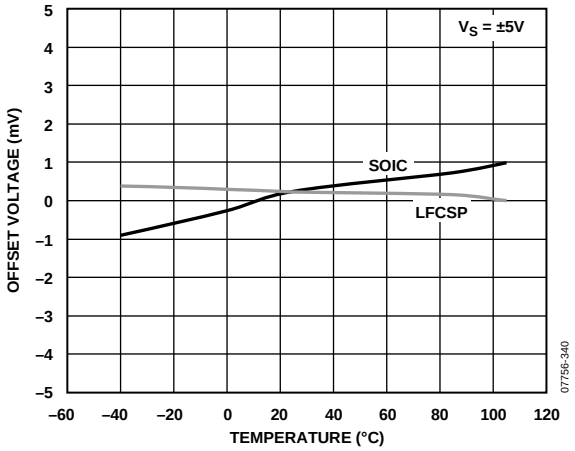

Figure 38. Offset Voltage vs. Temperature
(V_S = ±5 V)

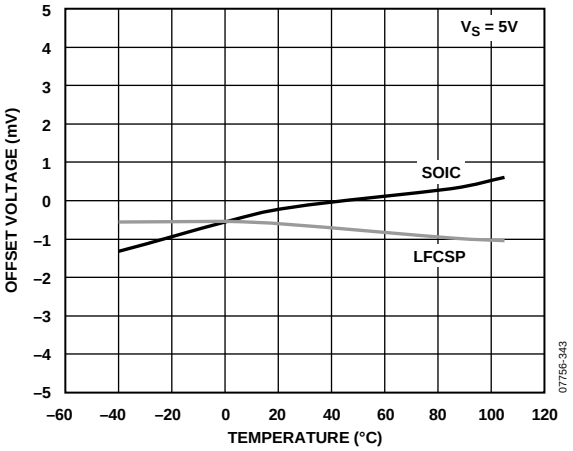

Figure 41. Offset Voltage vs. Temperature
(V_S = 5 V)

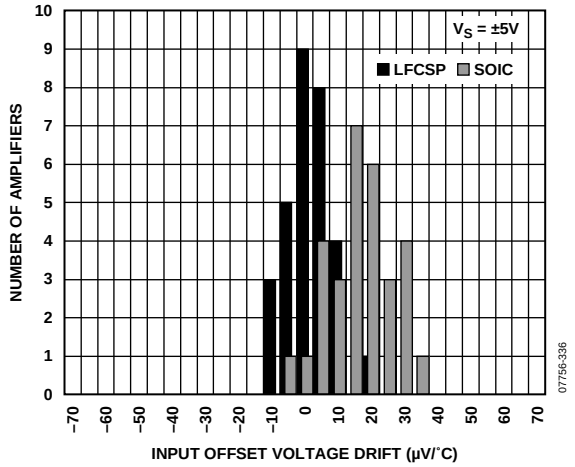

Figure 39. Input Offset Voltage Drift Histogram
(V_S = ±5V)

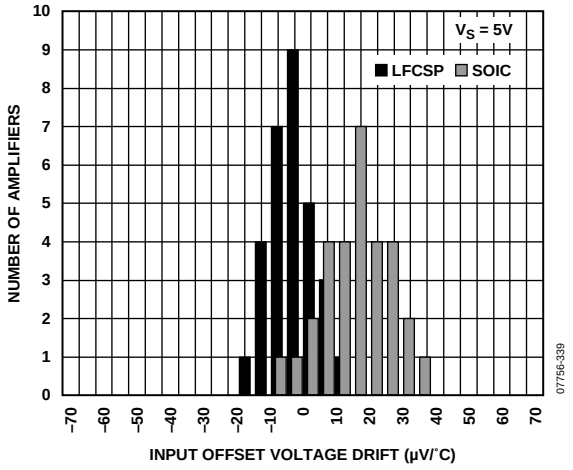

Figure 42. Input Offset Voltage Drift Histogram
(V_S = 5 V)

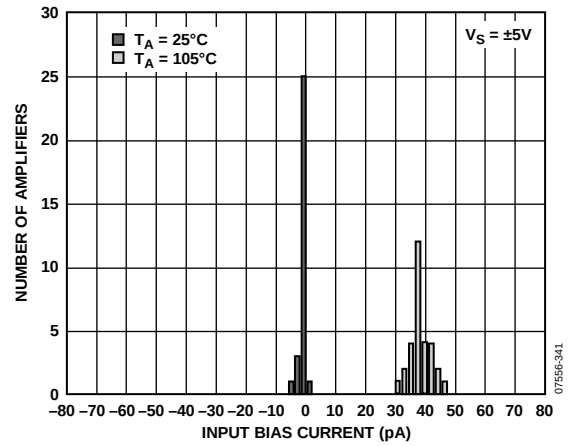

Figure 40. Input Bias Current Histogram over Temperature
(V_S = ±5 V)

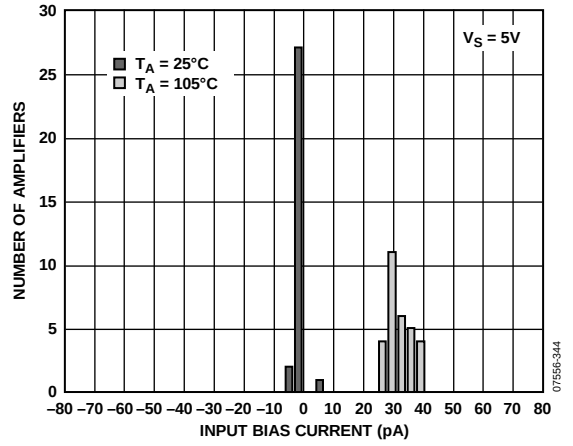

Figure 43. Input Bias Current Histogram over Temperature
(VS = 5 V)

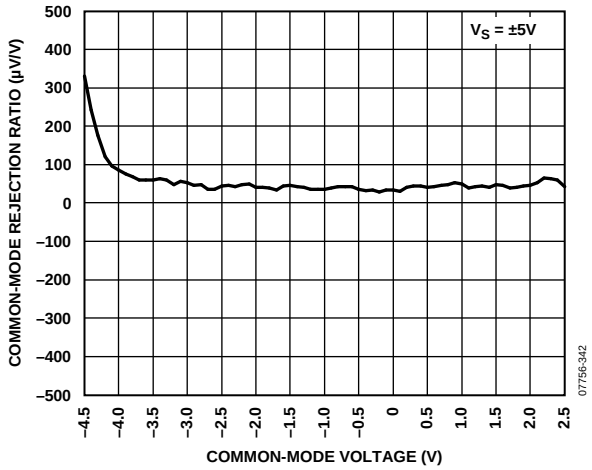

Figure 44. Common-Mode Rejection vs. Common-Mode Voltage, VS = ±5 V

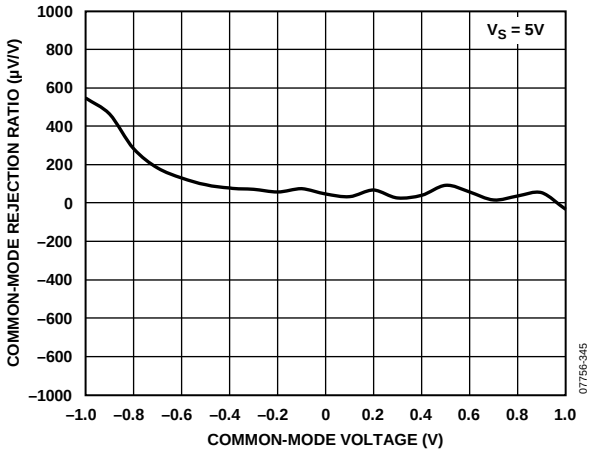

Figure 45. Common-Mode Rejection vs. Common-Mode Voltage, VS = 5 V

TEST CIRCUITS

The output feedback pins are used for ease of layout as shown in Figure 46 to Figure 51.

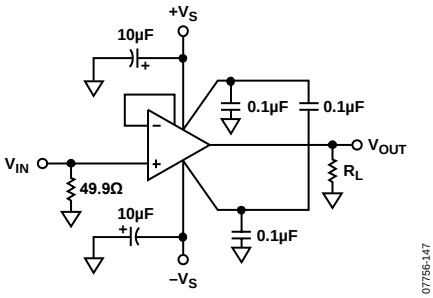

Figure 46. G = 1 Configuration

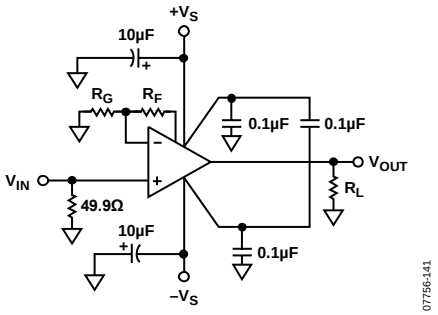

Figure 49. Noninverting Gain Configuration

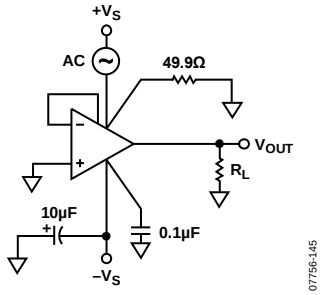

Figure 47. Positive Power Supply Rejection

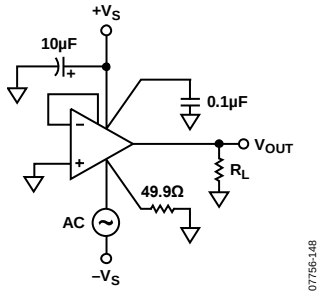

Figure 50. Negative Power Supply Rejection

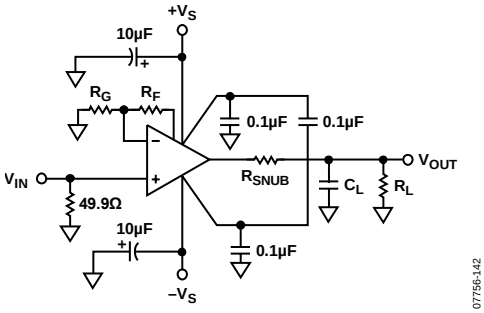

Figure 48. Capacitive Load Configuration

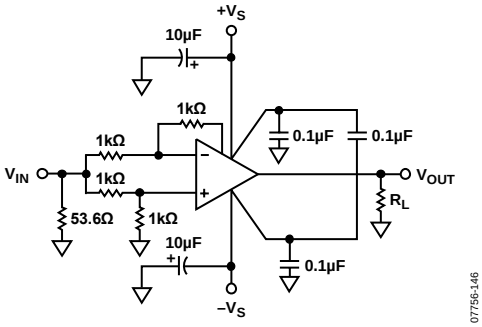

Figure 51. Common-Mode Rejection

THEORY OF OPERATION

The ADA4817-1/ADA4817-2 are voltage feedback operational amplifiers that combine new architecture for FET input operational amplifiers with the eXFCB process from Analog Devices, resulting in an outstanding combination of speed and low noise. The innovative high speed FET input stage handles common-mode signals from the negative supply to within 2.7 V of the positive rail. This stage is combined with an H-bridge to attain an 870 V/µs slew rate and low distortion, in addition to 4 nV/√Hz input voltage noise. The amplifier features a high speed output stage capable of driving heavy loads sourcing and sinking up to 40 mA of linear current. Supply current and offset current are laser trimmed for optimum performance. These specifications make the ADA4817-1/ADA4817-2 a great choice for high speed instrumentation and high resolution data acquisition systems. Their low noise, picoampere input current, precision offset, and high speed make them superb preamps for fast photo-diode applications.

CLOSED-LOOP FREQUENCY RESPONSE

The ADA4817-1/ADA4817-2 are classic voltage feedback amplifiers with an open-loop frequency response that can be approximated as the integrator response shown in Figure 54. Basic closed-loop frequency response for inverting and noninverting configurations can be derived from the schematics shown in Figure 52 and Figure 53.

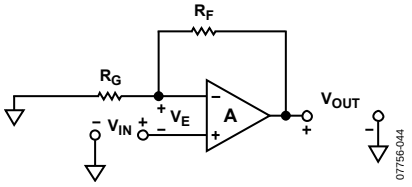

Figure 52. Noninverting Configuration

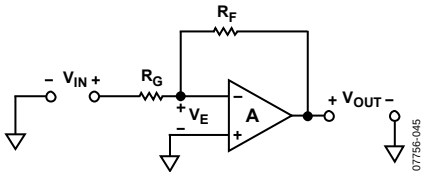

Figure 53. Inverting Configuration

NONINVERTING CLOSED-LOOP FREQUENCY RESPONSE

Solving for the transfer function,

$$\frac{V_O}{V_I} = \frac{2\pi \times f_{CROSSOVER}\left(R_G + R_F\right)}{\left(R_F + R_G\right)S + 2\pi \times f_{CROSSOVER} \times R_G} \quad (4)$$

where:

$f_{CROSSOVER}$ is the frequency where the open-loop gain of the amplifier equals 0 dB.

V_O is the output voltage.

V_I is the input voltage.

At dc,

$$\frac{V_O}{V_I} = \frac{R_F + R_G}{R_G} \quad (5)$$

The closed-loop −3 dB frequency is

$$f_{-3dB} = f_{CROSSOVER} \times \frac{R_G}{R_F + R_G} \quad (6)$$

INVERTING CLOSED-LOOP FREQUENCY RESPONSE

Solving for the transfer function,

$$\frac{V_O}{V_I} = \frac{-2\pi \times f_{CROSSOVER} \times R_F}{\left(R_F + R_G\right)S + 2\pi \times f_{CROSSOVER} \times R_G} \quad (7)$$

At dc

$$\frac{V_O}{V_I} = -\frac{R_F}{R_G} \quad (8)$$

Solve for closed-loop −3 dB frequency by

$$f_{-3dB} = f_{CROSSOVER} \times \frac{R_G}{R_F + R_G} \quad (9)$$

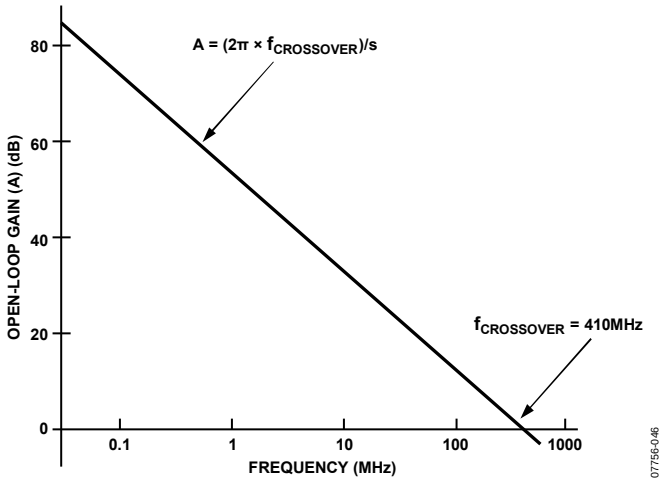

Figure 54. Open-Loop Gain vs. Frequency

The closed-loop bandwidth is inversely proportional to the noise gain of the op amp circuit, $(R_F + R_G)/R_G$. This simple model is accurate for noise gains above 2. The actual bandwidth of circuits with noise gains at or below 2 is higher than those predicted with this model due to the influence of other poles in the frequency response of the real op amp.

Figure 55 shows the dc errors of the voltage feedback amplifier. For both inverting and noninverting configurations,

$$V_{OUT}\ (error) =$$

$$I_{b+} \times R_S\left(\frac{R_G + R_F}{R_G}\right) - I_{b-} \times R_F + V_{OS}\left(\frac{R_G + R_F}{R_G}\right) \quad (10)$$

where I_b is the bias current.

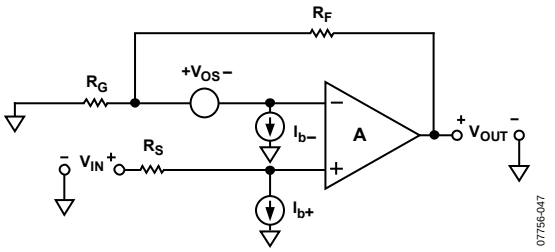

Figure 55. DC Errors of the Voltage Feedback Amplifier

The voltage error due to I_{b+} and I_{b-} is minimized if $R_S = R_F \parallel R_G$ (though with the ADA4817-1/ADA4817-2 input currents in the picoamp range, this is likely not a concern). To include common-mode effects and power supply rejection effects, total V_{OS} can be modeled by

$$V_{OS} = V_{OSnom} + \frac{\Delta V_S}{PSR} + \frac{\Delta V_{CM}}{CMR} \quad (11)$$

where:
V_{OS} is the offset voltage.

$V_{OS_{nom}}$ is the offset voltage specified at nominal conditions.

ΔV_S is the change in power supply from nominal conditions.
PSR is the power supply rejection.
ΔV_{CM} is the change in common-mode voltage from nominal conditions.
CMR is the common-mode rejection.

WIDEBAND OPERATION

The ADA4817-1/ADA4817-2 provides excellent performance as a high speed buffer. Figure 52 shows the circuit used for wideband characterization for high gains. The impedance at the summing junction ($R_F \parallel R_G$) forms a pole in the loop response of the amplifier with the input capacitance of the amplifier of 1.3 pF. This pole can cause peaking and ringing if its frequency is too low. Feedback resistances of 100 Ω to 400 Ω are recommended because they minimize the peaking and they do not degrade the performance of the output stage. Peaking in the frequency response can also be compensated for with a small feedback capacitor (C_F) in parallel with the feedback resistor, or a series resistor in the noninverting input, as shown in Figure 56.

The distortion performance depends on the following variables:

- The closed-loop gain of the application
- Whether it is inverting or noninverting
- Amplifier loading
- Signal frequency and amplitude
- Board layout

The best performance is usually obtained in the G + 1 configuration with no feedback resistance, big output load resistors, and small board parasitic capacitances.

DRIVING CAPACITIVE LOADS

In general, high speed amplifiers have a difficult time driving capacitive loads. This is particularly true in low closed-loop gains, where the phase margin is the lowest.

The difficulty arises because the load capacitance, C_L, forms a pole with the output resistance, R_O, of the amplifier. The pole can be described by the following equation:

$$f_P = \frac{1}{2\pi R_O C_L} \quad (12)$$

If this pole occurs too close to the unity-gain crossover point, the phase margin degrades. Degradation is due to the additional phase loss associated with the pole.

Note that such capacitance introduces significant peaking in the frequency response. Larger capacitance values can be driven but must use a small series resistor, R_{SNUB}, at the output of the amplifier, as shown in Figure 56. Adding R_{SNUB} creates a zero that cancels the pole introduced by the load capacitance. Typical values for R_{SNUB} can range from 10 Ω to 50 Ω. The value is typically based on the circuit requirements. Figure 56 also shows another way to reduce the effect of the pole created by the capacitive load (C_L) by placing a capacitor (C_F) in the feedback loop parallel to the feedback resistor Typical capacitor values can range from 0.5 pF to 2 pF. Figure 59 shows the effect of adding a feedback capacitor to the frequency response.

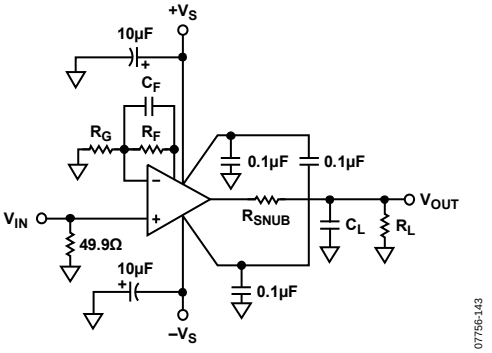

Figure 56. R_{SNUB} or C_F Used to Reduce Peaking

THERMAL CONSIDERATIONS

With 10 V power supplies and 19 mA quiescent current, the ADA4817-1/ADA4817-2 dissipate 190 mW with no load. This implies that with the thermal resistances listed in Table 4, the junction temperature is typically almost 25°C higher than the ambient temperature. The ADA4817-1/ADA4817-2 can maintain a constant bandwidth over temperature; therefore, an initial ramp up of the current consumption during warm-up is expected. V_{OS} can change up to 0.3 mV due to warm-up effects for an ADA4817-1/ADA4817-2 on ± 5 V. The input bias current typically increases by a factor of 1.7 for every 10°C rise in temperature.

Heavy loads increase power dissipation and raise the chip junction temperature as described in the Absolute Maximum Ratings section. Take care not to exceed the rated power dissipation of the package.

POWER-DOWN OPERATION

The ADA4817-1/ADA4817-2 are equipped with separate power-down pins ($\overline{PD}$) for each amplifier that allow the user the ability to reduce the quiescent supply current when an amplifier is inactive from 19 mA to below 2 mA. The power-down threshold levels are referenced to the $+V_S$ pin. The amplifier is enabled when the $\overline{PD}$ pin voltage is within 0.9 V of the $+V_S$ supply. The amplifier is disabled when the $\overline{PD}$ pin voltage is at least 3.5 V from the $+V_S$ supply. Table 8 shows the required thresholds for power-down with supplies of ±5 V and 3 V, −2 V, over temperature. If the $\overline{PD}$ pin is not used, connect it to the positive power supply to ensure proper start-up.

Table 8. $\overline{PD}$ Pin Control

Supply Voltages	±5 V	+3 V, −2 V
Amplifier Enabled	>4.1 V	>2.1 V
Amplifier Disabled	<1.5 V	<−0.5 V

When the amplifier is powered down with the supplies of +3 V and −2 V, the $\overline{PD}$ pin needs to be driven below ground to ensure the power-down. This may be a problem if a microcontroller is being used to drive the $\overline{PD}$ pin. The circuit in Figure 57 can be added to ensure that the required threshold is met.

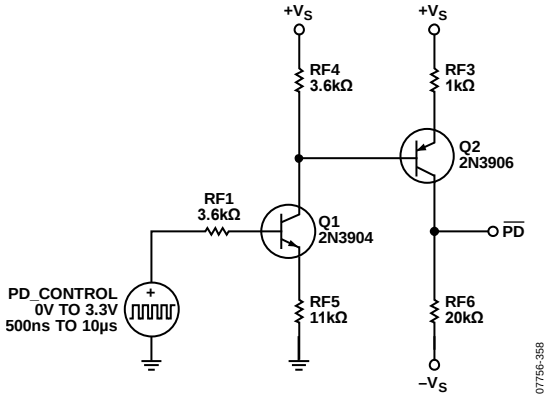

Figure 57. Power-Down Circuit

The plot in Figure 58 shows that the $\overline{PD}$ pin is driven to the positive rail when the microcontroller logic is high, and to the negative rail when the microcontroller logic is low. The RF5 and RF6 resistors must be chosen to be sufficiently high so that minimal current is drawn by the circuit.

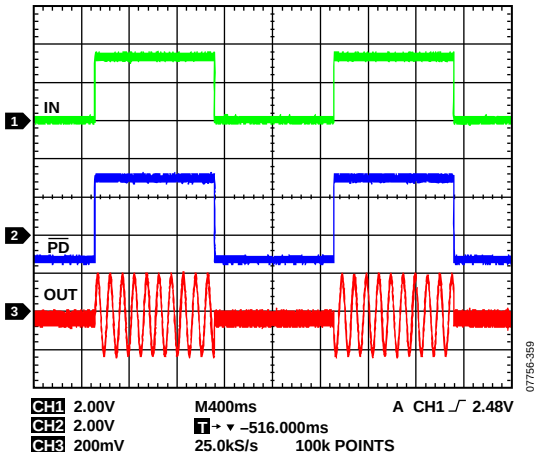

Figure 58. Power-Down Operation

CAPACITIVE FEEDBACK

Due to package variations and pin to pin parasitics between the single and the dual models, the ADA4817-2 has a little more peaking then the ADA4817-1, especially at a gain of 2. The recommended method to tame the peaking is to place a feedback capacitor across the feedback resistor. Figure 59 shows the small signal frequency response of the ADA4817-2 at a gain of 2 vs. C_F. At first, no C_F was used to show the peaking; but then two other values of 0.5 pF and 1 pF were used to show how to reduce the peaking or even eliminate it. If the power consumption is a factor in the system, using a larger feedback capacitor is acceptable as long as a feedback capacitor is used across it to control the peaking, as shown in Figure 59.

However, if power consumption is not an issue, a lower value feedback resistor, such as 200 Ω, does not require any additional feedback capacitance to maintain flatness and lower peaking.

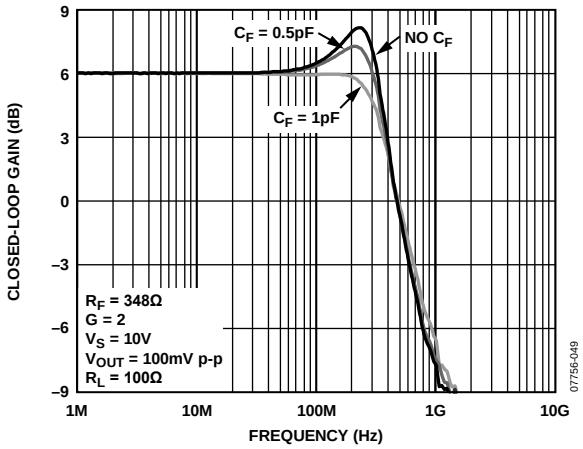

Figure 59. Small Signal Frequency Response vs. Feedback Capacitor (ADA4817-2)

HIGHER FREQUENCY ATTENUATION

There is another package variation problem between the SOIC and the LFCSP package. The SOIC package shows approximately 1 dB to 1.5 dB of additional peaking at a gain of 1, due to the parasitic capacitances in the SOIC package, which is not recommended for very high frequency parts that exceed 1 GHz. A good approach to reduce the peaking is to place a resistor, R_S, in series with the noninverting input, which creates a first-order pole formed by R_S and C_{IN}, the common-mode input capacitance.

Figure 60 shows the higher frequency attenuation, which reduces the peaking but also reduces the −3 dB bandwidth.

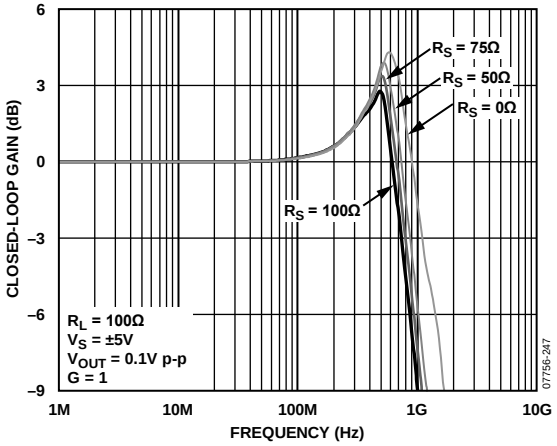

Figure 60. Small Signal Frequency Response for Various R_S (SOIC)

As shown in Figure 60, the peaking dropped by almost 2 dB when R_S = 0 Ω to R_S = 100 Ω, and in return, the −3 dB bandwidth dropped from 1 GHz to 700 MHz. To maintain the −3 dB bandwidth and to reduce peaking, an RLC circuit is recommended instead of R_S, as shown in Figure 61.

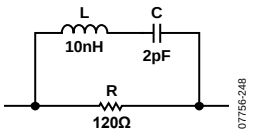

Figure 61. RLC Circuit

The R in parallel to the series LC forms a notch that can be shaped to compensate for the peaking produced by the amplifier. The result is a smooth 1 GHz −3 dB bandwidth, 250 MHz 0.1 dB flatness, and less than 1 dB of peaking. Place this circuit in the path of the noninverting input when the ADA4817-1/ADA4817-2 are used at a gain of 1. The RLC values may need adjustment depending on the source impedance and the flatness and bandwidth required. Figure 62 shows the frequency response after the RLC circuit is in place.

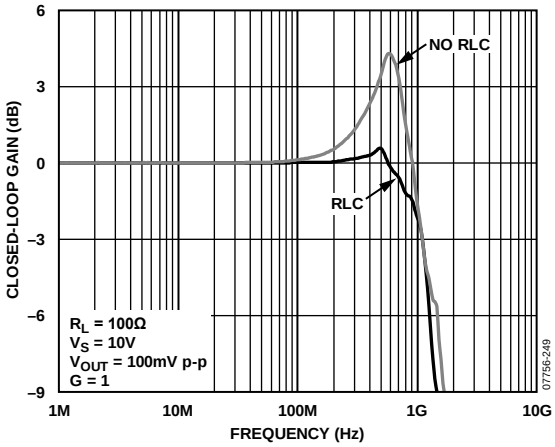

Figure 62. Frequency Response with RLC Circuit

LAYOUT, GROUNDING, AND BYPASSING CONSIDERATIONS

Laying out the PCB is usually the last step in the design process and often proves to be one of the most critical. A good design can be rendered useless because of poor layout. Because the ADA4817-1/ADA4817-2 can operate into the radio frequency (RF) spectrum, high frequency board layout considerations must be taken into account. The PCB layout, signal routing, power supply bypassing, and grounding all must be addressed to ensure optimal performance.

SIGNAL ROUTING

The ADA4817-1/ADA4817-2 feature a low distortion pinout with a dedicated feedback pin that allows a compact layout. The dedicated feedback pin reduces the distance from the output to the inverting input, which greatly simplifies the routing of the feedback network.

When laying out the ADA4817-1/ADA4817-2 as a unity-gain amplifier, it is recommended to place a short but wide trace between the dedicated feedback pins and the inverting input to the amplifier to minimize stray parasitic inductance.

To minimize parasitic inductances, use ground planes under high frequency signal traces. However, remove the ground plane from under the input and output pins to minimize the formation of parasitic capacitors, which degrades phase margin. Run signals are susceptible to noise pickup on the internal layers of the PCB, which can provide maximum shielding.

POWER SUPPLY BYPASSING

Power supply bypassing is a critical aspect of the PCB design process. For best performance, properly bypass the ADA4817-1/ADA4817-2 power supply pins.

A parallel connection of capacitors from each of the power supply pins to ground works best. Paralleling different values and sizes of capacitors helps ensure that the power supply pins see a low ac impedance across a wide band of frequencies, which is important for minimizing the coupling of noise into the amplifier. Starting directly at the power supply pins, place the smallest value and sized component on the same side of the board as the amplifier, and as close as possible to the amplifier, and connect it to the ground plane. Repeat this process for the next largest value capacitor. It is recommended to use a 0.1 µF ceramic, 0508 case for the ADA4817-1/ADA4817-2.

The 0508 case offers low series inductance and excellent high frequency performance. The 0.1 µF provides low impedance at high frequencies. Place a 10 µF electrolytic capacitor in parallel with the 0.1 µF. The 10 µF electrolytic capacitor provides low ac impedance at low frequencies. Smaller values of electrolytic capacitors can be used depending on the circuit requirements. Additional smaller value capacitors help provide a low impedance path for unwanted noise out to higher frequencies but are not always necessary.

Placement of the capacitor returns (grounds) is also important. Returning the grounds of the capacitor close to the amplifier load is critical for distortion performance. Keeping the distance of the capacitors short, but equal from the load, is optimal for performance.

In some cases, bypassing between the two supplies can help to improve PSRR and to maintain distortion performance in crowded or difficult layouts. Bypassing is another option to improve performance.

Minimizing the trace length and widening the trace from the capacitors to the amplifier reduces the trace inductance. A series inductance with the parallel capacitance can form a tank circuit, which can introduce high frequency ringing at the output. This additional inductance can also contribute to increased distortion due to high frequency compression at the output. Minimize the use of vias in the direct path to the amplifier power supply pins because vias can introduce parasitic inductance, which can lead to instability. When required to use vias, choose multiple large diameter vias because this lowers the equivalent parasitic inductance.

GROUNDING

The use of ground and power planes is encouraged as a method of providing low impedance returns for power supply and signal currents. Ground and power planes can also help to reduce stray trace inductance and to provide a low thermal path for the amplifier. Do not use ground and power planes under any of the pins. The mounting pads and the ground or power planes can form a parasitic capacitance at the input of the amplifier. Stray capacitance on the inverting input and the feedback resistor form a pole, which degrades the phase margin, leading to instability. Excessive stray capacitance on the output also forms a pole, which degrades phase margin.

EXPOSED PAD

The ADA4817-1/ADA4817-2 feature an exposed pad, which lowers the thermal resistance by 25% compared to a standard SOIC plastic package. The exposed pad of the ADA4817-1/ADA4817-2 floats internally, which provides the maximum flexibility and ease of use. It can be connected to the ground plane or to the negative power supply plane. In cases where thermal heating is not an issue, the exposed pad can be left floating.

The use of thermal vias or heat pipes can also be incorporated into the design of the mounting pad for the exposed pad. These additional vias help to lower the overall junction to ambient temperature (θ_{JA}). Using a heavier weight copper on the surface to which the exposed paddle of the amplifier is soldered can greatly reduce the overall thermal resistance seen by the ADA4817-1/ADA4817-2.

LEAKAGE CURRENTS

Poor PCB layout, contaminants, and the board insulator material can create leakage currents that are much larger than the input bias current of the ADA4817-1/ADA4817-2. Any voltage differential between the inputs and nearby runs sets up leakage currents through the PCB insulator, for example, 1 V/100 GΩ = 10 pA. Similarly, any contaminants, such as skin oils on the board, can create significant leakage. To reduce leakage significantly, put a guard ring (shield) around the inputs and input leads that are driven to the same voltage potential as the inputs. This way there is no voltage potential between the inputs and surrounding area to set up any leakage currents. For the guard ring to be completely effective, it must be driven by a relatively low impedance source and it must completely surround the input leads on all sides (above and below) when using a multilayer board.

Another effect that can cause leakage currents is the charge absorption of the insulator material itself. Minimizing the amount of material between the input leads and the guard ring helps to reduce the absorption. In addition, low absorption materials, such as Teflon® or ceramic, can be necessary in some instances.

INPUT CAPACITANCE

Along with bypassing and ground, high speed amplifiers can be sensitive to parasitic capacitance between the inputs and ground. A few picofarads of capacitance reduces the input impedance at high frequencies, in turn increasing the gain of the amplifier, causing peaking of the frequency response or even oscillations if severe enough. It is recommended to place the external passive components connected to the input pins as close as possible to the inputs to avoid parasitic capacitance. The ground and power planes must be kept at a small distance from the input pins on all layers of the board.

INPUT-TO-INPUT/OUTPUT COUPLING

To minimize capacitive coupling between the inputs and outputs, ensure that the output signal traces are not parallel with the inputs. In addition, ensure that the input traces are not close to each other. A minimum of 7 mils between the two inputs is recommended.

APPLICATIONS INFORMATION

LOW DISTORTION PINOUT

The ADA4817-1/ADA4817-2 feature a low distortion pinout from Analog Devices. The new pinout provides two advantages over the traditional pinout. The first advantage is improved second harmonic distortion performance, which is accomplished by the physical separation of the noninverting input pin and the negative power supply pin. The second advantage is the simplification of the layout due to the dedicated feedback pin and easy routing of the gain set resistor back to the inverting input pin. This pinout allows a compact layout, which helps to minimize parasitics and increase stability.

The designer does not need to use the dedicated feedback pin to provide feedback for the ADA4817-1/ADA4817-2. The output pin of the ADA4817-1/ADA4817-2 can still be used to provide feedback to the inverting input of the ADA4817-1/ADA4817-2.

WIDEBAND PHOTODIODE PREAMP

The wide bandwidth and low noise of the ADA4817-1/ADA4817-2 make it an ideal choice for transimpedance amplifiers, such as those used for signal conditioning with high speed photodiodes. Figure 63 shows a current to voltage converter with an electrical model of a photodiode. The basic transfer function is

$$V_{OUT} = \frac{I_{PHOTO} \times R_F}{1 + sC_F R_F} \quad (13)$$

where:
I_{PHOTO} is the output current of the photodiode.
R_F and C_F are the parallel combination that sets the signal bandwidth.

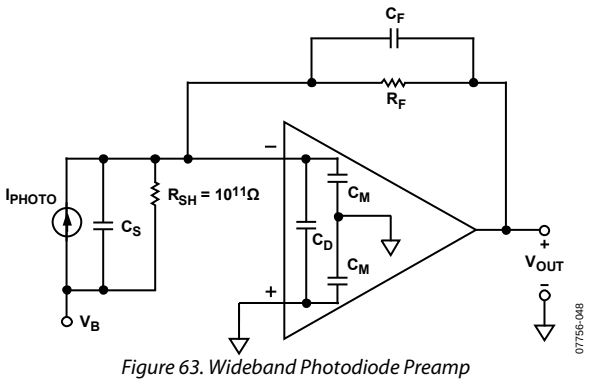

Figure 63. Wideband Photodiode Preamp

The stable bandwidth attainable with this preamp is a function of R_F, the gain bandwidth product of the amplifier, and the total capacitance at the summing junction of the amplifier, including the photodiode capacitance (C_S) and the amplifier input capacitance. R_F and the total capacitance produce a pole in the loop transmission of the amplifier that can result in peaking and instability. Adding C_F creates a zero in the loop transmission that compensates for the effect of the pole and reduces the signal bandwidth. It can be shown that the signal bandwidth obtained with a 45° phase margin ($f_{(45)}$) is defined by

$$f_{(45)} = \sqrt{\frac{f_{CR}}{2\pi \times R_F \times (C_S + C_M + C_D)}} \quad (14)$$

where:
f_{CR} is the amplifier crossover frequency.
R_F is the feedback resistor.
C_S is the source capacitance including the photodiode and the board parasitic.
C_M is the common-mode capacitance of the amplifier.
C_D is the differential capacitance of the amplifier.

The C_F value that produces $f_{(45)}$ is shown to be

$$C_F = \sqrt{\frac{C_S + C_M + C_D}{2\pi \times R_F \times f_{CR}}} \quad (15)$$

The frequency response shows less peaking if larger C_F values are used.

Figure 64 shows the preamplifier output noise over frequency.

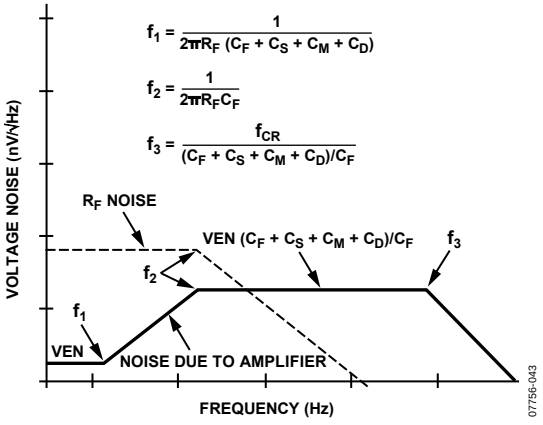

Figure 64. Photodiode Voltage Noise Contributions

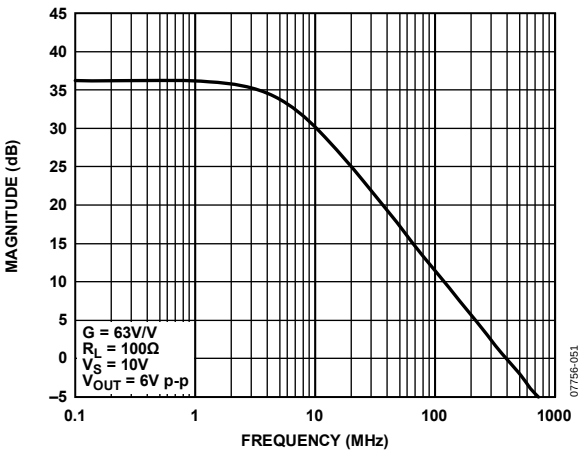

Figure 65. Photodiode Preamp Frequency Response

The pole in the loop transmission translates to a zero in the noise gain of the amplifier, leading to an amplification of the input voltage noise over frequency.

The loop transmission zero introduced by C_F limits the amplification. The noise gain bandwidth extends past the preamp signal bandwidth and is eventually rolled off by the decreasing loop gain of the amplifier. The current equivalent noise from the inverting terminal is typically negligible for most applications. The innovative architecture used in the ADA4817-1/ADA4817-2 makes balancing both inputs unnecessary, as opposed to traditional FET input amplifiers. Therefore, minimizing the impedance seen from the noninverting terminal to ground at all frequencies is critical for optimal noise performance.

Integrating the square of the output voltage noise spectral density over frequency and then taking the square root allows the user to obtain the total rms output noise of the preamp. Table 9 summarizes approximations for the amplifier and feedback and source resistances. Noise components for an example preamp with R_F = 50 kΩ, C_S = 30 pF, and C_F = 0.5 pF (bandwidth of about 6.4 MHz) are also listed. VEN is the equivalent voltage noise and IEN is the equivalent current noise.

Table 9. RMS Noise Contributions of Photodiode Preamp

Contributor	Expression	RMS Noise with R_F = 50 kΩ, C_S = 30 pF, C_F = 0.5 pF
R_F	$\sqrt{4kT \times R_F \times f_2 \times 1.57}$	94 µV
VEN Amp	$VEN \times \frac{C_S + C_M + C_D + C_F}{C_F} \times \sqrt{f_3 \times 1.57}$	777.5 µV
IEN Amp	$IEN \times R_F \times \sqrt{f_2 \times 1.57}$	0.4 µV
Total		783 µV

HIGH SPEED JFET INPUT INSTRUMENTATION AMPLIFIER

Figure 66 shows an example of a high speed instrumentation amplifier with a high input impedance using the ADA4817-1/ ADA4817-2. The dc transfer function is

$$V_{OUT} = (V_N - V_P)\left(1 + \frac{2R_F}{R_G}\right) \quad (16)$$

For G = 1, it is recommended that the feedback resistors for the two preamps be set to 0 Ω and the gain resistor be open.

The system bandwidth for G = 1 is 400 MHz. For gains higher than 2, the bandwidth is set by the preamp, and it can be approximated by

$$In\text{-}amp_{-3\,dB} = (f_{CR} \times R_G)/(2 \times R_F)$$

The match of resistor ratios, R1:R2 to R3:R4, primarily determine the common-mode rejection of the in-amp and it is estimated by

$$\frac{V_O}{V_{CM}} = \frac{(\delta 1 - \delta 2)}{(1 + \delta 1)\,\delta 2} \quad (17)$$

The summing junction impedance for the preamps is equal to $R_F \,||\, 0.5(R_G)$. Keep this value relatively low to improve the bandwidth response like in the previous example.

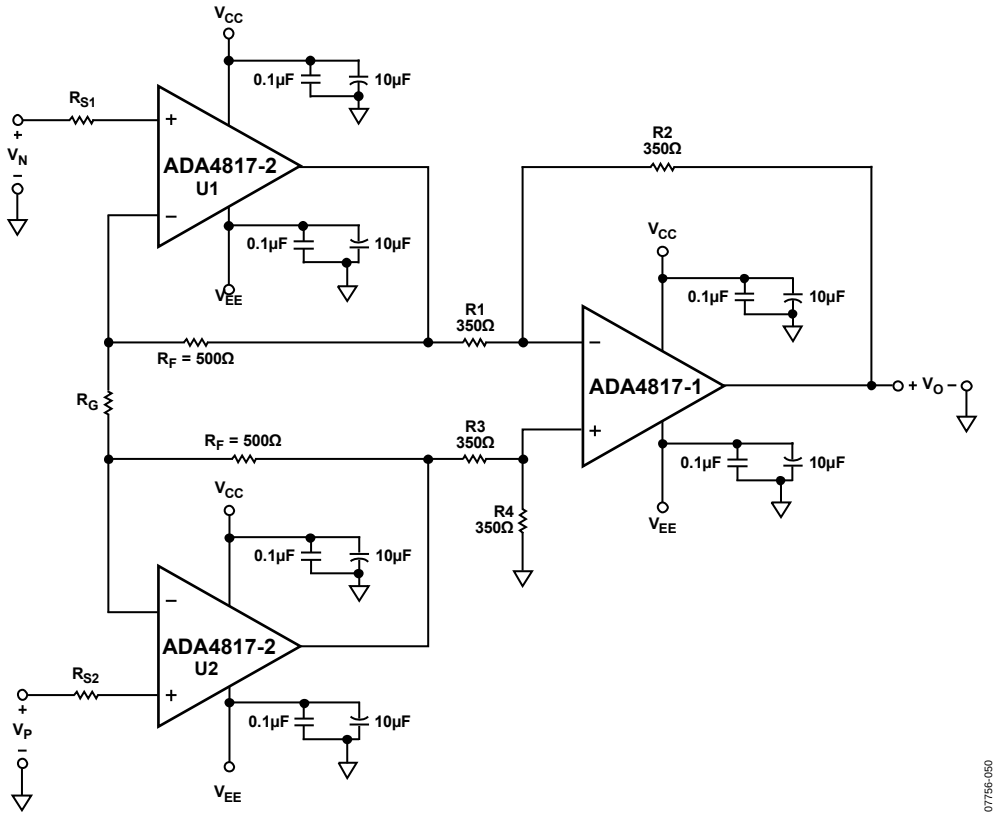

Figure 66. High Speed Instrumentation Amplifier

ACTIVE LOW-PASS FILTER (LPF)

Active low-pass filters are used in many applications such as antialiasing filters and high frequency communication intermediate frequency (IF) strips.

With a 410 MHz gain bandwidth product and high slew rate, the ADA4817-1/ADA4817-2 is an ideal candidate for active filters. Moreover, thanks to the low input bias current provided by the FET stage, the ADA4817-1/ADA4817-2 eliminate any dc errors. Figure 67 shows the frequency response of 90 MHz and 45 MHz LPFs. In addition to the bandwidth requirements, the slew rate must be capable of supporting the full power bandwidth of the filter. In this case, a 90 MHz bandwidth with a 2 V p-p output swing requires at least 870 V/µs. This performance is achievable at 90 MHz only because of the wide bandwidth and high slew rate of the ADA4817-1/ADA4817-2.

The circuit shown in Figure 68 is a 4-pole, Sallen-Key LPF. The filter comprises two identical cascaded Sallen-Key LPF sections, each with a fixed gain of G = 2. The net gain of the filter is equal to G = 4 or 12 dB. The actual gain shown in Figure 67 is 12 dB. This gain does not take into account the output voltage being divided in half by the series matching termination resistor, R_T, and the load resistor.

Setting the resistors equal to each other greatly simplifies the design equations for the Sallen-Key filter. To achieve 90 MHz, set the R value to 182 Ω. However, if the R value is doubled, the corner frequency is cut in half to 45 MHz, which is a straightforward approach to tune the filter by multiplying the R value (182 Ω) by the ratio of 90 MHz and the new corner frequency in megahertz. Figure 67 shows the output of each stage of the filter and the two different filters corresponding to R = 182 Ω and R = 365 Ω. It is not recommended to increase the corner frequency beyond 90 MHz due to bandwidth and slew rate limitations, unless unity-gain stages are acceptable.

Resistor values are kept low for minimal noise contribution, offset voltage, and optimal frequency response. Due to the low capacitance values used in the filter circuit, the PCB layout and minimization of parasitics is critical. A few picofarads can detune the corner frequency, f_C, of the filter. The capacitor values shown in Figure 68 actually incorporate some stray PCB capacitance.

Capacitor selection is critical for optimal filter performance. Capacitors with low temperature coefficients, such as NPO ceramic capacitors and silver mica, are good choices for filter elements.

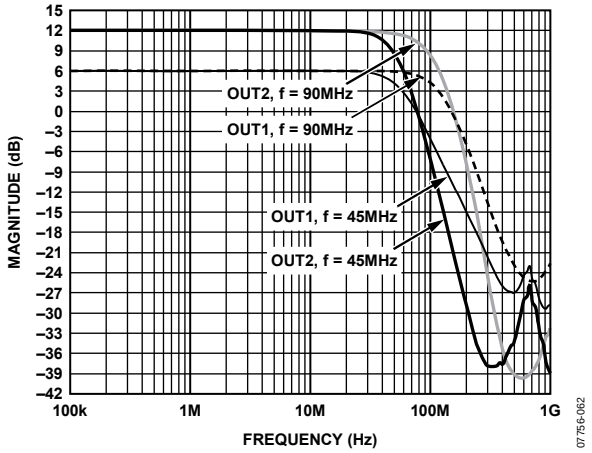

Figure 67. Low-Pass Filter Response

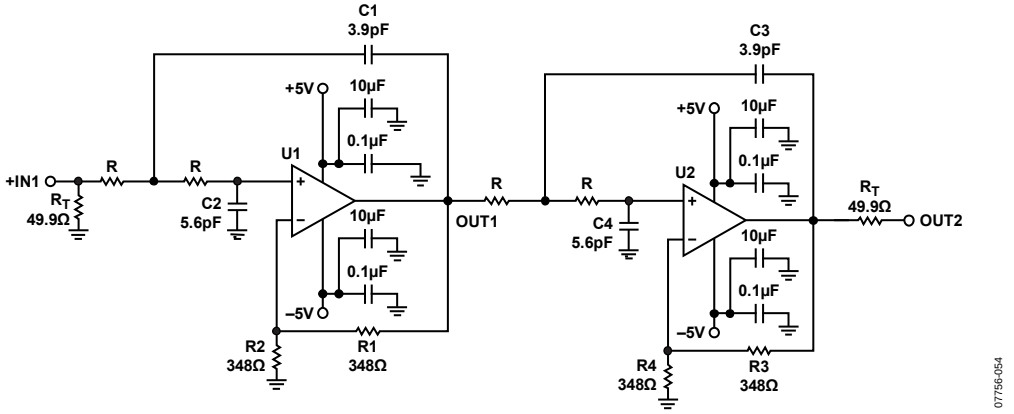

Figure 68. 4-Pole, Sallen-Key LPF (ADA4817-2)

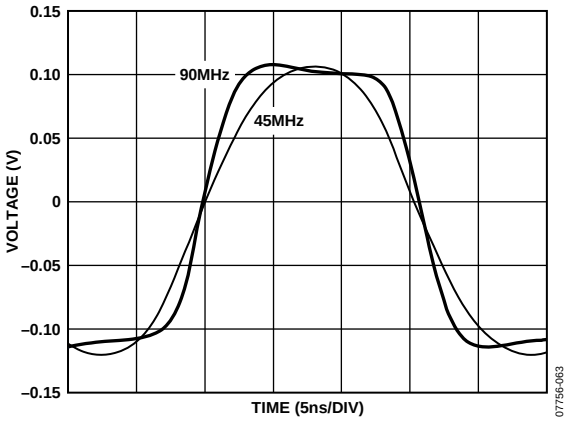

Figure 69. Small Signal Transient Response (Low-Pass Filter)

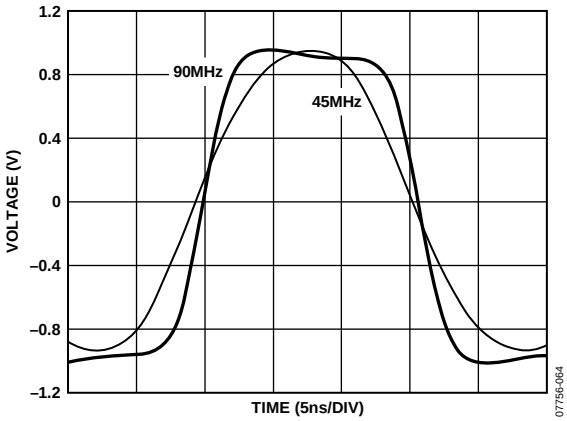

Figure 70. Large Signal Transient Response (Low-Pass Filter)

OUTLINE DIMENSIONS

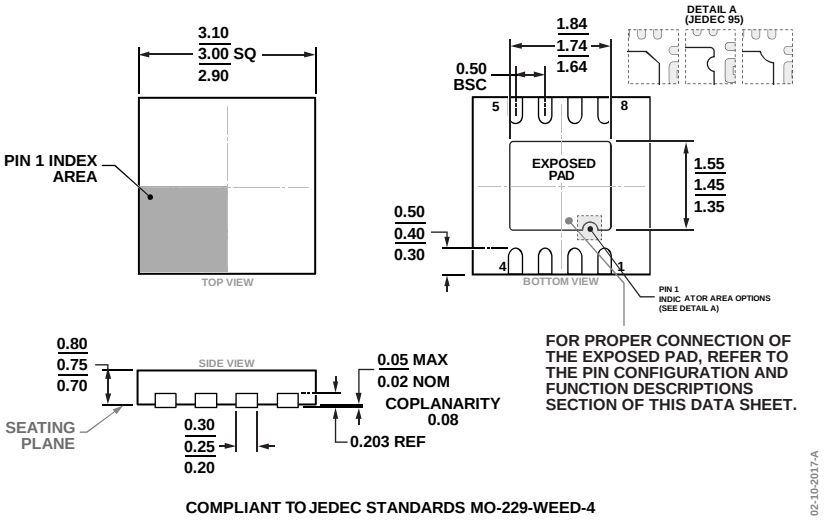

Figure 71. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-13)
Dimensions shown in millimeters

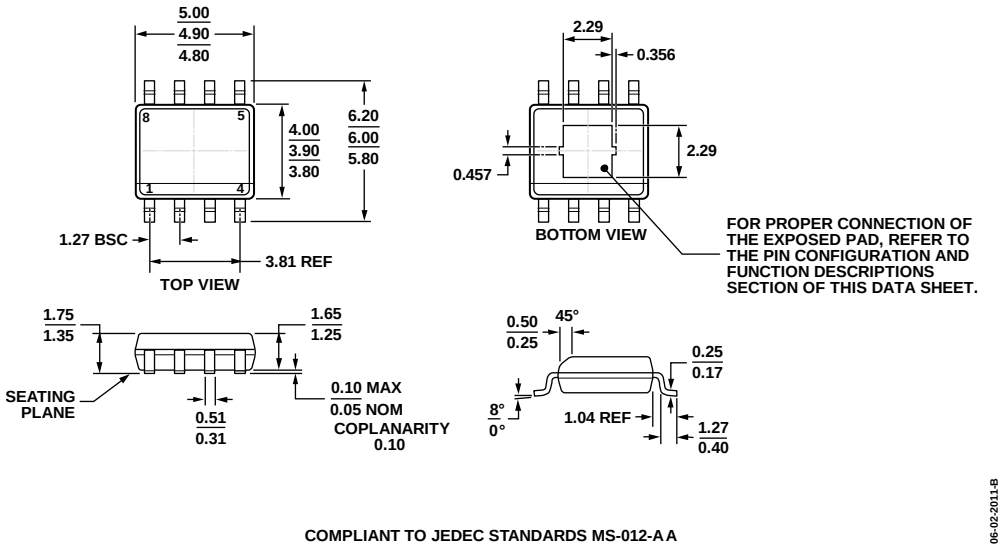

Figure 72. 8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]
(RD-8-1)
Dimensions shown in millimeters

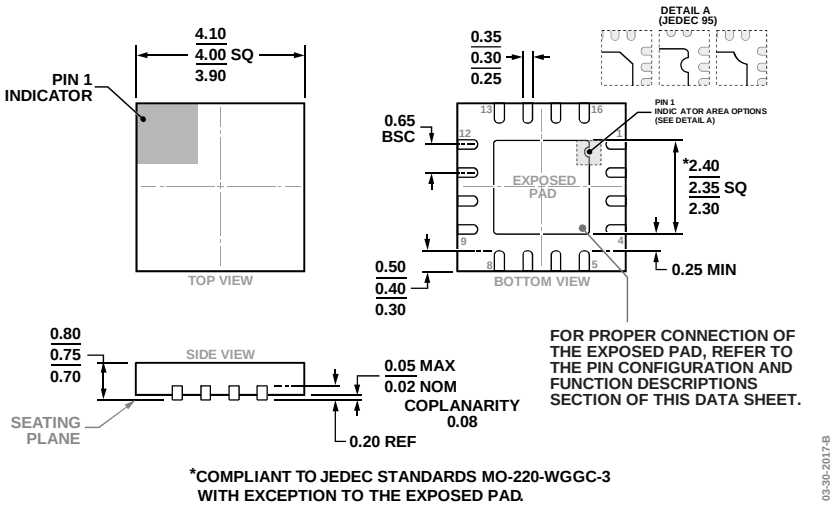

Figure 73.16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity	Marking Code
ADA4817-1ACPZ-RL	−40°C to +105°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-13	5000	H1F
ADA4817-1ACPZ-R7	−40°C to +105°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-13	1500	H1F
ADA4817-1ARDZ	−40°C to +105°C	8-Lead Standard Small Outline Package with Exposed Pad	RD-8-1	1	
ADA4817-1ARDZ-RL	−40°C to +105°C	8-Lead Standard Small Outline Package with Exposed Pad	RD-8-1	2500	
ADA4817-1ARDZ-R7	−40°C to +105°C	8-Lead Standard Small Outline Package with Exposed Pad	RD-8-1	1000	
ADA4817-2ACPZ-RL	−40°C to +105°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-20	5000	
ADA4817-2ACPZ-R7	−40°C to +105°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-20	1500	
ADA4817-2ACP-EBZ		Evaluation Board for 16-Lead LFCSP			

[1] Z = RoHS Compliant Part.

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ADA4817-1ARDZ ADA4817-1ACPZ-R7 ADA4817-1ACPZ-RL ADA4817-1ARDZ-R7 ADA4817-1ARDZ-RL ADA4817-2ACPZ-R7 ADA4817-2ACPZ-RL ADA4817-1ACPZ-R2 ADA4817-2ACPZ-R2