

## 1. General description

Planar passivated very sensitive gate four quadrant triac in a SOT54 (TO-92) plastic package intended for use in applications requiring enhanced noise immunity and direct interfacing to logic ICs and low power gate drivers.

## 2. Features and benefits

- Direct interfacing to logic level ICs
- Enhanced current surge capability
- Enhanced noise immunity
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Very sensitive gate in four quadrants

## 3. Applications

- General purpose low power motor control
- Home appliances
- Industrial process control
- Low power AC Fan controllers

## 4. Quick reference data

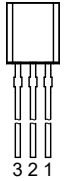
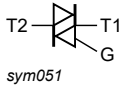
Table 1. Quick reference data

| Symbol                        | Parameter                            | Conditions  | Min | Typ | Max  | Unit |
|-------------------------------|--------------------------------------|---|-----|-----|------|------|
| $V_{DRM}$                     | repetitive peak off-state voltage    |   | -   | -   | 600  | V    |
| $I_{T(RMS)}$                  | RMS on-state current                 | full sine wave; $T_{lead} \leq 45\text{ °C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a> | -   | -   | 1    | A    |
| $I_{TSM}$                     | non-repetitive peak on-state current | full sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>   | -   | -   | 12.5 | A    |
|                               |                                      | full sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 16.7\text{ ms}$   | -   | -   | 13.8 | A    |
| $T_j$                         | junction temperature                 |   | -   | -   | 125  | °C   |
| <b>Static characteristics</b> |                                      |   |     |     |      |      |
| $I_{GT}$                      | gate trigger current                 | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>                      | 0.2 | -   | 3    | mA   |
|                               |                                      | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>                      | 0.2 | -   | 3    | mA   |

| Symbol                         | Parameter                             | Conditions  | Min | Typ | Max | Unit       |
|--------------------------------|---------------------------------------|---|-----|-----|-----|------------|
|                                |                                       | $V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2\text{- G-}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 7</a>   | 0.2 | -   | 3   | mA         |
|                                |                                       | $V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2\text{- G+}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 7</a>   | 0.2 | -   | 5   | mA         |
| $I_H$                          | holding current                       | $V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 9</a>   | -   | -   | 7   | mA         |
| $V_T$                          | on-state voltage                      | $I_T = 1.4\text{ A}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>   | -   | 1.3 | 1.6 | V          |
| <b>Dynamic characteristics</b> |                                       |   |     |     |     |            |
| $dV_D/dt$                      | rate of rise of off-state voltage     | $V_{DM} = 402\text{ V}; T_j = 110\text{ }^\circ\text{C}; (V_{DM} = 67\% \text{ of } V_{DRM});$ exponential waveform; gate open circuit; <a href="#">Fig. 12</a> | 80  | -   | -   | V/ $\mu$ s |
| $dV_{com}/dt$                  | rate of change of commutating voltage | $V_D = 400\text{ V}; T_j = 110\text{ }^\circ\text{C}; dI_{com}/dt = 0.44\text{ A/ms}; I_T = 1\text{ A};$ gate open circuit                                      | 0.5 | -   | -   | V/ $\mu$ s |

## 5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description     | Simplified outline   | Graphic symbol  |
|-----|--------|-----------------|--|---|
| 1   | T2     | main terminal 2 |  <p>TO-92 (SOT54)</p> |  <p>sym051</p> |
| 2   | G      | gate            |  |   |
| 3   | T1     | main terminal 1 |  |   |

## 6. Ordering information

Table 3. Ordering information

| Type number | Package |   |         |
|-------------|---------|---|---------|
|             | Name    | Description   | Version |
| Z0103MA0    | TO-92   | plastic single-ended leaded (through hole) package; 3 leads | SOT54   |

## 7. Limiting values

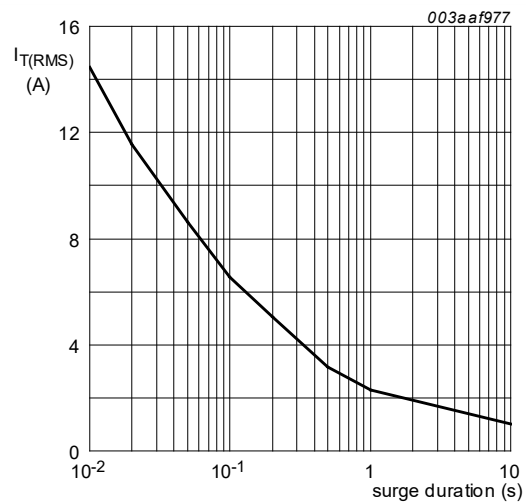
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol       | Parameter                            | Conditions  | Min | Max  | Unit             |
|--------------|--------------------------------------|---|-----|------|------------------|
| $V_{DRM}$    | repetitive peak off-state voltage    |   | -   | 600  | V                |
| $I_{T(RMS)}$ | RMS on-state current                 | full sine wave; $T_{lead} \leq 45\text{ °C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a> | -   | 1    | A                |
| $I_{TSM}$    | non-repetitive peak on-state current | full sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>   | -   | 12.5 | A                |
|              |                                      | full sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 16.7\text{ ms}$   | -   | 13.8 | A                |
| $I^2t$       | $I^2t$ for fusing                    | $t_p = 10\text{ ms}$ ; SIN  | -   | 0.78 | A <sup>2</sup> s |
| $di_T/dt$    | rate of rise of on-state current     | $I_G = 20\text{ mA}$ ; T2+ G+   | -   | 50   | A/ $\mu$ s       |
|              |                                      | $I_G = 20\text{ mA}$ ; T2+ G-   | -   | 50   | A/ $\mu$ s       |
|              |                                      | $I_G = 20\text{ mA}$ ; T2- G-   | -   | 50   | A/ $\mu$ s       |
|              |                                      | $I_G = 20\text{ mA}$ ; T2- G+   | -   | 20   | A/ $\mu$ s       |
| $I_{GM}$     | peak gate current                    |   | -   | 1    | A                |
| $P_{GM}$     | peak gate power                      |   | -   | 2    | W                |
| $P_{G(AV)}$  | average gate power                   | over any 20 ms period   | -   | 0.1  | W                |
| $T_{stg}$    | storage temperature                  |   | -40 | 150  | °C               |
| $T_j$        | junction temperature                 |   | -   | 125  | °C               |



**Fig. 1. RMS on-state current as a function of lead temperature; maximum values**



$f = 50\text{ Hz}$ ;  $T_{lead} = 45\text{ °C}$

**Fig. 2. RMS on-state current as a function of surge duration; maximum values**

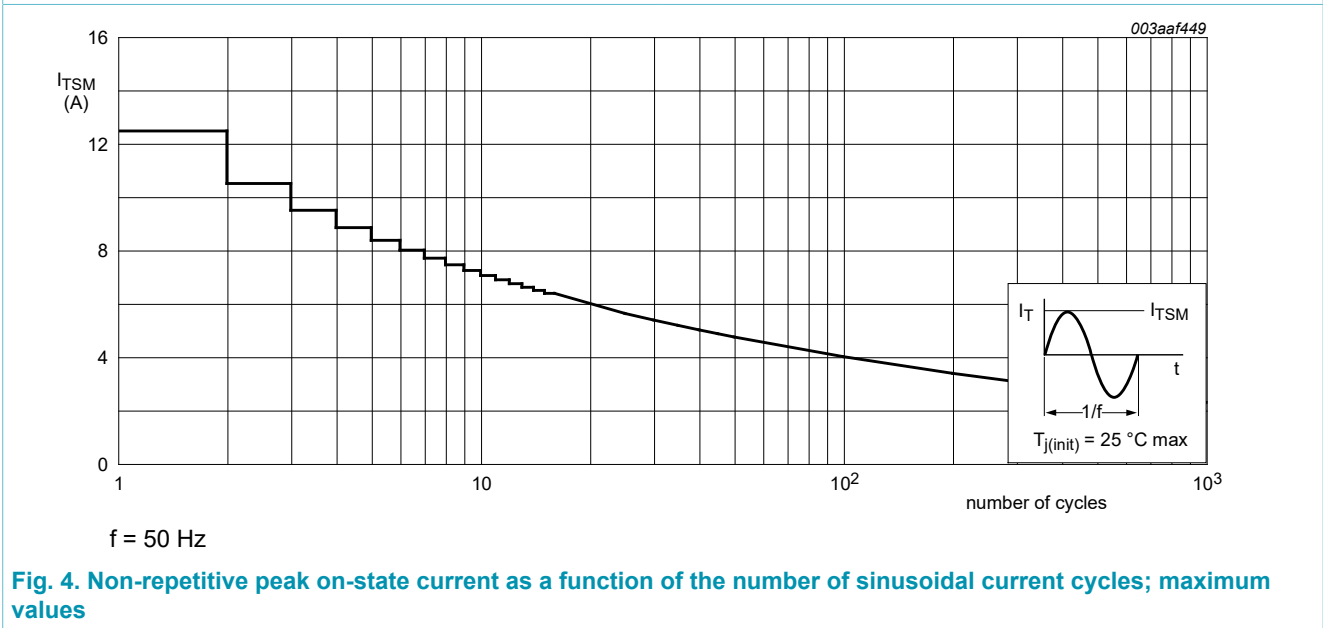




Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

## 8. Thermal characteristics

Table 5. Thermal characteristics

| Symbol           | Parameter  | Conditions  | Min | Typ | Max | Unit |
|------------------|--|---|-----|-----|-----|------|
| $R_{th(j-lead)}$ | thermal resistance from junction to lead             | full cycle; <a href="#">Fig. 6</a>                          | -   | -   | 60  | K/W  |
| $R_{th(j-a)}$    | thermal resistance from junction to ambient free air | full cycle; printed circuit board mounted; lead length 4 mm | -   | 150 | -   | K/W  |



Fig. 6. Transient thermal impedance from junction to lead as a function of pulse width

## 9. Characteristics

Table 6. Characteristics

| Symbol                         | Parameter                             | Conditions   | Min | Typ | Max | Unit             |
|--------------------------------|---------------------------------------|--|-----|-----|-----|------------------|
| <b>Static characteristics</b>  |                                       |  |     |     |     |                  |
| $I_{GT}$                       | gate trigger current                  | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>  | 0.2 | -   | 3   | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>  | 0.2 | -   | 3   | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>  | 0.2 | -   | 3   | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>  | 0.2 | -   | 5   | mA               |
| $I_L$                          | latching current                      | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>  | -   | -   | 7   | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G-;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>  | -   | -   | 20  | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2- G-;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>  | -   | -   | 7   | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2- G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>  | -   | -   | 7   | mA               |
| $I_H$                          | holding current                       | $V_D = 12\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 9</a>  | -   | -   | 7   | mA               |
| $V_T$                          | on-state voltage                      | $I_T = 1.4\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 10</a>  | -   | 1.3 | 1.6 | V                |
| $V_{GT}$                       | gate trigger voltage                  | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ;<br><a href="#">Fig. 11</a>   | -   | -   | 1   | V                |
|                                |                                       | $V_D = 600\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 125\text{ }^\circ\text{C}$ ;<br><a href="#">Fig. 11</a>   | 0.2 | -   | -   | V                |
| $I_D$                          | off-state current                     | $V_D = 600\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$   | -   | -   | 0.5 | mA               |
| <b>Dynamic characteristics</b> |                                       |  |     |     |     |                  |
| $dV_D/dt$                      | rate of rise of off-state voltage     | $V_{DM} = 402\text{ V}$ ; $T_j = 110\text{ }^\circ\text{C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit; <a href="#">Fig. 12</a> | 80  | -   | -   | V/ $\mu\text{s}$ |
| $dV_{com}/dt$                  | rate of change of commutating voltage | $V_D = 400\text{ V}$ ; $T_j = 110\text{ }^\circ\text{C}$ ; $dI_{com}/dt = 0.44\text{ A/ms}$ ; $I_T = 1\text{ A}$ ; gate open circuit                             | 0.5 | -   | -   | V/ $\mu\text{s}$ |



Fig. 7. Normalized gate trigger current as a function of junction temperature



Fig. 8. Normalized latching current as a function of junction temperature



Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 1.13 \text{ V}$   
 $R_s = 0.31 \Omega$   
 (1)  $T_j = 125^{\circ}\text{C}$ ; typical values  
 (2)  $T_j = 125^{\circ}\text{C}$ ; maximum values  
 (3)  $T_j = 25^{\circ}\text{C}$ ; maximum values

Fig. 10. On-state current as a function of on-state voltage





Fig. 11. Normalized gate trigger voltage as a function of junction temperature



$$A = \frac{dV_D(T_j \text{ } ^\circ\text{C}) / dt}{dV_D(25 \text{ } ^\circ\text{C}) / dt}$$

Fig. 12. Normalized critical rate of rise of off-state voltage as a function of junction temperature; typical values

### 10. Package outline



**Fig. 13. Package outline TO-92 (SOT54)**

# 11. Legal information

## Data sheet status

| Document status [1][2]         | Product status [3] | Definition  |
|--------------------------------|--------------------|---|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
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