WM8524

24-bit 192kHz Stereo DAC with 2Vrms Ground Referenced Line Output

DESCRIPTION

The WM8524 is a stereo DAC with integral charge pump and hardware control interface. This provides 2Vrms line driver outputs using a single 3.3V power supply rail.

The device features ground-referenced outputs and the use of a DC servo to eliminate the need for line driving coupling capacitors and effectively eliminate power on pops and clicks.

The device is controlled and configured via a hardware control interface.

The device supports all common audio sampling rates between 8kHz and 192kHz using all common MCLK fs rates. The audio interface operates in slave mode.

The WM8524 has a 3.3V tolerant digital interface, allowing logic up to 3.3V to be connected.

The device is available in a 16-pin TSSOP.

FEATURES

- High performance stereo DAC with ground referenced line driver
- Audio Performance
    - 106dB SNR ('A-weighted')
    - -89dB THD @ -1dBFS
- 120dB mute attenuation
- All common sample rates from 8kHz to 192kHz supported
- Hardware control mode
- Data formats: LJ, RJ, I²S
- Maximum 1mV DC offset on Line Outputs
- Pop/Click suppressed Power Up/Down Sequencer
- AVDD and LINEVDD +3.3V ±10% allowing single supply
- 16-lead TSSOP package
- Operating temperature range: -40°C to 85°C

APPLICATIONS

- Consumer digital audio applications requiring 2Vrms output
    - Games Consoles
    - Set Top Box
    - A/V Receivers
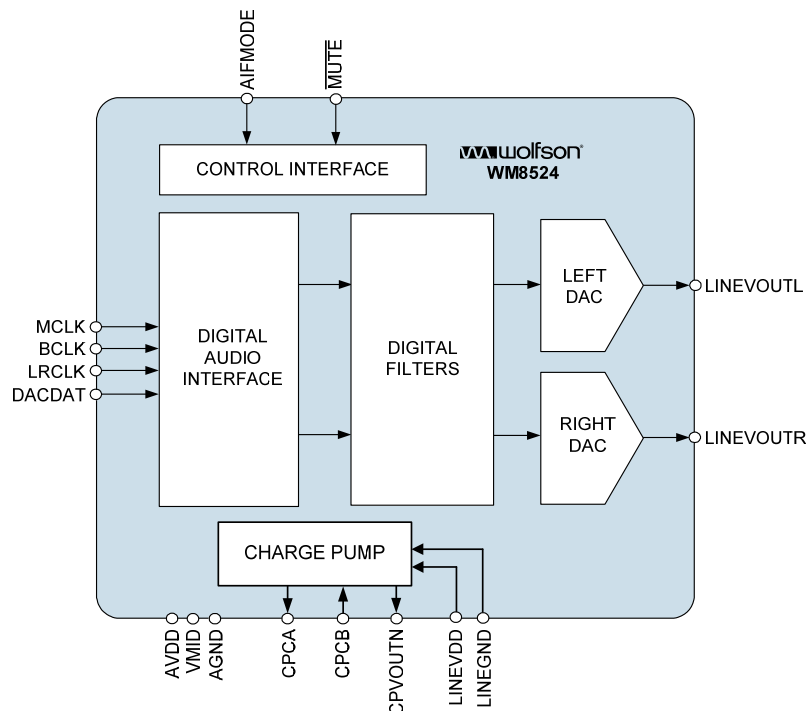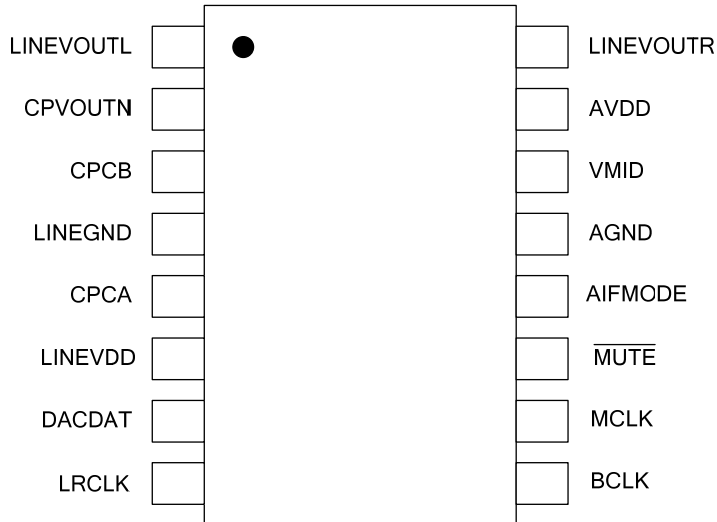   - DVD Players
    - Digital TV

BLOCK DIAGRAM

TABLE OF CONTENTS

PIN CONFIGURATION

LINEVOUTL	●	LINEVOUTR
CPVOUTN		AVDD
CPCB		VMID
LINEGND		AGND
CPCA		AIFMODE
LINEVDD		$\overline{\text{MUTE}}$
DACDAT		MCLK
LRCLK		BCLK

ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8524CGEDT	−40°C to +85°C	16 lead TSSOP (Pb-free)	MSL1	260°C
WM8524CGEDT/R	−40°C to +85°C	16-lead TSSOP (Pb-free, tape and reel)	MSL1	260°C

Note:

Reel quantity = 2000

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	LINEVOUTL	Analogue Out	Left line output
2	CPVOUTN	Analogue Out	Charge Pump negative rail decoupling pin
3	CPCB	Analogue Out	Charge Pump fly back capacitor pin
4	LINEGND	Supply	Charge Pump ground
5	CPCA	Analogue Out	Charge Pump fly back capacitor pin
6	LINEVDD	Supply	Charge Pump supply
7	DACDAT	Digital In	Digital audio interface data input
8	LRCLK	Digital In	Digital audio interface left/right clock
9	BCLK	Digital In	Digital audio interface bit clock
10	MCLK	Digital In	Master clock
11	$\overline{\text{MUTE}}$	Digital In	0 = Mute enabled 1 = Mute disabled
12	AIFMODE	Digital In Tri-level	0 = 24-bit Left Justified 1 = 24-bit I^{2}S Z = 24-bit Right Justified
13	AGND	Supply	Analogue ground
14	VMID	Analogue Out	Analogue midrail decoupling pin
15	AVDD	Supply	Analogue supply
16	LINEVOUTR	Analogue Out	Right line output

Note: Tri-level pins which require the 'Z' state to be selected should be left floating (open)

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
AVDD, LINEVDD	-0.3V	+4.5V
Voltage range digital inputs	LINEGND -0.3V	LINEVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Temperature range, T_A	-40°C	+125°C
Storage temperature after soldering	-65°C	+150°C

Notes:

1. Analogue grounds must always be within 0.3V of each other.

2. LINEVDD and AVDD must always be within 0.3V of each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue supply range	AVDD, LINEVDD		2.97	3.3	3.63	V
Ground	AGND, LINEGND			0		V

ELECTRICAL CHARACTERISTICS

Test Conditions

LINEVDD=AVDD=3.3V, LINEGND=AGND=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Output Levels						
Output Level		0dBFS	1.89	2.1	2.31	Vrms
Load Impedance			1			kΩ
Load Capacitance		No external RC filter			300	pF
		With filter shown in Figure 16			1	µF
DAC Performance						
Signal to Noise Ratio	SNR	R_L = 10kΩ A-weighted		106		dB
		R_L = 10kΩ Un-weighted		104		dB
Dynamic Range	DNR	R_L = 10kΩ A-weighted		104		dB
Total Harmonic Distortion	THD	-1dBFS		-89		dB
		0dBFS		-86		dB
AVDD + LINEVDD Power Supply Rejection Ratio	PSRR	100Hz		54		dB
		1kHz		54		dB
		20kHz		50		dB
Channel Separation		1kHz		100		dB
		20Hz to 20kHz		95		dB
System Absolute Phase				0		degrees
Channel Level Matching				0.1		dB
Mute Attenuation				-120		dB
DC Offset at LINEVOUTL and LINEVOUTR			-1	0	1	mV
Digital Logic Levels						
Input HIGH Level	V_{IH}		0.7× LINEVDD			V
Input LOW Level	V_{IL}				0.3× LINEVDD	V
Input Capacitance				10		pF
Input Leakage			-0.9		0.9	µA

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum theoretical full scale output signal and the output with no input signal applied.

2. Total Harmonic Distortion (dB) – THD is the level of the rms value of the sum of harmonic distortion products relative to the amplitude of the measured output signal.

3. All performance measurements carried out with 20kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.

4. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.

POWER CONSUMPTION MEASUREMENTS

Test Conditions LINEVDD=AVDD=3.3V, LINEGND=AGND=0V, T_A=+25°C, Slave Mode, quiescent (no signal)				
	TEST CONDITIONS	**IAVDD (mA)**	**ILINEVDD (mA)**	**TOTAL (mA)**
Off	No clocks applied	0.8	1.1	1.9
fs=48kHz, MCLK=256fs				
Standby	$\overline{\text{MUTE}}$ = 0	0.2	2.2	2.4
Playback	$\overline{\text{MUTE}}$ = 1	4.8	6.0	10.8
fs=96kHz, MCLK=256fs				
Standby	$\overline{\text{MUTE}}$ = 0	0.2	2.9	3.1
Playback	$\overline{\text{MUTE}}$ = 1	5.5	8.5	14.0
fs=192kHz, MCLK=128fs				
Standby	$\overline{\text{MUTE}}$ = 0	0.2	2.9	3.1
Playback	$\overline{\text{MUTE}}$ = 1	5.5	8.5	14.0

SIGNAL TIMING REQUIREMENTS
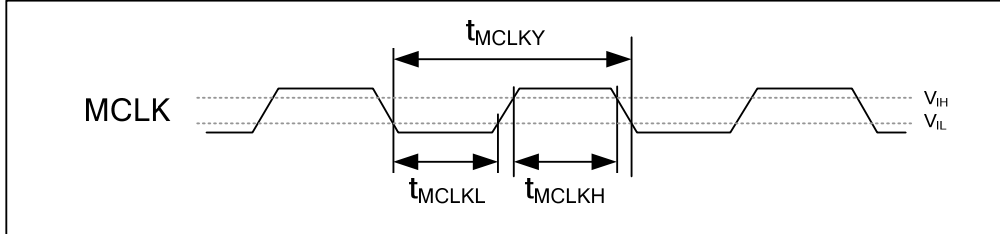
SYSTEM CLOCK TIMING

Figure 1 System Clock Timing Requirements

Test Conditions

LINEVDD=AVDD=2.97~3.63V, LINEGND=AGND=0V, T_A=+25°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Master Clock Timing Information					
MCLK cycle time	t_{MCLKY}	27		500	ns
MCLK high time	t_{MCLKH}	11			ns
MCLK low time	t_{MCLKL}	11			ns
MCLK duty cycle (t_{MCLKH}/t_{MCLKL})		40:60		60:40	%

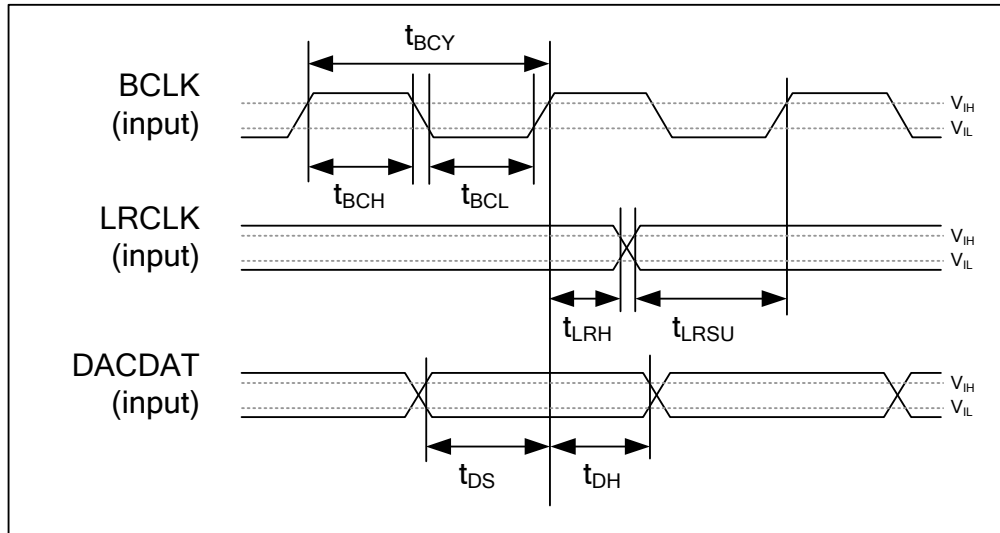## AUDIO INTERFACE TIMING – SLAVE MODE

Figure 2 Digital Audio Data Timing – Slave Mode

Test Conditions

LINEVDD=AVDD=2.97~3.63V, LINEGND=AGND=0V, T_A=+25°C, Slave Mode

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	27			ns
BCLK pulse width high	t_{BCH}	11			ns
BCLK pulse width low	t_{BCL}	11			ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}	7			ns
LRCLK hold time from BCLK rising edge	t_{LRH}	5			ns
DACDAT hold time from LRCLK rising edge	t_{DH}	5			ns
DACDAT set-up time to BCLK rising edge	t_{DS}	7			ns

Table 1 Slave Mode Audio Interface Timing

Note:

BCLK period should always be greater than or equal to MCLK period.
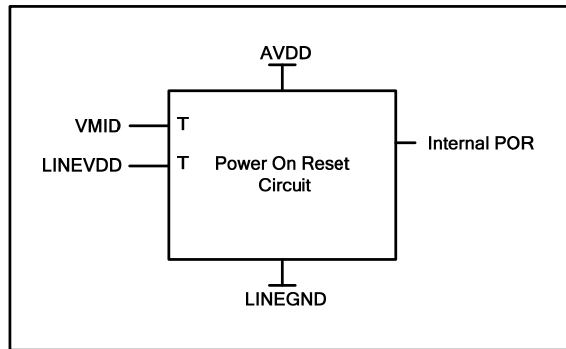
POWER ON RESET CIRCUIT

Figure 3 Internal Power on Reset Circuit Schematic

The WM8524 includes an internal Power-On-Reset circuit, as shown in Figure 3, which is used to reset the DAC digital logic into a default state after power up. The POR circuit is powered by AVDD and has as its inputs VMID and LINEVDD. It asserts POR low if VMID or LINEVDD are below a minimum threshold.
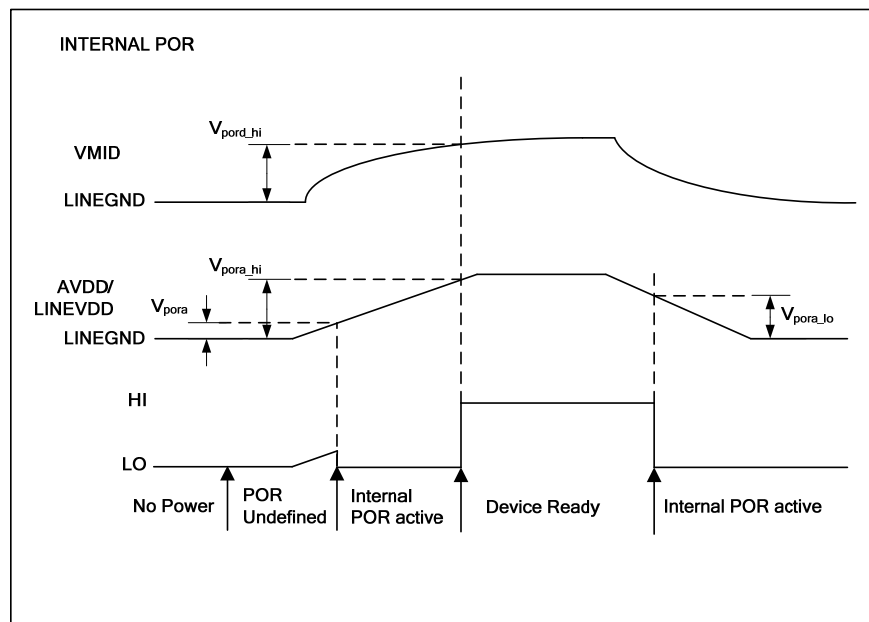

Figure 4 Typical Power Timing Requirements

Figure 4 shows a typical power-up sequence where LINEVDD comes up with AVDD. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee POR is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. After VMID rises to V_{pord_hi} and AVDD rises to $V_{pora\_hi,}$ POR is released high and all registers are in their default state and writes to the control interface may take place.

On power down, PORB is asserted low whenever LINEVDD or AVDD drop below the minimum threshold V_{pora_low}.

Test Conditions

LINEVDD = AVDD = 3.3V   AGND = LINEGND = 0V, T_A = +25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Input Timing Information						
VDD level to POR defined (LINEVDD/AVDD rising)	V_{pora}	Measured from LINEGND		158		mV
VDD level to POR rising edge (VMID rising)	V_{pord_hi}	Measured from LINEGND	0.63	0.8	1	V
VDD level to POR rising edge (LINEVDD/AVDD rising)	V_{pora_hi}	Measured from LINEGND	1.44	1.8	2.18	V
VDD level to POR falling edge (LINEVDD/AVDD falling)	V_{pora_lo}	Measured from LINEGND	0.96	1.46	1.97	V

Table 2 Power on Reset

Note: All values are simulated results

DEVICE DESCRIPTION

INTRODUCTION

The WM8524 provides high fidelity, 2Vrms ground referenced stereo line output from a single supply line with minimal external components. The integrated DC servo eliminates the requirement for external mute circuitry by minimising DC transients at the output during power up/down. The device is well-suited to both stereo and multi-channel systems.

The device supports all common audio sampling rates between 8kHz and 192kHz using common MCLK fs rates, with a slave mode audio interface.

The WM8524 supports a simple hardware control mode, allowing access to 24-bit LJ, RJ and I2S audio interface formats, as well as a mute control. An internal audio interface clock monitor automatically mutes the DAC output if the BCLK is interrupted.

DIGITAL AUDIO INTERFACE

The digital audio interface is used for inputting audio data to the WM8524. The digital audio interface uses three pins:

- DACDAT: DAC data input
- LRCLK: Left/Right data alignment clock
- BCLK: Bit clock, for synchronisation

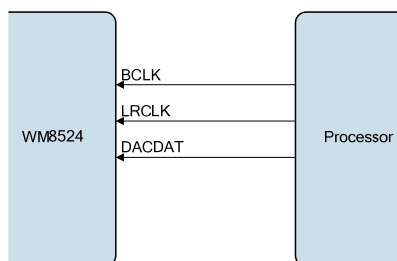The WM8524 digital audio interface operates as a slave as shown in Figure 5.

Figure 5 Slave Mode

INTERFACE FORMATS

The WM8524 supports three different audio data formats:

- Left justified
- Right justified
- I²S

All three of these modes are MSB first. They are described in Audio Data Formats on page 13. Refer to the "Electrical Characteristics" section for timing information.

AUDIO DATA FORMATS

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a LRCLK transition.   All other bits are transmitted before (MSB first).   Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition.
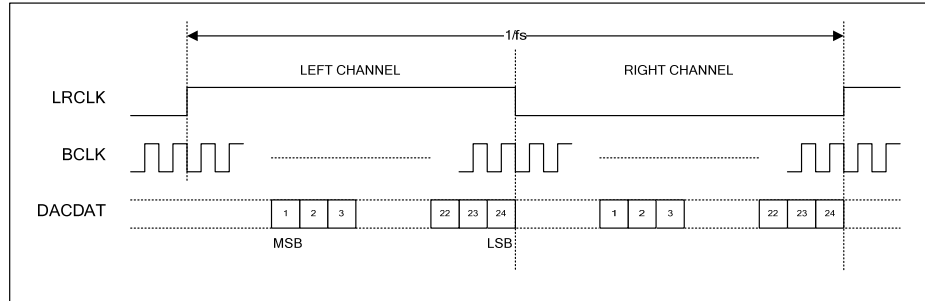

Figure 6 Right Justified Audio Interface (24-bit word length)

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCLK transition.   The other bits up to the LSB are then transmitted in order.   Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.
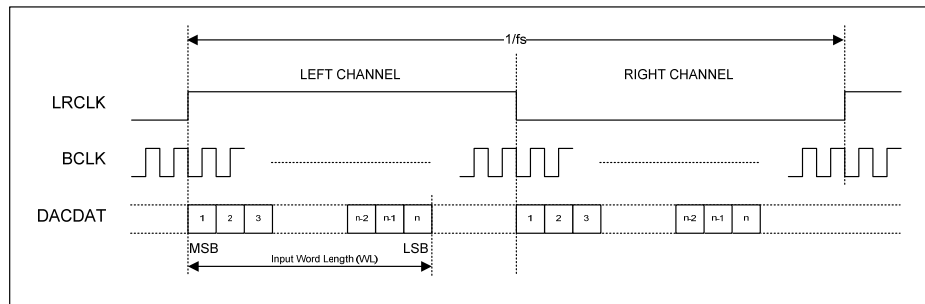

Figure 7 Left Justified Audio Interface (assuming n-bit word length)

In I^{2}S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order.   Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.
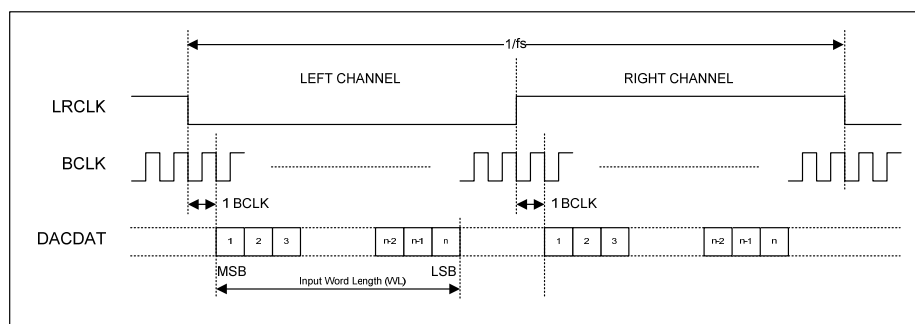
Figure 8 I^{2}S Justified Audio Interface (assuming n-bit word length)

DIGITAL AUDIO DATA SAMPLING RATES

The external master clock is applied directly to the MCLK input pin. In a system where there are a number of possible sources for the reference clock, it is recommended that the clock source with the lowest jitter be used for the master clock to optimise the performance of the WM8524.

The WM8524 has a detection circuit that automatically determines the relationship between the master clock frequency (MCLK) and the sampling rate (LRCLK), to within ±32 system clock periods. The MCLK must be synchronised with the LRCLK, although the device is tolerant of phase variations or jitter on the MCLK.

If during sample rate change the ratio between MCLK and LRCLK varies more than once within 1026 LRCLK periods, then it is recommended that the device be taken into the standby state or the off state before the sample rate change and held in standby until the sample rate change is complete. This will ensure correct operation of the detection circuit on the return to the enabled state. For details on the standby state, please refer to the Power up and down control section of the datasheet on page 16.

The DAC supports MCLK to LRCLK ratios of 128fs to 1152fs and sampling rates of 8kHz to 192kHz.

Table 3 shows typical master clock frequencies and sampling rates supported by the WM8524 DAC.

Sampling Rate LRCLK	MASTER CLOCK FREQUENCY (MHz)						
	128fs	**192fs**	**256fs**	**384fs**	**512fs**	**768fs**	**1152fs**
8kHz	Unavailable	Unavailable	2.048	3.072	4.096	6.144	9.216
32kHz	Unavailable	Unavailable	8.192	12.288	16.384	24.576	36.864
44.1kHz	Unavailable	Unavailable	11.2896	16.9344	22.5792	33.8688	Unavailable
48kHz	Unavailable	Unavailable	12.288	18.432	24.576	36.864	Unavailable
88.2kHz	11.2896	16.9344	22.5792	33.8688	Unavailable	Unavailable	Unavailable
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable	Unavailable
176.4kHz	22.5792	33.8688	Unavailable	Unavailable	Unavailable	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable	Unavailable

Table 3 MCLK Frequencies and Audio Sample Rates

HARDWARE CONTROL INTERFACE

The device is configured according to logic levels applied to the hardware control pins as described in Table 4.

PIN NAME	PIN NUMBER	DESCRIPTION
$\overline{\text{MUTE}}$	11	**Mute Control** 0 = Mute 1 = Normal operation
AIFMODE	12	**Audio Interface Mode** 0 = 24-bit LJ 1 = 24-bit I^{2}S Z = 24-bit RJ

Table 4 Hardware Control Pin Configuration

MUTE

The $\overline{\text{MUTE}}$ pin controls the DAC mute to both left and right channels. When the mute is asserted a softmute is applied to ramp the signal down in 800 samples. When the mute is de-asserted the signal returns to full scale in one step.

POWER UP AND DOWN CONTROL

The MCLK, BCLK and $\overline{\text{MUTE}}$ pins are monitored to control how the device powers up or down, and this is summarised in Figure 9 below.
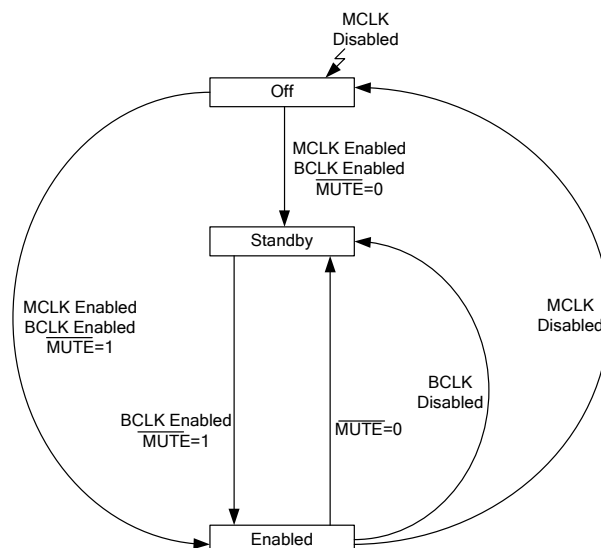

Figure 9 Hardware Power Sequence Diagram

Off to Enable

To power up the device to enabled, start MCLK and BCLK and set $\overline{\text{MUTE}}$ = 1.

Off to Standby

To power up the device to standby, start MCLK and BCLK and set $\overline{\text{MUTE}}$ = 0. Once the device is in standby mode, BCLK can be disabled and the device will remain in standby mode.

Standby to Enable

To transition from the standby state to the enabled state, set the $\overline{\text{MUTE}}$ pin to logic 1 and start BCLK.

Enable to Standby

To power down to a standby state leaving the charge pump running, either set the $\overline{\text{MUTE}}$ pin to logic 0 or stop BCLK. MCLK must continue to run in these situations. The device will automatically mute and power down quietly in either case.

Note: It is recommended that the device is placed in standby mode before sample rate change if the sample rate changes more than once in 1026 LRCLK periods, as detailed in Digital Audio Data Sampling Rates on page 14.

Enable to Off

To power down the device completely, stop MCLK at any time. It is recommended that the device is placed into standby mode as described above before stopping MCLK to allow a quiet shutdown.

For the timing of the off state to enabled state transition (power on to audio out timing), and the enabled state to standby state transition (the shutdown timing), please refer to WTN0302.
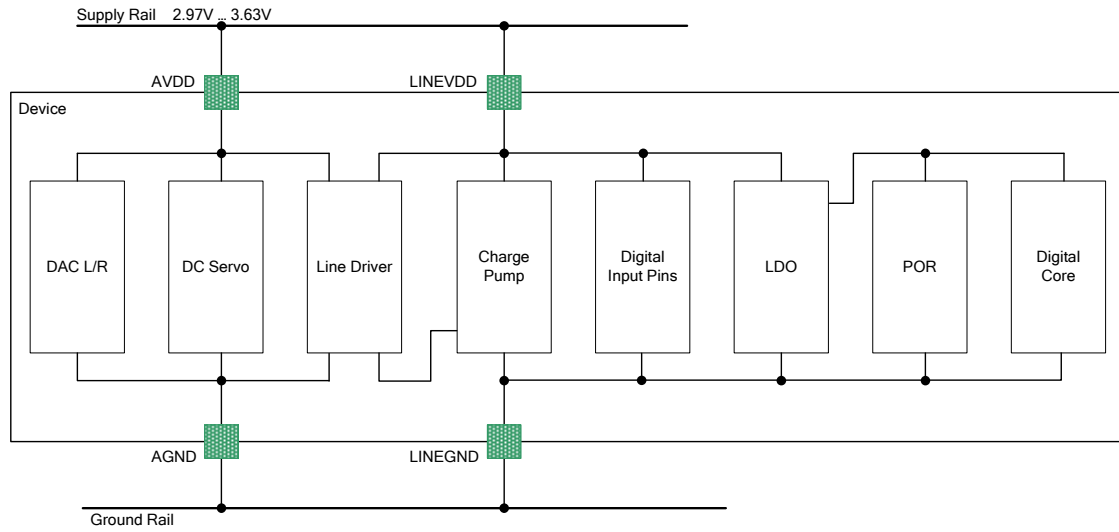
POWER DOMAINS

Figure 10 Power Domain Diagram

POWER DOMAIN	NAME	BLOCKS USING THIS DOMAIN	DOMAIN DESCRIPTION
DAC Power Supplies			
3.3V ± 10%	AVDD	Line Driver DAC DC Servo	Analogue Supply
3.3V ± 10%	LINEVDD	Charge Pump Digital LDO Digital Pad buffers	Analogue Supply
Internally Generated Power Supplies and References			
1.65V ± 10%	VMID	DAC, LDO	Ext decoupled resistor string
-3.3V ± 10%	CPVOUTN	Line Driver	Charge pump generated voltage

Table 5 Power Domains

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC Filter – 256fs to 1152fs					
Passband	± 0.1dB			0.454fs	
Passband Ripple				0.1	dB
Stopband		0.546fs			
Stopband attenuation	f > 0.546fs	-50			dB
Group Delay			10		Fs
DAC Filter – 128fs and 192fs					
Passband	± 0.1dB			0.247fs	
Passband Ripple				0.1	dB
Stopband		0.753fs			
Stopband attenuation	f > 0.753fs	-50			dB
Group Delay			10		Fs

TERMINOLOGY

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)

2. Pass-band Ripple – any variation of the frequency response in the pass-band region
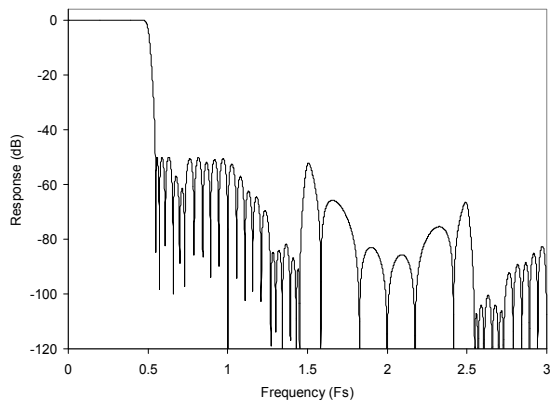
DAC FILTER RESPONSES

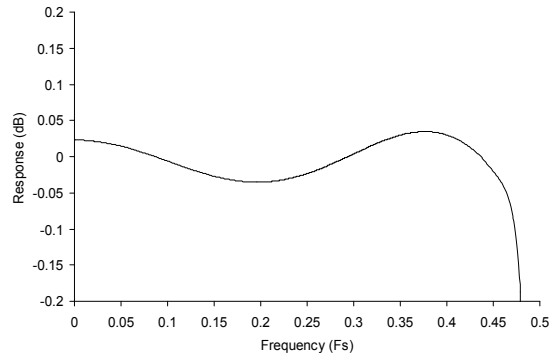**Figure 11 DAC Digital Filter Frequency Response
– 256fs to 1152fs Clock Modes**

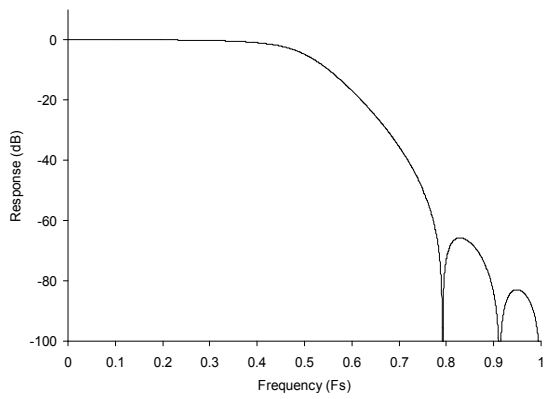**Figure 12 DAC Digital Filter Ripple – 256fs to 1152fs Clock
Modes**

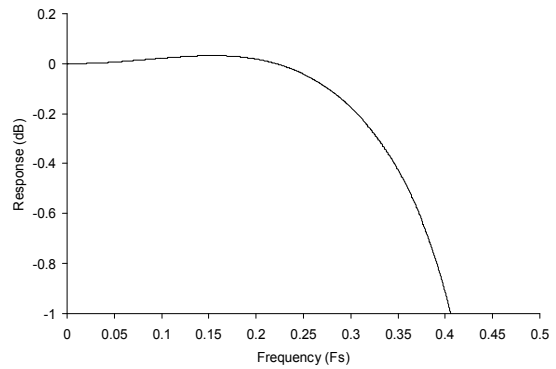**Figure 13 DAC Digital Filter Frequency Response
– 128fs and 192fs Clock Modes**

**Figure 14 DAC Digital Filter Ripple – 128fs to 192fs Clock
Modes**

APPLICATIONS INFORMATION
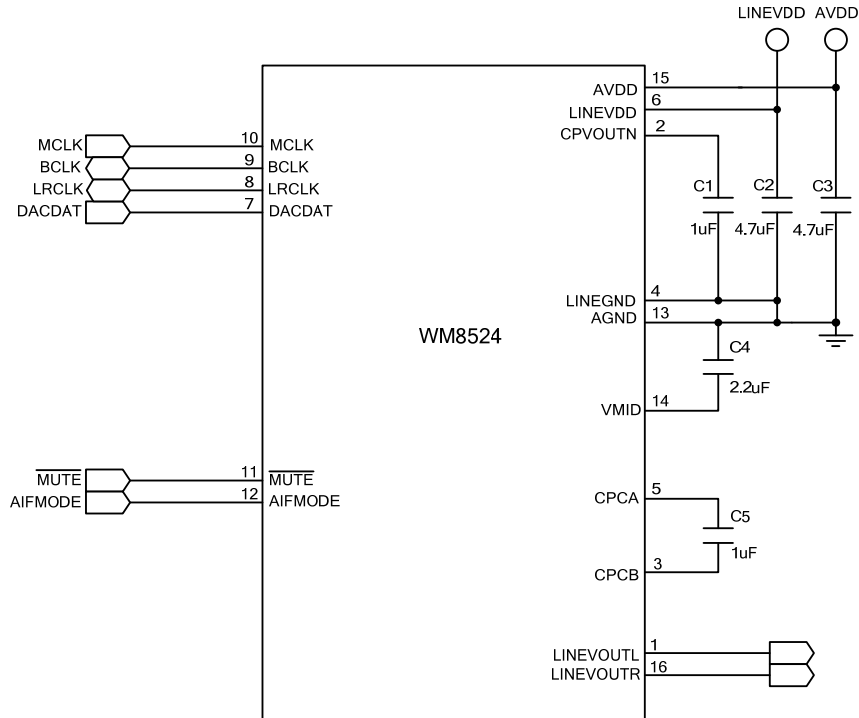
RECOMMENDED EXTERNAL COMPONENTS

Figure 15 Recommended External Components

Notes:

1. Wolfson recommend using a single, common ground plane. Where this is not possible, care should be taken to optimize split ground configuration for audio performance.

2. Charge Pump fly-back capacitor C5 should be placed as close to WM8524 as possible, followed by Charge Pump decoupling capacitor C1, then LINEVDD and VMID decoupling capacitors. See Recommended PCB Layout on p21.

3. Capacitor types should be chosen carefully. Capacitors with very low ESR are recommended for optimum performance.
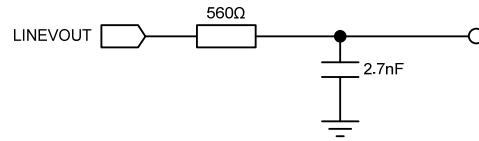
RECOMMENDED ANALOGUE LOW PASS FILTER

Figure 16 Recommended Analogue Low Pass Filter (one channel shown)

An external single-pole RC filter is recommended if the device is driving a wideband amplifier. Other filter architectures may provide equally good results.

The filter shown in Figure 16 has a -3dB cut-off at 105.26kHz and a droop of 0.15dB at 20kHz. The typical output from the WM8524 is 2.1Vrms – when a 10kΩ load is placed at the output of this recommended filter the amplitude across this load is 1.99Vrms.
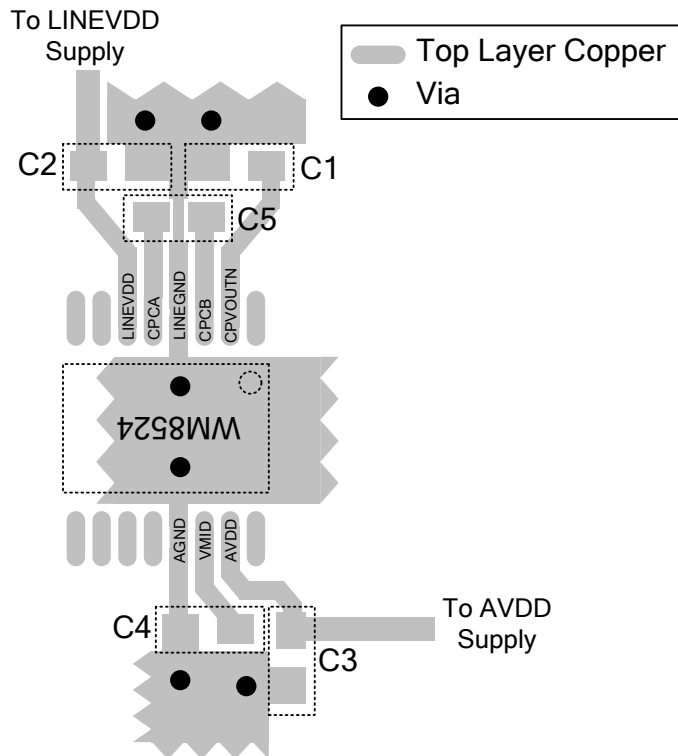
RECOMMENDED PCB LAYOUT

Figure 17 Recommended PCB Layout

Notes:

1. C5 should be placed as close to WM8524 as possible, with minimal track lengths to reduce inductance and maximise performance of the charge pump. Vias should be avoided in the tracking to C5.

2. C1 is then next most important and should also be placed as close as possible to the WM8524. Again, minimise track lengths and avoid vias to reduce parasitic inductance.

3. C2 and C4 are then next most important, and lastly C3.

4. The WM8524 evaluation board, details available at www.wolfsonmicro.com, shows an example of good component placement and layout to maximise performance with a minimal BOM.

RELEVANT APPLICATION NOTES

The following application notes, available from www.wolfsonmicro.com, may provide additional guidance for use of the WM8524.

DEVICE PERFORMANCE:

WTN0302 – WM8524 Recommended Power Sequence and Timing

WAN0129 – Decoupling and Layout Methodology for Wolfson DACs, ADCs and CODECs

WAN0144 – Using Wolfson Audio DACs and CODECs with Noisy Supplies
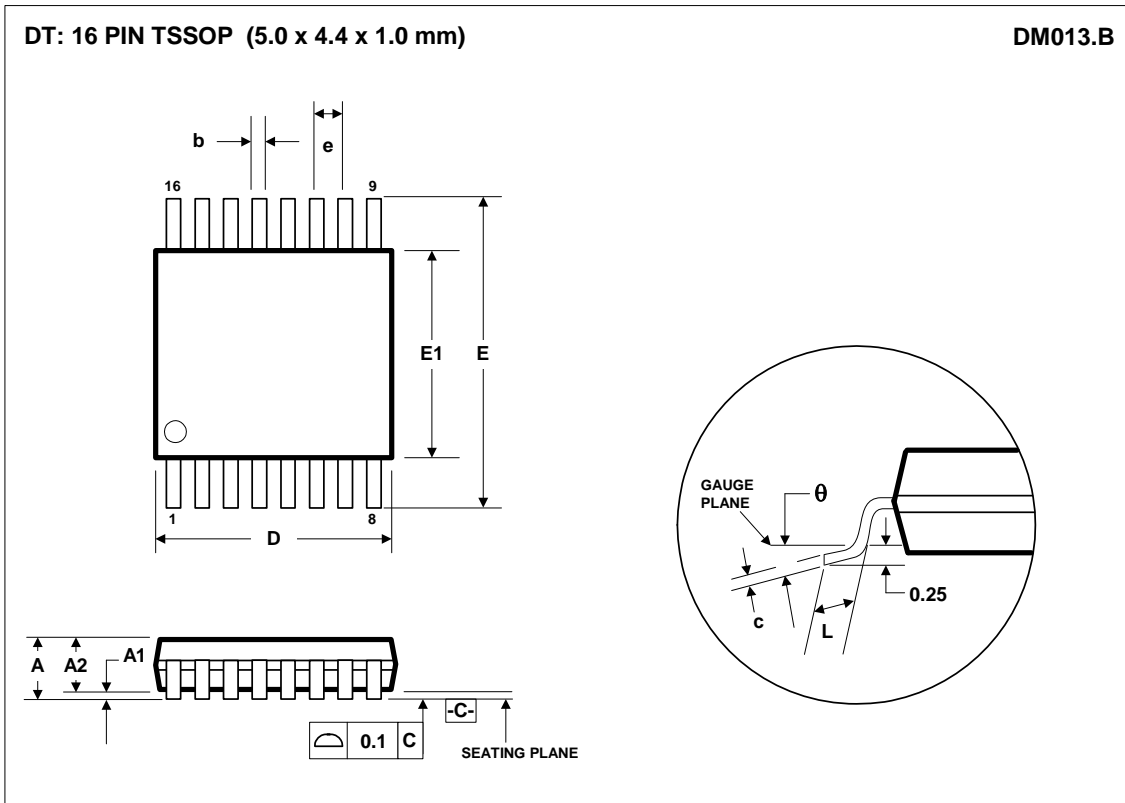
GENERAL:

WAN0108 – Moisture Sensitivity Classification and Plastic IC Packaging

WAN0109 – ESD Damage in Integrated Circuits: Causes and Prevention

WAN0158 – Lead-Free Solder Profiles for Lead-Free Components

WAN0161 – Electronic End-Product Design for ESD

PACKAGE DIMENSIONS

DT: 16 PIN TSSOP (5.0 x 4.4 x 1.0 mm)   **DM013.B**

Symbols	Dimensions (mm)		
	MIN	**NOM**	**MAX**
A	-----	-----	1.20
A$_1$	0.05	-----	0.15
A$_2$	0.80	1.00	1.05
b	0.19	-----	0.30
c	0.09	-----	0.20
D	4.90	5.00	5.10
e	0.65 BSC		
E	6.4 BSC		
E$_1$	4.30	4.40	4.50
L	0.45	0.60	0.75
θ	0°	-----	8°
REF:	JEDEC.95, MO-153		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MO-153, VARIATION = AB. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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REVISION HISTORY

DATE	REV	ORIGINATOR	CHANGES
25/10/11	4.1	JMacD	Order codes changed from WM8524GEDT and WM8524GEDT/R to WM8524CGEDT and WM8524CGEDT/R to reflect change to copper wire bonding.

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