# CSD25402Q3A –20 V P-Channel NexFET™ Power MOSFET

## 1 Features

- Ultra-Low $Q_g$ and $Q_{gd}$
- Low Thermal Resistance
- Low $R_{DS(on)}$
- Pb and Halogen Free
- RoHS Compliant
- SON 3.3 mm × 3.3 mm Plastic Package

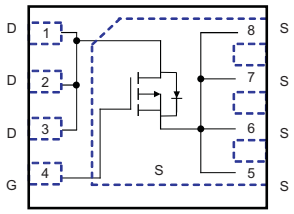
## 2 Applications

- DC-DC Converters
- Battery Management
- Load Switch
- Battery Protection

## 3 Description

This –20-V, 7.7-mΩ NexFET™ power MOSFET is designed to minimize losses in power conversion load management applications with a SON 3.3 mm × 3.3 mm package that offers an excellent thermal performance for the size of the device.

**Top View**




### Product Summary

| $T_A$ = 25°C | | TYPICAL VALUE | | UNIT |
|---|---|---|---|---|
| $V_{DS}$ | Drain-to-source voltage | –20 | | V |
| $Q_g$ | Gate charge total (–4.5 V) | 7.5 | | nC |
| $Q_{gd}$ | Gate charge gate to drain | 1.1 | | nC |
| $R_{DS(on)}$ | Drain-to-source on resistance | $V_{GS}$ = –1.8 V | 74 | mΩ |
| | | $V_{GS}$ = –2.5 V | 13.3 | mΩ |
| | | $V_{GS}$ = –4.5 V | 7.7 | mΩ |
| $V_{th}$ | Threshold voltage | –0.9 | | V |

### Ordering Information(1)

| DEVICE | QTY | MEDIA | PACKAGE | SHIP |
|---|---|---|---|---|
| CSD25402Q3A | 2500 | 13-Inch Reel | SON 3.3 mm × 3.3 mm Plastic Package | Tape and Reel |
| CSD25402Q3AT | 250 | 7-Inch Reel | | |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

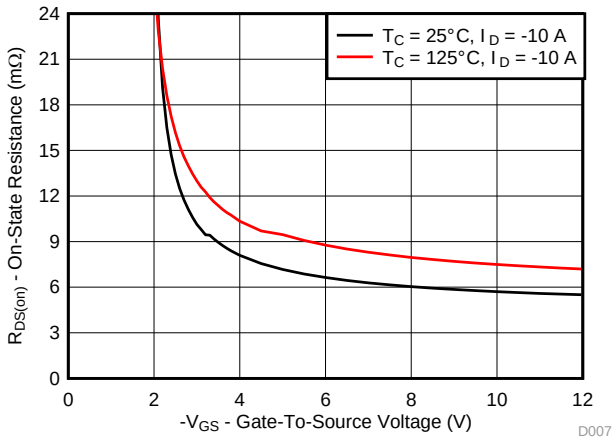
### Absolute Maximum Ratings

| $T_A$ = 25°C | | VALUE | UNIT |
|---|---|---|---|
| $V_{DS}$ | Drain-to-source voltage | –20 | V |
| $V_{GS}$ | Gate-to-source voltage | +12 or –12 | V |
| $I_D$ | Continuous drain current, $T_C$ = 25°C | –76 | A |
| | Continuous drain current (package limit) | –35 | A |
| | Continuous drain current(1) | –15 | A |
| $I_{DM}$ | Pulsed drain current(2) | –148 | A |
| $P_D$ | Power dissipation(1) | 2.8 | W |
| | Power dissipation, $T_C$ = 25°C | 69 | W |
| $T_J$ | Operating junction temperature | –55 to 150 | °C |
| $T_{stg}$ | Storage temperature | –55 to 150 | °C |

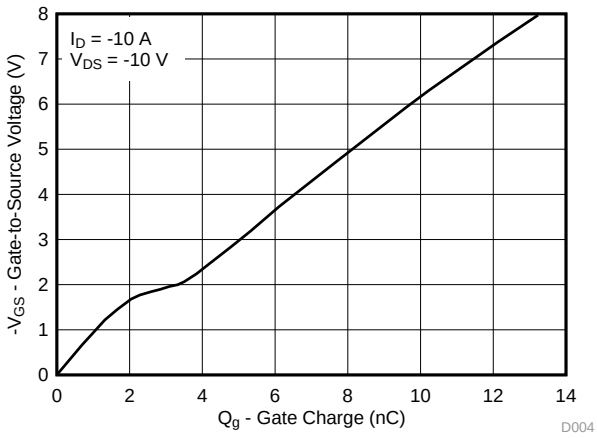
(1) Typical $R_{\theta JA}$ = 45°C/W on 1 inch$^2$ Cu (2 oz.) on 0.060 inch thick FR4 PCB.

(2) Max $R_{\theta JC}$ = 2.3°C/W, pulse duration ≤100 µs, duty cycle ≤1%

### $R_{DS(on)}$ vs $V_{GS}$




### Gate Charge



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision A (July 2015) to Revision B** **Page**

- Updated Package Dimensions drawing ... 8
- Updated PCB drawing. ... 9
- Updated Stencil Pattern drawing. ... 9

**Changes from Original (December 2013) to Revision A** **Page**

- Added part number to title. ... 1
- Added 7-inch reel to *Ordering Information* table ... 1
- Lowered typical $R_{\theta JA}$ from 55 to 45°C/W in *Absolute Maximum Ratings Table* footnote. ... 1
- Increased max pulsed current to –148 A. ... 1
- Added line for max power dissipation with the case temperature held to 25°C in *Absolute Maximum Ratings Table*. ... 1
- Updated pulsed current conditions. ... 1
- Updated Figure 1 to a normalized $R_{\theta JC}$ curve. ... 4
- Updated SOA in Figure 10 ... 6

# 5 Specifications

## 5.1 Electrical Characteristics

($T_A$ = 25°C unless otherwise stated)

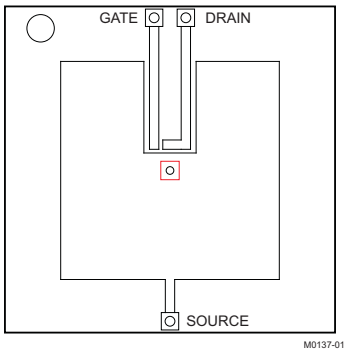
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **STATIC CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-to-source voltage | $V_{GS}$ = 0 V, $I_D$ = –250 µA | –20 | | | V |
| $I_{DSS}$ | Drain-to-source leakage current | $V_{GS}$ = 0 V, $V_{DS}$ = –16 V | | | –1 | µA |
| $I_{GSS}$ | Gate-to-source leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = ±12 V | | | –100 | nA |
| $V_{GS(th)}$ | Gate-to-source threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = –250 µA | –0.65 | –0.90 | –1.15 | V |
| $R_{DS(on)}$ | Drain-to-source on resistance | $V_{GS}$ = –1.8 V, $I_D$ = –1 A | | 74 | 300 | mΩ |
| | | $V_{GS}$ = –2.5 V, $I_D$ = –10 A | | 13.3 | 15.9 | mΩ |
| | | $V_{GS}$ = –4.5 V, $I_D$ = –10 A | | 7.7 | 8.9 | mΩ |
| $g_{fs}$ | Transconductance | $V_{DS}$ = –10 V, $I_D$ = –10 A | | 59 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{ISS}$ | Input capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = –10 V, $f$ = 1 MHz | | 1380 | 1790 | pF |
| $C_{OSS}$ | Output capacitance | | | 763 | 992 | pF |
| $C_{RSS}$ | Reverse transfer capacitance | | | 39 | 51 | pF |
| $R_G$ | Series gate resistance | | | 3.7 | 7.4 | Ω |
| $Q_g$ | Gate charge total (–4.5 V) | $V_{DS}$ = –10 V, $I_D$ = –10 A | | 7.5 | 9.7 | nC |
| $Q_{gd}$ | Gate charge gate to drain | | | 1.1 | | nC |
| $Q_{gs}$ | Gate charge gate to source | | | 2.4 | | nC |
| $Q_{g(th)}$ | Gate charge at $V_{th}$ | | | 1.0 | | nC |
| $Q_{OSS}$ | Output charge | $V_{DS}$ = –10 V, $V_{GS}$ = 0 V | | 7.6 | | nC |
| $t_{d(on)}$ | Turn on delay time | $V_{DS}$ = –10 V, $V_{GS}$ = –4.5 V, $I_D$ = –10 A , $R_G$ = 5 Ω | | 10 | | ns |
| $t_r$ | Rise time | | | 7 | | ns |
| $t_{d(off)}$ | Turn off delay time | | | 25 | | ns |
| $t_f$ | Fall time | | | 12 | | ns |
| **DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Diode forward voltage | $I_S$ = –10 A, $V_{GS}$ = 0 V | | –0.8 | –1 | V |
| $Q_{rr}$ | Reverse recovery charge | $V_{DS}$ = –8.5 V, $I_F$ = –10 A, di/dt = 200 A/µs | | 10.3 | | nC |
| $t_{rr}$ | Reverse recovery time | | | 21 | | ns |

## 5.2 Thermal Information

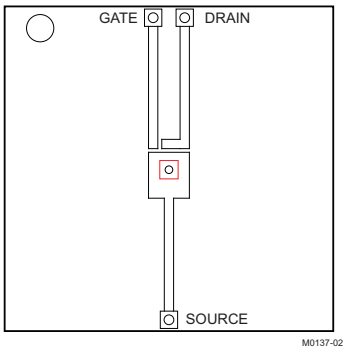
($T_A$ = 25°C unless otherwise stated)

| THERMAL METRIC | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-case thermal resistance(1) | | | 2.3 | °C/W |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance(1)(2) | | | 55 | °C/W |

(1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch$^2$ (6.45 cm$^2$), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1 inch$^2$ (6.45 cm$^2$), 2 oz. (0.071 mm thick) Cu.




Max $R_{\theta JA}$ = 55°C/W when mounted on 1 inch$^2$ of 2 oz. Cu.




Max $R_{\theta JA}$ = 175°C/W when mounted on minimum pad area of 2 oz. Cu.

## 5.3 Typical MOSFET Characteristics

($T_A$ = 25°C unless otherwise stated)

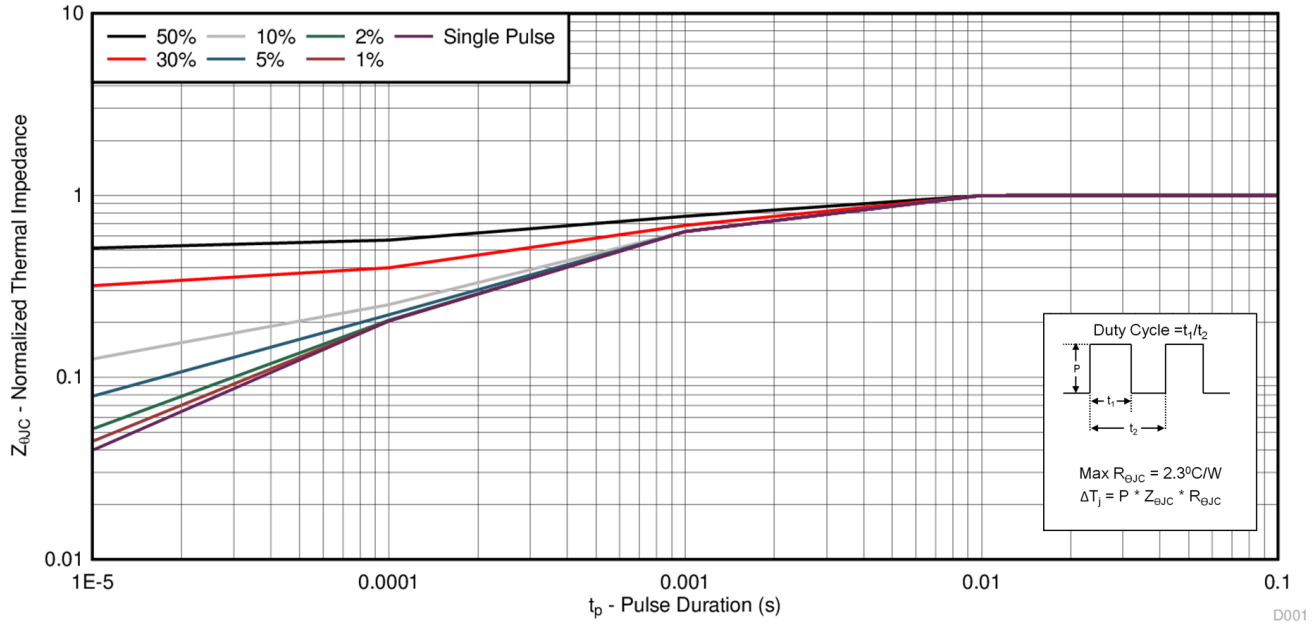



**Figure 1. Transient Thermal Impedance**

## Typical MOSFET Characteristics (continued)

($T_A$ = 25°C unless otherwise stated)

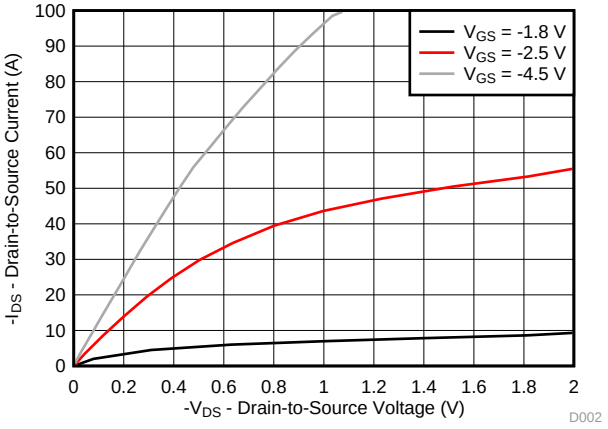
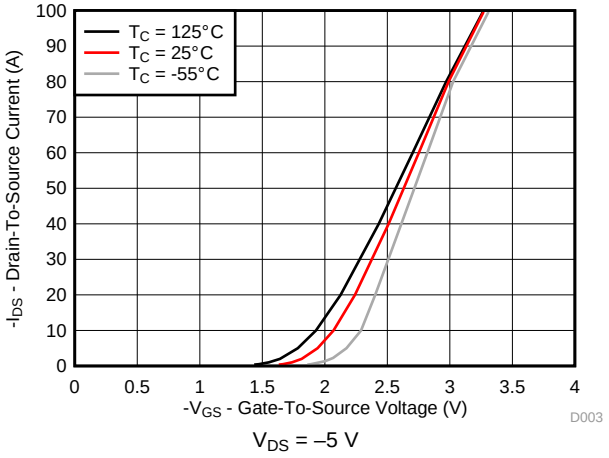
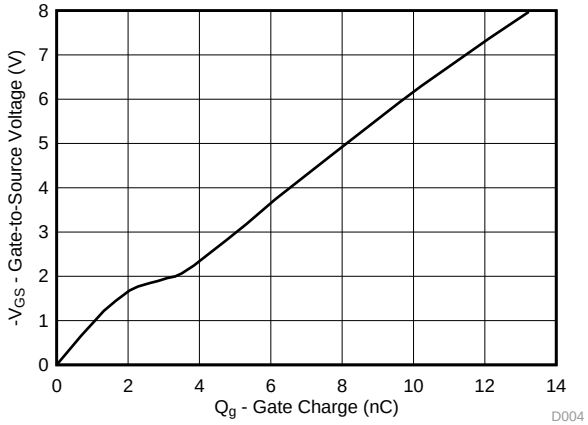



**Figure 2. Saturation Characteristics**




VDS = –5 V

**Figure 3. Transfer Characteristics**




ID = –10 A VDS = –10 V

**Figure 4. Gate Charge**

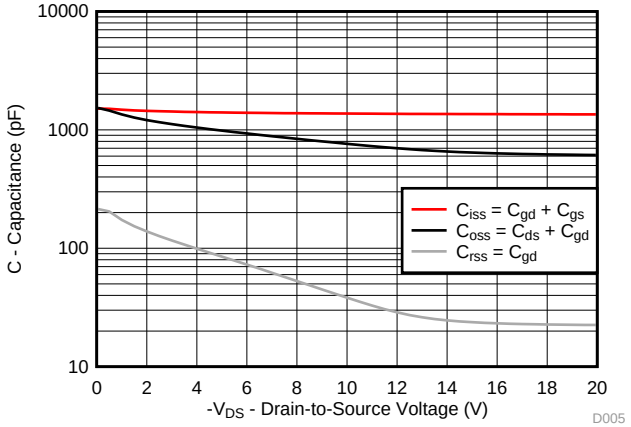
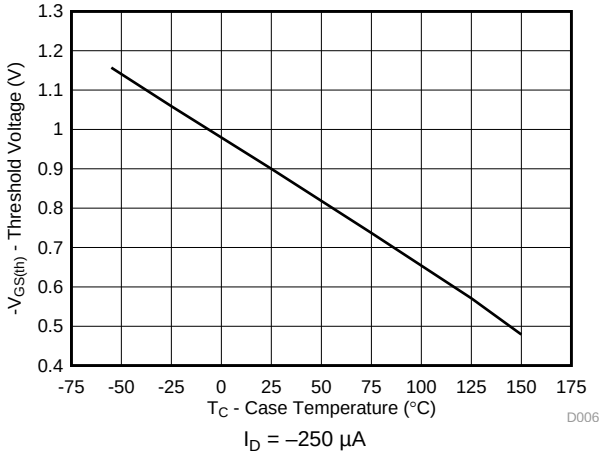



**Figure 5. Capacitance**




ID = –250 µA

**Figure 6. Threshold Voltage vs Temperature**

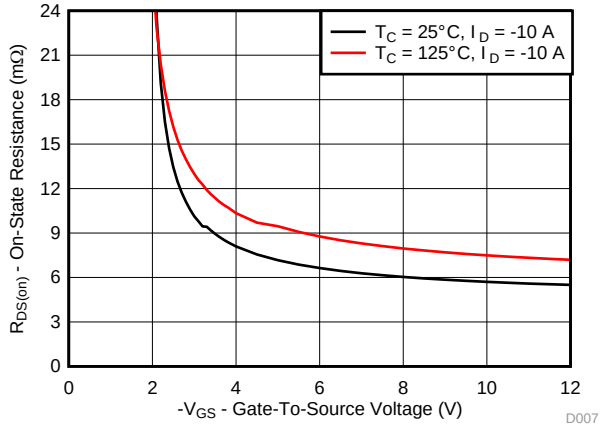
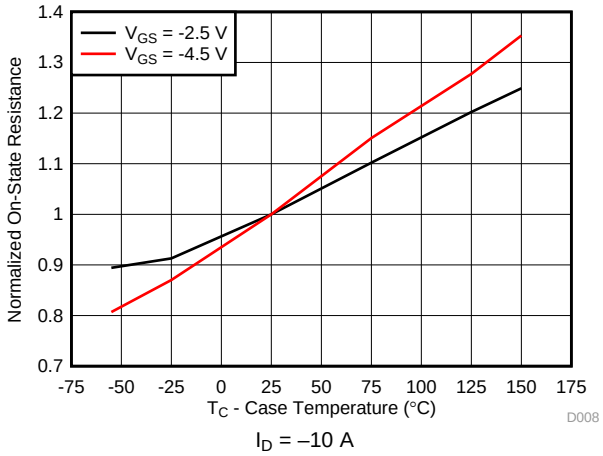



**Figure 7. On-State Resistance vs Gate-to-Source Voltage**

## Typical MOSFET Characteristics (continued)

($T_A$ = 25°C unless otherwise stated)




ID = –10 A

**Figure 8. Normalized On-State Resistance vs Temperature**

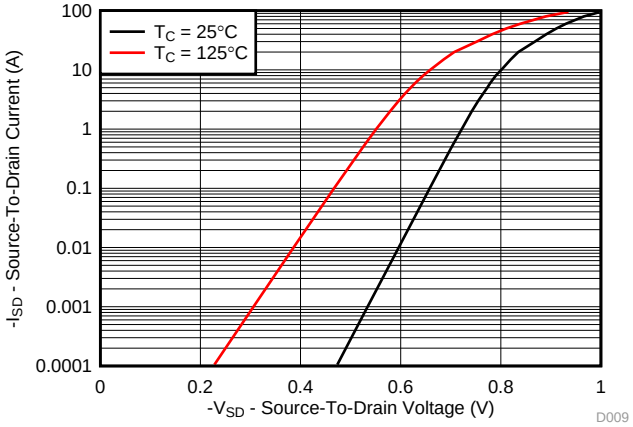
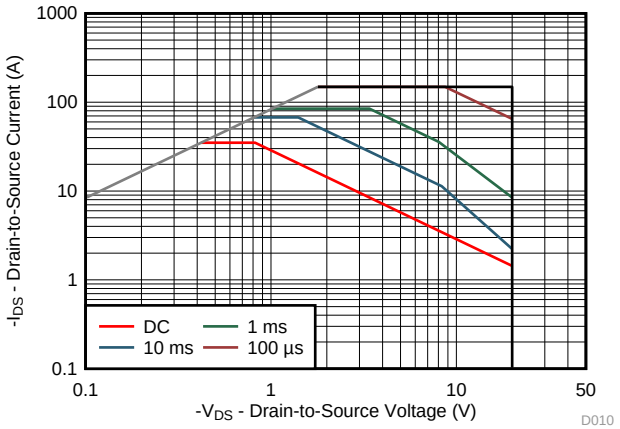



**Figure 9. Typical Diode Forward Voltage**




Single Pulse, Max $R_{\theta JC}$ = 2.3°C/W

**Figure 10. Maximum Safe Operating Area**

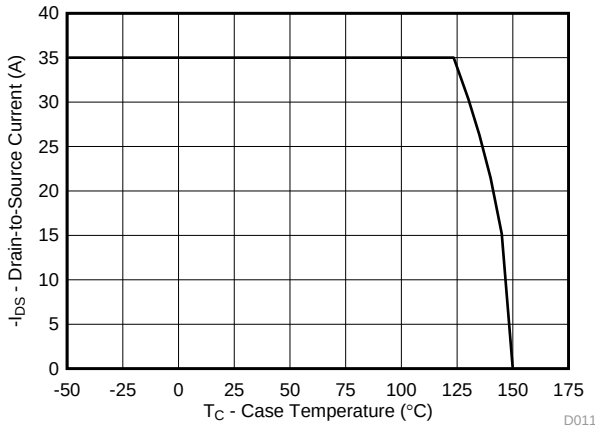



**Figure 11. Maximum Drain Current vs Temperature**

# 6 Device and Documentation Support

## 6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 6.2 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

## 6.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 6.4 Glossary

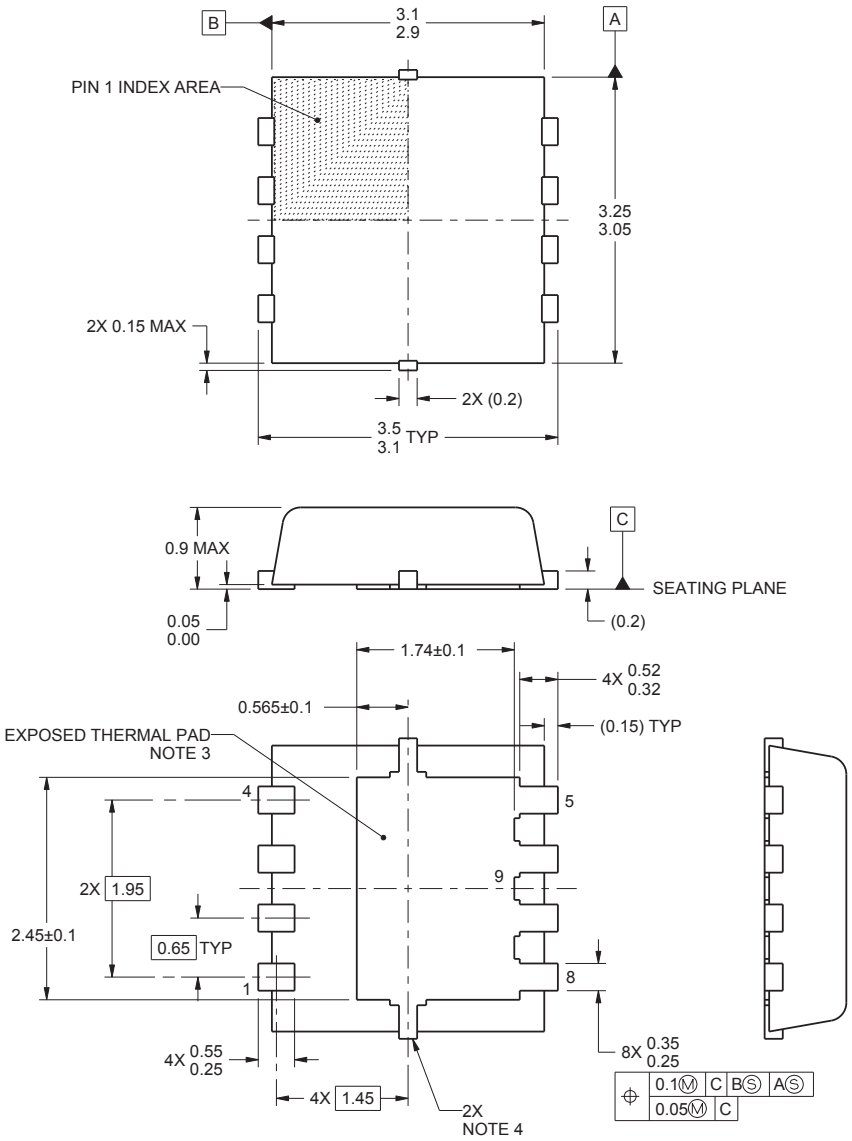
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 7 Mechanical, Packaging, and Orderable Information

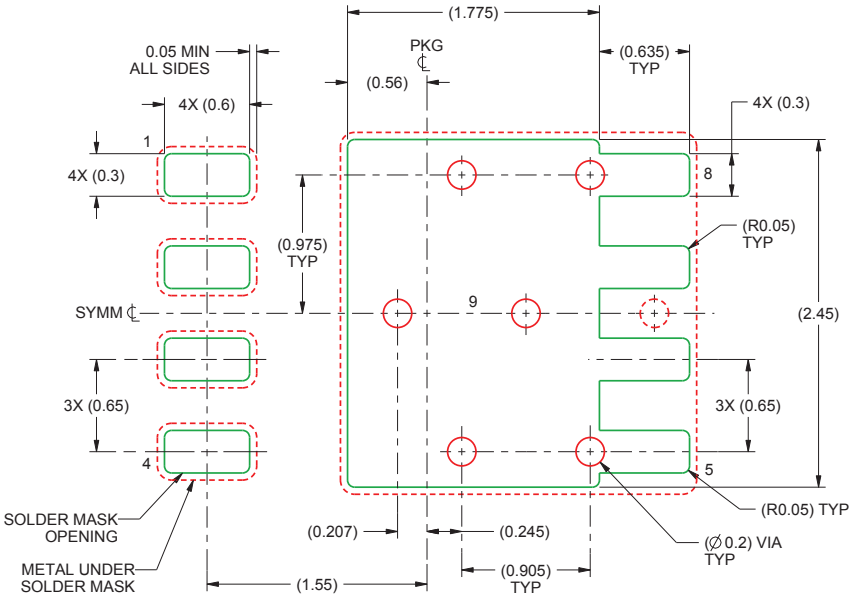
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 7.1 Q3A Package Dimensions




1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. All dimensions do not include mold flash or protrusions.

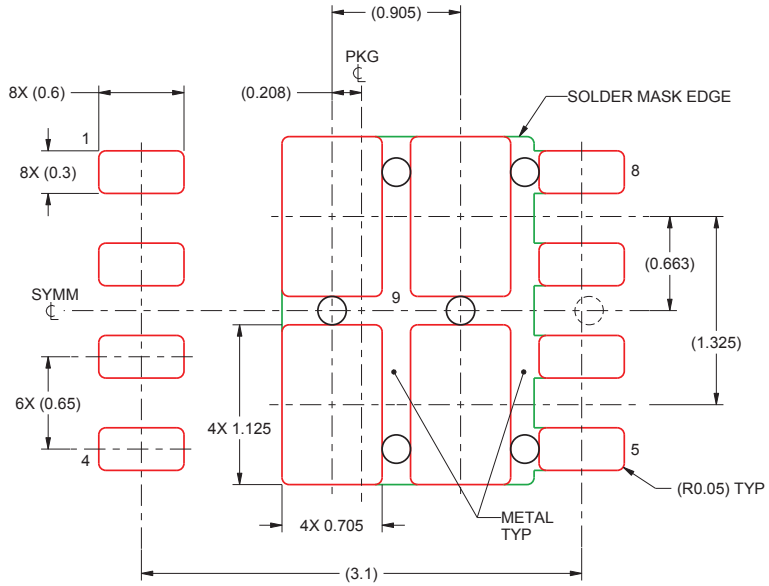
## 7.2 Q3A Recommended PCB Pattern




1. This package is designed to be soldered to a thermal pad on the board. For more information, see *QFN/SON PCB Attachment* application report, SLUA271.
2. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

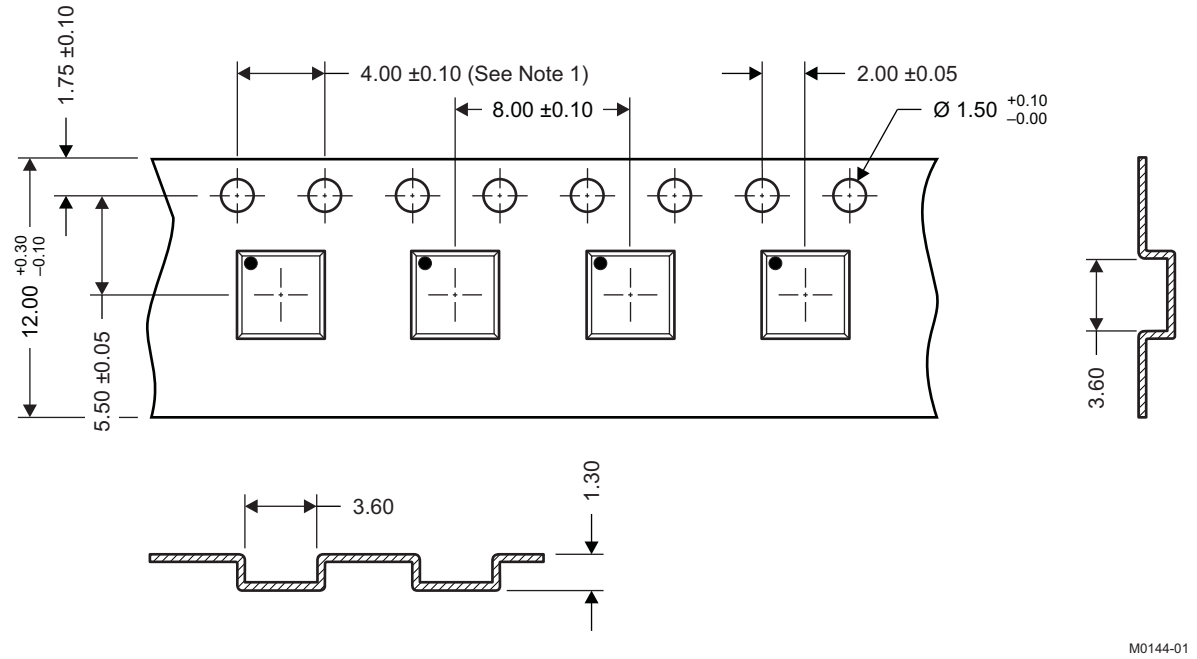
For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

## 7.3 Q3A Recommended Stencil Pattern




1. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 7.4 Q3A Tape and Reel Information




Notes:
1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm, unless otherwise specified
5. Thickness: 0.30 ±0.05 mm
6. MSL1 260°C (IR and convection) PbF reflow compatible

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CSD25402Q3A | ACTIVE | VSONP | DNH | 8 | 2500 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -55 to 150 | 25402 | Samples |
| CSD25402Q3AT | ACTIVE | VSONP | DNH | 8 | 250 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -55 to 150 | 25402 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

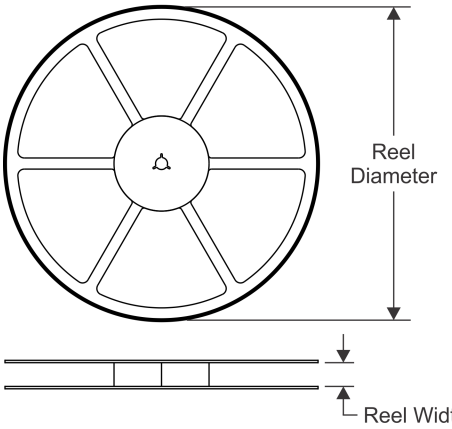
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

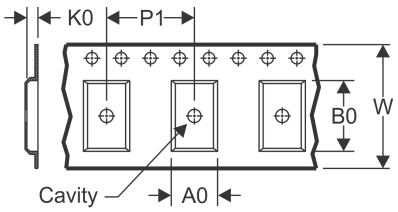
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

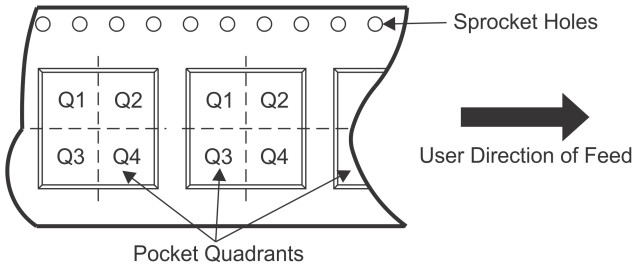



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

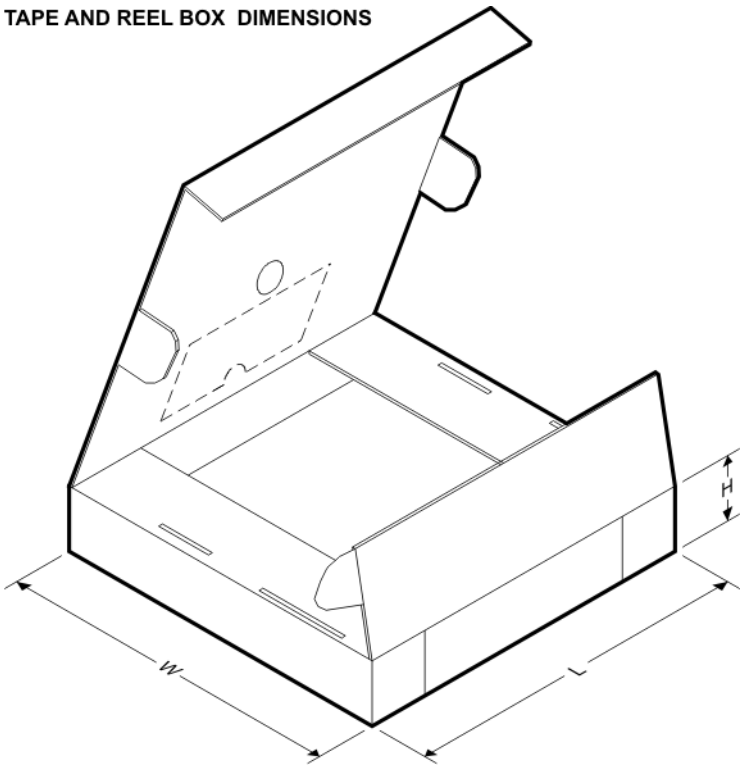
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CSD25402Q3A | VSONP | DNH | 8 | 2500 | 330.0 | 12.4 | 3.6 | 3.6 | 1.2 | 8.0 | 12.0 | Q1 |
| CSD25402Q3AT | VSONP | DNH | 8 | 250 | 180.0 | 12.4 | 3.6 | 3.6 | 1.2 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CSD25402Q3A | VSONP | DNH | 8 | 2500 | 340.0 | 340.0 | 38.0 |
| CSD25402Q3AT | VSONP | DNH | 8 | 250 | 190.0 | 190.0 | 30.0 |

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