SN54HC191-DIE 4-Bit Synchronous Up/Down Binary Counter

1 Features

- Wide Operating Voltage Range
- Low Power Consumption
- Low Input Current
- Single Down/Up Count-Control Line
- Look-Ahead Circuitry Enhances Speed of Cascaded Counters
- Fully Synchronous in Count Modes
- Asynchronously Presettable With Load Control

2 Description

The SN54HC191-DIE is a 4-bit synchronous, reversible, up/down binary counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four flip-flops are triggered on a low- to high-level transition of the clock (CLK) input if the count-enable ($\overline{CTEN}$) input is low. A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up, and when D/$\overline{U}$ is high, it counts down.

These counters feature a fully independent clock circuit. Change at the control ($\overline{CTEN}$ and D/$\overline{U}$) inputs that modifies the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter is dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, each of the outputs can be preset to either level by placing a low on the load ($\overline{LOAD}$) input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the level of CLK. This feature allows the counters to be used as modulo-N dividers simply by modifying the count length with the preset inputs.

Two outputs are available to perform the cascading function: ripple clock ($\overline{RCO}$) and maximum/minimum (MAX/MIN) count. MAX/MIN produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down, or maximum (9 or 15) counting up. $\overline{RCO}$ produces a low-level output pulse under those same conditions, but only while CLK is low. The counters can be cascaded easily by feeding $\overline{RCO}$ to $\overline{CTEN}$ of the succeeding counter if parallel clocking is used, or to CLK if parallel enabling is used. MAX/MIN can be used to accomplish look ahead for high-speed operation.

Ordering Information[1]

PRODUCT	PACKAGE DESIGNATOR	PACKAGE	ORDERABLE PART NUMBER	PACKAGE QUANTITY
SN54HC191	TD	Bare die in waffle pack[2]	SN54HC191TDE1	154
			SN54HC191TDE2	10

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

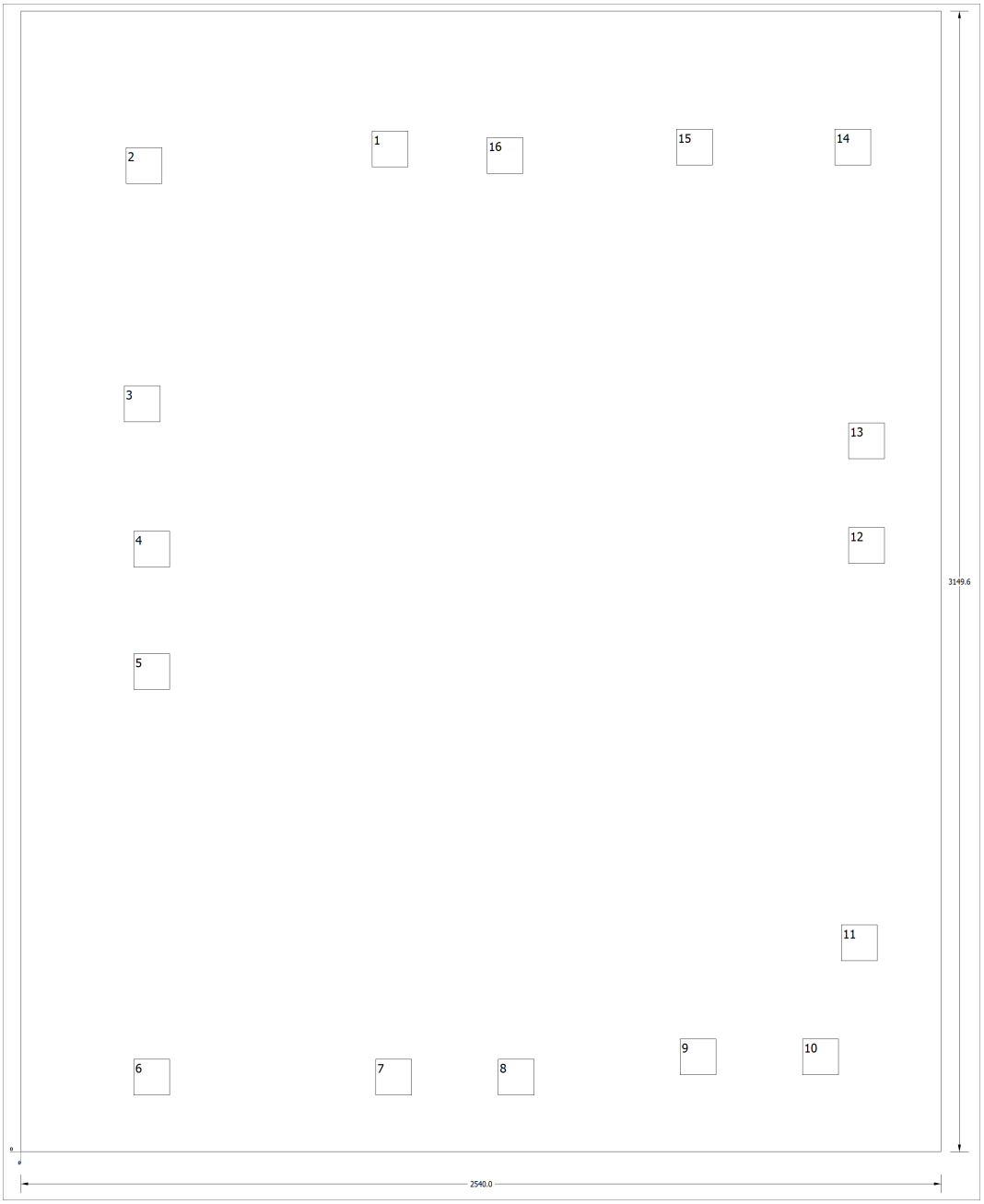
(2) Processing is per the Texas Instruments space production baseline and is in compliance with the Texas Instruments Quality Control System in effect at the time of manufacture. Electrical screening consists of DC parametric and functional testing at room temperature only. Unless otherwise specified by Texas Instruments AC performance and performance over temperature is not warranted. Visual Inspection is performed in accordance with MIL-STD-883 Test Method 2010 Condition B at 75X minimum.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

3 Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
10.5 mils.	Silicon with backgrind	Floating	TiW/AlCu2%	1199 nm



Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
B	1	968.527	2718.587	1068.553	2818.613
QB	2	290.347	2672.867	390.373	2772.893
QA	3	285.267	2015.007	385.293	2115.033
$\overline{\text{CTEN}}$	4	310.667	1613.687	410.693	1713.713
D/$\overline{\text{U}}$	5	310.667	1275.867	410.693	1375.893
QC	6	310.667	155.727	410.693	255.753
QD	7	978.687	155.727	1078.713	255.753
GND	8	1316.507	155.727	1416.533	255.753
D	9	1819.427	211.607	1919.453	311.633
C	10	2157.247	211.607	2257.273	311.633
$\overline{\text{LOAD}}$	11	2263.927	526.567	2363.953	626.593
MAX/MIN	12	2284.247	1623.847	2384.273	1723.873
$\overline{\text{RCO}}$	13	2284.247	1913.407	2384.273	2013.433
CLK	14	2246.147	2723.667	2346.173	2823.693
A	15	1809.267	2723.667	1909.293	2823.693
VCC	16	1286.027	2700.807	1386.053	2800.833

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN54HC191TDE1	ACTIVE			0	154	TBD	Call TI	N / A for Pkg Type	25 Only		Samples
SN54HC191TDE2	ACTIVE			0	10	TBD	Call TI	N / A for Pkg Type	25 Only		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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