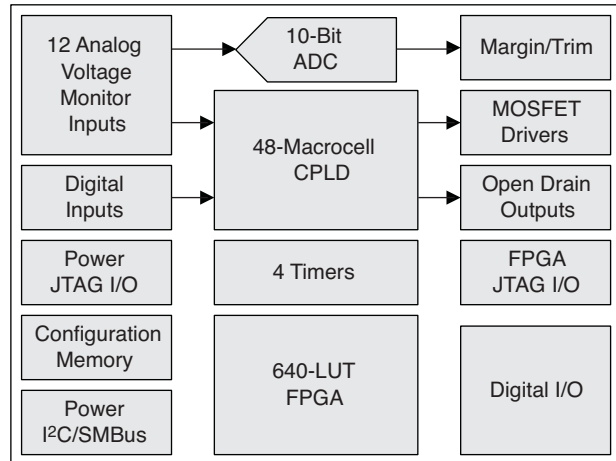


### Features

- Precision Voltage Monitoring Increases Reliability**
  - 12 independent analog monitor inputs
  - Differential inputs for remote ground sense
  - Two programmable threshold comparators per analog input
  - Hardware window comparison
  - 10-bit ADC for I<sup>2</sup>C monitoring
- High-Voltage FET Drivers Enable Integration**
  - Power supply ramp up/down control
  - Programmable current and voltage output
  - Independently configurable for FET control or digital output
- Power Supply Margin and Trim Functions**
  - Trim and margin up to eight power supplies
  - Dynamic voltage control through I<sup>2</sup>C
  - Independent Digital Closed-Loop Trim function for each output
- Programmable Timers Increase Control Flexibility**
  - Four independent timers
  - 32 μs to 2 second intervals for timing sequences
- PLD Resources Integrate Power and Digital Functions**
  - 48-macrocell CPLD
  - 640 LUT4s FPGA
  - Up to 107 digital I/Os
  - Up to 6.1 Kbits distributed RAM
- Programmable sysIO™ Buffer Supports a Range of Interfaces**
  - LVCMOS 3.3/2.5/1.8/1.5/1.2
  - LVTTTL
- System-Level Support**
  - Single 3.3V supply operation
  - Industrial temperature range: -40°C to +85°C
- In-System Programmability Reduces Risk**
  - Integrated non-volatile configuration memory
  - JTAG programming interface
- Package Options**
  - 128-pin TQFP
  - 208-ball ftBGA
  - RoHS compliant and halogen-free

### Block Diagram



### Description

The Lattice Platform Manager integrates board power management (hot-swap, sequencing, monitoring, reset generation, trimming and margining) and digital board management functions (reset tree, non-volatile error logging, glue logic, board digital signal monitoring and control, system bus interface, etc.) into a single integrated solution.

The Platform Manager device provides 12 independent analog input channels to monitor up to 12 power supply test points. Up to 12 of these input channels can be monitored through differential inputs to support remote ground sensing. Each of the analog input channels is monitored through two independently programmable comparators to support both high/low and in-bounds/out-of-bounds (window-compare) monitor functions. Up to six general purpose 5V tolerant digital inputs are also provided for miscellaneous control functions.

There are 16 open-drain digital outputs that can be used for controlling DC-DC converters, low-drop-out regulators (LDOs) and opto-couplers, as well as for supervisory and general purpose logic interface functions. Four of these outputs (HVOUT1-HVOUT4) may be configured as high-voltage MOSFET drivers. In high-voltage mode these outputs can provide up to 12V for driving the gates of n-channel MOSFETs so that they can be used as high-side power switches controlling the supplies with a programmable ramp rate for both ramp up and ramp down.

The board power management function can be implemented using an internal 48-macrocell CPLD. The status of all of the comparators on the analog input channels as well as the general purpose digital inputs are used as inputs by the CPLD array, and all digital outputs (open-drain as well as HVOUT) may be controlled by the CPLD.

Four independently programmable timers can create delays and time-outs ranging from 32  $\mu$ s to 2 seconds.

The Platform Manager device incorporates up to eight DACs for generating trimming voltage to control the output voltage of a DC-DC converter. Additionally, each power supply output voltage can be maintained typically within 0.5% tolerance across various load conditions using the Digital Closed Loop Control mode.

The internal 10-bit A/D converter can both be used to monitor the VMON voltage through the I<sup>2</sup>C bus as well as for implementing digital closed loop mode for maintaining the output voltage of all power supplies controlled by the monitoring and trimming section of the Platform Manager device.

The FPGA section of the Platform Manager is optimized to meet the requirements of board management functions including reset distribution, boundary scan management, fault logging, FPGA load control, and system bus interface. The FPGA section uses look-up tables (LUTs) and distributed memories for flexible and efficient logic implementation. This instant-on capability enables the Platform Manager devices to integrate control functions that are required as soon as power is applied to the board.

Power management functions can be integrated into the CPLD and digital board management functions can be integrated into the FPGA using the LogiBuilder tool provided by PAC-Designer<sup>®</sup> software. In addition, the FPGA designs can also be implemented in VHDL or Verilog HDL through the ispLEVER<sup>®</sup> software design tool.

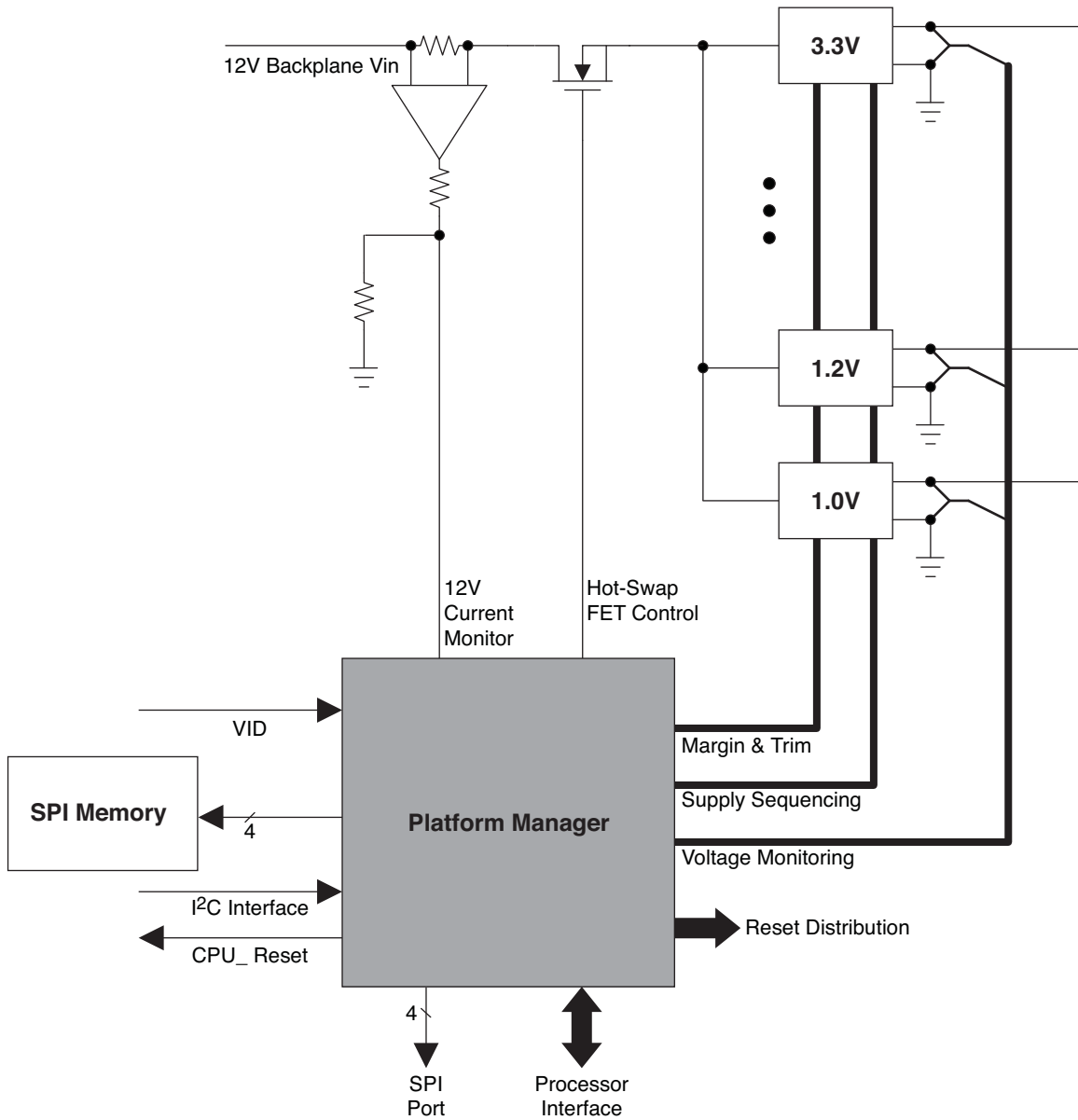
The Platform Manager IC supports a hardware I<sup>2</sup>C/SMBus slave interface that can be used to measure voltages through the Analog to Digital Converter or is used for trimming and margining using a microcontroller.

There are two JTAG ports integrated into the Platform Manager device: Power JTAG and FPGA JTAG. The Power JTAG interface is used to program the power section of the Platform Manager and the FPGA JTAG is used to configure the FPGA portion of the device. The FPGA configuration memory can be changed in-system without interrupting the operation of the board management section. However, the Power Management section of the platform Manager cannot be changed without interrupting the power management operation.

**Table 1. Platform Manager Family Selection Table**

| Parameter       | LPTM10-1247  | LPTM10-12107   |
|-----------------|--------------|----------------|
| Analog Inputs   | 12           | 12             |
| Margin and Trim | 6            | 8              |
| Total I/O       | 47           | 107            |
| CPLD Macrocells | 48           | 48             |
| FPGA LUTs       | 640          | 640            |
| Package         | 128-pin TQFP | 208-ball ftBGA |

Figure 1. Typical Platform Manager Application



Note: See reference design, IP documentation and application notes for more information on implementation of individual functions called out above.

**Absolute Maximum Ratings<sup>1, 2, 3</sup>**

|   |               |
|---|---------------|
| Power Management Core Supply $P_{VCCD}$ . . . . .                                       | -0.5 to 4.5V  |
| Power Management Analog Supply $P_{VCCA}$ . . . . .                                     | -0.5 to 4.5V  |
| Power Management Digital Input Supply $P_{VCCA}$ (IN[1:4]) $P_{VCCINP}$ . . . . .       | -0.5 to 6V    |
| Power Management JTAG Logic Supply $P_{VCCJ}$ . . . . .                                 | -0.5 to 6V    |
| Power Management Alternate E <sup>2</sup> programming supply APS <sup>4</sup> . . . . . | -0.5 to 4V    |
| Power Management Digital Input Voltage (All Digital I/O Pins) $V_{IN}$ . . . . .        | -0.5 to 6V    |
| VMON Input Voltage . . . . .  | -0.5 to 6V    |
| VMON Input Voltage Ground Sense . . . . .   | -0.5 to 6V    |
| Voltage Applied to Power Management Tri-stated Pins (HVOUT[1:4]) . . . . .              | -0.5 to 13.3V |
| Voltage Applied to Power Management Tri-stated Pins (OUT[5:16]) . . . . .               | -0.5 to 6V    |
| Maximum Sink Current on Any Power Management Output . . . . .                           | 23 mA         |
| FPGA Supply Voltage $V_{CC}$ . . . . .  | -0.5 to 3.75V |
| FPGA Supply Voltage $V_{CCAUX}$ . . . . .   | -0.5 to 3.75V |
| FPGA Output Supply Voltage $V_{CCIO}$ . . . . .   | -0.5 to 3.75V |
| FPGA I/O Tri-state Voltage Applied <sup>5</sup> . . . . .                               | -0.5 to 3.75V |
| FPGA Dedicated Input Voltage Applied <sup>5</sup> . . . . .                             | -0.5 to 4.25V |
| Device Storage Temperature . . . . .  | -65 to +150°C |
| Junction Temperature $T_J$ . . . . .  | +125°C        |

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND (FPGA section) or GND A/D (Power sections).
4. The APS pin MUST be left floating when  $P_{VCCD}$  and  $P_{VCCA}$  are powered.
5. Overshoot and undershoot of -2V to ( $V_{IHMAX} + 2$ ) volts is permitted for a duration of <20 ns.

## Recommended Operating Conditions

| Symbol                 | Parameter   | Conditions                            | Min.                                | Max.  | Units |
|------------------------|---|---------------------------------------|-------------------------------------|-------|-------|
| $P_{VCCD}, P_{VCCA}^1$ | Core supply voltage at pin                          |                                       | 2.8                                 | 3.96  | V     |
| $P_{VCCINP}$           | Digital input supply for IN[1:4] at pin             |                                       | 2.25                                | 5.5   | V     |
| $P_{VCCJ}$             | JTAG logic supply voltage at pin                    |                                       | 2.25                                | 3.6   | V     |
| APS                    | Alternate E <sup>2</sup> programming supply at pin  | $P_{VCCD}$ and $P_{VCCA}$ powered     | No Connect<br>Must Be Left Floating |       |       |
|                        |   | $P_{VCCD}$ and $P_{VCCA}$ not powered | 3.0                                 | 3.6   | V     |
| $V_{IN}$               | Input voltage at digital input pins                 |                                       | -0.3                                | 5.5   | V     |
| $V_{MON}$              | Input voltage at $V_{MON}$ pins                     |                                       | -0.3                                | 5.9   | V     |
| $V_{MONGS}$            | Input voltage at $V_{MONGS}$ pins                   |                                       | -0.2                                | 0.3   | V     |
| $V_{OUT}$              | Open-drain output voltage                           | OUT[5:16] pins                        | -0.3                                | 5.5   | V     |
|                        |   | HVOUT[1:4] pins in open-drain mode    | -0.3                                | 13.0  | V     |
| $V_{CC}^2$             | FPGA Core Supply Voltage                            |                                       | 3.135                               | 3.465 | V     |
| $V_{CCAUX}^2$          | FPGA Auxiliary Supply Voltage                       |                                       | 3.135                               | 3.465 | V     |
| $V_{CCIO}^3$           | FPGA I/O Driver Supply Voltage                      | $V_{CCIO0}, V_{CCIO1}, V_{CCIO3}$     | 1.14                                | 3.465 | V     |
|                        |   | $V_{CCIO2}$                           | 2.25                                | 3.6   | V     |
| $t_{JCOM}$             | Junction Temperature Commercial Operation           | Power applied                         | 0                                   | +85   | °C    |
| $t_{JIND}$             | Junction Temperature Industrial Operation           | Power applied                         | -40                                 | +100  | °C    |
| $t_{JFLASHCOM}$        | Junction Temperature, Flash Programming, Commercial |                                       | 0                                   | +85   | °C    |
| $t_{JFLASHIND}$        | Junction Temperature, Flash Programming, Industrial |                                       | -40                                 | +100  | °C    |

1.  $P_{VCCD}$  and  $P_{VCCA}$  must always be tied together.

2.  $V_{CC}$  and  $V_{CCAUX}$  must always be tied together. Also, like power supplies must be tied together. For example, if  $V_{CCIO}$  and  $V_{CC}$  are both 3.3V, they must also be the same supply.

3. See recommended voltages by I/O standard in subsequent table.

## Digital I/O Hot Socketing Specifications<sup>1, 2, 3</sup>

| Symbol   | Parameter                    | Condition                         | Min. | Typ. | Max     | Units |
|----------|------------------------------|-----------------------------------|------|------|---------|-------|
| $I_{DK}$ | Input or I/O leakage Current | $0 \leq V_{IN} \leq V_{IH}$ (MAX) | —    | —    | +/-1000 | μA    |

1. Assumes monotonic rise/fall rates for  $V_{CC}$ ,  $V_{CCAUX}$ , and  $V_{CCIO}$ .

2.  $0 \leq V_{CC} \leq V_{CC} (MAX)$ ,  $0 \leq V_{CCIO} \leq V_{CCIO} (MAX)$  and  $0 \leq V_{CCAUX} \leq V_{CCAUX} (MAX)$ .

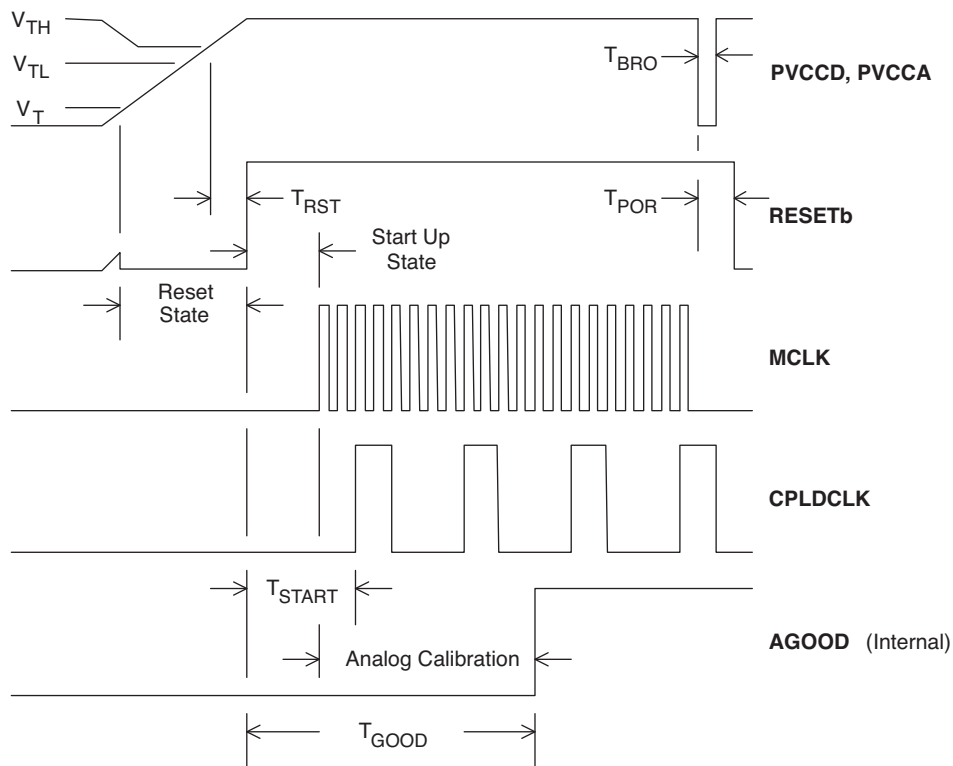
3.  $I_{DK}$  is additive to  $I_{PU}$ ,  $I_{PD}$  or  $I_{BH}$ .

## Power-On Reset – Power Management Section

| Symbol      | Parameter  | Conditions | Min. | Typ. | Max. | Units   |
|-------------|--|------------|------|------|------|---------|
| $T_{RST}$   | Delay from $V_{TH}$ to start-up state                            |            |      |      | 100  | $\mu s$ |
| $T_{START}$ | Delay from RESEtb HIGH to CPLDCLK rising edge                    |            |      | 5    | 10   | $\mu s$ |
| $T_{GOOD}$  | Power-on reset to valid VMON comparator output and AGOOD is true |            |      |      | 2.5  | ms      |
| $T_{BRO}$   | Minimum duration brown out required to trigger RESEtb            |            | 1    |      | 5    | $\mu s$ |
| $T_{POR}$   | Delay from brown out to reset state.                             |            |      |      | 13   | $\mu s$ |
| $V_{TL}$    | Threshold below which RESEtb is LOW <sup>1</sup>                 |            |      |      | 2.3  | V       |
| $V_{TH}$    | Threshold above which RESEtb is HIGH <sup>1</sup>                |            | 2.7  |      |      | V       |
| $V_T$       | Threshold above which RESEtb is valid <sup>1</sup>               |            | 0.8  |      |      | V       |
| $C_L$       | Capacitive load on RESEtb for master/slave operation             |            |      |      | 200  | pF      |

1. Corresponds to PVCCA and PVCCD supply voltages.

**Figure 2. Power Management Section Power-On Reset**



## ESD Performance

| Pin Group | ESD Stress | Min. | Units |
|-----------|------------|------|-------|
| All pins  | HBM        | 1500 | V     |
|           | CDM        | 1000 | V     |

## DC Electrical Characteristics<sup>1, 2, 3, 4</sup>

| Symbol       | Parameter   | Conditions                   | Typ. <sup>5</sup> | Max. | Units |
|--------------|---|------------------------------|-------------------|------|-------|
| $P_{ICC}$    | Power Management section supply current           | Normal operation             |                   | 40   | mA    |
| $P_{ICCNIP}$ | Power Management section supply current           | Normal operation             |                   | 5    | mA    |
| $P_{ICCNJ}$  | Power Management section supply current           | Normal operation             |                   | 1    | mA    |
| $I_{CC}^1$   | FPGA Core Power Supply                            |                              | 8.7               |      | mA    |
| $I_{CCAUX}$  | FPGA Auxiliary Power Supply<br>$V_{CCAUX} = 3.3V$ | During initialization (0MHz) | 7                 |      | mA    |
| $I_{CCIO}$   | FPGA Bank Power Supply <sup>6</sup>               | During initialization (0MHz) | 2.4               |      | mA    |

- For further information on FPGA section supply current, please see details of additional technical documentation at the end of this data sheet.
- Assumes all FPGA section I/O pins are held at  $V_{CCIO}$  or GND.
- FPGA Frequency = 0 MHz.
- Typical FPGA user pattern.
- $T_J = 25^\circ C$ , power supplies at nominal voltage.
- Per bank,  $V_{CCIO} = 2.5V$ . Does not include pull-up/pull-down.

## FPGA Supply Current (Sleep Mode)<sup>1, 2</sup>

| Symbol      | Parameter                      | Conditions | Typ. <sup>3</sup> | Max. | Units   |
|-------------|--------------------------------|------------|-------------------|------|---------|
| $I_{CC}^1$  | FPGA Core Power Supply         | Sleep Mode | 12                | 25   | $\mu A$ |
| $I_{CCAUX}$ | FPGA Auxiliary Power Supply    |            | 1                 | 25   | $\mu A$ |
| $I_{CCIO}$  | Bank Power Supply <sup>4</sup> |            | 2                 | 30   | $\mu A$ |

- Assumes all inputs are configured as LVCMOS and held at the  $V_{CCIO}$  or GND.
- Frequency = 0MHz.
- $T_A = 25^\circ C$ , power supplies at nominal voltage.
- Per bank.

## DC Electrical Characteristics – FPGA General Purpose I/O

### Over Recommended Operating Conditions

| Symbol                 | Parameter                                | Condition  | Min.           | Typ. | Max.           | Units   |
|------------------------|--|--|----------------|------|----------------|---------|
| $I_{IL}, I_{IH}^{1,4}$ | Input or I/O Leakage                     | $0 \leq V_{IN} \leq (V_{CCIO} - 0.2V)$   | —              | —    | 10             | $\mu A$ |
|                        |  | $(V_{CCIO} - 0.2V) < V_{IN} \leq 3.6V$   | —              | —    | 40             | $\mu A$ |
| $I_{PU}$               | I/O Active Pull-up Current               | $0 \leq V_{IN} \leq 0.7 V_{CCIO}$  | -30            | —    | -150           | $\mu A$ |
| $I_{PD}$               | I/O Active Pull-down Current             | $V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MAX)$   | 30             | —    | 150            | $\mu A$ |
| $I_{BHLS}$             | Bus Hold Low sustaining current          | $V_{IN} = V_{IL} (MAX)$  | 30             | —    | —              | $\mu A$ |
| $I_{BHHS}$             | Bus Hold High sustaining current         | $V_{IN} = 0.7V_{CCIO}$   | -30            | —    | —              | $\mu A$ |
| $I_{BHLO}$             | Bus Hold Low Overdrive current           | $0 \leq V_{IN} \leq V_{IH} (MAX)$  | —              | —    | 150            | $\mu A$ |
| $I_{BHHO}$             | Bus Hold High Overdrive current          | $0 \leq V_{IN} \leq V_{IH} (MAX)$  | —              | —    | -150           | $\mu A$ |
| $V_{BHT}^3$            | Bus Hold trip Points                     | $0 \leq V_{IN} \leq V_{IH} (MAX)$  | $V_{IL} (MAX)$ | —    | $V_{IH} (MIN)$ | V       |
| C1                     | I/O Capacitance <sup>2</sup>             | $V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V,$<br>$V_{CC} = Typ., V_{IO} = 0 \text{ to } V_{IH} (MAX)$ | —              | 8    | —              | pf      |
| C2                     | Dedicated Input Capacitance <sup>2</sup> | $V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V,$<br>$V_{CC} = Typ., V_{IO} = 0 \text{ to } V_{IH} (MAX)$ | —              | 8    | —              | pf      |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2.  $T_A$  25°C,  $f = 1.0MHz$
3. Please refer to  $V_{IL}$  and  $V_{IH}$  in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. When  $V_{IH}$  is higher than  $V_{CCIO}$ , a transient current typically of 30ns in duration or less with a peak current of 6mA can occur on the high-to-low transition.



**Programming and Erase Supply Current<sup>1, 2, 3, 4</sup>**

| Symbol             | Parameter  | Typ. <sup>5</sup> | Max. | Units |
|--------------------|--|-------------------|------|-------|
| I <sub>APS</sub>   | Power Management P <sub>VCCA/D</sub> Programming Current |                   | 40   | mA    |
| I <sub>CC</sub>    | FPGA Core Power Supply                                   | 11                |      | mA    |
| I <sub>CCAUX</sub> | FPGA Auxiliary Power Supply<br>V <sub>CCAUX</sub> = 3.3V | 10                |      | mA    |
| I <sub>CCIO</sub>  | FPGA Bank Power Supply <sup>6</sup>                      | 2                 |      | mA    |

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all I/O pins are held at V<sub>CCIO</sub> or GND.
3. Typical user pattern.
4. JTAG programming is at 25 MHz.
5. T<sub>J</sub> = 25°C, power supplies at nominal voltage.
6. Per bank. V<sub>CCIO</sub> = 2.5V. Does not include pull-up/pull-down.

**Voltage Monitors**

| Symbol                    | Parameter   | Conditions | Min.  | Typ. | Max.  | Units |
|---------------------------|---|------------|-------|------|-------|-------|
| R <sub>IN</sub>           | Input resistance                                    |            | 55    | 65   | 75    | kΩ    |
| C <sub>IN</sub>           | Input capacitance                                   |            |       | 8    |       | pF    |
| V <sub>MON</sub> Range    | Programmable trip-point range                       |            | 0.075 |      | 5.734 | V     |
| V <sub>Z</sub> Sense      | Near-ground sense threshold                         |            | 70    | 75   | 80    | mV    |
| V <sub>MON</sub> Accuracy | Absolute accuracy of any trip-point <sup>1</sup>    |            |       | 0.2  | 0.7   | %     |
|                           | Single-ended V <sub>MON</sub> pins <sup>2, 3</sup>  |            |       | 0.3  | 0.9   | %     |
| HYST                      | Hysteresis of any trip-point (relative to setting)  |            |       | 1    |       | %     |
| CMR                       | Common mode rejection                               |            |       | 60   |       | dB    |
| t <sub>PD16</sub>         | Propagation delay input to output glitch filter OFF |            |       | 16   |       | μs    |
| t <sub>PD64</sub>         | Propagation delay input to output glitch filter ON  |            |       | 64   |       | μs    |

1. Guaranteed by characterization across P<sub>VCCA</sub> range, operating temperature, process.
2. Single-ended V<sub>MON</sub> inputs in 128-pin TQFP package only. Single-ended V<sub>MON</sub> input pins include: 59 (V<sub>MON1</sub>), 83 (V<sub>MON9</sub>), 84 (V<sub>MON10</sub>), 86 (V<sub>MON11</sub>), 88 (V<sub>MON12</sub>).
3. No adjacent digital I/O pin switching noise as described in the following table for single-ended V<sub>MON</sub> trip point error.

**Single-Ended Voltage Monitor Trip Point Error<sup>1</sup>**

| Symbol                    | Parameter  | Conditions   | Min. | Typ. | Max. | Units |
|---------------------------|--|--|------|------|------|-------|
| V <sub>MON</sub> Error SE | Single-ended trip point error (with adjacent switching noise) <sup>2</sup> | Pins 85, 87, 89<br>F <sub>SWITCH</sub> = 10MHz                                 |      | 2    |      | mV    |
|                           | Single-ended trip point error (no adjacent switching noise) <sup>2</sup>   | Pins 85, 87, 89<br>F <sub>SWITCH</sub> = 0Hz;<br>All other digital I/O = 10MHz |      | 1    |      | mV    |

1. Single-ended V<sub>MON</sub> inputs in 128-pin TQFP package only. Affected single-ended V<sub>MON</sub> input pins only include: 83 (V<sub>MON9</sub>), 84 (V<sub>MON10</sub>), 86 (V<sub>MON11</sub>), and 88 (V<sub>MON12</sub>). Single-ended V<sub>mon</sub> input pin 59 (V<sub>MON1</sub>) is not affected by adjacent switching noise.
2. Defined as TQFP package option adjacent digital I/O pins 85 (PR4B), 87 (PR3D) and 89 (PR2D) configured as outputs switching (F<sub>SWITCH</sub>) at 10MHz into a 33pF load capacitance.

## High Voltage FET Drivers

| Symbol               | Parameter                               | Conditions                | Min. | Typ. | Max. | Units |
|----------------------|---|---------------------------|------|------|------|-------|
| V <sub>PP</sub>      | Gate driver output voltage              | 12V setting               | 11.5 | 12   | 12.5 | V     |
|                      |   | 10V setting               | 9.6  | 10   | 10.4 |       |
|                      |   | 8V setting                | 7.7  | 8    | 8.3  |       |
|                      |   | 6V setting                | 5.8  | 6    | 6.2  |       |
| I <sub>OUTSRC</sub>  | Gate driver source current (HIGH state) | Four settings in software |      | 12.5 |      | μA    |
|                      |   |                           |      | 25   |      |       |
|                      |   |                           |      | 50   |      |       |
|                      |   |                           |      | 100  |      |       |
| I <sub>OUTSINK</sub> | Gate driver sink current (LOW state)    | FAST OFF mode             | 2000 | 3000 |      | μA    |
|                      |   | Controlled ramp settings  |      | 100  |      |       |
|                      |   |                           |      | 250  |      |       |
|                      |   |                           | 500  |      |      |       |

## Margin/Trim DAC Output Characteristics

| Symbol               | Parameter  | Conditions   | Min. | Typ.       | Max. | Units |
|----------------------|--|--|------|------------|------|-------|
|                      | Resolution   |  |      | 8 (7+sign) |      | Bits  |
| FSR                  | Full scale range                                       |  |      | +/-320     |      | mV    |
| LSB                  | LSB step size  |  |      | 2.5        |      | mV    |
| I <sub>OUT</sub>     | Output source/sink current                             |  | -200 |            | 200  | μA    |
| BPZ                  | Bipolar zero output voltage (code=80h)                 | Offset 1   |      | 0.6        |      | V     |
|                      |  | Offset 2   |      | 0.8        |      |       |
|                      |  | Offset 3   |      | 1.0        |      |       |
|                      |  | Offset 4   |      | 1.25       |      |       |
| TS                   | TrimCell output voltage settling time <sup>1</sup>     | DAC code changed from 80H to FFH or 80H to 00H             |      |            | 2.5  | ms    |
|                      |  | Single DAC code change                                     |      | 256        |      | μs    |
| C_LOAD               | Maximum load capacitance                               |  |      |            | 50   | pF    |
| T <sub>UPDATEM</sub> | Update time through I <sup>2</sup> C port <sup>2</sup> | MCLK = 8 MHz   |      | 260        |      | μs    |
| TOSE                 | Total open loop supply voltage error <sup>3</sup>      | Full scale DAC corresponds to ±5% supply voltage variation | -1%  |            | +1%  | V/V   |

1. To 1% of set value with 50pf load connected to trim pins.

2. Total time required to update a single TRIMx output value by setting the associated DAC through the I<sup>2</sup>C port.

3. This is the total resultant error in the trimmed power supply output voltage referred to any DAC code due to the DAC's INL, DNL, gain, output impedance, offset error and bipolar offset error across the industrial temperature range and the Platform Manager operating P<sub>VCCA</sub> and P<sub>VCCD</sub> ranges.

## ADC Characteristics

| Symbol               | Parameter               | Conditions                         | Min. | Typ.    | Max.             | Units         |
|----------------------|-------------------------|------------------------------------|------|---------|------------------|---------------|
|                      | ADC Resolution          |                                    |      | 10      |                  | Bits          |
| $T_{\text{CONVERT}}$ | Conversion Time         | Time from I <sup>2</sup> C Request |      |         | 200              | $\mu\text{s}$ |
| $V_{\text{IN}}$      | Input range Full Scale  | Programmable Attenuator = 1        | 0    |         | 2.048            | V             |
|                      |                         | Programmable Attenuator = 3        | 0    |         | 5.9 <sup>1</sup> | V             |
| ADC Step Size        | LSB                     | Programmable Attenuator = 1        |      | 2       |                  | mV            |
|                      |                         | Programmable Attenuator = 3        |      | 6       |                  | mV            |
| Eattenuator          | Error Due to Attenuator | Programmable Attenuator = 3        |      | +/- 0.1 |                  | %             |

1. Maximum voltage is limited by  $V_{\text{MONX}}$  pin (theoretical maximum is 6.144V).

## ADC Error Budget Across Entire Operating Temperature Range

| Symbol     | Parameter  | Conditions   | Min. | Typ.  | Max. | Units |
|------------|--|--|------|-------|------|-------|
| TADC Error | Total Measurement Error at Any Voltage (Differential Analog Inputs) <sup>1</sup> | Measurement Range 600 mV - 2.048V, VMONxGS > -100mV, Attenuator =1 | -8   | +/-4  | 8    | mV    |
|            |  | Measurement Range 600 mV - 2.048V, VMONxGS > -200mV, Attenuator =1 |      | +/-6  |      | mV    |
|            |  | Measurement Range 0 - 2.048V, VMONxGS > -200mV, Attenuator =1      |      | +/-10 |      | mV    |
|            | Total Measurement Error at Any Voltage (Single-Ended Analog Inputs) <sup>2</sup> | Measurement Range 600 mV - 2.048V, Attenuator =1                   | -8   | +/-4  | 8    | mV    |

1. Total error, guaranteed by characterization, includes INL, DNL, Gain, Offset, and PSR specifications of the ADC.

2. Single-ended  $V_{\text{MON}}$  inputs in 128-pin TQFP package only. Single-ended Vmon input pins include: 59 (VMON1), 83 (VMON9), 84 (VMON10), 86 (VMON11), 88 (VMON12).

## Digital Specifications – Power Management Section Dedicated Inputs

Over Recommended Operating Conditions

| Symbol           | Parameter  | Conditions                              | Min.             | Typ. | Max.             | Units   |
|------------------|--|---|------------------|------|------------------|---------|
| $I_{IL}, I_{IH}$ | Input leakage, no pull-up/pull-down                      |   |                  |      | +/-10            | $\mu A$ |
| $I_{PU}$         | Input pull-up current (PTMS, PTDI, PTDISEL, PATDI, MCLK) |   |                  | 70   |                  | $\mu A$ |
| $V_{IL}$         | Voltage input, logic low <sup>1</sup>                    | PTDI, PTMS, PATDI, PTDISEL, 3.3V supply |                  |      | 0.8              | V       |
|                  |  | PTDI, PTMS, PATDI, PTDISEL, 2.5V supply |                  |      | 0.7              |         |
|                  |  | SCL, SDA                                |                  |      | 30% $P_{VCCD}$   |         |
|                  |  | IN[1:4]                                 |                  |      | 30% $P_{VCCINP}$ |         |
| $V_{IH}$         | Voltage input, logic high <sup>1</sup>                   | PTDI, PTMS, PATDI, PTDISEL, 3.3V supply | 2.0              |      |                  | V       |
|                  |  | PTDI, PTMS, PATDI, PTDISEL, 2.5V supply | 1.7              |      |                  |         |
|                  |  | SCL, SDA                                | 70% $P_{VCCD}$   |      | $P_{VCCD}$       |         |
|                  |  | IN[1:4]                                 | 70% $P_{VCCINP}$ |      | $P_{VCCINP}$     |         |

1. SCL, SDA referenced to  $P_{VCCD}$ ; IN[1:4] referenced to  $P_{VCCINP}$ ; PTDO, PTDI, PTMS, PATDI, PTDISEL referenced to  $P_{VCCJ}$ .

## Digital Specifications – Power Management Section Dedicated Outputs

Over Recommended Operating Conditions

| Symbol          | Parameter                     | Conditions   | Min. | Typ. | Max.             | Units   |
|-----------------|-------------------------------|--|------|------|------------------|---------|
| $I_{OH-HVOUT}$  | Output leakage current        | HVOUT[1:4] in open drain mode and pulled up to 12V |      | 35   | 100              | $\mu A$ |
| $V_{OL}$        | HVOUT[1:4] (open drain mode), | $I_{SINK} = 10mA$                                  |      |      | 0.8              | V       |
|                 |                               | $I_{SINK} = 20mA$                                  |      |      | 0.8              |         |
| $V_{OH}$        | PTDO, MCLK, CPLDCLK           | $I_{SINK} = 4mA$                                   |      |      | 0.4              | V       |
|                 |                               | $I_{SRC} = 4mA$                                    |      |      | $P_{VCCD} - 0.4$ |         |
| $I_{SINKTOTAL}$ | All digital outputs           |  |      |      | 130              | mA      |

## sysIO Recommended Operating Conditions

| Standard    | V <sub>CCIO</sub> (V) |      |       |
|-------------|-----------------------|------|-------|
|             | Min.                  | Typ. | Max.  |
| LVC MOS 3.3 | 3.135                 | 3.3  | 3.465 |
| LVC MOS 2.5 | 2.375                 | 2.5  | 2.625 |
| LVC MOS 1.8 | 1.71                  | 1.8  | 1.89  |
| LVC MOS 1.5 | 1.425                 | 1.5  | 1.575 |
| LVC MOS 1.2 | 1.14                  | 1.2  | 1.26  |
| LV TTL      | 3.135                 | 3.3  | 3.465 |

## sysIO Single-Ended DC Electrical Characteristics

| Input/Output Standard    | V <sub>IL</sub> |                       | V <sub>IH</sub>       |          | V <sub>OL</sub> Max. (V) | V <sub>OH</sub> Min. (V) | I <sub>OL</sub> <sup>1</sup> (mA) | I <sub>OH</sub> <sup>1</sup> (mA) |
|--------------------------|-----------------|-----------------------|-----------------------|----------|--------------------------|--------------------------|-----------------------------------|-----------------------------------|
|                          | Min. (V)        | Max. (V)              | Min. (V)              | Max. (V) |                          |                          |                                   |                                   |
| LVC MOS 3.3              | -0.3            | 0.8                   | 2.0                   | 3.6      | 0.4                      | V <sub>CCIO</sub> - 0.4  | 16, 12, 8, 4                      | -14, -12, -8, -4                  |
|                          |                 |                       |                       |          | 0.2                      | V <sub>CCIO</sub> - 0.2  | 0.1                               | -0.1                              |
| LV TTL                   | -0.3            | 0.8                   | 2.0                   | 3.6      | 0.4                      | 2.4                      | 16                                | -16                               |
|                          |                 |                       |                       |          | 0.4                      | V <sub>CCIO</sub> - 0.4  | 12, 8, 4                          | -12, -8, -4                       |
| LVC MOS 2.5              | -0.3            | 0.7                   | 1.7                   | 3.6      | 0.4                      | V <sub>CCIO</sub> - 0.4  | 16, 12, 8, 4                      | -14, -12, -8, -4                  |
|                          |                 |                       |                       |          | 0.2                      | V <sub>CCIO</sub> - 0.2  | 0.1                               | -0.1                              |
| LVC MOS 1.8 <sup>2</sup> | -0.3            | 0.35V <sub>CCIO</sub> | 0.65V <sub>CCIO</sub> | 3.6      | 0.4                      | V <sub>CCIO</sub> - 0.4  | 16, 12, 8, 4                      | -14, -12, -8, -4                  |
|                          |                 |                       |                       |          | 0.2                      | V <sub>CCIO</sub> - 0.2  | 0.1                               | -0.1                              |
| LVC MOS 1.5 <sup>2</sup> | -0.3            | 0.35V <sub>CCIO</sub> | 0.65V <sub>CCIO</sub> | 3.6      | 0.4                      | V <sub>CCIO</sub> - 0.4  | 8, 4                              | -8, -4                            |
|                          |                 |                       |                       |          | 0.2                      | V <sub>CCIO</sub> - 0.2  | 0.1                               | -0.1                              |
| LVC MOS 1.2 <sup>2</sup> | -0.3            | 0.42                  | 0.78                  | 3.6      | 0.4                      | V <sub>CCIO</sub> - 0.4  | 6, 2                              | -6, -2                            |
|                          |                 |                       |                       |          | 0.2                      | V <sub>CCIO</sub> - 0.2  | 0.1                               | -0.1                              |

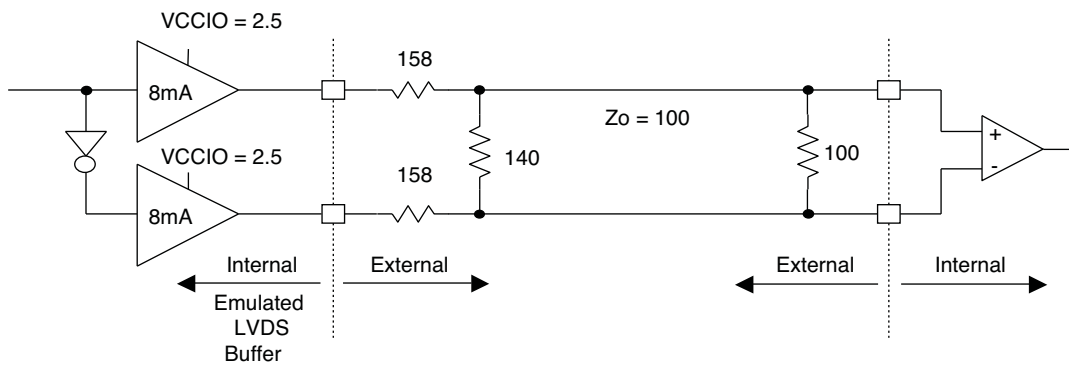
1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed  $n * 8\text{mA}$ . Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.
2. Lower voltage operation not supported for VCCIO2 bank pins.

## sysIO Differential Electrical Characteristics

### LVDS Emulation

FPGA section outputs can support LVDS outputs via emulation (LVDS25E), in addition to the LVDS support that is available. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3 is one possible solution for LVDS standard implementation. Resistor values in Figure 3 are industry standard values for 1% resistors.

**Figure 3. LVDS Using External Resistors (LVDS25E)**

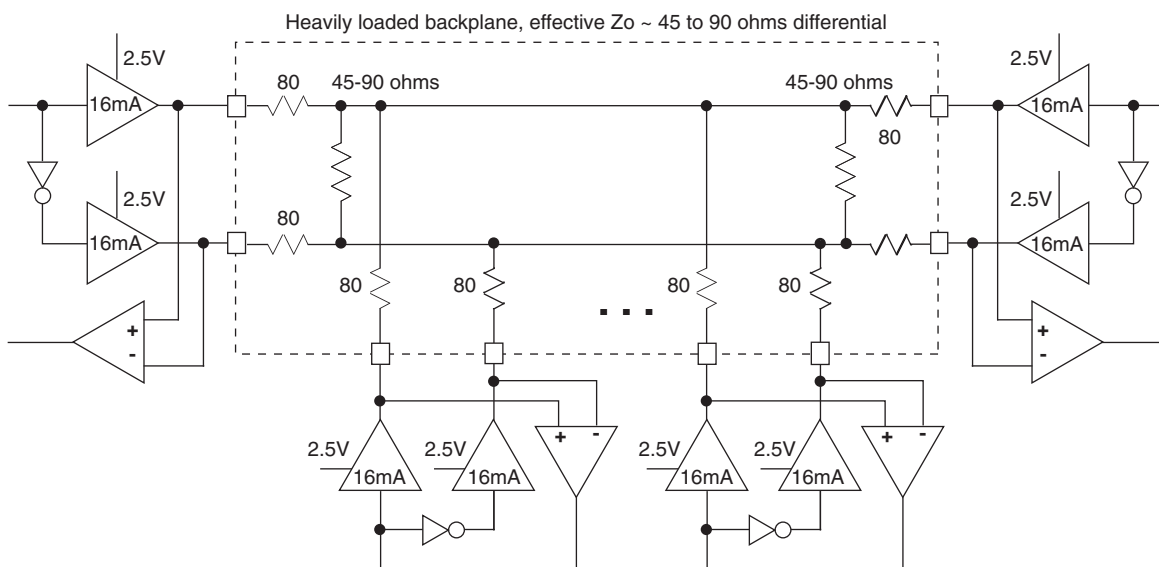


Note: All resistors are  $\pm 1\%$ .

### BLVDS Emulation

FPGA outputs support the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 4 is one possible solution for bi-directional multi-point differential signals.

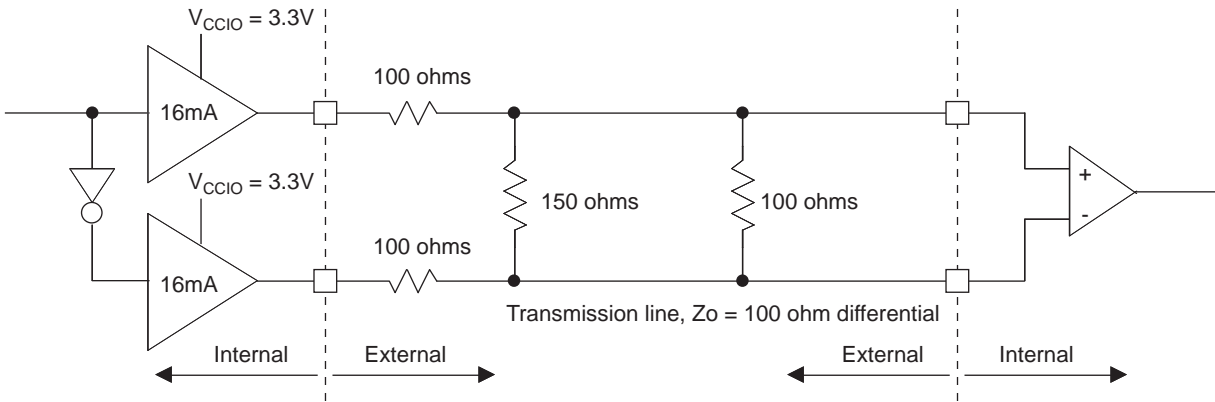
**Figure 4. BLVDS Multi-point Output Example**



### LVPECL Emulation

FPGA outputs support the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The scheme shown in Figure 5 is one possible solution for point-to-point signals.

Figure 5. Differential LVPECL

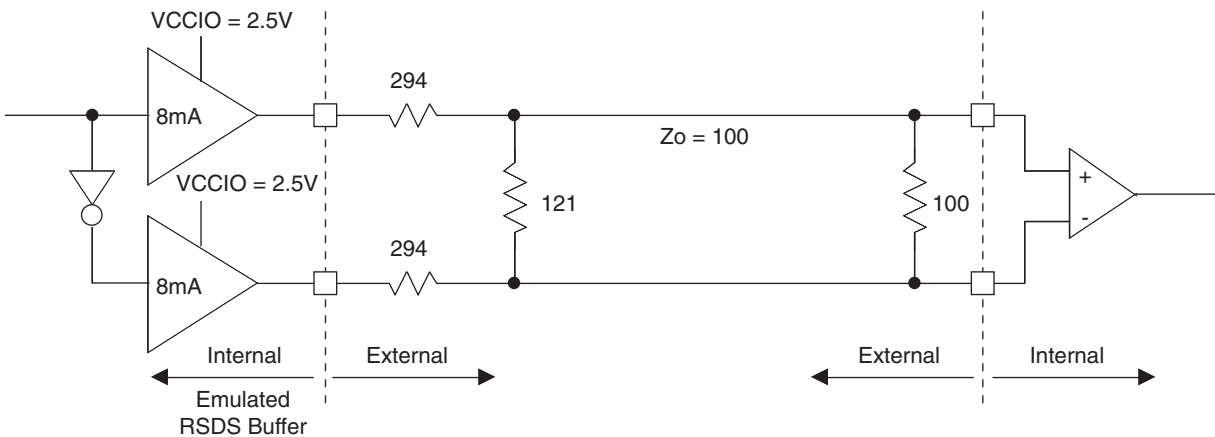


For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

**RSDS Emulation**

FPGA outputs support the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The scheme shown in Figure 6 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 6 are industry standard values for 1% resistors.

Figure 6. RSDS (Reduced Swing Differential Standard)



**Oscillator Transient Characteristics**

Over Recommended Operating Conditions

| Symbol         | Parameter   | Conditions              | Min. | Typ. | Max. | Units |
|----------------|---|-------------------------|------|------|------|-------|
| $f_{CLK}$      | Power Management internal master clock frequency (MCLK) |                         | 7.6  | 8    | 8.4  | MHz   |
| $f_{CLKEXT}$   | Power Management externally applied master clock (MCLK) |                         | 7.2  |      | 8.8  | MHz   |
| $f_{PLDCLK}$   | CPLDCLK output frequency                                | $f_{CLK} = 8\text{MHz}$ |      | 250  |      | kHz   |
| $f_{FPGA CLK}$ | FPGA internal master clock frequency                    |                         | 18   |      | 26   | MHz   |

## Power Management CPLD Timer Transient Characteristics

Over Recommended Operating Conditions

| Symbol        | Parameter  | Conditions              | Min.  | Typ. | Max.  | Units |
|---------------|--|-------------------------|-------|------|-------|-------|
| Timeout Range | Range of programmable timers (128 steps)           | $f_{CLK} = 8\text{MHz}$ | 0.032 |      | 1966  | ms    |
| Resolution    | Spacing between available adjacent timer intervals |                         |       |      | 13    | %     |
| Accuracy      | Timer accuracy                                     | $f_{CLK} = 8\text{MHz}$ | -6.67 |      | -12.5 | %     |

## Power Management I<sup>2</sup>C Port Characteristics

| Symbol        | Definition                                      | 100KHz |                  | 400KHz |                  | Units |
|---------------|---|--------|------------------|--------|------------------|-------|
|               |   | Min.   | Max.             | Min.   | Max.             |       |
| $F_{I^2C}$    | I <sup>2</sup> C clock/data rate                |        | 100 <sup>1</sup> |        | 400 <sup>1</sup> | KHz   |
| $T_{SU;STA}$  | After start                                     | 4.7    |                  | 0.6    |                  | us    |
| $T_{HD;STA}$  | After start                                     | 4      |                  | 0.6    |                  | us    |
| $T_{SU;DAT}$  | Data setup                                      | 250    |                  | 100    |                  | ns    |
| $T_{SU;STO}$  | Stop setup                                      | 4      |                  | 0.6    |                  | us    |
| $T_{HD;DAT}$  | Data hold; SCL= Vih_min = 2.1V                  | 0.3    | 3.45             | 0.3    | 0.9              | us    |
| $T_{LOW}$     | Clock low period                                | 4.7    |                  | 1.3    |                  | us    |
| $T_{HIGH}$    | Clock high period                               | 4      |                  | 0.6    |                  | us    |
| $T_F$         | Fall time; 2.25V to 0.65V                       |        | 300              |        | 300              | ns    |
| $T_R$         | Rise time; 0.65V to 2.25V                       |        | 1000             |        | 300              | ns    |
| $T_{TIMEOUT}$ | Detect clock low timeout                        | 25     | 35               | 25     | 35               | ms    |
| $T_{POR}$     | Device must be operational after power-on reset | 500    |                  | 500    |                  | ms    |
| $T_{BUF}$     | Bus free time between stop and start condition  | 4.7    |                  | 1.3    |                  | us    |

1. If  $F_{I^2C}$  is less than 50kHz, then the ADC DONE status bit is not guaranteed to be set after a valid conversion request is completed. In this case, waiting for the  $T_{CONVERT}$  minimum time after a convert request is made is the only way to guarantee a valid conversion is ready for readout. When  $F_{I^2C}$  is greater than 50kHz, ADC conversion complete is ensured by waiting for the DONE status bit.



## Timing for Power Management JTAG Operations

| Symbol             | Parameter                            | Conditions | Min. | Typ. | Max. | Units         |
|--------------------|--------------------------------------|------------|------|------|------|---------------|
| $t_{\text{SPEN}}$  | Program enable delay time            |            | 10   | —    | —    | $\mu\text{s}$ |
| $t_{\text{SPDIS}}$ | Program disable delay time           |            | 30   | —    | —    | $\mu\text{s}$ |
| $t_{\text{HVDIS}}$ | High voltage discharge time, program |            | 30   | —    | —    | $\mu\text{s}$ |
| $t_{\text{HVDIS}}$ | High voltage discharge time, erase   |            | 200  | —    | —    | $\mu\text{s}$ |
| $t_{\text{CEN}}$   | Falling edge of PTCK to PTDO active  |            | —    | —    | 15   | ns            |
| $t_{\text{CDIS}}$  | Falling edge of PTCK to PTDO disable |            | —    | —    | 15   | ns            |
| $t_{\text{SU1}}$   | Setup time                           |            | 5    | —    | —    | ns            |
| $t_{\text{H}}$     | Hold time                            |            | 10   | —    | —    | ns            |
| $t_{\text{CKH}}$   | PTCK clock pulse width, high         |            | 20   | —    | —    | ns            |
| $t_{\text{CKL}}$   | PTCK clock pulse width, low          |            | 20   | —    | —    | ns            |
| $f_{\text{MAX}}$   | Maximum PTCK clock frequency         |            | —    | —    | 25   | MHz           |
| $t_{\text{CO}}$    | Falling edge of PTCK to valid output |            | —    | —    | 15   | ns            |
| $t_{\text{PWV}}$   | Verify pulse width                   |            | 30   | —    | —    | $\mu\text{s}$ |
| $t_{\text{PWP}}$   | Programming pulse width              |            | 20   | —    | —    | ms            |

Figure 7. Erase (User Erase or Erase All) Timing Diagram

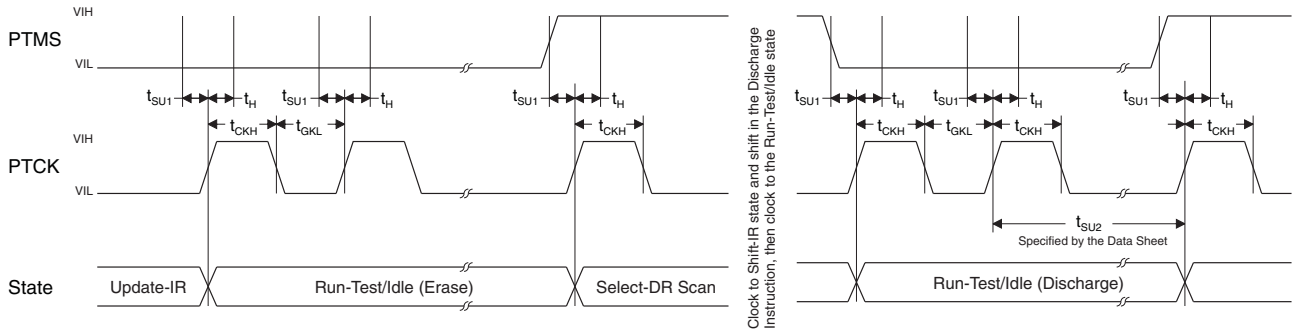
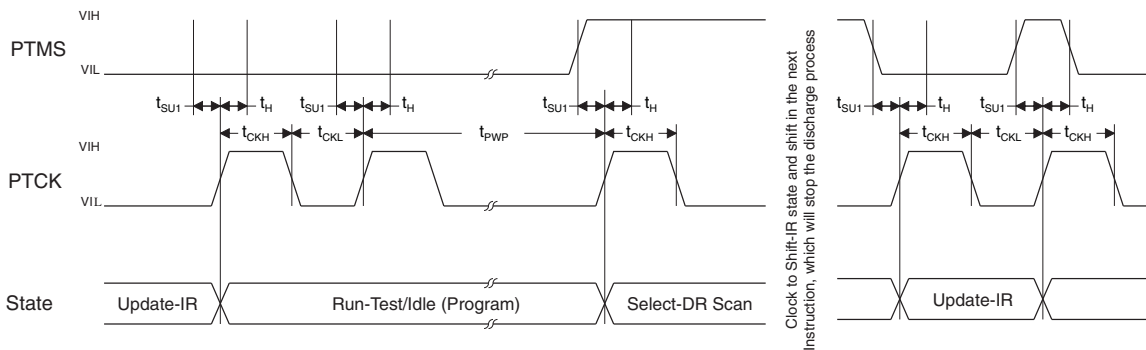
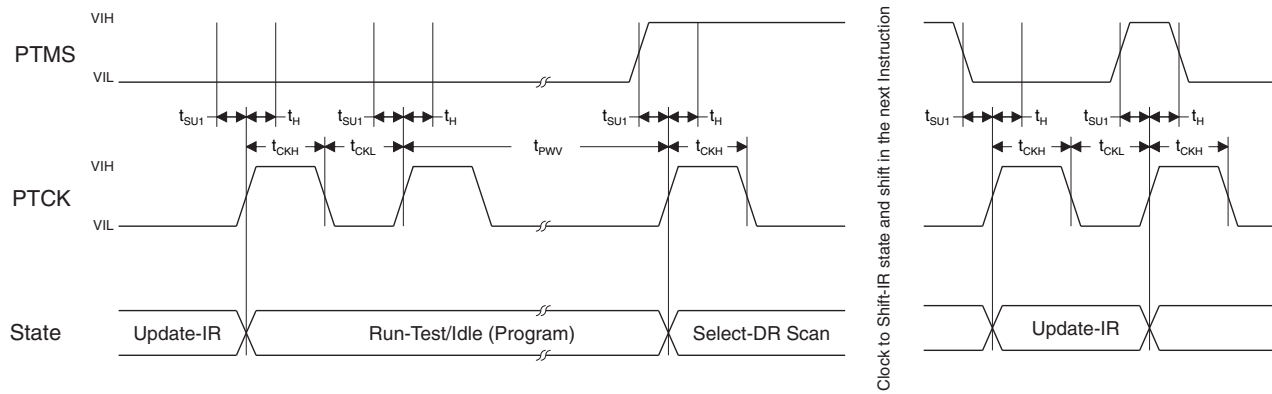


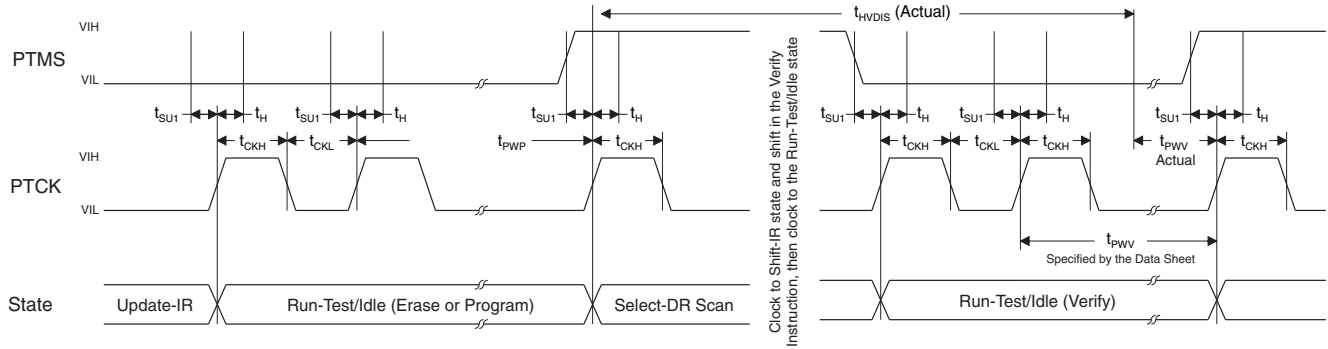
Figure 8. Programming Timing Diagram



**Figure 9. Verify Timing Diagram**



**Figure 10. Discharge Timing Diagram**



## Typical FPGA Building Block Function Performance<sup>1</sup>

### Pin-to-Pin Performance (LVCMOS25 12mA Drive)

| Function               | Timing | Units |
|------------------------|--------|-------|
| <b>Basic Functions</b> |        |       |
| 16-bit decoder         | 6.7    | ns    |
| 4:1 MUX                | 4.5    | ns    |
| 16:1 MUX               | 5.1    | ns    |

### Register-to-Register Performance

| Function                            | Timing | Units |
|-------------------------------------|--------|-------|
| <b>Basic Functions</b>              |        |       |
| 16:1 MUX                            | 487    | MHz   |
| 16-bit adder                        | 292    | MHz   |
| 16-bit counter                      | 388    | MHz   |
| 64-bit counter                      | 200    | MHz   |
| <b>Distributed Memory Functions</b> |        |       |
| 16x2 Single Port RAM                | 434    | MHz   |
| 64x2 Single Port RAM                | 320    | MHz   |
| 128x4 Single Port RAM               | 261    | MHz   |
| 32x2 Pseudo-Dual Port RAM           | 314    | MHz   |
| 64x4 Pseudo-Dual Port RAM           | 271    | MHz   |

1. The above timing numbers are generated using the Platform Manager design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

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## Derating Logic Timing

Logic Timing provided in the following sections of the data sheet and the Platform Manager design tool are worst case numbers in the operating range. Actual delays may be much faster. The Platform Manager design tool from Lattice can provide FPGA logic timing numbers at a particular temperature and voltage.

## FPGA Section External Switching Characteristics<sup>1</sup>

Over Recommended Operating Conditions

| Parameter  | Description                             | Min. | Max. | Units |
|--|---|------|------|-------|
| <b>General I/O Pin Parameters (Using Global Clock without PLL)<sup>1</sup></b> |   |      |      |       |
| t <sub>PD</sub>  | Best Case t <sub>PD</sub> Through 1 LUT | —    | 4.9  | ns    |
| t <sub>CO</sub>  | Best Case Clock to Output - From PFU    | —    | 5.7  | ns    |
| t <sub>SU</sub>  | Clock to Data Setup - To PFU            | 1.5  | —    | ns    |
| t <sub>H</sub>   | Clock to Data Hold - To PFU             | -0.1 | —    | ns    |
| f <sub>MAX_IO</sub>  | Clock Frequency of I/O and PFU Register | —    | 500  | MHz   |
| t <sub>SKEW_PRI</sub>  | Global Clock Skew Across Device         | —    | 240  | ps    |

1. General timing numbers based on LVCMOS2.5V, 12 mA.

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## FPGA Sleep Mode Timing

| Parameter            | Description              | Min. | Max. | Units |
|----------------------|--------------------------|------|------|-------|
| t <sub>PWRDN</sub>   | SLEEPN Low to Power Down | —    | 400  | ns    |
| t <sub>PWRUP</sub>   | SLEEPN High to Power Up  | —    | 600  | μs    |
| t <sub>WSLEEPN</sub> | SLEEPN Pulse Width       | 400  | —    | ns    |
| t <sub>WAWAKE</sub>  | SLEEPN Pulse Rejection   | —    | 100  | ns    |

## FPGA Section Internal Timing Parameters<sup>1</sup>

Over Recommended Operating Conditions

| Parameter                               | Description                                     | Min.  | Max. | Units |
|---|---|-------|------|-------|
| <b>PFU/PFF Logic Mode Timing</b>        |   |       |      |       |
| t <sub>LUT4_PFU</sub>                   | LUT4 delay (A to D inputs to F output)          | —     | 0.39 | ns    |
| t <sub>LUT6_PFU</sub>                   | LUT6 delay (A to D inputs to OFX output)        | —     | 0.62 | ns    |
| t <sub>LSR_PFU</sub>                    | Set/Reset to output of PFU                      | —     | 1.26 | ns    |
| t <sub>SUM_PFU</sub>                    | Clock to Mux (M0,M1) input setup time           | 0.15  | —    | ns    |
| t <sub>HM_PFU</sub>                     | Clock to Mux (M0,M1) input hold time            | -0.07 | —    | ns    |
| t <sub>SUD_PFU</sub>                    | Clock to D input setup time                     | 0.18  | —    | ns    |
| t <sub>HD_PFU</sub>                     | Clock to D input hold time                      | -0.04 | —    | ns    |
| t <sub>CK2Q_PFU</sub>                   | Clock to Q delay, D-type register configuration | —     | 0.56 | ns    |
| t <sub>LE2Q_PFU</sub>                   | Clock to Q delay latch configuration            | —     | 0.74 | ns    |
| t <sub>LD2Q_PFU</sub>                   | D to Q throughput delay when latch is enabled   | —     | 0.77 | ns    |
| <b>PFU Dual Port Memory Mode Timing</b> |   |       |      |       |
| t <sub>CORAM_PFU</sub>                  | Clock to Output                                 | —     | 0.56 | ns    |
| t <sub>SUDATA_PFU</sub>                 | Data Setup Time                                 | -0.25 | —    | ns    |
| t <sub>HDATA_PFU</sub>                  | Data Hold Time                                  | 0.39  | —    | ns    |
| t <sub>SUADDR_PFU</sub>                 | Address Setup Time                              | -0.65 | —    | ns    |
| t <sub>HADDR_PFU</sub>                  | Address Hold Time                               | 0.99  | —    | ns    |
| t <sub>SUWREN_PFU</sub>                 | Write/Read Enable Setup Time                    | -0.30 | —    | ns    |
| t <sub>HWREN_PFU</sub>                  | Write/Read Enable Hold Time                     | 0.47  | —    | ns    |
| <b>PIO Input/Output Buffer Timing</b>   |   |       |      |       |
| t <sub>IN_PIO</sub>                     | Input Buffer Delay                              | —     | 1.06 | ns    |
| t <sub>OUT_PIO</sub>                    | Output Buffer Delay                             | —     | 1.80 | ns    |

1. Internal parameters are characterized but not tested on every device.

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**FPGA Section Timing Adders<sup>1, 2, 3</sup>**
**Over Recommended Operating Conditions**

| Buffer Type             | Description            |       | Units |
|-------------------------|------------------------|-------|-------|
| <b>Input Adjusters</b>  |                        |       |       |
| LVTTL33                 | LVTTL                  | 0.01  | ns    |
| LVC MOS33               | LVC MOS 3.3            | 0.01  | ns    |
| LVC MOS25               | LVC MOS 2.5            | 0.00  | ns    |
| LVC MOS18               | LVC MOS 1.8            | 0.10  | ns    |
| LVC MOS15               | LVC MOS 1.5            | 0.19  | ns    |
| LVC MOS12               | LVC MOS 1.2            | 0.56  | ns    |
| <b>Output Adjusters</b> |                        |       |       |
| LVTTL33_4mA             | LVTTL 4mA drive        | 0.05  | ns    |
| LVTTL33_8mA             | LVTTL 8mA drive        | 0.08  | ns    |
| LVTTL33_12mA            | LVTTL 12mA drive       | -0.01 | ns    |
| LVTTL33_16mA            | LVTTL 16mA drive       | 0.70  | ns    |
| LVC MOS33_4mA           | LVC MOS 3.3 4mA drive  | 0.05  | ns    |
| LVC MOS33_8mA           | LVC MOS 3.3 8mA drive  | 0.08  | ns    |
| LVC MOS33_12mA          | LVC MOS 3.3 12mA drive | -0.01 | ns    |
| LVC MOS33_14mA          | LVC MOS 3.3 14mA drive | 0.70  | ns    |
| LVC MOS25_4mA           | LVC MOS 2.5 4mA drive  | 0.07  | ns    |
| LVC MOS25_8mA           | LVC MOS 2.5 8mA drive  | 0.13  | ns    |
| LVC MOS25_12mA          | LVC MOS 2.5 12mA drive | 0.00  | ns    |
| LVC MOS25_14mA          | LVC MOS 2.5 14mA drive | 0.47  | ns    |
| LVC MOS18_4mA           | LVC MOS 1.8 4mA drive  | 0.15  | ns    |
| LVC MOS18_8mA           | LVC MOS 1.8 8mA drive  | 0.06  | ns    |
| LVC MOS18_12mA          | LVC MOS 1.8 12mA drive | -0.08 | ns    |
| LVC MOS18_14mA          | LVC MOS 1.8 14mA drive | 0.09  | ns    |
| LVC MOS15_4mA           | LVC MOS 1.5 4mA drive  | 0.22  | ns    |
| LVC MOS15_8mA           | LVC MOS 1.5 8mA drive  | 0.07  | ns    |
| LVC MOS12_2mA           | LVC MOS 1.2 2mA drive  | 0.36  | ns    |
| LVC MOS12_6mA           | LVC MOS 1.2 6mA drive  | 0.07  | ns    |

1. Timing adders are characterized but not tested on every device.

2. LVC MOS timing is measured with the load specified in Switching Test Conditions table.

3. All other standards tested according to the appropriate specifications.

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## Flash Download Time

| Symbol               | Parameter  | Min. | Typ. | Max. | Units |
|----------------------|--|------|------|------|-------|
| $t_{\text{REFRESH}}$ | $V_{\text{CC}}$ or $V_{\text{CCAUX}}$ to Device I/O Active | —    | —    | 0.6  | ms    |

## FPGA JTAG Port Timing Specifications

| Symbol               | Parameter  | Min. | Max. | Units |
|----------------------|--|------|------|-------|
| $f_{\text{MAX}}$     | FTCK [BSCAN] clock frequency   | —    | 25   | MHz   |
| $t_{\text{BTCP}}$    | FTCK [BSCAN] clock pulse width                                       | 40   | —    | ns    |
| $t_{\text{BTCPH}}$   | FTCK [BSCAN] clock pulse width high                                  | 20   | —    | ns    |
| $t_{\text{BTCPL}}$   | FTCK [BSCAN] clock pulse width low                                   | 20   | —    | ns    |
| $t_{\text{BTS}}$     | FTCK [BSCAN] setup time  | 8    | —    | ns    |
| $t_{\text{BTH}}$     | FTCK [BSCAN] hold time   | 10   | —    | ns    |
| $t_{\text{BTRF}}$    | FTCK [BSCAN] rise/fall time  | 50   | —    | mV/ns |
| $t_{\text{BTCO}}$    | TAP controller falling edge of clock to output valid                 | —    | 10   | ns    |
| $t_{\text{BTCODIS}}$ | TAP controller falling edge of clock to output disabled              | —    | 10   | ns    |
| $t_{\text{BTCOEN}}$  | TAP controller falling edge of clock to output enabled               | —    | 10   | ns    |
| $t_{\text{BTCRS}}$   | BSCAN test capture register setup time                               | 8    | —    | ns    |
| $t_{\text{BTCRH}}$   | BSCAN test capture register hold time                                | 25   | —    | ns    |
| $t_{\text{BUTCO}}$   | BSCAN test update register, falling edge of clock to output valid    | —    | 25   | ns    |
| $t_{\text{BTUODIS}}$ | BSCAN test update register, falling edge of clock to output disabled | —    | 25   | ns    |
| $t_{\text{BTUPOEN}}$ | BSCAN test update register, falling edge of clock to output enabled  | —    | 25   | ns    |

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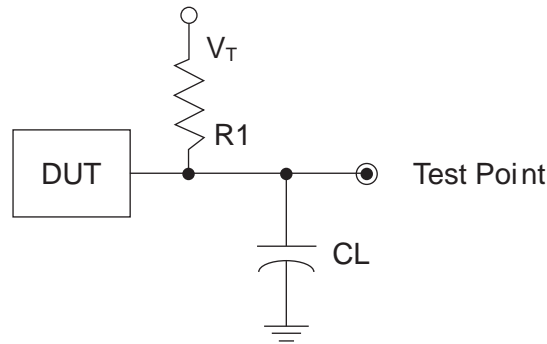




## FPGA Output Switching Test Conditions

Figure 12 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 2.

**Figure 12. Output Test Load, LVTTTL and LVCMOS Standards**



**Table 2. Test Fixture Required Components, Non-Terminated Interfaces**

| Test Condition                              | R <sub>1</sub> | C <sub>L</sub> | Timing Ref.                       | V <sub>T</sub>  |
|---|----------------|----------------|-----------------------------------|-----------------|
| LVTTTL and LVCMOS settings (L -> H, H -> L) | ∞              | 0pF            | LVTTTL, LVCMOS 3.3 = 1.5V         | —               |
|   |                |                | LVCMOS 2.5 = V <sub>CCIO</sub> /2 | —               |
|   |                |                | LVCMOS 1.8 = V <sub>CCIO</sub> /2 | —               |
|   |                |                | LVCMOS 1.5 = V <sub>CCIO</sub> /2 | —               |
|   |                |                | LVCMOS 1.2 = V <sub>CCIO</sub> /2 | —               |
| LVTTTL and LVCMOS 3.3 (Z -> H)              | 188            | 0pF            | 1.5                               | V <sub>OL</sub> |
| LVTTTL and LVCMOS 3.3 (Z -> L)              |                |                |                                   | V <sub>OH</sub> |
| Other LVCMOS (Z -> H)                       |                |                | V <sub>CCIO</sub> /2              | V <sub>OL</sub> |
| Other LVCMOS (Z -> L)                       |                |                | V <sub>CCIO</sub> /2              | V <sub>OH</sub> |
| LVTTTL + LVCMOS (H -> Z)                    |                |                | V <sub>OH</sub> - 0.15            | V <sub>OL</sub> |
| LVTTTL + LVCMOS (L -> Z)                    |                |                | V <sub>OL</sub> - 0.15            | V <sub>OH</sub> |

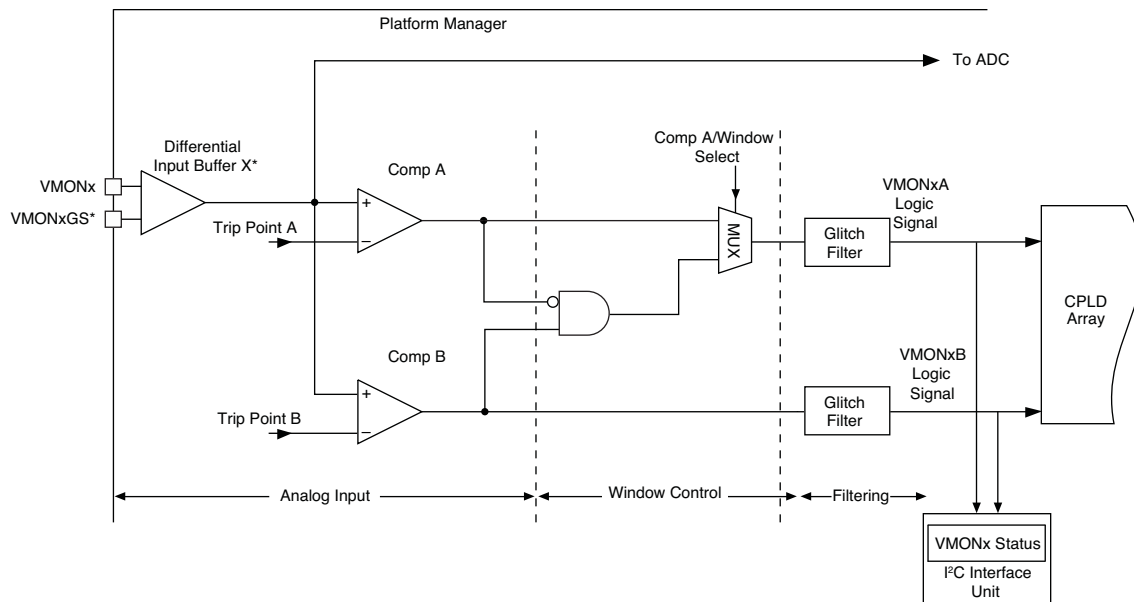
Note: Output test conditions for all other interfaces are determined by the respective standards.

## Architecture Details

### Analog Monitor Inputs

The Platform Manager provides 12 independently programmable voltage monitor input circuits as shown in Figure 13. Two individually programmable trip-point comparators are connected to an analog monitoring input. Each comparator reference has 368 programmable trip points over the range of 0.664V to 5.734V. Additionally, a 75mV ‘zero-detect’ threshold is selectable which allows the voltage monitors to determine if a monitored signal has dropped to ground level. This feature is especially useful for determining if a power supply’s output has decayed to a substantially inactive condition after it has been switched off.

**Figure 13. Platform Manager Voltage Monitors**



\*Differential Input Buffer X and VMONxGS pins are not present for single-ended VMONx inputs in the 128-pin TQFP package option.

Figure 13 shows the functional block diagram of one of the 12 voltage monitor inputs - ‘x’ (where x = 1...12). Each voltage monitor can be divided into three sections: Analog Input, Window Control, and Filtering. The first section provides a differential input buffer to monitor the power supply voltage through VMONx+ (to sense the positive terminal of the supply) and VMONxGS (to sense the power supply ground). Differential voltage sensing minimizes inaccuracies in voltage measurement with ADC and monitor thresholds due to the potential difference between the Platform Manager device ground and the ground potential at the sensed node on the circuit board.

The voltage output of the differential input buffer is monitored by two individually programmable trip-point comparators, shown as CompA and CompB. Table 3 shows all 368 trip points spanning the range 0.664V to 5.734V to which a comparator’s threshold can be set. Note that for the 128-pin TQFP package option, the differential input buffer shown above is not present for any of the single-ended VMON input pins. Those pins are: 59 (VMON1), 83 (VMON9), 84 (VMON10), 86 (VMON11), 88 (VMON12).

Each comparator outputs a HIGH signal to the CPLD if the voltage at its positive terminal is greater than its programmed trip point setting, otherwise it outputs a LOW signal.

Hysteresis is provided by the comparators to reduce false triggering as a result of input noise. The hysteresis provided by the voltage monitor is a function of the input divider setting. Table 5 lists the typical hysteresis versus voltage monitor trip-point.

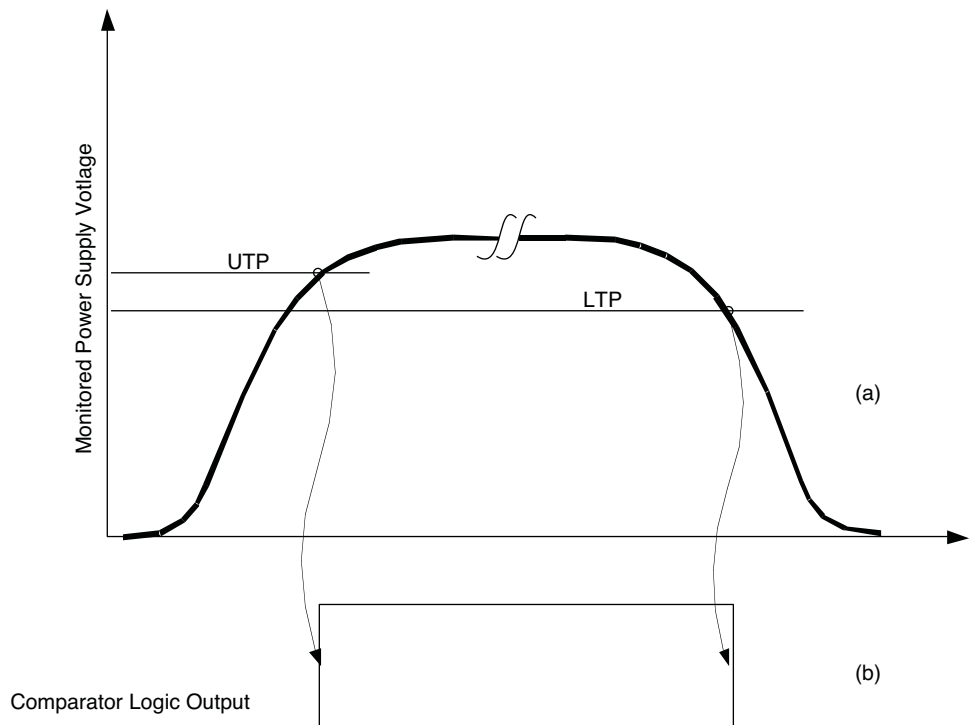
## AGOOD Logic Signal

All the VMON comparators auto-calibrate immediately after a power-on reset event. During this time, the digital glitch filters are also initialized. This process completion is signalled by an internally generated logic signal: AGOOD. All logic using the VMON comparator logic signals must wait for the AGOOD signal to become active.

## Programmable Over-Voltage and Under-Voltage Thresholds

Figure 14 (a) shows the power supply ramp-up and ramp-down voltage waveforms. Because of hysteresis, the comparator outputs change state at different thresholds depending on the direction of excursion of the monitored power supply.

**Figure 14. (a) Power Supply Voltage Ramp-up and Ramp-down Waveform and the Resulting Comparator Output, (b) Corresponding to Upper and Lower Trip Points**



During power supply ramp-up the comparator output changes from logic 0 to 1 when the power supply voltage crosses the upper trip point (UTP). During ramp down the comparator output changes from logic state 1 to 0 when the power supply voltage crosses the lower trip point (LTP). To monitor for over voltage fault conditions, the UTP should be used. To monitor under-voltage fault conditions, the LTP should be used.

Tables 3 and 4 show both the under-voltage and over-voltage trip points, which are automatically selected in software depending on whether the user is monitoring for an over-voltage condition or an under-voltage condition.

**Table 3. Trip Point Table Used For Over-Voltage Detection**

| Fine Range Setting | Coarse Range Setting |       |       |       |       |       |       |       |       |       |       |       |
|--------------------|----------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
|                    | 1                    | 2     | 3     | 4     | 5     | 6     | 7     | 8     | 9     | 10    | 11    | 12    |
| 1                  | 0.790                | 0.941 | 1.120 | 1.333 | 1.580 | 1.885 | 2.244 | 2.665 | 3.156 | 3.758 | 4.818 | 5.734 |
| 2                  | 0.786                | 0.936 | 1.114 | 1.326 | 1.571 | 1.874 | 2.232 | 2.650 | 3.139 | 3.738 | 4.792 | 5.703 |
| 3                  | 0.782                | 0.930 | 1.108 | 1.319 | 1.563 | 1.864 | 2.220 | 2.636 | 3.123 | 3.718 | 4.766 | 5.674 |
| 4                  | 0.778                | 0.926 | 1.102 | 1.312 | 1.554 | 1.854 | 2.209 | 2.622 | 3.106 | 3.698 | 4.741 | 5.643 |
| 5                  | 0.773                | 0.921 | 1.096 | 1.305 | 1.546 | 1.844 | 2.197 | 2.607 | 3.089 | 3.678 | 4.715 | 5.612 |
| 6                  | 0.769                | 0.916 | 1.090 | 1.298 | 1.537 | 1.834 | 2.185 | 2.593 | 3.072 | 3.657 | 4.689 | 5.581 |
| 7                  | 0.765                | 0.911 | 1.084 | 1.290 | 1.529 | 1.825 | 2.173 | 2.579 | 3.056 | 3.637 | 4.663 | 5.550 |
| 8                  | 0.761                | 0.906 | 1.078 | 1.283 | 1.520 | 1.815 | 2.161 | 2.565 | 3.039 | 3.618 | 4.638 | 5.520 |
| 9                  | 0.756                | 0.901 | 1.072 | 1.276 | 1.512 | 1.805 | 2.149 | 2.550 | 3.022 | 3.598 | 4.612 | 5.489 |
| 10                 | 0.752                | 0.896 | 1.066 | 1.269 | 1.503 | 1.795 | 2.137 | 2.536 | 3.005 | 3.578 | 4.586 | 5.459 |
| 11                 | 0.748                | 0.891 | 1.060 | 1.262 | 1.495 | 1.785 | 2.125 | 2.522 | 2.988 | 3.558 | 4.561 | 5.428 |
| 12                 | 0.744                | 0.886 | 1.054 | 1.255 | 1.486 | 1.774 | 2.113 | 2.507 | 2.971 | 3.537 | 4.535 | 5.397 |
| 13                 | 0.739                | 0.881 | 1.048 | 1.248 | 1.478 | 1.764 | 2.101 | 2.493 | 2.954 | 3.517 | 4.509 | 5.366 |
| 14                 | 0.735                | 0.876 | 1.042 | 1.240 | 1.470 | 1.754 | 2.089 | 2.479 | 2.937 | 3.497 | 4.483 | 5.336 |
| 15                 | 0.731                | 0.871 | 1.036 | 1.233 | 1.461 | 1.744 | 2.077 | 2.465 | 2.920 | 3.477 | 4.457 | 5.305 |
| 16                 | 0.727                | 0.866 | 1.030 | 1.226 | 1.453 | 1.734 | 2.064 | 2.450 | 2.903 | 3.457 | 4.431 | 5.274 |
| 17                 | 0.723                | 0.861 | 1.024 | 1.219 | 1.444 | 1.724 | 2.052 | 2.436 | 2.886 | 3.437 | 4.406 | 5.244 |
| 18                 | 0.718                | 0.856 | 1.018 | 1.212 | 1.436 | 1.714 | 2.040 | 2.422 | 2.869 | 3.416 | 4.380 | 5.213 |
| 19                 | 0.714                | 0.851 | 1.012 | 1.205 | 1.427 | 1.704 | 2.028 | 2.407 | 2.852 | 3.396 | 4.355 | 5.183 |
| 20                 | 0.710                | 0.846 | 1.006 | 1.198 | 1.419 | 1.694 | 2.016 | 2.393 | 2.836 | 3.376 | 4.329 | 5.152 |
| 21                 | 0.706                | 0.841 | 1.000 | 1.190 | 1.410 | 1.684 | 2.004 | 2.379 | 2.819 | 3.356 | 4.303 | 5.121 |
| 22                 | 0.701                | 0.836 | 0.994 | 1.183 | 1.402 | 1.673 | 1.992 | 2.365 | 2.802 | 3.336 | 4.277 | 5.090 |
| 23                 | 0.697                | 0.831 | 0.988 | 1.176 | 1.393 | 1.663 | 1.980 | 2.350 | 2.785 | 3.316 | 4.251 | 5.059 |
| 24                 | 0.693                | 0.826 | 0.982 | 1.169 | 1.385 | 1.653 | 1.968 | 2.337 | 2.768 | 3.296 | 4.225 | 5.030 |
| 25                 | 0.689                | 0.821 | 0.976 | 1.162 | 1.376 | 1.643 | 1.956 | 2.323 | 2.752 | 3.276 | 4.199 | 4.999 |
| 26                 | 0.684                | 0.816 | 0.970 | 1.155 | 1.369 | 1.633 | 1.944 | 2.309 | 2.735 | 3.256 | 4.174 | 4.968 |
| 27                 | 0.680                | 0.810 | 0.964 | 1.148 | 1.361 | 1.623 | 1.932 | 2.294 | 2.718 | 3.236 | 4.149 | 4.937 |
| 28                 | 0.676                | 0.805 | 0.958 | 1.140 | 1.352 | 1.613 | 1.920 | 2.280 | 2.701 | 3.216 | 4.123 | 4.906 |
| 29                 | 0.672                | 0.800 | 0.952 | 1.133 | 1.344 | 1.603 | 1.908 | 2.266 | 2.684 | 3.196 | 4.097 | 4.876 |
| 30                 | 0.668                | 0.795 | 0.946 | 1.126 | —     | 1.593 | 1.896 | 2.251 | —     | 3.176 | 4.071 | 4.845 |
| Low-V Sense        | 75mV                 |       |       |       |       |       |       |       |       |       |       |       |

**Table 4. Trip Point Table Used For Under-Voltage Detection**

| Fine Range Setting | Coarse Range Setting |       |       |       |       |       |       |       |       |       |       |       |
|--------------------|----------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
|                    | 1                    | 2     | 3     | 4     | 5     | 6     | 7     | 8     | 9     | 10    | 11    | 12    |
| 1                  | 0.786                | 0.936 | 1.114 | 1.326 | 1.571 | 1.874 | 2.232 | 2.650 | 3.139 | 3.738 | 4.792 | 5.703 |
| 2                  | 0.782                | 0.930 | 1.108 | 1.319 | 1.563 | 1.864 | 2.220 | 2.636 | 3.123 | 3.718 | 4.766 | 5.674 |
| 3                  | 0.778                | 0.926 | 1.102 | 1.312 | 1.554 | 1.854 | 2.209 | 2.622 | 3.106 | 3.698 | 4.741 | 5.643 |
| 4                  | 0.773                | 0.921 | 1.096 | 1.305 | 1.546 | 1.844 | 2.197 | 2.607 | 3.089 | 3.678 | 4.715 | 5.612 |
| 5                  | 0.769                | 0.916 | 1.090 | 1.298 | 1.537 | 1.834 | 2.185 | 2.593 | 3.072 | 3.657 | 4.689 | 5.581 |
| 6                  | 0.765                | 0.911 | 1.084 | 1.290 | 1.529 | 1.825 | 2.173 | 2.579 | 3.056 | 3.637 | 4.663 | 5.550 |
| 7                  | 0.761                | 0.906 | 1.078 | 1.283 | 1.520 | 1.815 | 2.161 | 2.565 | 3.039 | 3.618 | 4.638 | 5.520 |
| 8                  | 0.756                | 0.901 | 1.072 | 1.276 | 1.512 | 1.805 | 2.149 | 2.550 | 3.022 | 3.598 | 4.612 | 5.489 |
| 9                  | 0.752                | 0.896 | 1.066 | 1.269 | 1.503 | 1.795 | 2.137 | 2.536 | 3.005 | 3.578 | 4.586 | 5.459 |
| 10                 | 0.748                | 0.891 | 1.060 | 1.262 | 1.495 | 1.785 | 2.125 | 2.522 | 2.988 | 3.558 | 4.561 | 5.428 |
| 11                 | 0.744                | 0.886 | 1.054 | 1.255 | 1.486 | 1.774 | 2.113 | 2.507 | 2.971 | 3.537 | 4.535 | 5.397 |
| 12                 | 0.739                | 0.881 | 1.048 | 1.248 | 1.478 | 1.764 | 2.101 | 2.493 | 2.954 | 3.517 | 4.509 | 5.366 |
| 13                 | 0.735                | 0.876 | 1.042 | 1.240 | 1.470 | 1.754 | 2.089 | 2.479 | 2.937 | 3.497 | 4.483 | 5.336 |
| 14                 | 0.731                | 0.871 | 1.036 | 1.233 | 1.461 | 1.744 | 2.077 | 2.465 | 2.920 | 3.477 | 4.457 | 5.305 |
| 15                 | 0.727                | 0.866 | 1.030 | 1.226 | 1.453 | 1.734 | 2.064 | 2.450 | 2.903 | 3.457 | 4.431 | 5.274 |
| 16                 | 0.723                | 0.861 | 1.024 | 1.219 | 1.444 | 1.724 | 2.052 | 2.436 | 2.886 | 3.437 | 4.406 | 5.244 |
| 17                 | 0.718                | 0.856 | 1.018 | 1.212 | 1.436 | 1.714 | 2.040 | 2.422 | 2.869 | 3.416 | 4.380 | 5.213 |
| 18                 | 0.714                | 0.851 | 1.012 | 1.205 | 1.427 | 1.704 | 2.028 | 2.407 | 2.852 | 3.396 | 4.355 | 5.183 |
| 19                 | 0.710                | 0.846 | 1.006 | 1.198 | 1.419 | 1.694 | 2.016 | 2.393 | 2.836 | 3.376 | 4.329 | 5.152 |
| 20                 | 0.706                | 0.841 | 1.000 | 1.190 | 1.410 | 1.684 | 2.004 | 2.379 | 2.819 | 3.356 | 4.303 | 5.121 |
| 21                 | 0.701                | 0.836 | 0.994 | 1.183 | 1.402 | 1.673 | 1.992 | 2.365 | 2.802 | 3.336 | 4.277 | 5.090 |
| 22                 | 0.697                | 0.831 | 0.988 | 1.176 | 1.393 | 1.663 | 1.980 | 2.350 | 2.785 | 3.316 | 4.251 | 5.059 |
| 23                 | 0.693                | 0.826 | 0.982 | 1.169 | 1.385 | 1.653 | 1.968 | 2.337 | 2.768 | 3.296 | 4.225 | 5.030 |
| 24                 | 0.689                | 0.821 | 0.976 | 1.162 | 1.376 | 1.643 | 1.956 | 2.323 | 2.752 | 3.276 | 4.199 | 4.999 |
| 25                 | 0.684                | 0.816 | 0.970 | 1.155 | 1.369 | 1.633 | 1.944 | 2.309 | 2.735 | 3.256 | 4.174 | 4.968 |
| 26                 | 0.680                | 0.810 | 0.964 | 1.148 | 1.361 | 1.623 | 1.932 | 2.294 | 2.718 | 3.236 | 4.149 | 4.937 |
| 27                 | 0.676                | 0.805 | 0.958 | 1.140 | 1.352 | 1.613 | 1.920 | 2.280 | 2.701 | 3.216 | 4.123 | 4.906 |
| 28                 | 0.672                | 0.800 | 0.952 | 1.133 | 1.344 | 1.603 | 1.908 | 2.266 | 2.684 | 3.196 | 4.097 | 4.876 |
| 29                 | 0.668                | 0.795 | 0.946 | 1.126 | 1.335 | 1.593 | 1.896 | 2.251 | 2.667 | 3.176 | 4.071 | 4.845 |
| 30                 | 0.664                | 0.790 | 0.940 | 1.119 | —     | 1.583 | 1.884 | 2.236 | —     | 3.156 | 4.045 | 4.815 |
| Low-V Sense        | 75mV                 |       |       |       |       |       |       |       |       |       |       |       |

**Table 5. Comparator Hysteresis vs. Trip-Point**

| Trip-point Range (V) |            | Hysteresis (mV) |
|----------------------|------------|-----------------|
| Low Limit            | High Limit |                 |
| 0.664                | 0.79       | 8               |
| 0.79                 | 0.941      | 10              |
| 0.94                 | 1.12       | 12              |
| 1.119                | 1.333      | 14              |
| 1.326                | 1.58       | 17              |
| 1.583                | 1.885      | 20              |
| 1.884                | 2.244      | 24              |
| 2.236                | 2.665      | 28              |
| 2.65                 | 3.156      | 34              |
| 3.156                | 3.758      | 40              |
| 4.045                | 4.818      | 51              |
| 4.815                | 5.734      | 61              |
| 75 mV                |            | 0 (Disabled)    |

The window control section of the voltage monitor circuit is an AND gate (with inputs: an inverted COMPA “ANDed” with COMPB signal) and a multiplexer that supports the ability to develop a ‘window’ function without using any of the CPLD resources. Through the use of the multiplexer, voltage monitor’s ‘A’ output may be set to report either the status of the ‘A’ comparator, or the window function of both comparator outputs. The voltage monitor’s ‘A’ output indicates whether the input signal is between or outside the two comparator thresholds. **Important:** This windowing function is only valid in cases where the threshold of the ‘A’ comparator is set to a value higher than that of the ‘B’ comparator. Table 6 shows the operation of window function logic.

**Table 6. Voltage Monitor Windowing Logic**

| Input Voltage  | Comp A | Comp B | Window (B and Not A) | Comment              |
|--|--------|--------|----------------------|----------------------|
| $V_{IN} < \text{Trip-point B} < \text{Trip-point A}$ | 0      | 0      | 0                    | Outside window, low  |
| $\text{Trip-point B} < V_{IN} < \text{Trip-point A}$ | 0      | 1      | 1                    | Inside window        |
| $\text{Trip-point B} < \text{Trip-point A} < V_{IN}$ | 1      | 1      | 0                    | Outside window, high |

Note that when the ‘A’ output of the voltage monitor circuit is set to windowing mode, the ‘B’ output continues to monitor the output of the ‘B’ comparator. This can be useful in that the ‘B’ output can be used to augment the windowing function by determining if the input is above or below the windowing range.

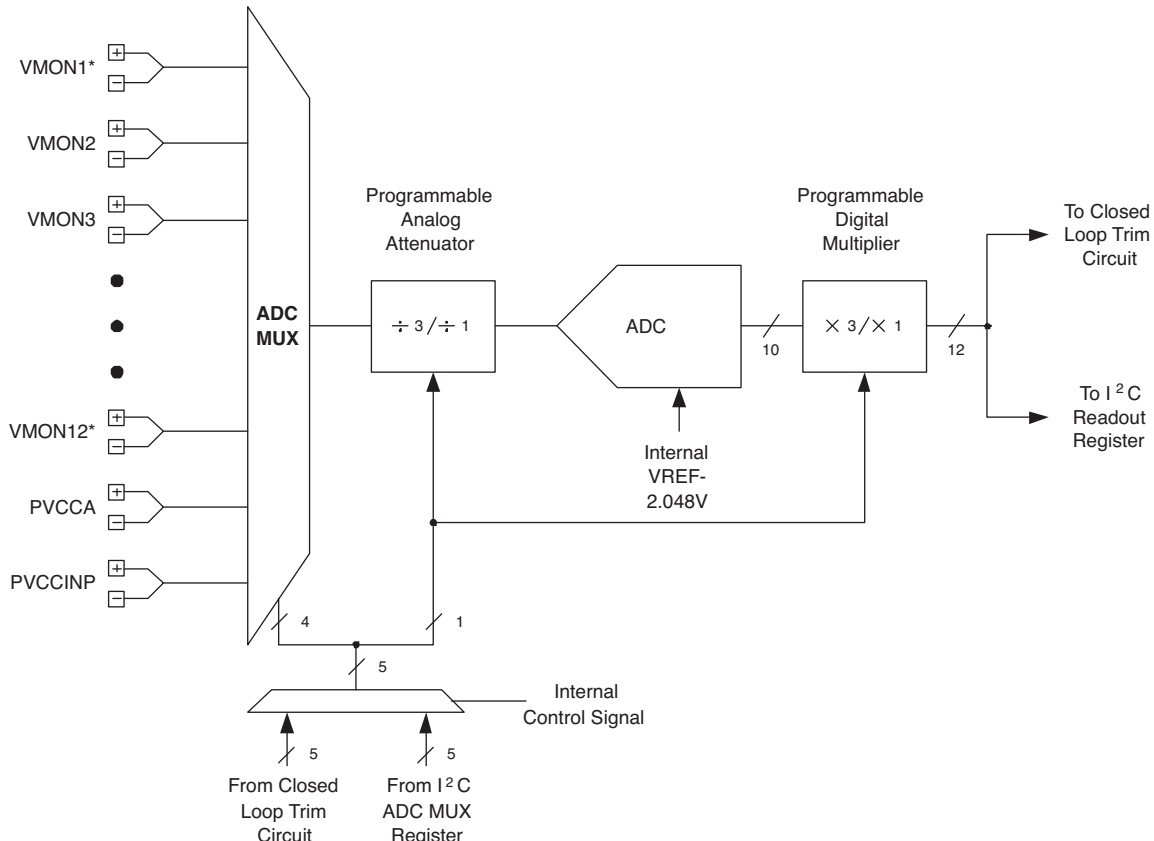
The third section in the Platform Manager’s input voltage monitor is a digital filter. When enabled, the comparator output will be delayed by a filter time constant of 64  $\mu\text{s}$ , and is especially useful for reducing the possibility of false triggering from noise that may be present on the voltages being monitored. When the filter is disabled, the comparator output will be delayed by 16  $\mu\text{s}$ . In both cases, enabled or disabled, the filters also provide synchronization of the input signals to the CPLD clock. This synchronous sampling feature effectively eliminates the possibility of race conditions from occurring in any subsequent logic that is implemented in the Platform Manager’s internal CPLD logic.

The comparator status can be read from the I<sup>2</sup>C interface. For details on the I<sup>2</sup>C interface, please refer to the I<sup>2</sup>C/SMBUS Interface section of this data sheet.

### VMON Voltage Measurement with the Internal Analog to Digital Converter (ADC)

The Platform Manager has an internal analog to digital converter that can be used for measuring the voltages at the VMON inputs. The ADC is also used in closed loop trimming of DC-DC converters. Close loop trimming is covered later in this document.

Figure 15. ADC Monitoring VMON1 to VMON12



\*VMON1 and VMON9 to VMON12 are single-ended inputs for the 128-pin TQFP package option.

Figure 15 shows the ADC circuit arrangement within the Platform Manager device. The ADC can measure all analog input voltages through the multiplexer, ADC MUX. The programmable attenuator between the ADC mux and the ADC can be configured as divided-by-3 or divided-by-1 (no attenuation). The divided-by-3 setting is used to measure voltages from 0V to 6V range and divided-by-1 setting is used to measure the voltages from 0V to 2V range. Note that for the 128-pin TQFP package option, the VMON1 and VMON9 to VMON12 input pins are single-ended inputs, not differential as shown above.

A microcontroller can place a request for any VMON voltage measurement at any time through the I<sup>2</sup>C bus. Upon the receipt of an I<sup>2</sup>C command, the ADC will be connected to the I<sup>2</sup>C selected VMON through the ADC MUX. The ADC output is then latched into the I<sup>2</sup>C readout registers.

#### Calculation

The algorithm to convert the ADC code to the corresponding voltage takes into consideration the attenuation bit value. In other words, if the attenuation bit is set, then the 10-bit ADC result is automatically multiplied by 3 to calculate the actual voltage at that V<sub>MON</sub> input. Thus, the I<sup>2</sup>C readout register is 12 bits instead of 10 bits. The following formula can always be used to calculate the actual voltage from the ADC code.

**Voltage at the VMONx Pins**

$VMON = ADC \text{ code (12 bits}^1, \text{ converted to decimal)} * 2mV$

<sup>1</sup>Note: ADC\_VALUE\_HIGH (8 bits), ADC\_VALUE\_LOW (4 bits) read from I<sup>2</sup>C/SMBUS interface

**Controlling Power Supply Output Voltage by Margin/Trim Block**

One of the key features of the Platform Manager is its ability to make adjustments to the power supplies that it may also be monitoring and/or sequencing. This is accomplished through the Trim and Margin Block of the device. The Trim and Margin Block can adjust voltages of up to eight different power supplies through TrimCells as shown in Figure 16. The DC-DC blocks in the figure represent virtually any type of DC power supply that has a trim or voltage adjustment input. This can be an off-the-shelf unit or custom circuit designed around a switching regulator IC.

The interface between the Platform Manager and the DC power supply is represented by a single resistor (R1 to R8) to simplify the diagram. Each of these resistors represents a resistor network.

Other control signals driving the Margin/Trim Block are:

- CPLD\_VPS[1:0] – Voltage profile selection signals generated by the CPLD. These control signals are common to all eight TrimCells and are used to select the active voltage profile for all TrimCells together.
- ADC input – Used to determine the trimmed DC-DC converter voltage.
- CPLD\_CLT\_EN – Only from the CPLD, used to enable closed loop trimming of all TrimCells together.

Next to each DC-DC converter, four voltages are shown. These voltages correspond to the operating voltage profile of the Margin/Trim Block.

When the CPLD\_VPS[1:0] = 00, representing Voltage Profile 0: (Voltage Profile 0 is recommended to be used for the normal circuit operation)

The output voltage of the DC-DC converter controlled by the Trim 1 pin of the Platform Manager will be 1V and that TrimCell is operating in closed loop trim mode. At the same time, the DC-DC converters controlled by Trim 2, Trim 3 and Trim 8 pins output 1.2V, 1.5V and 3.3V respectively.

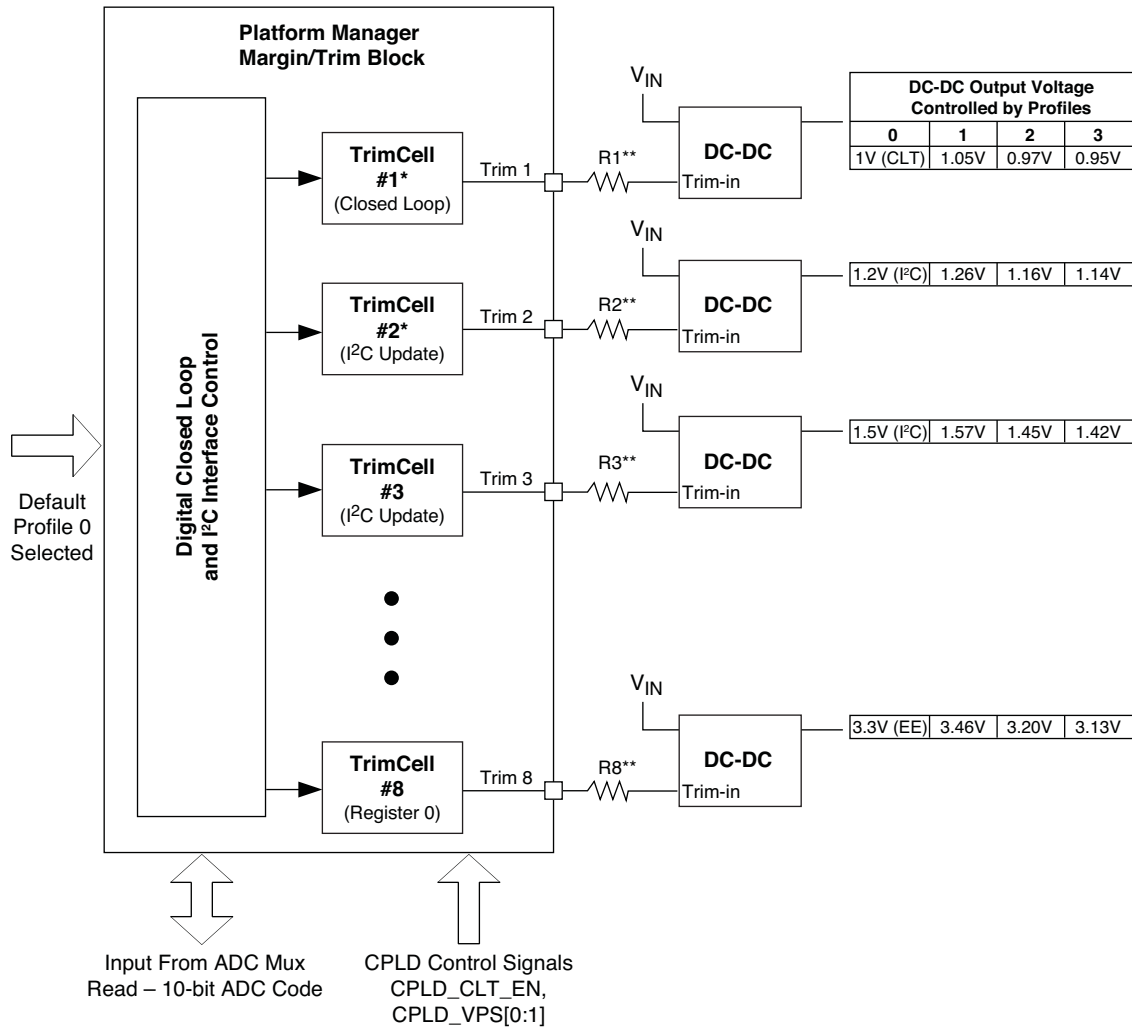
When the CPLD\_VPS[1:0] = 01, representing Voltage Profile 1 being active:

The DC-DC output voltage controlled by Trim 1, 2, 3, and 8 pins will be 1.05V, 1.26V, 1.57V, and 3.46V. These supply voltages correspond to 5% above their respective normal operating voltage (also called as margin high).

Similarly, when CPLD\_VPS[1:0] = 11, all DC-DC converters are margined low by 5%.



Figure 16. Platform Manager Trim and Margin Block



\*TrimCell #1 and TrimCell #2 (Trim 1 and Trim 2) are not available in the 128-pin TQFP package option.  
\*\*Indicates resistor network

There are up to eight TrimCells in the Platform Manager device, enabling simultaneous control of up to eight individual power supplies (six in the 128-pin TQFP package option). Each TrimCell can generate up to four trimming voltages to control the output voltage of the DC-DC converter.

Figure 17. TrimCell Driving a Typical DC-DC Converter

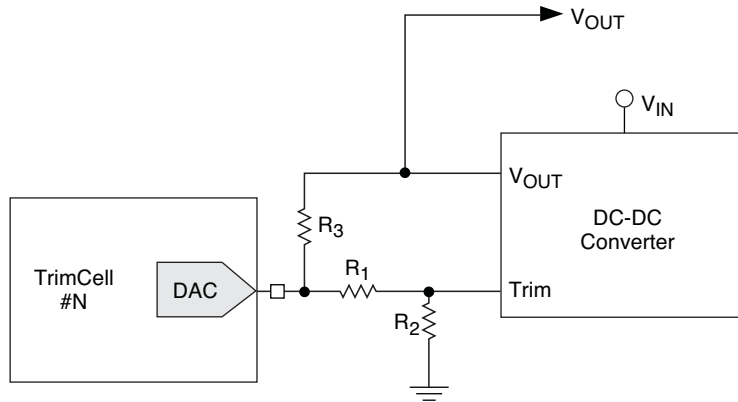
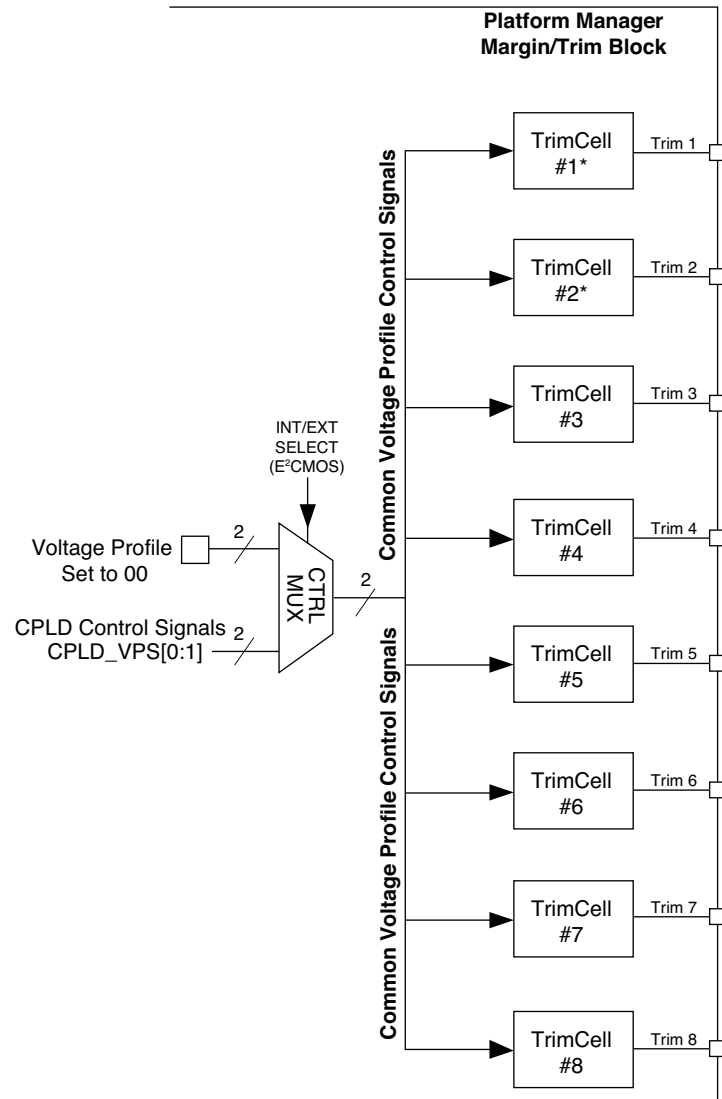


Figure 17 shows the resistor network between the TrimCell #N in the Platform Manager and the DC-DC converter. The values of these resistors depend on the type of DC-DC converter used and its operating voltage range. The method to calculate the values of the resistors R1, R2, and R3 are described in a separate application note.

**Voltage Profile Control**

The Platform Manager Margin/TrimBlock consists of up to eight TrimCells. Each of these trim cells integrates four output voltage configurations. The operational voltage profile of the TrimCell is determined by two bits called voltage profile selection bits. The TrimBlock provides 2-bit voltage profile selection bits which are shared by all eight TrimCells. The TrimBlock voltage profile can be set to profile zero or can be controlled by the CPLD through signals CPLD\_VPS[0:1]. An E<sup>2</sup>CMOS<sup>®</sup> configuration bit determines whether the voltage profile control is set to profile 0 or it is controlled by CPLD.

Figure 18. Voltage Profile Control



\*TrimCell #1 and TrimCell #2 (Trim 1 and Trim 2) are not available in the 128-pin TQFP package option.

### TrimCell Architecture

The TrimCell block diagram is shown in Figure 19. The 8-bit DAC at the output provides the trimming voltage required to set the output voltage of a programmable supply. Each TrimCell can be operated in any one of the four voltage profiles. In each voltage profile the output trimming voltage can be set to a preset value. There are six 8-bit registers in each TrimCell that, depending on the operational mode, set the DAC value. Of these, four DAC values (DAC Register 0 to DAC Register 3) are stored in the E<sup>2</sup>CMOS memory while the remaining register contents are stored in volatile registers. Two multiplexers (Mode Mux and Profile Mux) control the routing of the code to the DAC. The Profile Mux can be controlled by common TrimCell voltage profile control signals.

Figure 19. Platform Manager Output TrimCell

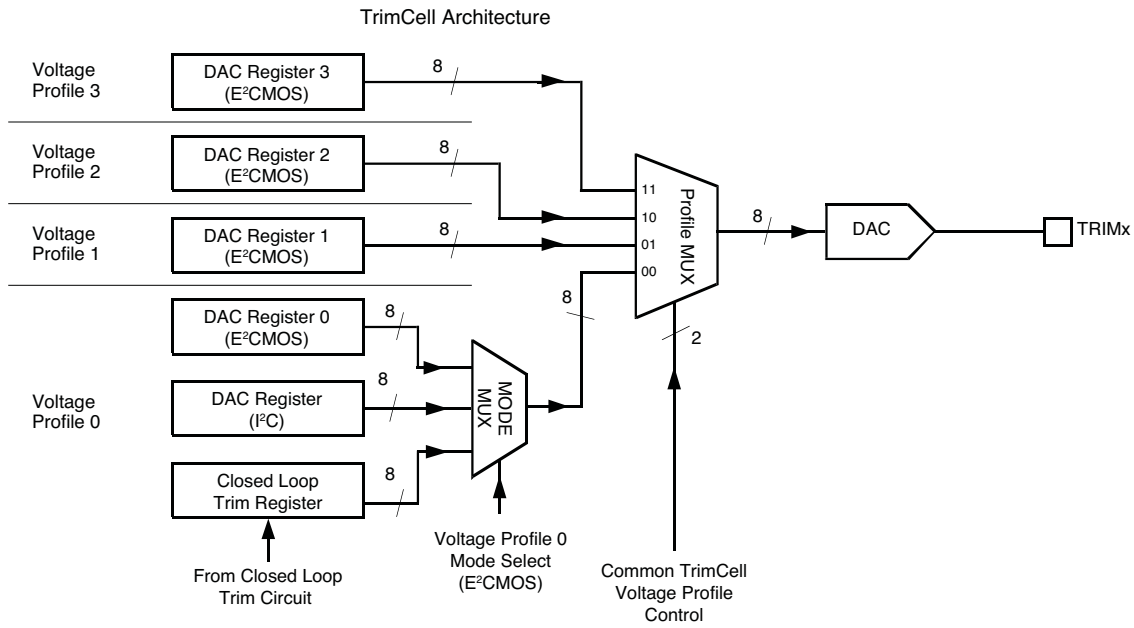


Figure 16 shows four power supply voltages next to each DC-DC converter. When the Profile MUX is set to Voltage Profile 3, the DC supply controlled by Trim 1 will be at 0.95V, the DC supply controlled by Trim 2 will be at 1.14V, 1.43V for Trim 3 and 3.14V for Trim 8. When Voltage Profile 0 is selected, Trim 1 will set the supply to 1V, Trim 2 and Trim 3 will be set by the values that have been loaded using I<sup>2</sup>C at 1.2 and 1.5V, and Trim 8 will be set to 3.3V.

Table 7 summarizes the voltage profile selection and the corresponding DAC output trimming voltage. The voltage profile selection is common to all eight TrimCells.

Table 7. TrimCell Voltage Profile and Operating Modes

| CPLD_VPS[1:0] | Selected Voltage Profile | Selected Mode                        | Trimming Voltage is Controlled by    |
|---------------|--------------------------|--------------------------------------|--------------------------------------|
| 11            | Voltage Profile 3        | —                                    | DAC Register 3 (E <sup>2</sup> CMOS) |
| 10            | Voltage Profile 2        | —                                    | DAC Register 2 (E <sup>2</sup> CMOS) |
| 01            | Voltage Profile 1        | —                                    | DAC Register 1 (E <sup>2</sup> CMOS) |
| 00            | Voltage Profile 0        | DAC Register 0 Select                | DAC Register 0 (E <sup>2</sup> CMOS) |
|               |                          | DAC Register I <sup>2</sup> C Select | DAC Register (I <sup>2</sup> C)      |
|               |                          | Digital Closed Loop Trim             | Closed Loop Trim Register            |

**TrimCell Operation in Voltage Profiles 1, 2 and 3:** The output trimming voltage is determined by the code stored in the DAC Registers 1, 2, and 3 corresponding to the selected Voltage Profile.

**TrimCell Operation in Voltage Profile 0:** The Voltage Profile 0 has three operating modes. They are DAC Register 0 Select mode, DAC Register I<sup>2</sup>C Select mode and Closed Loop Trim mode. The mode selection is stored in the E<sup>2</sup>CMOS configuration memory. Each of the eight TrimCells can be independently set to different operating modes during Voltage Profile 0 mode of operation.

**DAC Register 0 Select Mode:** The contents of DAC register 0 are stored in the internal E<sup>2</sup>CMOS memory. When Voltage Profile 0 is selected, the DAC will be loaded with the value stored in DAC Register 0.

**DAC Register I<sup>2</sup>C Select Mode:** This mode is used if the power management arrangement requires an external microcontroller to control the DC-DC converter output voltage. The microcontroller updates the contents of the

DAC Register I<sup>2</sup>C on the fly to set the trimming voltage to a desired value. The DAC Register I<sup>2</sup>C is a volatile register and is reset to 80H (DAC at Bipolar zero) upon power-on. The external microcontroller writes the correct DAC code in this DAC Register I<sup>2</sup>C before enabling the programmable power supply.

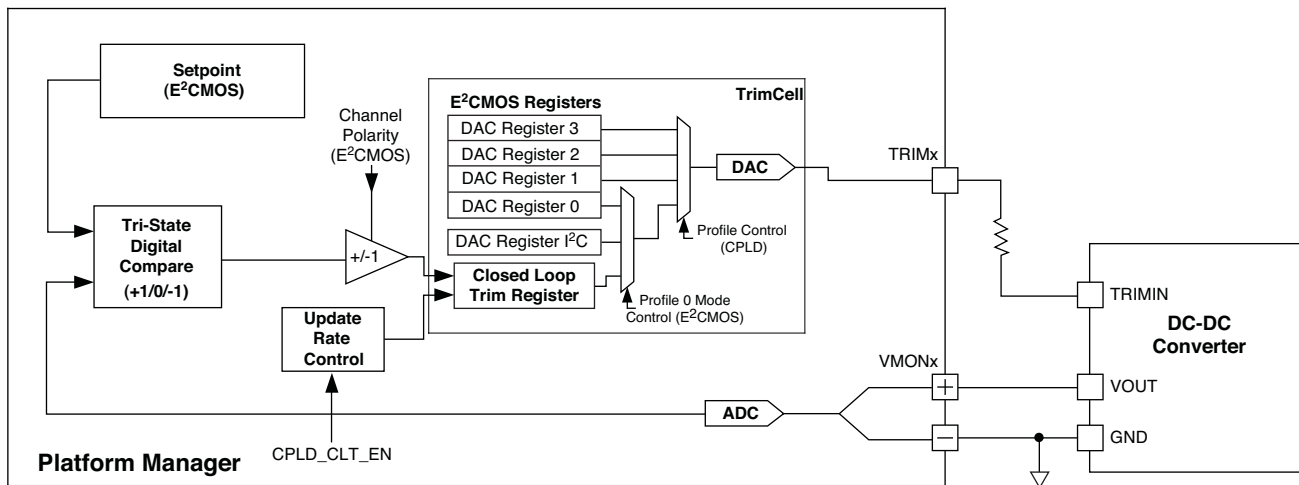
**Digital Closed Loop Trim Mode**

Closed loop trim mode operation can be used when tight control over the DC-DC converter output voltage at a desired value is required. The closed loop trim mechanism operates by comparing the measured output voltage of the DC-DC converter with the internally stored voltage setpoint. The difference between the setpoint and the actual DC-DC converter voltage generates an error voltage. This error voltage adjusts the DC-DC converter output voltage toward the setpoint. This operation iterates until the setpoint and the DC-DC converter voltage are equal.

Figure 20 shows the closed loop trim operation of a TrimCell. At regular intervals (as determined by the Update Rate Control register) the Platform Manager device initiates the closed loop power supply voltage correction cycle through the following blocks:

- Non-volatile **Setpoint** register stores the desired output voltage
- Internal **ADC** is used to measure the voltage of the DC-DC converter
- **Tri-state comparator** is used to compare the measured voltage from the ADC with the **Setpoint** register contents. The output of the tri-state comparator can be one of the following:
  - +1 if the setpoint voltage is greater than the DC-DC converter voltage
  - -1 if the setpoint voltage is less than the DC-DC converter voltage
  - 0 if the setpoint voltage is equal to the DC-DC converter voltage
- **Channel polarity control** determines the polarity of the error signal
- **Closed loop trim register** is used to compute and store the DAC code corresponding to the error voltage. The contents of the Closed Loop Trim will be incremented or decremented depending on the channel polarity and the tri-state comparator output. If the tri-state comparator output is 0, the closed loop trim register contents are left unchanged.
- The **DAC** in the **TrimCell** is used to generate the analog error voltage that adjusts the attached DC-DC converter output voltage.

**Figure 20. Digital Closed Loop Trim Operation**



The closed loop trim cycle interval is programmable and is set by the update rate control register. The following table lists the programmable update interval that can be selected by the update rate register.

**Table 8. Output DAC Update Rate in Digital Closed Loop Mode**

| Update Rate Control Value | Update Interval |
|---------------------------|-----------------|
| 00                        | 580 $\mu$ s     |
| 01                        | 1.15 ms         |
| 10                        | 9.22 ms         |
| 11                        | 18.5 ms         |

There is a one-to-one relationship between the selected TrimCell and the corresponding VMON input for the closed loop operation. For example, if TrimCell 3 is used to control the power supply in the closed loop trim mode, VMON3 must be used to monitor its output power supply voltage.

The closed loop operation can only be started by activating the internally generated CPLD signal, called CPLD\_CLT\_EN, in PAC-Designer software. The selection of Voltage Profile 0, however, can be either through the fixed default value or through the CPLD signals CPLD\_VPS0 and CPLD\_VPS1.

**Closed Loop Start-up Behavior**

The contents of the closed loop register, upon power-up, will contain a value 80h (Bipolar-zero) value. The DAC output voltage will be equal to the programmed Offset voltage. Usually under this condition, the power supply output will be close to its nominal voltage. If the power supply trimming should start after reaching its desired output voltage, the corresponding DAC code can be loaded into the closed loop trim register through I<sup>2</sup>C (same address as the DAC register I<sup>2</sup>C mode) before activating the CPLD\_CLT\_EN signal.

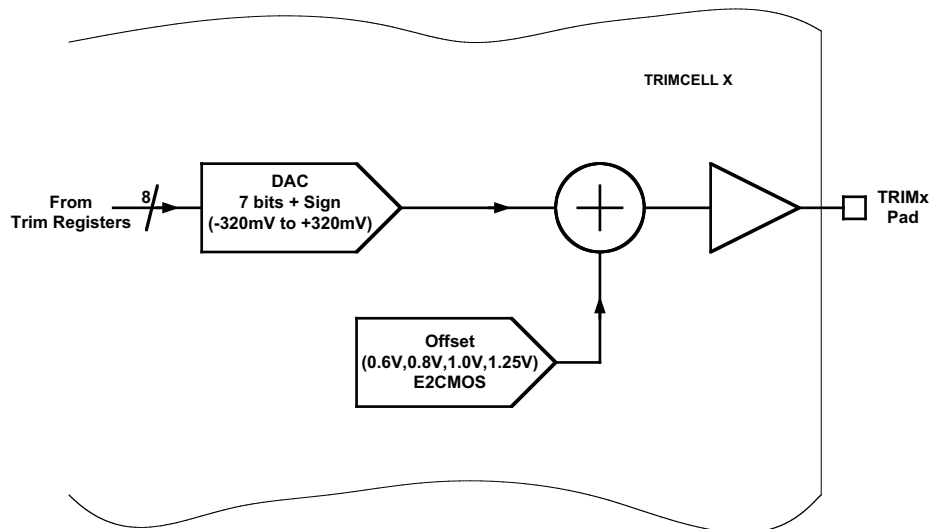
**Details of the Digital to Analog Converter (DAC)**

Each trim cell has an 8-bit bipolar DAC to set the trimming voltage (Figure 21). The full-scale output voltage of the DAC is +/- 320 mV. A code of 80H results in the DAC output set at its bi-polar zero value.

The voltage output from the DAC is added to a programmable offset value and the resultant voltage is then applied to the trim output pin. The offset voltage is typically selected to be approximately equal to the DC-DC converter open circuit trim node voltage. This results in maximizing the DC-DC converter output voltage range.

The programmed offset value can be set to 0.6V, 0.8V, 1.0V or 1.25V. This value selection is stored in E<sup>2</sup>CMOS memory and cannot be changed dynamically.

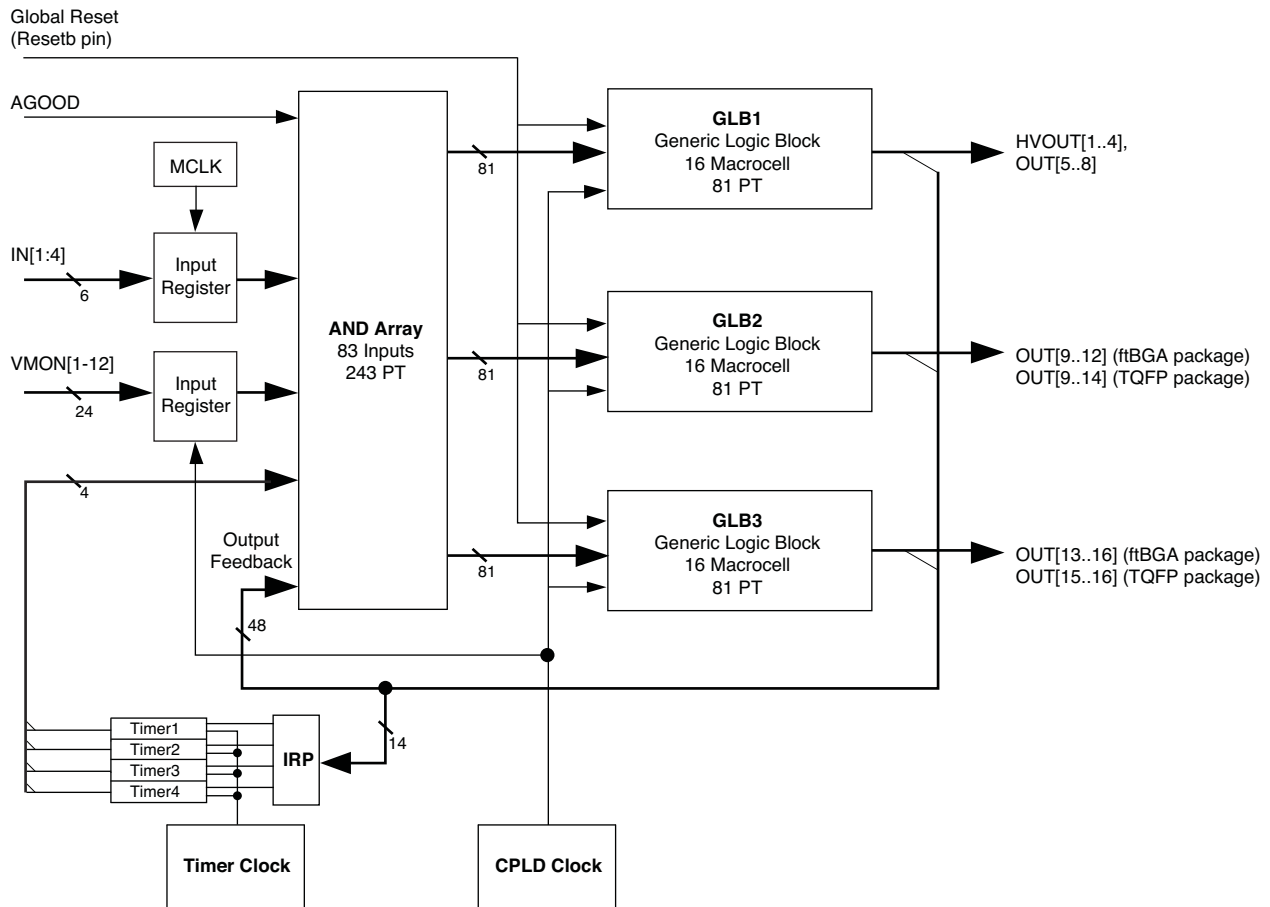
**Figure 21. Offset Voltage is Added to DAC Output Voltage to Derive Trim Pad Voltage**



### CPLD Block

Figure 22 shows the Platform Manager power management CPLD architecture, which is derived from the Lattice ispMACH® 4000 CPLD. The power management CPLD architecture allows the flexibility in designing various state machines and control functions used for power supply management. The AND array has 83 inputs and generates 243 product terms. These 243 product terms are divided into three groups of 81 for each of the generic logic blocks, GLB1, GLB2, and GLB3. Each GLB is made up of 16 macrocells. In total, there are 48 macrocells in the Platform Manager device. The output signals of the Platform Manager device are derived from GLBs as shown in Figure 22. Additionally, GLB3 generates the timer control.

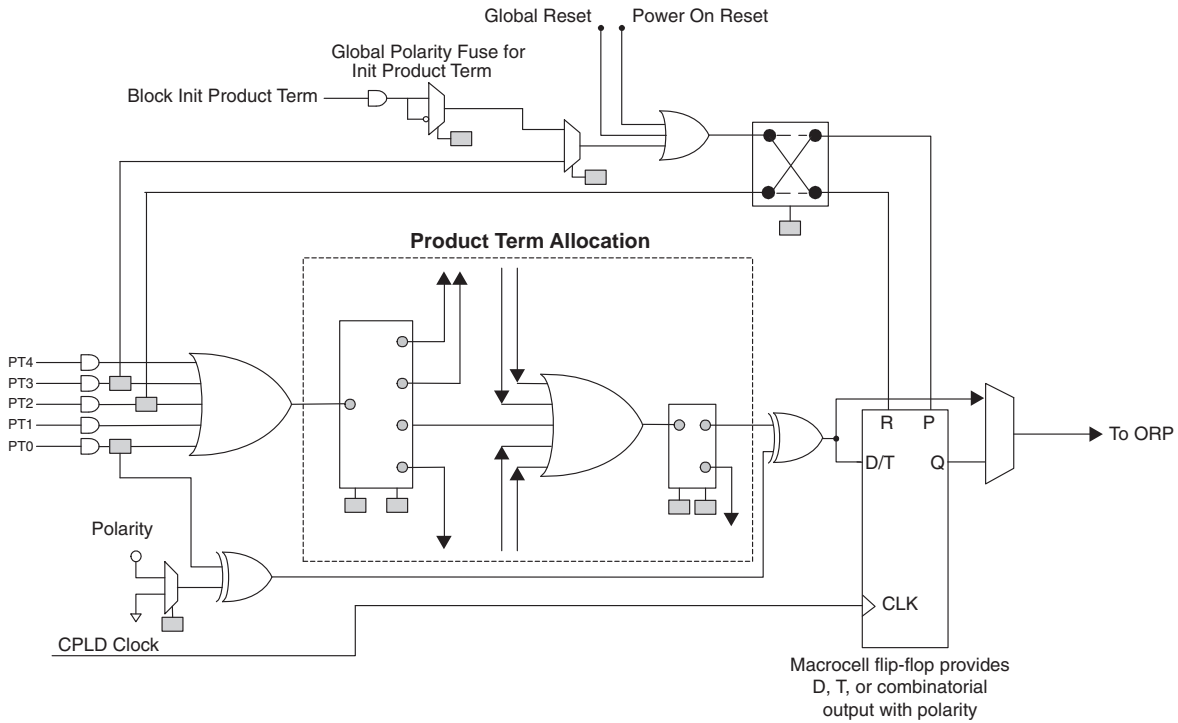
**Figure 22. Platform Manager CPLD Architecture**



### Macrocell Architecture

The macrocell shown in Figure 23 is the heart of the CPLD. The basic macrocell has five product terms that feed the OR gate and the flip-flop. The flip-flop in each macrocell is independently configured. It can be programmed to function as a D-Type or T-Type flip-flop. Combinatorial functions are realized by bypassing the flip-flop. The polarity control and XOR gates provide additional flexibility for logic synthesis. The flip-flop's clock is driven from the common CPLD clock that is generated by dividing the 8 MHz master clock (MCLK) by 32. The macrocell also supports asynchronous reset and preset functions, derived from either product terms, the global reset input, or the power-on reset signal. The resources within the macrocells share routing and contain a product term allocation array. The product term allocation array greatly expands the CPLD's ability to implement complex logical functions by allowing logic to be shared between adjacent blocks and distributing the product terms to allow for wider decode functions. All the digital inputs are registered by MCLK and the VMON comparator outputs are registered by the CPLD Clock to synchronize them to the CPLD logic.

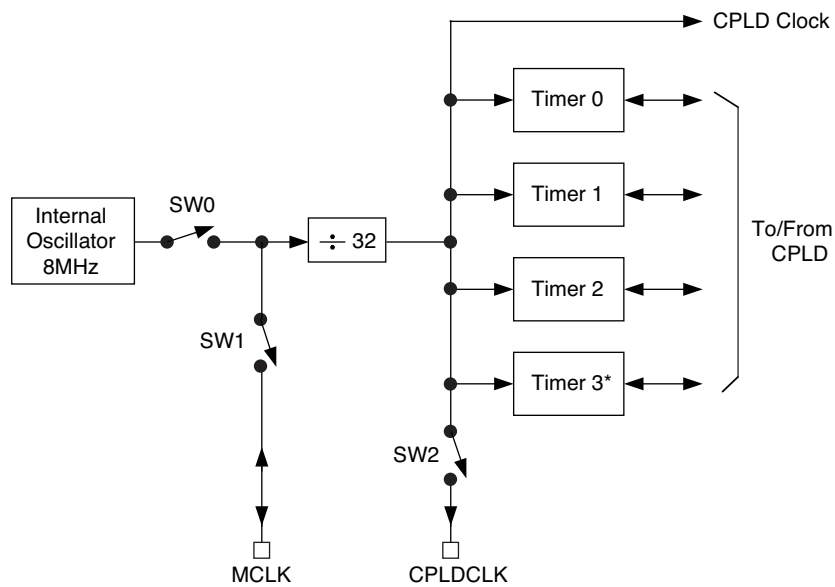
Figure 23. Macrocell Block Diagram



**Clock and Timer Functions**

Figure 24 shows a block diagram of the Platform Manager's internal clock and timer systems. The master clock operates at a fixed frequency of 8MHz, from which a fixed 250kHz CPLD clock is derived.

Figure 24. Clock and Timer System



\*Used as part of FPGA timer functionality.

The internal oscillator runs at a fixed frequency of 8 MHz. This signal is used as a source for the CPLD and timer clocks. It is also used for clocking the comparator outputs and clocking the digital filters in the voltage monitor cir-



cuits, ADC and trim circuits. The Platform Manager can be programmed to operate in two modes: Master mode and Slave mode. Table 9 summarizes the operating modes of Platform Manager.

**Table 9. Platform Manager Operating Modes**

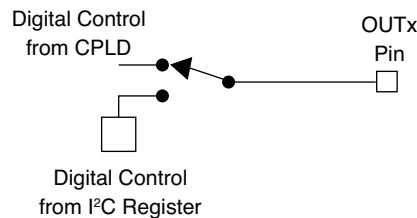
| Timer Operating Mode | SW0    | SW1    | Condition   | Comments                    |
|----------------------|--------|--------|---|-----------------------------|
| Master               | Closed | Closed | When more than one Platform Manager is used in a board, one of them should be configured to operate in this mode.                                 | MCLK pin outputs 8MHz clock |
| Slave                | Open   | Closed | When more than one Platform Managers is used in a board. Other than the master, the rest of the Platform Managers should be programmed as slaves. | MCLK pin is input           |

A divide-by-32 prescaler divides the internal 8MHz oscillator (or external clock, if selected) down to 250kHz for the CPLD clock and for the programmable timers. This CPLD clock may be made available on the CPLDCLK pin by closing SW2. Each of the four timers provides independent timeout intervals ranging from 32 μs to 1.96 seconds in 128 steps.

### CPLD Digital Outputs

The Platform Manager provides 20 digital outputs, HVOUT[1:4] and OUT[5:16]. Outputs OUT[5:16] are permanently configured as open drain to provide a high degree of flexibility when interfacing to logic signals, LEDs, optocouplers, and power supply control inputs. The HVOUT[1:4] pins can be configured as either high voltage FET drivers or open drain outputs. Each of these outputs may be controlled either from the CPLD or from the I<sup>2</sup>C bus. The determination whether a given output is under CPLD or I<sup>2</sup>C control may be made on a pin-by-pin basis (see Figure 25). For further details on controlling the outputs through I<sup>2</sup>C, please see the I<sup>2</sup>C/SMBUS Interface section of this data sheet.

**Figure 25. Digital Output Pin Configuration**



### High Voltage Outputs

In addition to being usable as digital open-drain outputs, the Platform Manager’s HVOUT1-HVOUT4 output pins can be programmed to operate as high-voltage FET drivers. Figure 26 shows the details of the HVOUT gate drivers. Each of these outputs may be controlled from the CPLD or from the I<sup>2</sup>C bus (see Figure 26). For further details on controlling the outputs through I<sup>2</sup>C, please see the I<sup>2</sup>C/SMBUS Interface section of this data sheet.

Figure 26. Basic Function Diagram for an Output in High Voltage MOSFET Gate Driver Mode

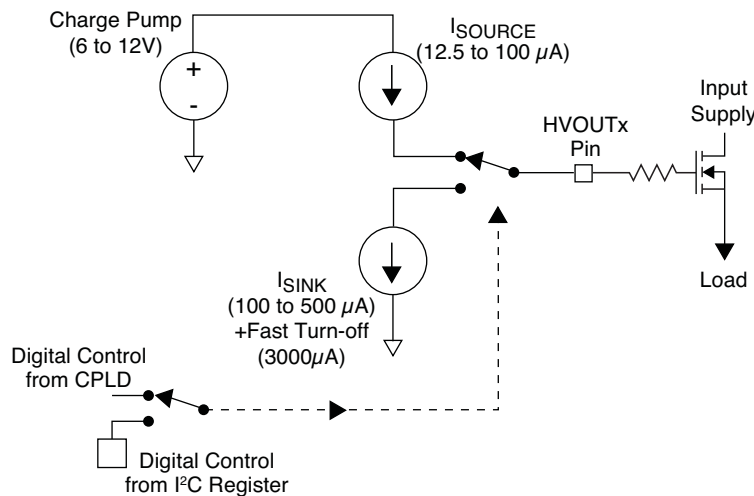


Figure 26 shows the HVOUT circuitry when programmed as a FET driver. In this mode the output either sources current from a charge pump or sinks current. The maximum voltage that the output level at the pin will rise to is also programmable between 6V and 12V. The maximum voltage levels that are required depend on the gate-to-source threshold of the FET being driven and the power supply voltage being switched. The maximum voltage level needs to be sufficient to bias the gate-to-source threshold on and also accommodate the load voltage at the FET’s source, since the source pin of the FET to provide a wide range of ramp rates is tied to the supply of the target board. When the HVOUT pin is sourcing current, charging a FET gate, the source current is programmable between 12.5μA and 100μA. When the driver is turned to the off state, the driver will sink current to ground, and this sink current is also programmable between 3000μA and 100μA to control the turn-off rate.

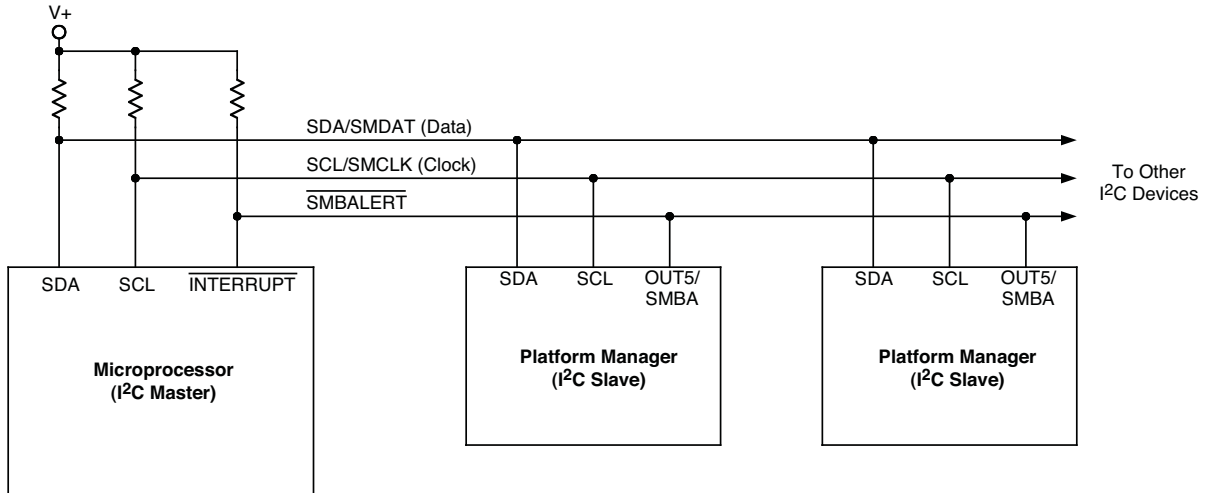
**Programmable Output Voltage Levels for HVOUT1- HVOUT4**

There are four selectable steps for the output voltage of the FET drivers when in FET driver mode. The voltage that the pin is capable of driving to can be programmed from 6V to 12V in 2V steps.

**Power I<sup>2</sup>C/SMBUS Interface**

I<sup>2</sup>C and SMBus are low-speed serial interface protocols designed to enable communications among a number of devices on a circuit board. The Platform Manager supports a 7-bit addressing of the I<sup>2</sup>C communications protocol, as well as SMBTimeout and SMBAlert features of the SMBus, enabling it to easily integrated into many types of modern power management systems. Figure 27 shows a typical I<sup>2</sup>C configuration, in which one or more Platform Managers are slaved to a supervisory microcontroller. SDA is used to carry data signals, while SCL provides a synchronous clock signal. The SMBAlert line is only present in SMBus systems. The 7-bit I<sup>2</sup>C address is fully programmable through the power JTAG port.

Figure 27. Platform Manager in I<sup>2</sup>C/SMBUS System



In both the I<sup>2</sup>C and SMBus protocols, the bus is controlled by a single master device at any given time. This master device generates the SCL clock signal and coordinates all data transfers to and from a number of slave devices. The Platform Manager is configured as a slave device, and cannot independently coordinate data transfers. Each slave device on a given I<sup>2</sup>C bus is assigned a unique address. The Platform Manager implements the 7-bit addressing portion of the standard. Any 7-bit address can be assigned to the Platform Manager device by programming through JTAG. When selecting a device address, one should note that several addresses are reserved by the I<sup>2</sup>C and/or SMBus standards, and should not be assigned to Platform Manager devices to assure bus compatibility. Table 10 lists these reserved addresses.

Table 10. I<sup>2</sup>C/SMBus Reserved Slave Device Addresses

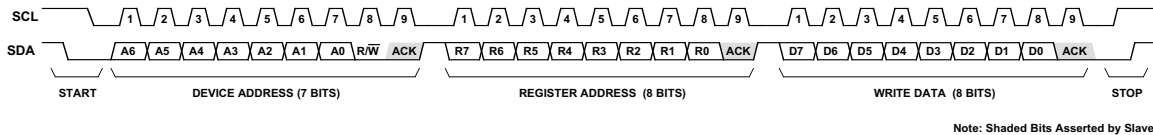
| Address  | R/W bit | I <sup>2</sup> C function Description | SMBus Function               |
|----------|---------|---------------------------------------|------------------------------|
| 0000 000 | 0       | General Call Address                  | General Call Address         |
| 0000 000 | 1       | Start Byte                            | Start Byte                   |
| 0000 001 | x       | CBUS Address                          | CBUS Address                 |
| 0000 010 | x       | Reserved                              | Reserved                     |
| 0000 011 | x       | Reserved                              | Reserved                     |
| 0000 1xx | x       | HS-mode master code                   | HS-mode master code          |
| 0001 000 | x       | NA                                    | SMBus Host                   |
| 0001 100 | x       | NA                                    | SMBus Alert Response Address |
| 0101 000 | x       | NA                                    | Reserved for ACCESS.bus      |
| 0110 111 | x       | NA                                    | Reserved for ACCESS.bus      |
| 1100 001 | x       | NA                                    | SMBus Device Default Address |
| 1111 0xx | x       | 10-bit addressing                     | 10-bit addressing            |
| 1111 1xx | x       | Reserved                              | Reserved                     |

The Platform Manager's I<sup>2</sup>C/SMBus interface allows data to be both written to and read from the device. A data write transaction (Figure 28) consists of the following operations:

1. Start the bus transaction
2. Transmit the device address (7 bits) along with a low write bit
3. Transmit the address of the register to be written to (8 bits)
4. Transmit the data to be written (8 bits)
5. Stop the bus transaction

To start the transaction, the master device holds the SCL line high while pulling SDA low. Address and data bits are then transferred on each successive SCL pulse, in three consecutive byte frames of nine SCL pulses. Address and data are transferred on the first 8 SCL clocks in each frame, while an acknowledge signal is asserted by the slave device on the 9th clock in each frame. Both data and addresses are transferred in a most-significant-bit-first format. The first frame contains the 7-bit device address, with bit 8 held low to indicate a write operation. The second frame contains the register address to which data will be written, and the final frame contains the actual data to be written. Note that the SDA signal is only allowed to change when the SCL is low, as raising SDA when SCL is high signals the end of the transaction.

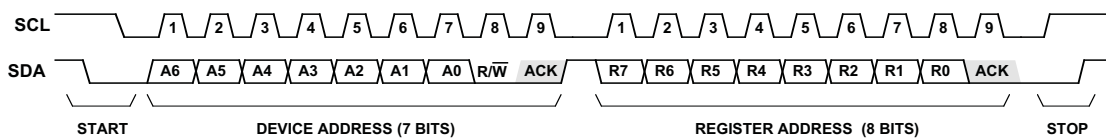
**Figure 28. I<sup>2</sup>C Write Operation**



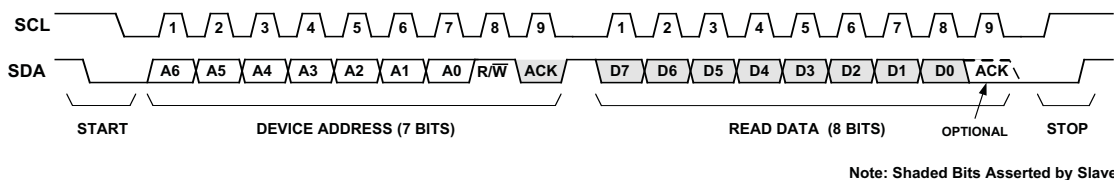
Reading a data byte from the Platform Manager requires two separate bus transactions (Figure 29). The first transaction writes the register address from which a data byte is to be read. Note that since no data is being written to the device, the transaction is concluded after the second byte frame. The second transaction performs the actual read. The first frame contains the 7-bit device address with the R/W bit held High. In the second frame the Platform Manager asserts data out on the bus in response to the SCL signal. Note that the acknowledge signal in the second frame is asserted by the master device and not the Platform Manager.

**Figure 29. I<sup>2</sup>C Read Operation**

**STEP 1: WRITE REGISTER ADDRESS FOR READ OPERATION**



**STEP 2: READ DATA FROM THAT REGISTER**



The Platform Manager provides 26 registers that can be accessed through its I<sup>2</sup>C interface. These registers provide the user with the ability to monitor and control the device's inputs and outputs, and transfer data to and from the device. Table 11 provides a summary of these registers.

**Table 11. I<sup>2</sup>C Control Registers**

| Register Address | Register Name  | Read/Write | Description  | Value After POR <sup>1,2</sup> |
|------------------|----------------|------------|--|--------------------------------|
| 0x00             | vmon_status0   | R          | VMON input status Vmon[4:1]                        | ----                           |
| 0x01             | vmon_status1   | R          | VMON input status Vmon[8:5]                        | ----                           |
| 0x02             | vmon_status2   | R          | VMON input status Vmon[12:9]                       | ----                           |
| 0x03             | output_status0 | R          | Output status OUT[8:5], HVOUT[4:1]                 | ----                           |
| 0x04             | output_status1 | R          | Output status OUT[12:9]<br>208-ball ftBGA package  | X 12 11 X 10 9 X X             |
|                  |                |            | Output status OUT[14:9]<br>128-pin TQFP package    | 14 X X 13 10 9 12 11           |
| 0x05             | output_status2 | R          | Output status OUT[16:13]<br>208-ball ftBGA package | X X X X 16 15 14 13            |
|                  |                |            | Output status OUT[16:15]<br>128-pin TQFP package   | ---- 16 15 X X                 |
| 0x06             | input_status   | R          | Input status IN[4:1]                               | X X X X ----                   |
| 0x07             | adc_value_low  | R          | ADC D[3:0] and status                              | ---- X X X 1                   |
| 0x08             | adc_value_high | R          | ADC D[11:4]  | ----                           |
| 0x09             | adc_mux        | R/W        | ADC Attenuator and MUX[3:0]                        | X X X 1 1 1 1 1                |
| 0x0A             | UES_byte0      | R          | UES[7:0]   | ----                           |
| 0x0B             | UES_byte1      | R          | UES[15:8]  | ----                           |
| 0x0C             | UES_byte2      | R          | UES[23:16]   | ----                           |
| 0x0D             | UES_byte3      | R          | UES[31:24]   | ----                           |
| 0x0E             | gp_output1     | R/W        | GPOUT[8:1]   | 0 0 0 1 0 0 0 0                |
| 0x0F             | gp_output2     | R/W        | GPOUT[12:9]<br>208-ball ftBGA package              | X 12 11 X 10 9 X X             |
|                  |                |            | GPOUT[14:9]<br>128-pin TQFP package                | 14 X X 13 10 9 12 11           |
| 0x10             | gp_output3     | R/W        | GPOUT[16:13]<br>208-ball ftBGA package             | X X X X 16 15 14 13            |
|                  |                |            | GPOUT[16:15]<br>128-pin TQFP package               | ---- 16 15 X X                 |
| 0x11             | input_value    | R/W        | CPLD Input Register [6:2]                          | X X 0 0 0 0 0 X                |
| 0x12             | reset          | W          | Resets device on write                             | N/A                            |
| 0x13             | trim1_trim     | R/W        | Trim DAC 1 [7:0] <sup>3</sup>                      | 1 0 0 0 0 0 0 0                |
| 0x14             | trim2_trim     | R/W        | Trim DAC 2 [7:0] <sup>3</sup>                      | 1 0 0 0 0 0 0 0                |
| 0x15             | trim3_trim     | R/W        | Trim DAC 3 [7:0]                                   | 1 0 0 0 0 0 0 0                |
| 0x16             | trim4_trim     | R/W        | Trim DAC 4 [7:0]                                   | 1 0 0 0 0 0 0 0                |
| 0x17             | trim5_trim     | R/W        | Trim DAC 5 [7:0]                                   | 1 0 0 0 0 0 0 0                |
| 0x18             | trim6_trim     | R/W        | Trim DAC 6 [7:0]                                   | 1 0 0 0 0 0 0 0                |
| 0x19             | trim7_trim     | R/W        | Trim DAC 7 [7:0]                                   | 1 0 0 0 0 0 0 0                |
| 0x1A             | trim8_trim     | R/W        | Trim DAC 8 [7:0]                                   | 1 0 0 0 0 0 0 0                |

1. "X" = Undefined output states can be observed.

2. "-" = State depends on device configuration or input status. For words 0x04 and 0x05, specific outputs corresponding to bit positions are called out. In all other cases, bits correspond to the order called out in the Description column.

3. Trim DAC 1 and Trim DAC 2 are not available in the 128-pin TQFP package option.

Several registers are provided for monitoring the status of the analog inputs. The three registers VMON\_STATUS[0:2] provide the ability to read the status of the VMON output comparators. The ability to read both the 'a' and 'b' comparators from each VMON input is provided through the VMON input registers. Note that if

a VMON input is configured to window comparison mode, then the corresponding VMONxA register bit will reflect the status of the window comparison.

**Figure 30. VMON Status Registers**

**0x00 - VMON\_STATUS0 (Read Only)**

|        |        |        |        |        |        |        |        |
|--------|--------|--------|--------|--------|--------|--------|--------|
| VMON4B | VMON4A | VMON3B | VMON3A | VMON2B | VMON2A | VMON1B | VMON1A |
| b7     | b6     | b5     | b4     | b3     | b2     | b1     | b0     |

**0x01 - VMON\_STATUS1 (Read Only)**

|        |        |        |        |        |        |        |        |
|--------|--------|--------|--------|--------|--------|--------|--------|
| VMON8B | VMON8A | VMON7B | VMON7A | VMON6B | VMON6A | VMON5B | VMON5A |
| b7     | b6     | b5     | b4     | b3     | b2     | b1     | b0     |

**0x02 - VMON\_STATUS2 (Read Only)**

|         |         |         |         |         |         |        |        |
|---------|---------|---------|---------|---------|---------|--------|--------|
| VMON12B | VMON12A | VMON11B | VMON11A | VMON10B | VMON10A | VMON9B | VMON9A |
| b7      | b6      | b5      | b4      | b3      | b2      | b1     | b0     |

It is also possible to directly read the value of the voltage present on any of the VMON inputs by using the Platform Manager’s ADC. Three registers provide the I<sup>2</sup>C interface to the ADC (Figure 31).

**Figure 31. ADC Interface Registers**

**0x07 - ADC\_VALUE\_LOW (Read Only)**

|    |    |    |    |    |    |    |      |
|----|----|----|----|----|----|----|------|
| D3 | D2 | D1 | D0 | 1  | 1  | 1  | DONE |
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0   |

**0x08 - ADC\_VALUE\_HIGH (Read Only)**

|     |     |    |    |    |    |    |    |
|-----|-----|----|----|----|----|----|----|
| D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 |
| b7  | b6  | b5 | b4 | b3 | b2 | b1 | b0 |

**0x09 - ADC\_MUX (Read/Write)**

|    |    |    |       |      |      |      |      |
|----|----|----|-------|------|------|------|------|
| X  | X  | X  | ATTEN | SEL3 | SEL2 | SEL1 | SEL0 |
| b7 | b6 | b5 | b4    | b3   | b2   | b1   | b0   |

To perform an A/D conversion, one must set the input attenuator and channel selector. Two input ranges may be set using the attenuator, 0 to 2.048V and 0 to 6.144V. Table 12 shows the input attenuator settings.

**Table 12. ADC Input Attenuator Control**

| ATTEN (ADC_MUX.4) | Resolution | Full-Scale Range |
|-------------------|------------|------------------|
| 0                 | 2mV        | 2.048 V          |
| 1                 | 6mV        | 6.144 V          |

The input selector may be set to monitor any one of the twelve VMON inputs, the PVCCA input, or the PVCCINP input. Table 13 shows the codes associated with each input selection.

**Table 13.  $V_{MON}$  Address Selection Table**

| Select Word         |                     |                     |                     | Input Channel |
|---------------------|---------------------|---------------------|---------------------|---------------|
| SEL3<br>(ADC_MUX.3) | SEL2<br>(ADC_MUX.2) | SEL1<br>(ADC_MUX.1) | SEL0<br>(ADC_MUX.0) |               |
| 0                   | 0                   | 0                   | 0                   | VMON1         |
| 0                   | 0                   | 0                   | 1                   | VMON2         |
| 0                   | 0                   | 1                   | 0                   | VMON3         |
| 0                   | 0                   | 1                   | 1                   | VMON4         |
| 0                   | 1                   | 0                   | 0                   | VMON5         |
| 0                   | 1                   | 0                   | 1                   | VMON6         |
| 0                   | 1                   | 1                   | 0                   | VMON7         |
| 0                   | 1                   | 1                   | 1                   | VMON8         |
| 1                   | 0                   | 0                   | 0                   | VMON9         |
| 1                   | 0                   | 0                   | 1                   | VMON10        |
| 1                   | 0                   | 1                   | 0                   | VMON11        |
| 1                   | 0                   | 1                   | 1                   | VMON12        |
| 1                   | 1                   | 0                   | 0                   | PVCCA         |
| 1                   | 1                   | 0                   | 1                   | PVCCINP       |

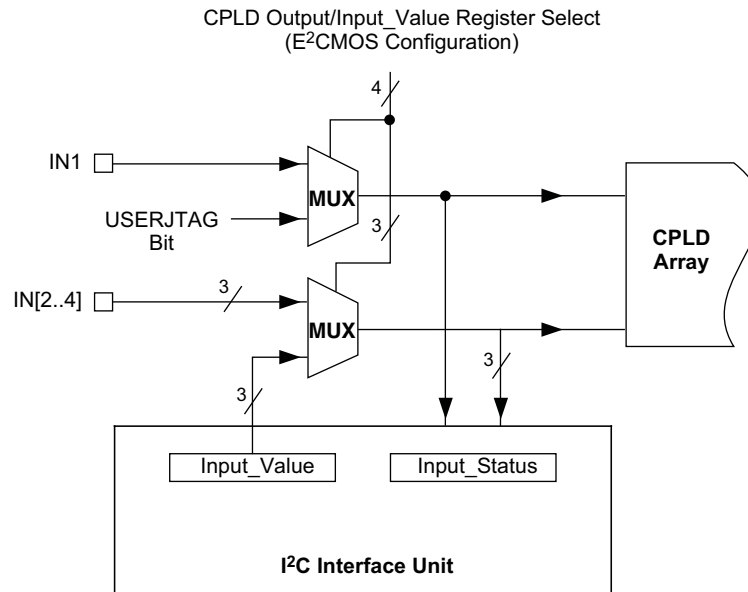
Writing a value to the ADC\_MUX register to set the input attenuator and selector will automatically initiate a conversion. When the conversion is in process, the DONE bit (ADC\_VALUE\_LOW.0) will be reset to 0. When the conversion is complete, this bit will be set to 1. When the conversion is complete, the result may be read out of the ADC by performing two I<sup>2</sup>C read operations; one for ADC\_VALUE\_LOW, and one for ADC\_VALUE\_HIGH. It is recommended that the I<sup>2</sup>C master load a second conversion command only after the completion of the current conversion command (Waiting for the DONE bit to be set to 1). An alternative would be to wait for a minimum specified time (see T<sub>CONVERT</sub> value in the specifications) and disregard checking the DONE bit.

Note that if the I<sup>2</sup>C clock rate falls below 50kHz (see F<sub>I<sup>2</sup>C</sub> note in specifications), the only way to insure a valid ADC conversion is to wait the minimum specified time (T<sub>CONVERT</sub>), as the operation of the DONE bit at clock rates lower than that cannot be guaranteed. In other words, if the I<sup>2</sup>C clock rate is less than 50kHz, the DONE bit may or may not assert even though a valid conversion result is available.

To insure every ADC conversion result is valid, preferred operation is to clock I<sup>2</sup>C at more than 50kHz and verify DONE bit status or wait for the full T<sub>CONVERT</sub> time period between subsequent ADC convert commands. If an I<sup>2</sup>C request is placed before the current conversion is complete, the DONE bit will be set to 1 only after the second request is complete.

The status of the digital input lines may also be monitored and controlled through I<sup>2</sup>C commands. Figure 32 shows the I<sup>2</sup>C interface to the IN[1:4] digital input lines. The input status may be monitored by reading the INPUT\_STATUS register, while input values to the CPLD array may be set by writing to the INPUT\_VALUE register. To be able to set an input value for the CPLD array, the input multiplexer associated with that bit needs to be set to the I<sup>2</sup>C register setting in E<sup>2</sup>CMOS memory otherwise the CPLD will receive its input from the INx pin.

Figure 32. I<sup>2</sup>C Digital Input Interface



**0x06 - INPUT\_STATUS (Read Only)**

|    |    |    |    |     |     |     |     |
|----|----|----|----|-----|-----|-----|-----|
| X  | X  | X  | X  | IN4 | IN3 | IN2 | IN1 |
| b7 | b6 | b5 | b4 | b3  | b2  | b1  | b0  |

**0x11 - INPUT\_VALUE (Read/Write)**

|    |    |     |     |    |    |    |    |
|----|----|-----|-----|----|----|----|----|
| X  | X  | I6* | I5* | I4 | I3 | I2 | X  |
| b7 | b6 | b5  | b4  | b3 | b2 | b1 | b0 |

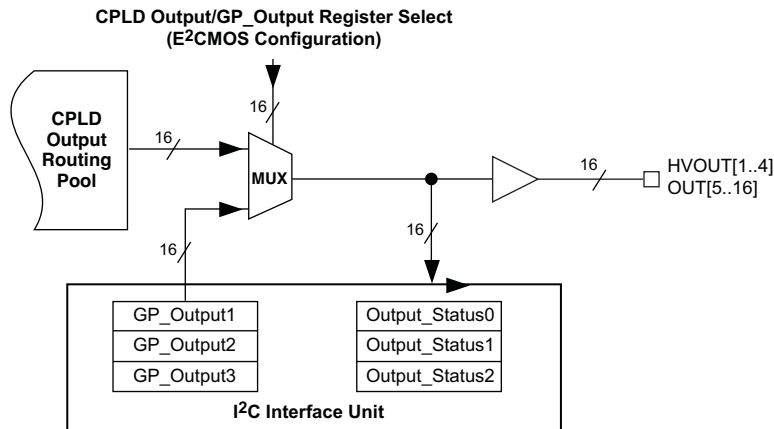
\*I5 and I6 are internal inputs to the CPLD that can only be configured by writing them via the I<sup>2</sup>C interface (no external pin connection).

The CPLD digital outputs may also be monitored and controlled through the I<sup>2</sup>C interface, as shown in Figure 33. The status of any given digital output may be read by reading the contents of the associated OUTPUT\_STATUS[2:0] register. Note that in the case of the outputs, the status reflected by these registers reflects the logic signal used to drive the pin, and does not sample the actual level present on the output pin. For example, if an output is set high but is not pulled up, the output status bit corresponding with that pin will read '1', but a high output signal will not appear on the pin. Digital inputs I5 and I6 are only accessible via the I<sup>2</sup>C interface. In other words, there are no external pin connections to these two inputs.

Digital outputs may also be optionally controlled directly by the I<sup>2</sup>C bus instead of by the CPLD array. The outputs may be driven either from the CPLD ORP or from the contents of the GP\_OUTPUT[2:0] registers with the choice user-settable in E<sup>2</sup>CMOS memory. Each output may be independently set to output from the CPLD or from the GP\_OUTPUT registers.



Figure 33. I<sup>2</sup>C Output Monitor and Control Logic



**0x03 - OUTPUT\_STATUS0 (Read Only)**

|      |      |      |      |        |        |        |        |
|------|------|------|------|--------|--------|--------|--------|
| OUT8 | OUT7 | OUT6 | OUT5 | HVOUT4 | HVOUT3 | HVOUT2 | HVOUT1 |
| b7   | b6   | b5   | b4   | b3     | b2     | b1     | b0     |

**0x04 - OUTPUT\_STATUS1 (Read Only), 208-ball ftBGA package option**

|    |       |       |    |       |      |    |    |
|----|-------|-------|----|-------|------|----|----|
| X  | OUT12 | OUT11 | X  | OUT10 | OUT9 | X  | X  |
| b7 | b6    | b5    | b4 | b3    | b2   | b1 | b0 |

**0x05 - OUTPUT\_STATUS2 (Read Only), 208-ball ftBGA package option**

|    |    |    |    |       |       |       |       |
|----|----|----|----|-------|-------|-------|-------|
| X  | X  | X  | X  | OUT16 | OUT15 | OUT14 | OUT13 |
| b7 | b6 | b5 | b4 | b3    | b2    | b1    | b0    |

**0x04 - OUTPUT\_STATUS1 (Read Only), 128-pin TQFP package option**

|       |    |    |       |       |      |       |       |
|-------|----|----|-------|-------|------|-------|-------|
| OUT14 | X  | X  | OUT13 | OUT10 | OUT9 | OUT11 | OUT12 |
| b7    | b6 | b5 | b4    | b3    | b2   | b1    | b0    |

**0x05 - OUTPUT\_STATUS2 (Read Only), 128-pin TQFP package option**

|    |    |    |    |       |       |    |    |
|----|----|----|----|-------|-------|----|----|
| X  | X  | X  | X  | OUT16 | OUT15 | X  | X  |
| b7 | b6 | b5 | b4 | b3    | b2    | b1 | b0 |

**0x0E - GP\_OUTPUT1 (Read/Write)**

|     |     |     |         |     |     |     |     |
|-----|-----|-----|---------|-----|-----|-----|-----|
| GP8 | GP7 | GP6 | GP5_ENb | GP4 | GP3 | GP2 | GP1 |
| b7  | b6  | b5  | b4      | b3  | b2  | b1  | b0  |

**0x0F - GP\_OUTPUT2 (Read/Write), 208-ball ftBGA package option**

|    |      |      |    |      |     |    |    |
|----|------|------|----|------|-----|----|----|
| X  | GP12 | GP11 | X  | GP10 | GP9 | X  | X  |
| b7 | b6   | b5   | b4 | b3   | b2  | b1 | b0 |

**0x10 - GP\_OUTPUT3 (Read/Write), 208-ball ftBGA package option**

|    |    |    |    |      |      |      |      |
|----|----|----|----|------|------|------|------|
| X  | X  | X  | X  | GP16 | GP15 | GP14 | GP13 |
| b7 | b6 | b5 | b4 | b3   | b2   | b1   | b0   |

**0x0F - GP\_OUTPUT2 (Read/Write), 128-pin TQFP package option**

|      |    |    |      |      |     |      |      |
|------|----|----|------|------|-----|------|------|
| GP14 | X  | X  | GP13 | GP10 | GP9 | GP11 | GP12 |
| b7   | b6 | b5 | b4   | b3   | b2  | b1   | b0   |

**0x10 - GP\_OUTPUT3 (Read/Write), 128-pin TQFP package option**

|    |    |    |    |      |      |    |    |
|----|----|----|----|------|------|----|----|
| X  | X  | X  | X  | GP16 | GP15 | X  | X  |
| b7 | b6 | b5 | b4 | b3   | b2   | b1 | b0 |

The UES word may also be read through the I<sup>2</sup>C interface, with the register mapping shown in Figure 34.

**Figure 34. I<sup>2</sup>C Register Mapping for UES Bits**

**0x0A - UES\_BYTE0 (Read Only)**

|      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|
| UES7 | UES6 | UES5 | UES4 | UES3 | UES2 | UES1 | UES0 |
| b7   | b6   | b5   | b4   | b3   | b2   | b1   | b0   |

**0x0B - UES\_BYTE1 (Read Only)**

|       |       |       |       |       |       |      |      |
|-------|-------|-------|-------|-------|-------|------|------|
| UES15 | UES14 | UES13 | UES12 | UES11 | UES10 | UES9 | UES8 |
| b7    | b6    | b5    | b4    | b3    | b2    | b1   | b0   |

**0x0C - UES\_BYTE2 (Read Only)**

|       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|
| UES23 | UES22 | UES21 | UES20 | UES19 | UES18 | UES17 | UES16 |
| b7    | b6    | b5    | b4    | b3    | b2    | b1    | b0    |

**0x0D - UES\_BYTE3 (Read Only)**

|       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|
| UES31 | UES30 | UES29 | UES28 | UES27 | UES26 | UES25 | UES24 |
| b7    | b6    | b5    | b4    | b3    | b2    | b1    | b0    |

The I<sup>2</sup>C interface also provides the ability to initiate reset operations. The Platform Manager may be reset by issuing a write of any value to the I<sup>2</sup>C RESET register (Figure 35). Note: The execution of the I<sup>2</sup>C reset command is equivalent to toggling the Resetb pin of the device. Refer to the Resetb Signal, RESET Command via JTAG or I<sup>2</sup>C section of this data sheet for further information.

**Figure 35. I<sup>2</sup>C Reset Register**

**0x12 - RESET (Write Only)**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| X  | X  | X  | X  | X  | X  | X  | X  |
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |

The Platform Manager also provides the user with the ability to program the trim values over the I<sup>2</sup>C interface, by writing the appropriate binary word to the associated trim register (Figure 36).

**Figure 36. I<sup>2</sup>C Trim Registers**

**0x13 - TRIM1\_TRIM (Read/Write)\***

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |

**0x14 - TRIM2\_TRIM (Read/Write)\***

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |

**0x15 - TRIM3\_TRIM (Read/Write)**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |

**0x16 - TRIM4\_TRIM (Read/Write)**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |

**0x17 - TRIM5\_TRIM (Read/Write)**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |

**0x18 - TRIM6\_TRIM (Read/Write)**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |

**0x19 - TRIM7\_TRIM (Read/Write)**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |

**0x1A - TRIM8\_TRIM (Read/Write)**

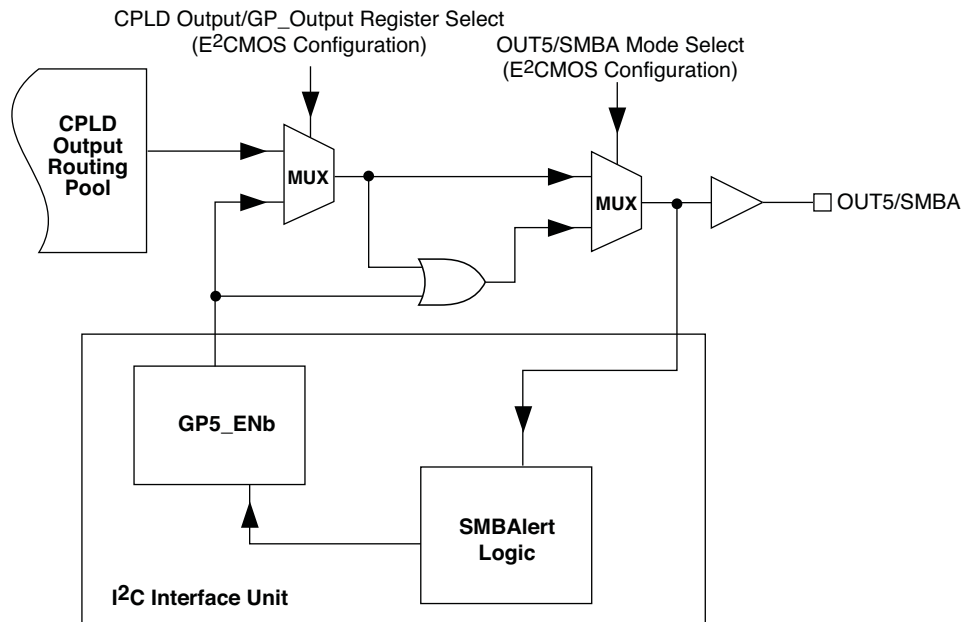
|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |

\*0x13 Trim 1 and 0x14 Trim 2 I<sup>2</sup>C registers are not available with 128-pin TQFP package option.

## SMBus SMBAAlert Function

The Platform Manager provides an SMBus SMBAAlert function so that it can request service from the bus master when it is used as part of an SMBus system. This feature is supported as an alternate function of OUT5. When the SMBAAlert feature is enabled, OUT5 is controlled by a combination of the CPLD ORP and the GP5\_ENb bit (Figure 37). *Note: To enable the SMBAAlert feature, the SMB\_Mode (E<sup>2</sup>CMOS bit) should be set in software.*

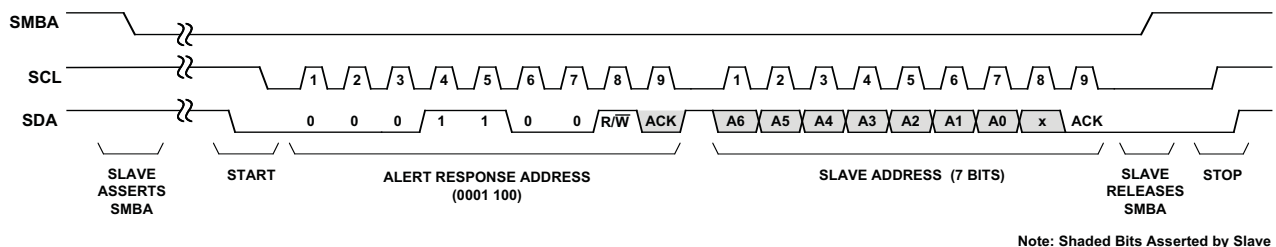
**Figure 37. Platform Manager SMBAAlert Logic**



The typical flow for an SMBAAlert transaction is as follows (Figure 38):

1. GP5\_ENb bit is forced (Via I<sup>2</sup>C write) to Low
2. Platform Manager CPLD logic pulls OUT5/SMBA Low
3. Master responds to interrupt from SMBA line
4. Master broadcasts a read operation using the SMBus Alert Response Address (ARA)
5. Platform Manager responds to read request by transmitting its device address
6. If transmitted device address matches Platform Manager address, it sets GP5\_ENb bit high.  
This releases OUT5/SMBA.

**Figure 38. SMBAAlert Bus Transaction**



After OUT5/SMBA has been released, the bus master (typically a microcontroller) may opt to perform some service functions in which it may send data to or read data from the Platform Manager. As part of the service functions, the bus master will typically need to clear whatever condition initiated the SMBAAlert request, and will also need to reset GP5\_ENb to re-enable the SMBAAlert function. For further information on the SMBus, the user should consult the SMBus Standard.

---

Designs using the SMBAlert feature are required to set the device's I<sup>2</sup>C/SMBus address to the lowest of all the addresses on that I<sup>2</sup>C/SMBus.

### **RESETb Signal, RESET Command via JTAG or I<sup>2</sup>C**

Activating the RESETb signal (Logic 0 applied to the RESETb pin) or issuing a reset instruction via JTAG or I<sup>2</sup>C will force the outputs to the following states independent of how these outputs have been configured in the PINS window:

- OUT5-16 will go high-impedance.
- HVOUT pins programmed for open drain operation will go high-impedance.
- HVOUT pins programmed for FET driver mode operation will pull down.

At the conclusion of the RESET event, these outputs will go to the states defined by the PINS window, and if a sequence has been programmed into the device, it will be re-started at the first step. The analog calibration will be re-done and consequently, the VMONs, ADCs, and DACs will not be operational until 2.5 milliseconds (max.) after the conclusion of the RESET event.

*CAUTION: Activating the RESETb signal or issuing a RESET command through I2C or JTAG during the Platform Manager device operation, results in the device aborting all operations and returning to the power-on reset state. The status of the power supplies which are being enabled by the Platform Manager will be determined by the state of the outputs shown above.*

## FPGA Architecture Details

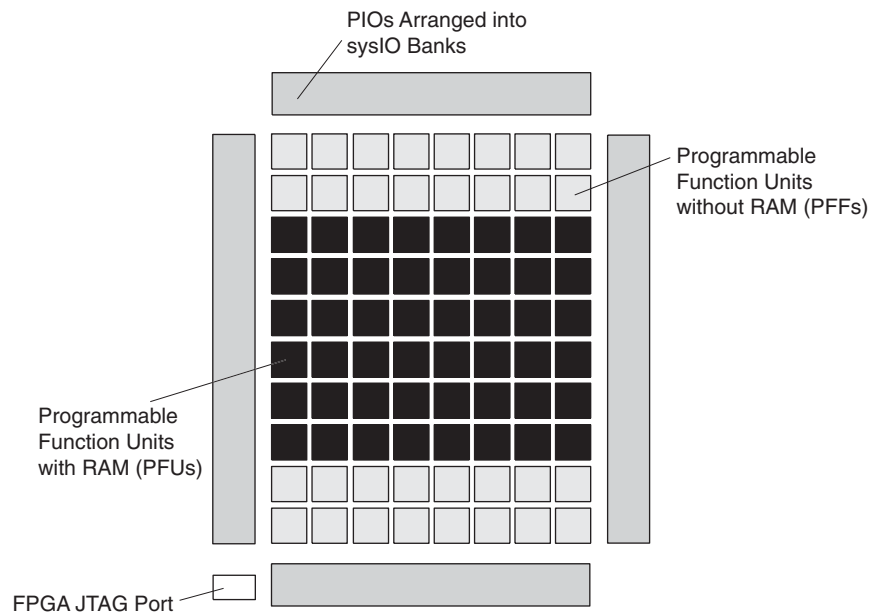
The Platform Manager FPGA architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). Figure 39 shows the block diagrams of the FPGA block.

The logic blocks are arranged in a two-dimensional grid with rows and columns. The PIO cells are located at the periphery of the device, arranged into banks. The PIOs utilize a flexible I/O buffer referred to as a sysIO interface that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and the Programmable Functional unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PFF block contains building blocks for logic, arithmetic, ROM, and register functions. Both the PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and effectively. Logic blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The FPGA JTAG port supports programming and configuration of the FPGA as well as access to the user logic.

**Figure 39. Top View of the FPGA Section**

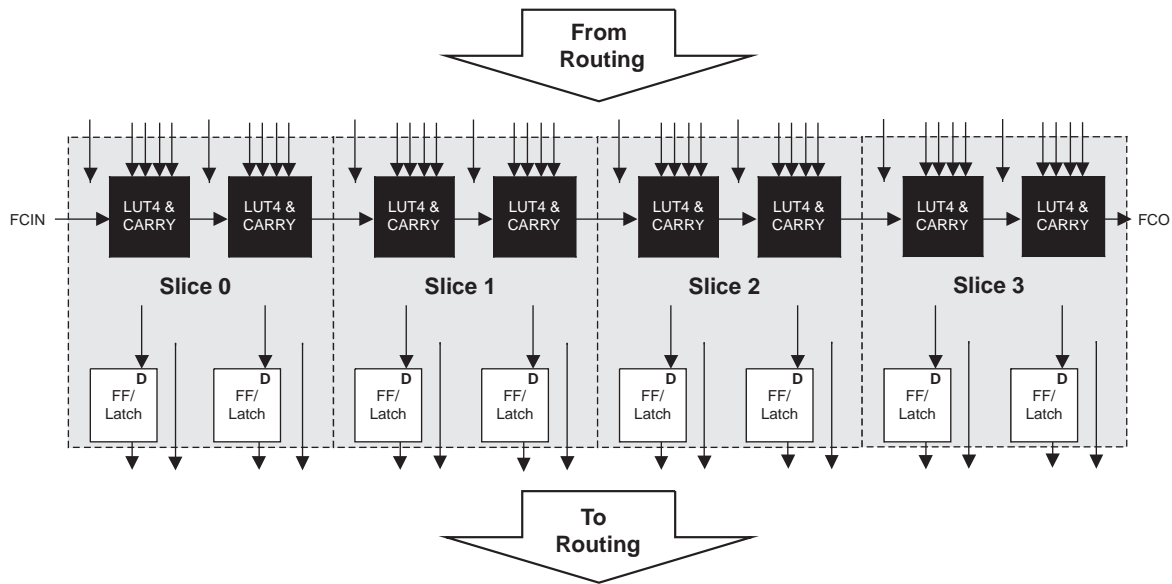


### PFU Blocks

The core of the FPGA section consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM, and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic, and Distributed ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered 0 to 3 as shown in Figure 40. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 40. PFU Diagram

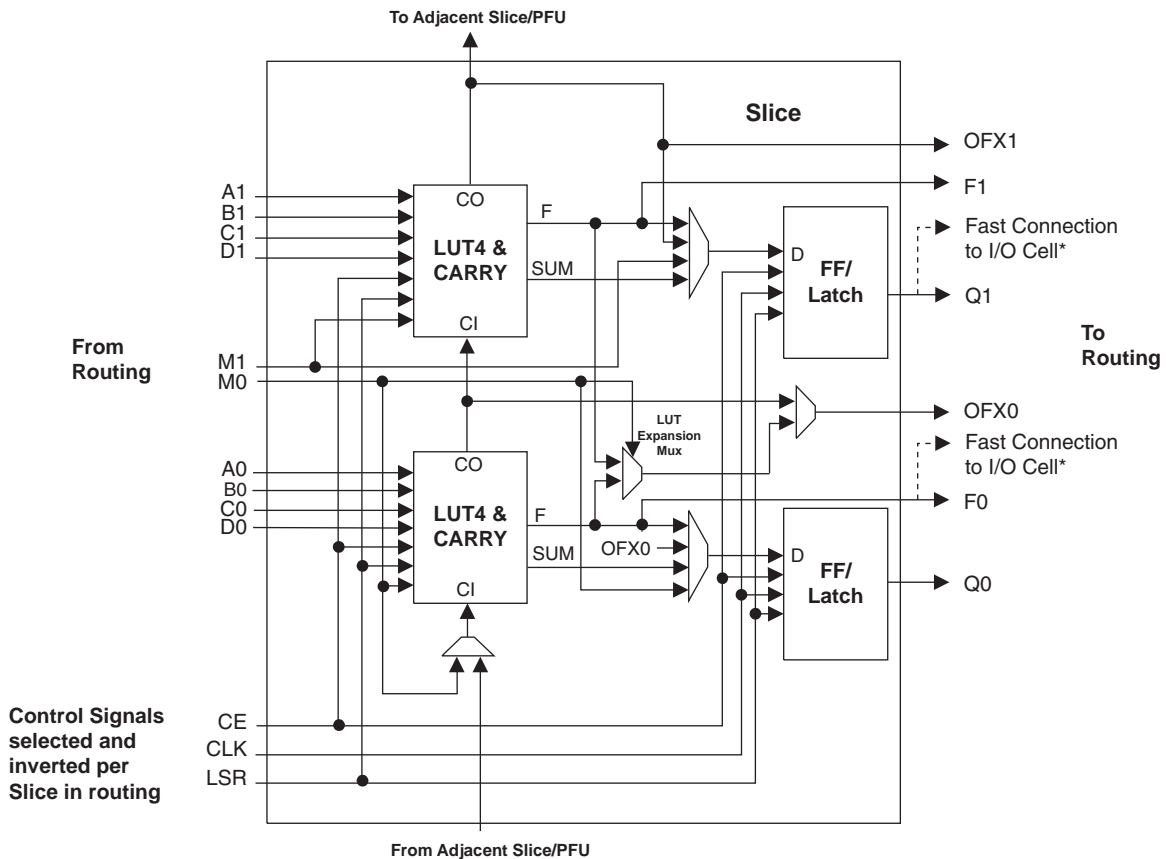


## Slice

Each slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7, and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select, and wider RAM/ROM functions. Figure 41 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge/level clocks.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent slice/PFU). There are 7 outputs: 6 to the routing and one to the carry-chain (to the adjacent slice/PFU). Table 14 lists the signals associated with each slice.

Figure 41. Slice Diagram



Notes:  
 Some inter-Slice signals are not shown.  
 \* Only PFUs at the edges have fast connections to the I/O cell.

Table 14. Slice Signal Descriptions

| Function | Type             | Signal Names   | Description  |
|----------|------------------|----------------|--|
| Input    | Data signal      | A0, B0, C0, D0 | Inputs to LUT4   |
| Input    | Data signal      | A1, B1, C1, D1 | Inputs to LUT4   |
| Input    | Multi-purpose    | M0/M1          | Multipurpose Input   |
| Input    | Control signal   | CE             | Clock Enable   |
| Input    | Control signal   | LSR            | Local Set/Reset  |
| Input    | Control signal   | CLK            | System Clock   |
| Input    | Inter-PFU signal | FCIN           | Fast Carry In <sup>1</sup>   |
| Output   | Data signals     | F0, F1         | LUT4 output register bypass signals                                  |
| Output   | Data signals     | Q0, Q1         | Register Outputs   |
| Output   | Data signals     | OFX0           | Output of a LUT5 MUX   |
| Output   | Data signals     | OFX1           | Output of a LUT6, LUT7, LUT8 <sup>2</sup> MUX depending on the slice |
| Output   | Inter-PFU signal | FCO            | Fast Carry Out <sup>1</sup>  |

1. See Figure 40 for connection details.  
 2. Requires two PFUs.



**Modes of Operation**

Each slice is capable of four modes of operation: Logic, Ripple, RAM, and ROM. The slice in the PFF is capable of all modes except RAM. Table 15 lists the modes and the capability of the slice blocks.

**Table 15. Slice Modes**

|           | Logic              | Ripple                | RAM     | ROM          |
|-----------|--------------------|-----------------------|---------|--------------|
| PFU Slice | LUT 4x2 or LUT 5x1 | 2-bit Arithmetic Unit | SP 16x2 | ROM 16x1 x 2 |
| PFF Slice | LUT 4x2 or LUT 5x1 | 2-bit Arithmetic Unit | N/A     | ROM 16x1 x 2 |

**Logic Mode:** In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables (LUT4). A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger lookup tables such as LUT6, LUT7, and LUT8 can be constructed by concatenating other slices.

**Ripple Mode:** Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Two additional signals, Carry Generate and Carry Propagate, are generated per slice in this mode, allowing fast arithmetic functions to be constructed by concatenating slices.

**RAM Mode:** In this mode, distributed RAM can be constructed using each LUT block as a 16x2-bit memory. Through the combination of LUTs and slices, a variety of different memories can be constructed.

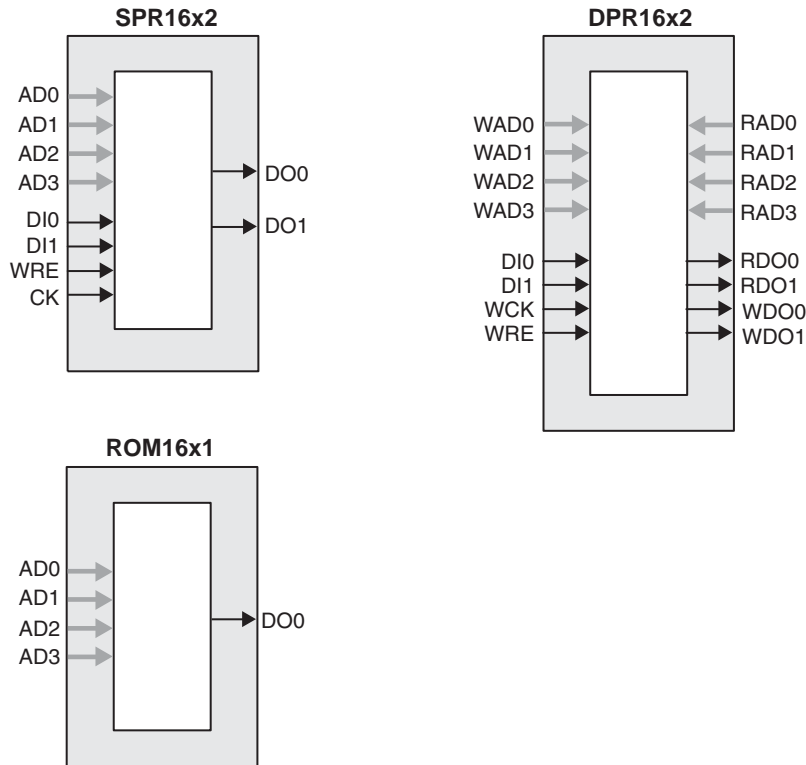
The Platform Manager design tool supports the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 16 shows the number of slices required to implement different distributed RAM primitives. Figure 42 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two slices. One slice functions as the read-write port, while the other companion slice supports the read-only port. For more information on RAM mode in the FPGA section, please see details of additional technical documentation at the end of this data sheet.

**Table 16. Number of Slices Required For Implementing Distributed RAM**

|                  | SPR16x2 | DPR16x2 |
|------------------|---------|---------|
| Number of Slices | 1       | 2       |

Note: SPR = Single Port RAM, DPR = Dual Port RAM

Figure 42. Distributed Memory Primitives



**ROM Mode:** The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

**PFU Modes of Operation**

Slices can be combined within a PFU to form larger functions. Table 17 tabulates these modes and documents the functionality possible at the PFU level.

Table 17. PFU Modes of Operation

| Logic                   | Ripple            | RAM                        | ROM         |
|-------------------------|-------------------|----------------------------|-------------|
| LUT 4x8 or MUX 2x1 x 8  | 2-bit Add x 4     | SPR16x2 x 4<br>DPR16x2 x 2 | ROM16x1 x 8 |
| LUT 5x4 or MUX 4x1 x 4  | 2-bit Sub x 4     | SPR16x4 x 2<br>DPR16x4 x 1 | ROM16x2 x 4 |
| LUT 6x 2 or MUX 8x1 x 2 | 2-bit Counter x 4 | SPR16x8 x 1                | ROM16x4 x 2 |
| LUT 7x1 or MUX 16x1 x 1 | 2-bit Comp x 4    |                            | ROM16x8 x 1 |

**Routing**

There are many resources provided in the FPGA to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

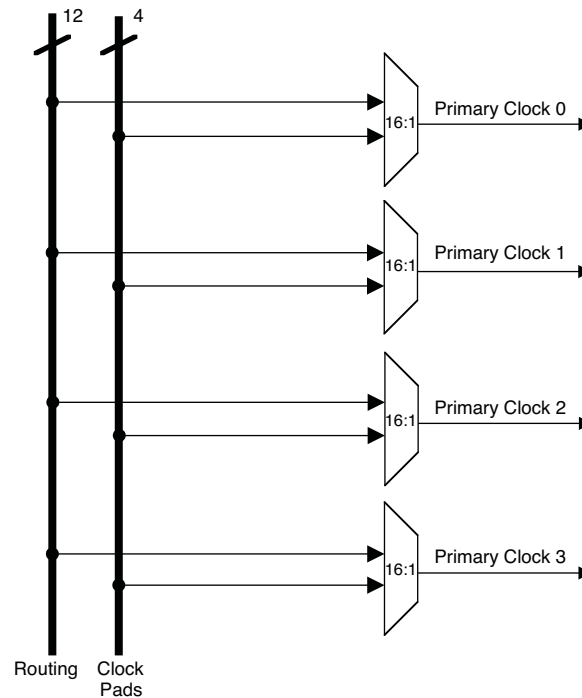
The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The Platform Manager design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

## Clock/Control Distribution Network

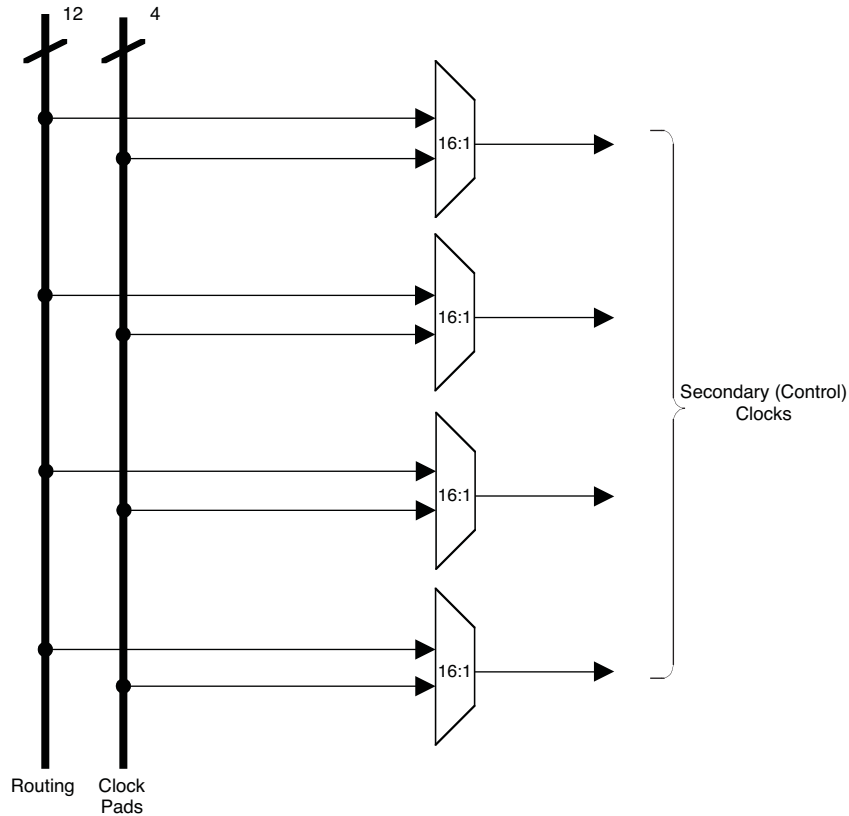
The FPGA section provides global signals that are available to all PFUs. These signals consist of four primary clocks and four secondary clocks. Primary clock signals are generated from four 16:1 muxes as shown in Figure 43. The available clock sources are four dual function clock pins and 12 internal routing signals.

**Figure 43. FPGA Primary Clocks**



Four secondary clocks are generated from four 16:1 muxes as shown in Figure 44. Four of the secondary clock sources come from dual function clock pins and 12 come from internal routing.

Figure 44. FPGA Secondary Clocks



## PIO Groups

FPGA PIO cells are assembled into two different types of PIO groups, those with four PIO cells and those with six PIO cells. PIO groups with four I/Os are placed on the left and right sides of the device while PIO groups with six I/Os are placed on the top and bottom. The individual PIO cells are connected to their respective sysIO buffers and pads.

Two adjacent PIOs can be joined to provide a complementary output driver pair. The I/O pin pairs are labeled as “T” and “C” to distinguish between the true and complement pins.

Figure 45. Group of Four Programmable I/O Cells

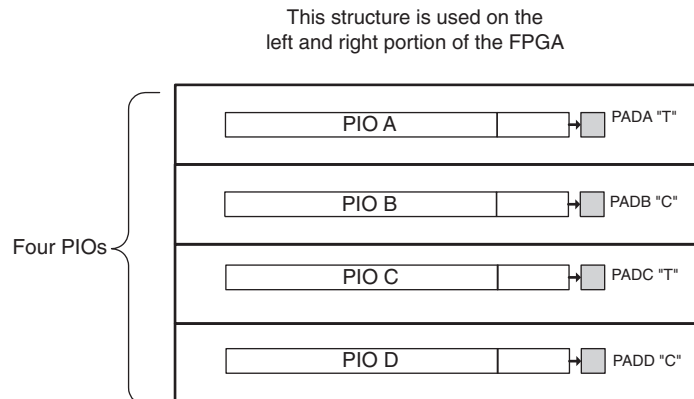
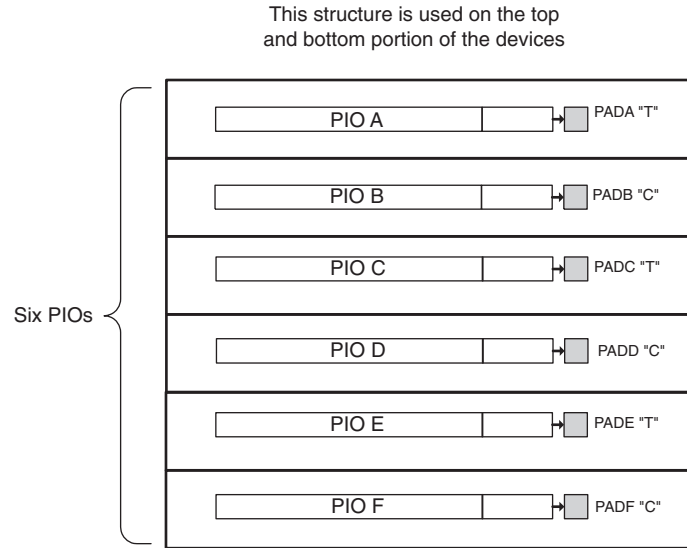


Figure 46. Group of Six Programmable I/O Cells

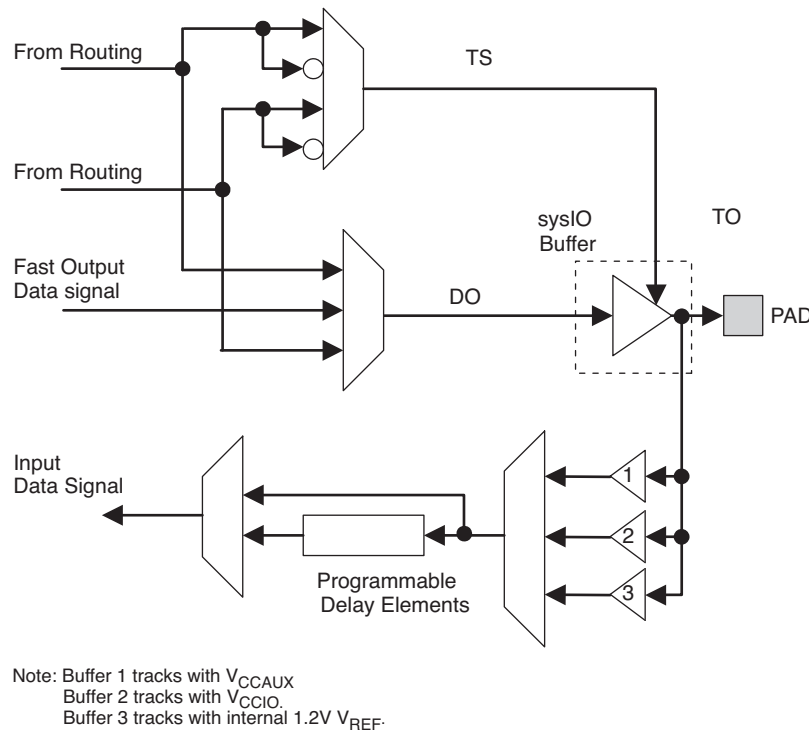


**PIO**

The PIO blocks provide the interface between the sysIO buffers and the internal PFU array blocks. These blocks receive output data from the PFU array and a fast output data signal from adjacent PFUs. The output data and fast output data signals are multiplexed and provide a single signal to the I/O pin via the sysIO buffer. Figure 47 shows the FPGA PIO logic.

The PIO receives an input signal from the pin via the sysIO buffer and provides this signal to the core of the FPGA fabric. In addition there are programmable elements that can be utilized by the design tools to avoid positive hold times.

Figure 47. PIO Block Diagram



## sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today’s systems including LVCMOS, TTL, BLVDS, LVDS and LVPECL.

FPGA output buffers and ratioed input buffers (LVTTTL and LVCMOS) are powered using  $V_{CCIO}$ . In addition to the bank  $V_{CCIO}$  supplies, the FPGA fabric has a  $V_{CC}$  core logic power supply, and a  $V_{CCAUX}$  supply that powers up a variety of internal circuits.

### Top and Bottom sysIO Buffer Pairs

The sysIO buffer pairs in the top and bottom banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (for ratioed or absolute input levels). The I/O pairs on the top and bottom of the devices also support differential input buffers.

### Left and Right sysIO Buffer Pairs

The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (supporting ratioed and absolute input levels). The devices also have a differential driver per output pair. The referenced input buffer can also be configured as a differential input buffer. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

### Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when  $V_{CC}$  and  $V_{CCAUX}$  have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all  $V_{CCIO}$  banks are active with valid input logic levels to properly control the output logic states of all the I/O

banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pull-up to  $V_{CCIO}$ . The I/O pins will maintain the blank configuration until  $V_{CC}$ ,  $V_{CCAUX}$  and  $V_{CCIO}$  have reached satisfactory levels at which time the I/Os will take on the user-configured settings.

The  $V_{CC}$  and  $V_{CCAUX}$  supply the power to the FPGA core fabric, whereas the  $V_{CCIO}$  supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, the I/O buffers should be powered up along with the FPGA core fabric. Therefore,  $V_{CCIO}$  supplies should be powered up together with the  $V_{CC}$  and  $V_{CCAUX}$  supplies. ( $V_{CC}$  and  $V_{CCAUX}$  must be physically tied together for proper operation).

### Supported Standards

The FPGA sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS and LVTTL. The buffer supports the LVTTL, LVCMOS 1.2, 1.5, 1.8, 2.5, and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS and LVPECL output emulation is also supported.

Tables 18 and 19 show the I/O standards (together with their supply and reference voltages) supported by the FPGA I/Os. For further information on utilizing the sysIO buffer to support a variety of standards please see the details of additional technical documentation at the end of this data sheet. *Note: I/O bank 2 pins do not support LVCMOS12, LVCMOS15 or LVCMOS18 standards.*

**Table 18. Supported Input Standards**

| Input Standard                 | VCCIO (Typ.) |      |                   |                   |                   |
|--------------------------------|--------------|------|-------------------|-------------------|-------------------|
|                                | 3.3V         | 2.5V | 1.8V <sup>1</sup> | 1.5V <sup>1</sup> | 1.2V <sup>1</sup> |
| <b>Single Ended Interfaces</b> |              |      |                   |                   |                   |
| LVTTL                          | X            | X    | X                 | X                 | X                 |
| LVCMOS33                       | X            | X    | X                 | X                 | X                 |
| LVCMOS25                       | X            | X    | X                 | X                 | X                 |
| LVCMOS18                       |              |      | X                 |                   |                   |
| LVCMOS15                       |              |      |                   | X                 |                   |
| LVCMOS12                       | X            | X    | X                 | X                 | X                 |

1. Not supported by I/O Bank 2 ( $V_{CCIO2}$ ).

**Table 19. Supported Output Standards**

| Output Standard                   | Drive                | VCCIO (Typ.) |
|-----------------------------------|----------------------|--------------|
| <b>Single-ended Interfaces</b>    |                      |              |
| LVTTL                             | 4mA, 8mA, 12mA, 16mA | 3.3          |
| LVCMOS33                          | 4mA, 8mA, 12mA, 14mA | 3.3          |
| LVCMOS25                          | 4mA, 8mA, 12mA, 14mA | 2.5          |
| LVCMOS18 <sup>1</sup>             | 4mA, 8mA, 12mA, 14mA | 1.8          |
| LVCMOS15 <sup>1</sup>             | 4mA, 8mA             | 1.5          |
| LVCMOS12 <sup>1</sup>             | 2mA, 6mA             | 1.2          |
| LVCMOS33, Open Drain              | 4mA, 8mA, 12mA, 14mA | —            |
| LVCMOS25, Open Drain              | 4mA, 8mA, 12mA, 14mA | —            |
| LVCMOS18, Open Drain <sup>1</sup> | 4mA, 8mA, 12mA, 14mA | —            |
| LVCMOS15, Open Drain <sup>1</sup> | 4mA, 8mA             | —            |
| LVCMOS12, Open Drain <sup>1</sup> | 2mA, 6mA             | —            |

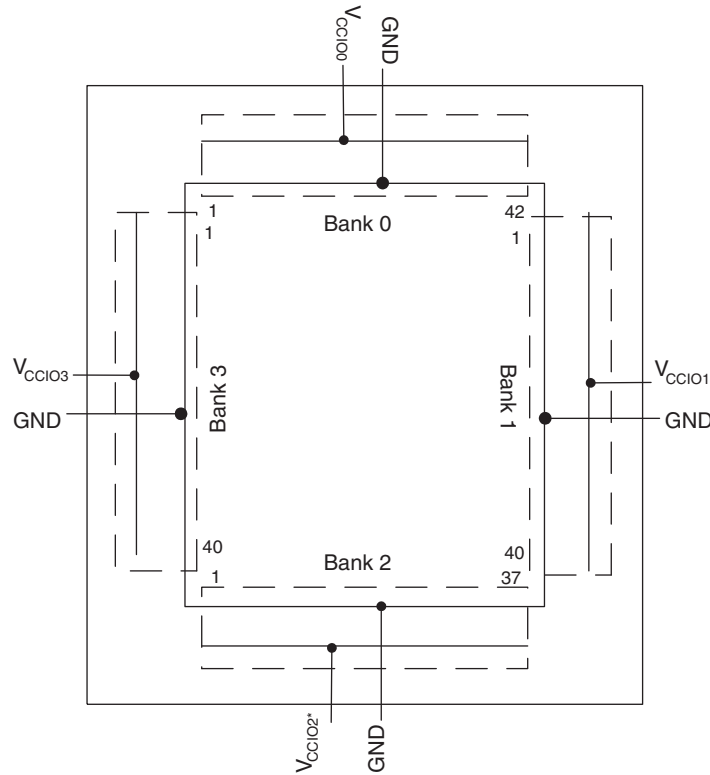
1. Not supported by I/O Bank 2 ( $V_{CCIO2}$ ).

## sysIO Buffer Banks

The FPGA I/O section has four banks (one bank per side).

Each sysIO buffer bank is capable of supporting multiple I/O standards. Each bank has its own I/O supply voltage ( $V_{CCIO}$ ) which allows it to be completely independent from the other banks. Figure 48 shows the sysIO banks organization around the FPGA fabric.

Figure 48. FPGA I/O Banks



\* $V_{CCIO2}$  is restricted to either 2.5V or 3.3V operation.

## Hot Socketing

The FPGA I/Os have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the FPGA I/Os ideal for many multiple power supply and hot-swap applications.

## Sleep Mode

The Platform Manager FPGA section has a sleep mode that allows standby current to be reduced dramatically during periods of system inactivity. Entry and exit to Sleep mode is controlled by the SLEEPN pin (see Pin Description Table).

During Sleep mode, the FPGA logic is non-operational, register contents are not maintained, and I/Os are tri-stated. Do not enter Sleep mode during device programming or configuration operation. In Sleep mode, power supplies are in their normal operating range, eliminating the need for external switching of power supplies. Table 20 compares the characteristics of Normal, Off and Sleep modes. Sleep mode does not shut down the power management section of the Platform Manager. If Sleep mode is not used, ensure that the SLEEPN pin is tied high via an external pull-up to VCC.



**Table 20. Characteristics of Normal, Off and Sleep Modes**

| Characteristic                  | Normal        | Off             | Sleep           |
|---------------------------------|---------------|-----------------|-----------------|
| SLEEPN Pin                      | High          | —               | Low             |
| Static I <sub>CC</sub>          | Typical <10mA | 0               | Typical <100μA  |
| I/O Leakage                     | <10μA         | <1mA            | <10μA           |
| Power Supplies VCC/VCCIO/VCCAUX | Normal Range  | 0               | Normal Range    |
| Logic Operation                 | User-defined  | Non-operational | Non-operational |
| I/O Operation                   | User-defined  | Tri-state       | Tri-state       |
| JTAG and Programming circuitry  | Operational   | Non-operational | Non-operational |

### SLEEPN Pin Characteristics

The SLEEPN pin behaves as an LVCMOS input with the voltage standard appropriate to the VCC supply for the device. This pin also has a weak pull-up, along with a Schmidt trigger and glitch filter to prevent false triggering. An external pull-up to VCC is recommended when Sleep Mode is not used to ensure the device stays in normal operation mode. Typically, the device enters sleep mode several hundred nanoseconds after SLEEPN is held at a valid low and restarts normal operation as specified in the Sleep Mode Timing table. The AC and DC specifications portion of this data sheet shows a detailed timing diagram. Note that Sleep mode does not shut down the power management section of the Platform Manager.

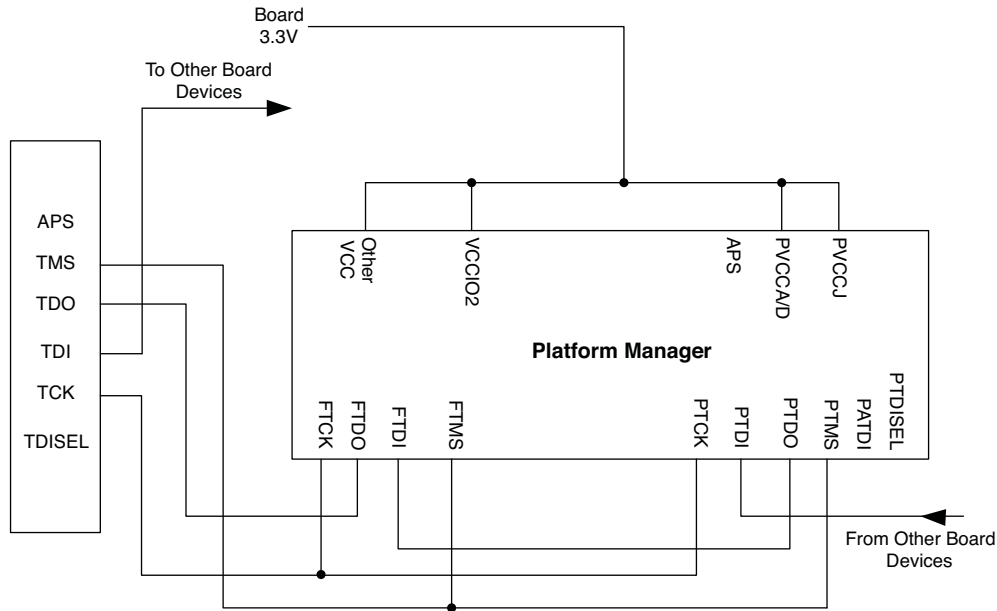
### Oscillator

The FPGA section has an internal CMOS oscillator. The oscillator can be routed as an input clock to the clock tree or to general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit to enable/disable the oscillator. The oscillator frequency ranges from 18MHz to 26MHz.

### In-System Programming – Power Management Section

The Platform Manager is an in-system programmable device. This is accomplished by integrating all E<sup>2</sup> configuration memory and control logic internally. Programming is performed through a 4-wire, IEEE 1149.1 compliant serial JTAG interface at normal logic levels. Once a device is programmed, all configuration information is stored internally, in non-volatile E<sup>2</sup>CMOS memory cells. The specifics of the IEEE 1149.1 serial interface and all Platform Manager instructions are described in the JTAG interface section of this data sheet.

Figure 49. Platform Manager JTAG Interconnection Configuration Diagram



## Programming Platform Manager: Alternate Method

Some applications require that the Platform Manager be programmed before turning the power on to the entire circuit board. To meet such application needs, the Platform Manager provides an alternate programming method which enables the programming of the Platform Manager device through the JTAG chain with a separate power supply applied just to the programming section of the Platform Manager device with the main power supply of the board turned off.

Three special purpose pins, APS, PATDI and PTDISEL, enable programming of the un-programmed Platform Manager under such circumstances. The APS pin provides power to the programming circuitry of the Platform Manager device (when PVCCD and PVCCA are unpowered). The PVCCJ pin must be powered to enable the JTAG port. The PATDI pin provides an alternate connection to the JTAG header while bypassing all the un-powered devices in the JTAG chain. PTDISEL pin enables switching between the PATDI and the standard JTAG signal PTDI. When the internally pulled-up PTDISEL = 1, standard PTDI pin is enabled and when the PTDISEL = 0, PATDI is enabled.

In order to use this feature the JTAG signals of the Platform Manager are connected to the header as shown in Figure 50. *Note: The Platform Manager should be the last device in the JTAG chain.*

After programming, the APS pin **MUST** be left floating when the PVCCD and PVCCA pins are powered.

### Alternate PTDI Selection Via JTAG Command

When the PTDISEL pin held high and four consecutive IDCODE instructions are issued, Platform Manager responds by making its active JTAG data input the PATDI pin. When PATDI is selected, data on its PTDI pin is ignored until the JTAG state machine returns to the Test-Logic-Reset state.

This method of selecting PATDI takes advantage of the fact that a JTAG device with an IDCODE register will automatically load its unique IDCODE instruction into the Instruction Register after a Test-Logic-Reset. This JTAG capability permits blind interrogation of devices so that their location in a serial chain can be identified without having to know anything about them in advance. A blind interrogation can be made using only the PTMS and PTCK control pins, which means PTDI and PTDO are not required for performing the operation. Figure 50 illustrates the logic for selecting whether the PTDI or PATDI pin is the active data input to Platform Manager.

Figure 50. Platform Manager Alternate PTDI Configuration Diagram

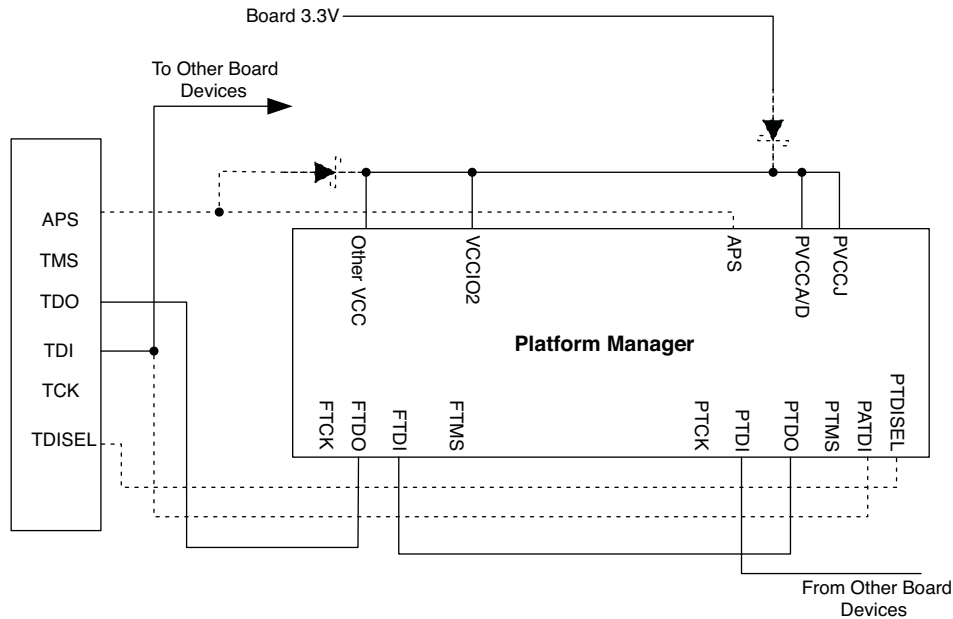


Figure 51. Power Manager PTDI/PATDI Pin Selection Diagram

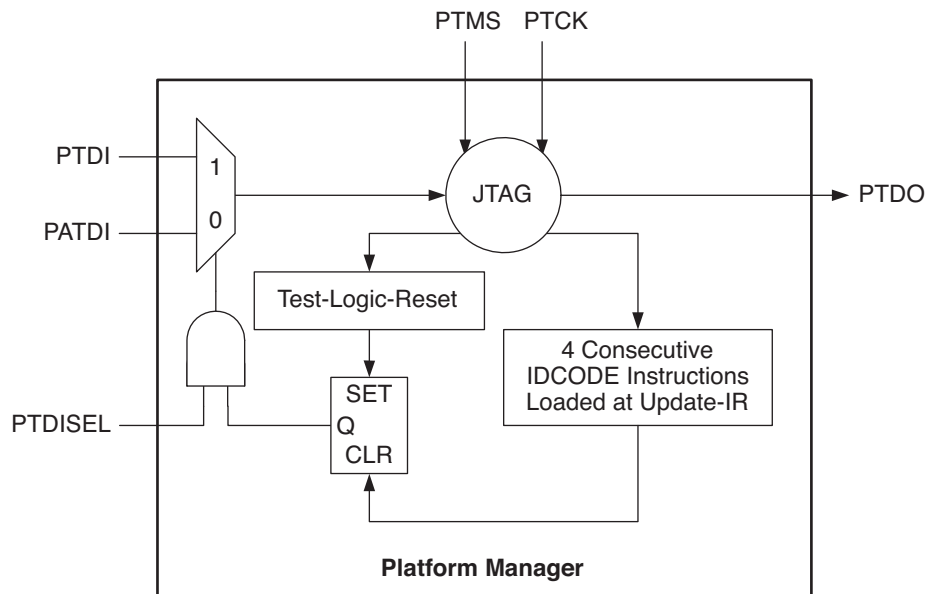


Table 21 shows in truth table form the same conditions required to select either PTDI or PATDI as in the logic diagram found in Figure 50.

**Table 21. Platform Manager PATDI/PTDI Selection Table**

| PTDISSEL Pin | JTAG State Machine Test-Logic-Reset | 4 Consecutive IDCODE Commands Loaded at Update-IR | Active JTAG Data Input Pin |
|--------------|-------------------------------------|---|----------------------------|
| H            | No                                  | Yes   | PATDI (PTDI Disabled)      |
| H            | Yes                                 | No  | PTDI (PATDI Disabled)      |
| L            | X                                   | X   | PATDI (PTDI Disabled)      |

Please refer to the Lattice application note AN6068, [Programming the ispPAC-POWR1220AT8 in a JTAG Chain Using the ATDI Pin](#). The application note includes specific SVF code examples and information on the use of Lattice design tools to verify device operation in alternate PTDI mode.

### APS Power Supply Pin

Because the APS pin directly powers the internal programming circuitry, the Platform Manager device can be programmed by applying power to the APS pin (without powering the entire device through the PVCCD and PVCCA pins). In addition, to enable the internal JTAG interface circuitry, power should be applied to the PVCCJ pin.

When the Platform Manager is powered by the APS pin, no power should be applied to the PVCCD and PVCCA pins. Additionally, other than JTAG I/O pins, all digital output pins are in Hi-Z state, HVOUT pins configured as MOSFET driver are driven low, and all other inputs are ignored.

To switch the power supply back to PVCCD and PVCCA pins, one should turn the APS supply and PVCCJ off before turning the regular supplies on. When PVCCD and PVCCA are turned back on for normal operation, APS **MUST** either be left floating or be grounded. Do not leave APS connected to a supply during normal operation.

### User Electronic Signature

A user electronic signature (UES) feature is included in the E<sup>2</sup>CMOS memory of the Platform Manager. This consists of 32 bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control data. The specifics of this feature are discussed in the IEEE 1149.1 serial interface section of this data sheet.

### Electronic Security

An electronic security “fuse” (ESF) bit is provided in every Platform Manager device to prevent unauthorized read-out of the E<sup>2</sup>CMOS configuration bit patterns. Once programmed, this cell prevents further access to the functional user bits in the device. This cell can only be erased by reprogramming the device, so the original configuration cannot be examined once programmed. Usage of this feature is optional. The specifics of this feature are discussed in the IEEE 1149.1 serial interface section of this data sheet.

### Production Programming Support

Once a final configuration is determined, an ASCII format JEDEC file can be created using the PAC-Designer software. Devices can then be ordered through the usual supply channels with the user’s specific configuration already preloaded into the devices. By virtue of its standard interface, compatibility is maintained with existing production programming equipment, giving customers a wide degree of freedom and flexibility in production planning.

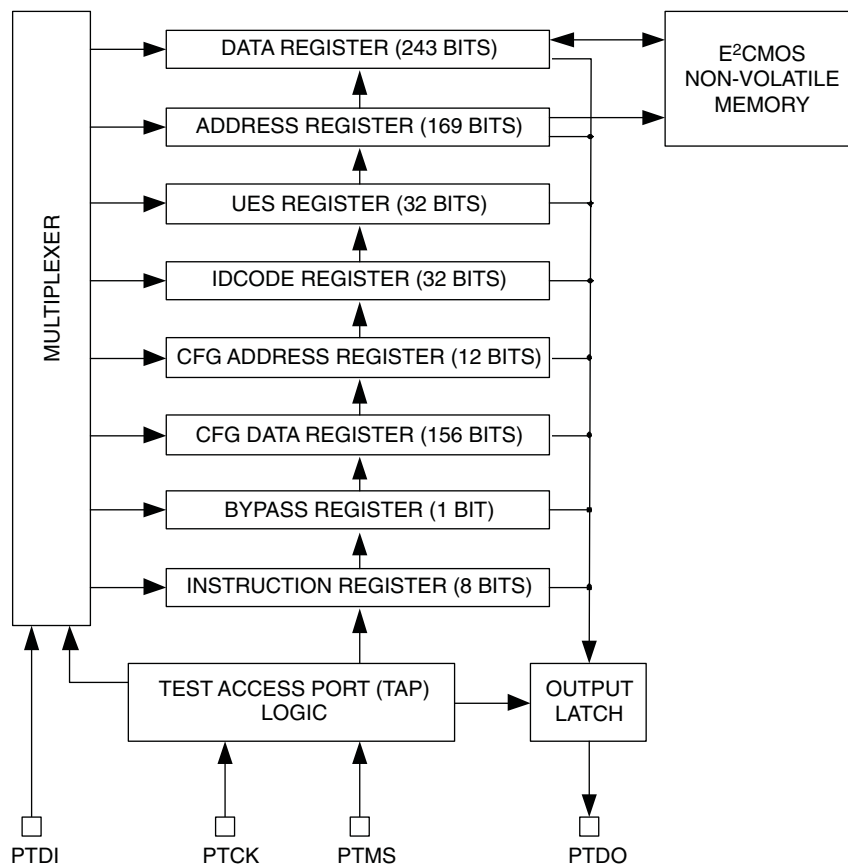
### Power Management JTAG Interface

Serial Port Programming Interface Communication with the Platform Manager is facilitated via an IEEE 1149.1 test access port (TAP). It is used by the Platform Manager as a serial programming interface. A brief description of the Platform Manager JTAG interface follows. For complete details of the reference specification, refer to the publication, Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990 (which now includes IEEE Std 1149.1a-1993).

### Overview

An IEEE 1149.1 test access port (TAP) provides the control interface for serially accessing the digital I/O of the Platform Manager. The TAP controller is a state machine driven with mode and clock inputs. Given in the correct sequence, instructions are shifted into an instruction register, which then determines subsequent data input, data output, and related operations. Device programming is performed by addressing the configuration register, shifting data in, and then executing a program configuration instruction, after which the data is transferred to internal E<sup>2</sup>CMOS cells. It is these non-volatile cells that store the configuration of the Platform Manager. A set of instructions are defined that access all data registers and perform other internal control operations. For compatibility between compliant devices, two data registers are mandated by the IEEE 1149.1 specification. Others are functionally specified, but inclusion is strictly optional. Finally, there are provisions for optional data registers defined by the manufacturer. The two required registers are the bypass and boundary-scan registers. Figure 52 shows how the instruction and various data registers are organized in an Platform Manager.

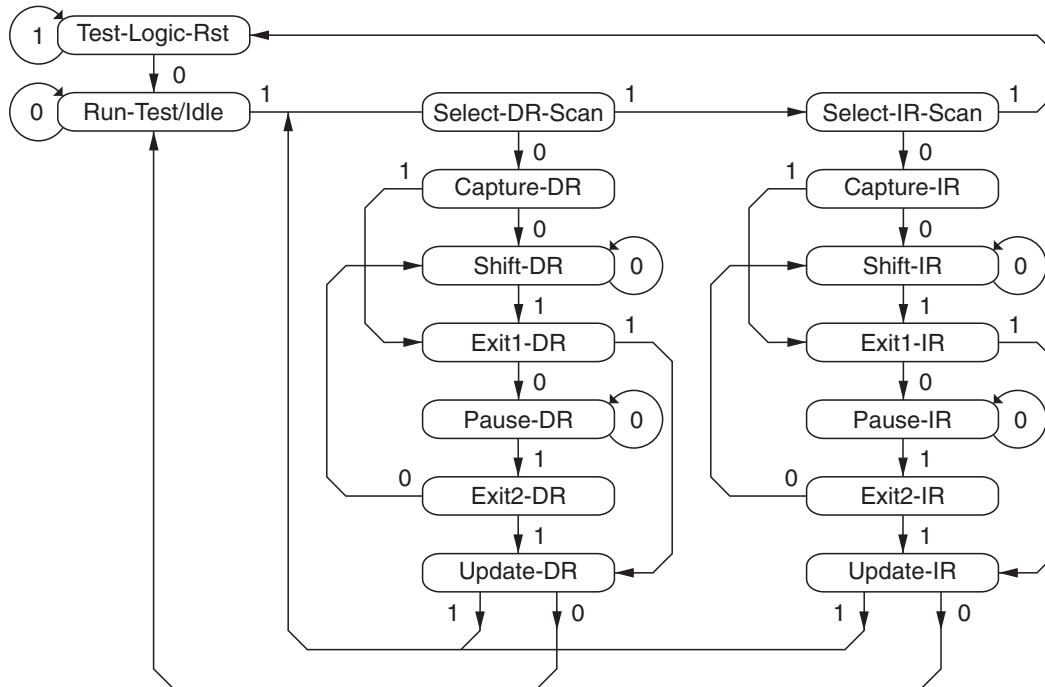
**Figure 52. Platform Manager CPLD TAP Registers**



### TAP Controller Specifics

The TAP is controlled by the Test Clock (PTCK) and Test Mode Select (PTMS) inputs. These inputs determine whether an Instruction Register or Data Register operation is performed. Driven by the PTCK input, the TAP consists of a small 16-state controller design. In a given state, the controller responds according to the level on the PTMS input as shown in Figure 53. Test Data In (PTDI) and PTMS are latched on the rising edge of PTCK, with Test Data Out (PTDO) becoming valid on the falling edge of PTCK. There are six steady states within the controller: Test-Logic-Reset, Run-Test/Idle, Shift-Data-Register, Pause-Data-Register, Shift-Instruction-Register and Pause-Instruction-Register. But there is only one steady state for the condition when PTMS is set high: the Test-Logic-Reset state. This allows a reset of the test logic within five PTCKs or less by keeping the PTMS input high. Test-Logic-Reset is the power-on default state.

Figure 53. TAP States



Note: The value shown adjacent to each state transition in this figure represents the signal present at PTMS at the time of a rising edge at PTCK.

When the correct logic sequence is applied to the PTMS and PTCK inputs, the TAP will exit the Test-Logic-Reset state and move to the desired state. The next state after Test-Logic-Reset is Run-Test/Idle. Until a data or instruction shift is performed, no action will occur in Run-Test/Idle (steady state = idle). After Run-Test/Idle, either a data or instruction shift is performed. The states of the Data and Instruction Register blocks are identical to each other differing only in their entry points. When either block is entered, the first action is a capture operation. For the Data Registers, the Capture-DR state is very simple: it captures (parallel loads) data onto the selected serial data path (previously chosen with the appropriate instruction). For the Instruction Register, the Capture-IR state will always load the IDCODE instruction. It will always enable the ID Register for readout if no other instruction is loaded prior to a Shift-DR operation. This, in conjunction with mandated bit codes, allows a “blind” interrogation of any device in a compliant IEEE 1149.1 serial chain. From the Capture state, the TAP transitions to either the Shift or Exit1 state. Normally the Shift state follows the Capture state so that test data or status information can be shifted out or new data shifted in. Following the Shift state, the TAP either returns to the Run-Test/Idle state via the Exit1 and Update states or enters the Pause state via Exit1. The Pause state is used to temporarily suspend the shifting of data through either the Data or Instruction Register while an external operation is performed. From the Pause state, shifting can resume by reentering the Shift state via the Exit2 state or be terminated by entering the Run-Test/Idle state via the Exit2 and Update states. If the proper instruction is shifted in during a Shift-IR operation, the next entry into Run-Test/Idle initiates the test mode (steady state = test). This is when the device is actually programmed, erased or verified. All other instructions are executed in the Update state.

### Test Instructions

Like data registers, the IEEE 1149.1 standard also mandates the inclusion of certain instructions. It outlines the function of three required and six optional instructions. Any additional instructions are left exclusively for the manufacturer to determine. The instruction word length is not mandated other than to be a minimum of two bits, with only the BYPASS and EXTEST instruction code patterns being specifically called out (all ones and all zeroes respectively). The Platform Manager contains the required minimum instruction set as well as one from the optional instruction set. In addition, there are several proprietary instructions that allow the device to be configured and verified. Table 22 lists the instructions supported by the Platform Manager JTAG Test Access Port (TAP) controller:

**Table 22. Power Management Section TAP Instruction Table**

| Instruction                  | Command Code | Comments   |
|------------------------------|--------------|--|
| BULK_ERASE                   | 0000 0011    | Bulk erase device  |
| BYPASS                       | 1111 1111    | Bypass – Connect PTDO to PTDI  |
| DISCHARGE                    | 0001 0100    | Fast VPP discharge   |
| ERASE_DONE_BIT               | 0010 0100    | Erases ‘Done’ bit only   |
| EXTEST                       | 0000 0000    | Bypass – Connect PTDO to PTDI  |
| IDCODE                       | 0001 0110    | Read contents of manufacturer ID code (32 bits)  |
| OUTPUTS_HIGHZ                | 0001 1000    | Force all outputs to High-Z state, FET outputs pulled low  |
| SAMPLE/PRELOAD               | 00011100     | Sample/Preload. Default to bypass.   |
| PROGRAM_DISABLE              | 0001 1110    | Disable program mode   |
| PROGRAM_DONE_BIT             | 0010 1111    | Program the Done bit   |
| PROGRAM_ENABLE               | 0001 0101    | Enable program mode  |
| PROGRAM_SECURITY             | 0000 1001    | Program security fuse  |
| RESET                        | 0010 0010    | Reset device (refer to the RESETb signal, RESET Command Via JTAG or I <sup>2</sup> C section of this data sheet) |
| IN1_RESET_JTAG_BIT           | 0001 0010    | Reset the JTAG bit associated with IN1 pin to 0  |
| IN1_SET_JTAG_BIT             | 0001 0011    | Set the JTAG bit associated with IN1 pin to 1  |
| CFG_ADDRESS                  | 0010 1011    | Select non-CPLD address register   |
| CFG_DATA_SHIFT               | 0010 1101    | Non-CPLD data shift  |
| CFG_ERASE                    | 0010 1001    | Erase just the non-CPLD configuration  |
| CFG_PROGRAM                  | 0010 1110    | Non-CPLD program   |
| CFG_VERIFY                   | 0010 1000    | Verify non-CPLD fuse map data  |
| CPLD_ADDRESS_SHIFT           | 0000 0001    | CPLD_Address register (169 bits)   |
| CPLD_DATA_SHIFT              | 0000 0010    | CPLD_Data register (243 bits)  |
| CPLD_INIT_ADDR_FOR_PROG_INCR | 0010 0001    | Initialize the address register for auto increment   |
| CPLD_PROG_INCR               | 0010 0111    | Program column register to E <sup>2</sup> CMOS and auto increment address register                               |
| CPLD_PROGRAM                 | 0000 0111    | Program CPLD data register to E <sup>2</sup> CMOS  |
| CPLD_VERIFY                  | 0000 1010    | Verify CPLD column data  |
| CPLD_VERIFY_INCR             | 0010 1010    | Load column register from ECMOS <sup>2</sup> and auto increment address register                                 |
| UES_PROGRAM                  | 0001 1010    | Program UES bits into E <sup>2</sup> CMOS  |
| UES_READ                     | 0001 0111    | Read contents of UES register from E <sup>2</sup> CMOS (32 bits)   |

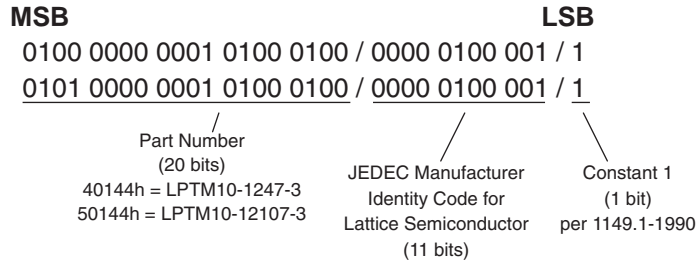
**BYPASS** is one of the three required instructions. It selects the Bypass Register to be connected between PTDI and PTDO and allows serial data to be transferred through the device without affecting the operation of the Platform Manager. The IEEE 1149.1 standard defines the bit code of this instruction to be all ones (11111111).

The required **SAMPLE/PRELOAD** instruction dictates the Boundary-Scan Register be connected between PTDI and PTDO. The Platform Manager has no boundary scan register, so for compatibility it defaults to the BYPASS mode whenever this instruction is received. The bit code for this instruction is defined by Lattice as shown in Table 22.

The **EXTEST** (external test) instruction is required and would normally place the device into an external boundary test mode while also enabling the boundary scan register to be connected between PTDI and PTDO. Again, since the Platform Manager has no boundary scan logic, the device is put in the BYPASS mode to ensure specification compatibility. The bit code of this instruction is defined by the 1149.1 standard to be all zeros (00000000).

The optional **IDCODE** (identification code) instruction is incorporated in the Platform Manager and leaves it in its functional mode when executed. It selects the Device Identification Register to be connected between PTDI and PTDO. The Identification Register is a 32-bit shift register containing information regarding the IC manufacturer, device type and version code (Figure 54). Access to the Identification Register is immediately available, via a TAP data scan operation, after power-up of the device, or by issuing a Test-Logic-Reset instruction. The bit code for this instruction is defined by Lattice as shown in Table 22.

**Figure 54. Platform Manager ID Code**



### Platform Manager Specific Instructions

There are 25 unique instructions specified by Lattice for the Platform Manager. These instructions are primarily used to interface to the various user registers and the E<sup>2</sup>CMOS non-volatile memory. Additional instructions are used to control or monitor other features of the device. A brief description of each unique instruction is provided in detail below, and the bit codes are found in Table 22.

**CPLD\_ADDRESS\_SHIFT** – This instruction is used to set the address of the CPLD AND/ARCH arrays for subsequent program or read operations. This instruction also forces the outputs into the OUTPUTS\_HIGHZ.

**CPLD\_DATA\_SHIFT** – This instruction is used to shift CPLD data into the register prior to programming or reading. This instruction also forces the outputs into the OUTPUTS\_HIGHZ.

**CPLD\_INIT\_ADDR\_FOR\_PROG\_INCR** – This instruction prepares the CPLD address register for subsequent CPLD\_PROG\_INCR or CPLD\_VERIFY\_INCR instructions.

**CPLD\_PROG\_INCR** – This instruction programs the CPLD data register for the current address and increments the address register for the next set of data.

**CPLD\_PROGRAM** – This instruction programs the selected CPLD AND/ARCH array column. The specific column is preselected by using CPLD\_ADDRESS\_SHIFT instruction. The programming occurs at the second rising edge of the PTCK in Run-Test-Idle JTAG state. The device must already be in programming mode (PROGRAM\_ENABLE instruction). This instruction also forces the outputs into the OUTPUTS\_HIGHZ.

**PROGRAM\_SECURITY** – This instruction is used to program the electronic security fuse (ESF) bit. Programming the ESF bit protects proprietary designs from being read out. The programming occurs at the second rising edge of the PTCK in Run-Test-Idle JTAG state. The device must already be in programming mode (PROGRAM\_ENABLE instruction). This instruction also forces the outputs into the OUTPUTS\_HIGHZ.

**CPLD\_VERIFY** – This instruction is used to read the content of the selected CPLD AND/ARCH array column. This specific column is preselected by using CPLD\_ADDRESS\_SHIFT instruction. This instruction also forces the outputs into the OUTPUTS\_HIGHZ.

**DISCHARGE** – This instruction is used to discharge the internal programming supply voltage after an erase or programming cycle and prepares Platform Manager for a read cycle. This instruction also forces the outputs into the OUTPUTS\_HIGHZ.

**CFG\_ADDRESS** – This instruction is used to set the address of the CFG array for subsequent program or read operations. This instruction also forces the outputs into the OUTPUTS\_HIGHZ.



**CFG\_DATA\_SHIFT** – This instruction is used to shift data into the CFG register prior to programming or reading. This instruction also forces the outputs into the OUTPUTS\_HIGHZ.

**CFG\_ERASE** – This instruction will bulk erase the CFG array. The action occurs at the second rising edge of PTCK in Run-Test-Idle JTAG state. The device must already be in programming mode (PROGRAM\_ENABLE instruction). This instruction also forces the outputs into the OUTPUTS\_HIGHZ.

**CFG\_PROGRAM** – This instruction programs the selected CFG array column. This specific column is preselected by using CFG\_ADDRESS instruction. The programming occurs at the second rising edge of the PTCK in Run-Test-Idle JTAG state. The device must already be in programming mode (PROGRAM\_ENABLE instruction). This instruction also forces the outputs into the OUTPUTS\_HIGHZ.

**CFG\_VERIFY** – This instruction is used to read the content of the selected CFG array column. This specific column is preselected by using CFG\_ADDRESS instruction. This instruction also forces the outputs into the OUTPUTS\_HIGHZ.

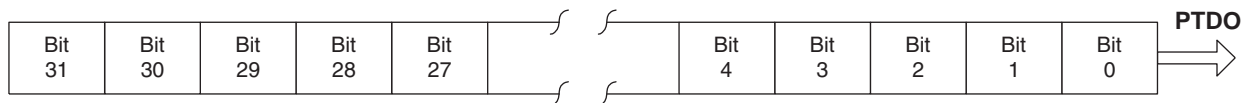
**BULK\_ERASE** – This instruction will bulk erase all E<sup>2</sup>CMOS bits (CFG, CPLD, UES, and ESF) in the Platform Manager. The device must already be in programming mode (PROGRAM\_ENABLE instruction). This instruction also forces the outputs into the OUTPUTS\_HIGHZ.

**OUTPUTS\_HIGHZ** – This instruction turns off all of the open-drain output transistors. Pins that are programmed as FET drivers will be placed in the active low state. This instruction is effective after Update-Instruction-Register JTAG state.

**PROGRAM\_ENABLE** – This instruction enables the programming mode of the Platform Manager. This instruction also forces the outputs into the OUTPUTS\_HIGHZ.

**IDCODE** – This instruction connects the output of the Identification Code Data Shift (IDCODE) Register to PTDO (Figure 55), to support reading out the identification code.

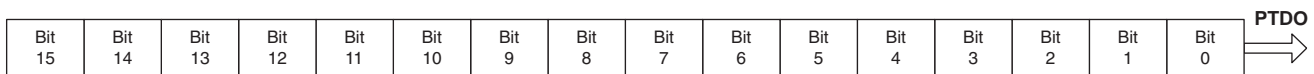
**Figure 55. IDCODE Register**



**PROGRAM\_DISABLE** – This instruction disables the programming mode of the Platform Manager. The Test-Logic-Reset JTAG state can also be used to cancel the programming mode of the Platform Manager.

**UES\_READ** – This instruction both reads the E<sup>2</sup>CMOS bits into the UES register and places the UES register between the PTDI and PTDO pins (as shown in Figure 56), to support programming or reading of the user electronic signature bits.

**Figure 56. UES Register**



**UES\_PROGRAM** – This instruction will program the content of the UES Register into the UES E<sup>2</sup>CMOS memory. The device must already be in programming mode (PROGRAM\_ENABLE instruction). This instruction also forces the outputs into the OUTPUTS\_HIGHZ.

**ERASE\_DONE\_BIT** – This instruction clears the 'Done' bit, which prevents the Platform Manager sequence from starting.

**PROGRAM\_DONE\_BIT** – This instruction sets the 'Done' bit, which enables the Platform Manager sequence to start.

**RESET** – This instruction resets the CPLD sequence and output macrocells.

**IN1\_RESET\_JTAG\_BIT** – This instruction clears the JTAG Register logic input 'IN1.' The CPLD input has to be configured to take input from the JTAG Register in order for this command to have effect on the sequence.

**IN1\_SET\_JTAG\_BIT** – This instruction sets the JTAG Register logic input 'IN1.' The CPLD input has to be configured to take input from the JTAG Register in order for this command to have effect on the sequence.

**CPLD\_VERIFY\_INCR** – This instruction reads out the CPLD data register for the current address and increments the address register for the next read.

**Notes:**

In all of the descriptions above, OUTPUTS\_HIGHZ refers both to the instruction and the state of the digital output pins, in which the open-drains are tri-stated and the FET drivers are pulled low.

Before any of the above programming instructions are executed, the respective E<sup>2</sup>CMOS bits need to be erased using the corresponding erase instruction.

## FPGA Section Configuration and Testing

The following section describes the configuration and testing features of the FPGA section of the Platform Manager device.

### IEEE 1149.1-Compliant Boundary Scan Testability

The FPGA section has boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: PTDI, PTDO, PTCK and PTMS. The test access port shares its power supply with one of the VCCIO2 banks and can operate with LVCMOS3.3 or 2.5.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.

### FPGA Section Configuration

The FPGA section contains a test access port that can be used for device configuration and programming.

The non-volatile memory of the FPGA section can be configured in two different modes:

- In IEEE 1532 mode via the IEEE 1149.1 port. In this mode, the device is off-line and I/Os are controlled by BSCAN registers.
- In background mode via the IEEE 1149.1 port. This allows the device to remain operational in user mode while reprogramming takes place.

The SRAM configuration memory can be configured in three different ways:

- At power-up via internal non-volatile memory.
- After a refresh command is issued via the IEEE 1149.1 port.
- In IEEE 1532 mode via the IEEE 1149.1 port.

Figure 57 provides a pictorial representation of the different programming modes available in the FPGA section of the Platform Manager. On power-up, the SRAM is ready to be configured with IEEE 1149.1 serial TAP port using IEEE 1532 protocols.

**Leave Alone I/O**

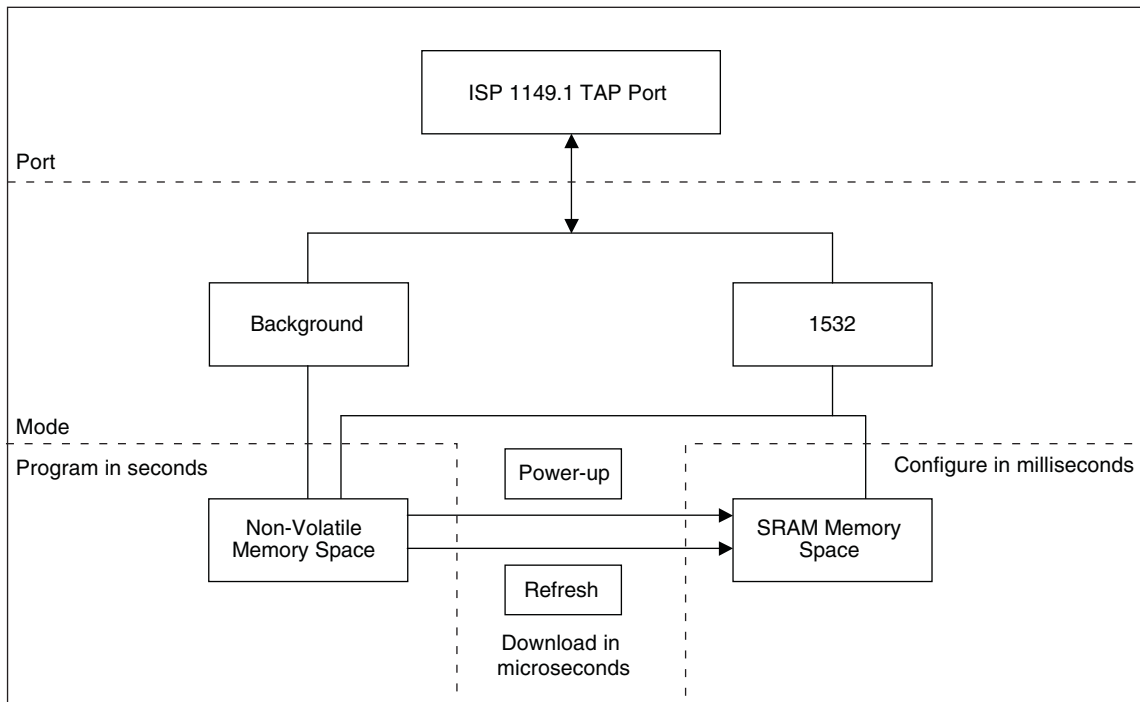
When using IEEE 1532 mode for non-volatile memory programming, SRAM configuration, or issuing a refresh command, users may specify I/Os as high, low, tri-stated or held at current value. This provides excellent flexibility for implementing systems where reconfiguration or reprogramming occurs on-the-fly.

**Security**

The FPGA section contains security bits that, when set, prevent the readback of the SRAM configuration and non-volatile memory spaces. Once set, the only way to clear the security bits is to erase the memory space.

For more information on device configuration, please see details of additional technical documentation at the end of this data sheet.

**Figure 57. FPGA Section Configuration and Programming**



## Pin Descriptions and Logic Signal Connections

| Ball/Pin Function   | 208-Ball ftBGA               | 128-Pin TQFP    | Bank | Dual Function        | Differential |
|---------------------|------------------------------|-----------------|------|----------------------|--------------|
| GND                 | A1, A16, T1, T16             | 13, 54, 78, 109 |      |                      |              |
| GNDIO0              | A4, G8, G9                   | 105, 127        | 0    |                      |              |
| GNDIO1              | A13, B13, C13, D13, A8       | 73, 95          | 1    |                      |              |
| GNDIO2              | T4, J10, J9                  | 57, 64          | 2    |                      |              |
| GNDIO3              | H1, J8, J7                   | 9, 32           | 3    |                      |              |
| PGND                |                              | 96, 128         |      |                      |              |
| PGNDA               | F14, L14                     |                 |      |                      |              |
| PGNDD               | E14, K14, D11, D14, J13, N12 |                 |      |                      |              |
| RESERVED            | J14                          | 58              |      |                      |              |
| PB2A                | R2                           |                 | 2    |                      | T            |
| PB2C                | T2                           |                 | 2    |                      | T            |
| PB2D                | T3                           |                 | 2    |                      | C            |
| PB3B                | P3                           | 39              | 2    |                      | C            |
| PB3C                | R3                           |                 | 2    |                      | T            |
| PB3D                | P4                           |                 | 2    |                      | C            |
| PB4A                | R4                           | 43              | 2    |                      | T            |
| PB4D                | T5                           |                 | 2    |                      | C            |
| PB4F                | R5                           |                 | 2    |                      | C            |
| PB5B                | P5                           | 51              | 2    | PCLK2_1 <sup>1</sup> | C            |
| PB5C                | P6                           |                 | 2    |                      | T            |
| PB5D                | N6                           |                 | 2    |                      | C            |
| PB6B                | R6                           | 53              | 2    | PCLK2_0 <sup>1</sup> | C            |
| PB6C                | T6                           |                 | 2    |                      | T            |
| PB7A                | T7                           |                 | 2    |                      | T            |
| PB7B                | R7                           |                 | 2    |                      | C            |
| PB7C                | N7                           |                 | 2    |                      | T            |
| PB7E                | P7                           |                 | 2    |                      | T            |
| PB8A                | R8                           | 56              | 2    |                      | T            |
| PB8C                | N8                           |                 | 2    |                      | T            |
| PB8D                | P8                           |                 | 2    |                      | C            |
| PB9A                | T9                           |                 | 2    |                      | T            |
| PB9C                | R9                           |                 | 2    |                      | T            |
| PB9D                | P9                           |                 | 2    |                      | C            |
| SLEEPN <sup>2</sup> | N9                           | 60              | 2    |                      |              |
| PB9F                | N10                          |                 | 2    |                      | C            |
| PL10A               | P1                           | 24              | 3    |                      | T            |
| PL10B               | R1                           |                 | 3    |                      | C            |
| PL10C               |                              | 26              | 3    |                      | T            |
| PL10D               | P2                           |                 | 3    |                      | C            |
| PL11A               | K3                           | 27              | 3    |                      | T            |
| PL11B               | L3                           |                 | 3    |                      | C            |
| PL11C               | M3                           | 28              | 3    |                      | T            |
| PL11D               | N3                           |                 | 3    |                      | C            |

**Pin Descriptions and Logic Signal Connections (Cont.)**

| Ball/Pin Function | 208-Ball ftBGA | 128-Pin TQFP | Bank | Dual Function | Differential |
|-------------------|----------------|--------------|------|---------------|--------------|
| PL2A              | F1             |              | 3    |               | T            |
| PL2B              | F2             | 3            | 3    |               | C            |
| PL3A              | F3             |              | 3    |               | T            |
| PL3B              | G2             |              | 3    |               | C            |
| PL3D              | G3             | 6            | 3    |               | C            |
| PL4A              | G1             |              | 3    |               | T            |
| PL4B              |                | 8            | 3    |               | C            |
| PL4D              | H2             |              | 3    |               | C            |
| PL5A              | G4             |              | 3    |               | T            |
| PL5B              | H4             |              | 3    | GSRN          | C            |
| PL5C              | J1             |              | 3    |               | T            |
| PL5D              | K1             |              | 3    |               | C            |
| PL6A              | K2             |              | 3    |               | T            |
| PL6D              | J2             |              | 3    |               | C            |
| PL7A              | H3             |              | 3    |               | T            |
| PL7B              | J3             |              | 3    |               | C            |
| PL7D              | J4             |              | 3    |               | C            |
| PL8A              | L1             |              | 3    |               | T            |
| PL8C              | M1             |              | 3    | TSALL         | T            |
| PL8D              | L2             |              | 3    |               | C            |
| PL9A              |                | 21           | 3    |               | T            |
| PL9C              | M2             | 23           | 3    |               | T            |
| PL9D              | N2             |              | 3    |               | C            |
| PR10A             | B9             |              | 1    |               | T            |
| PR10C             | C9             |              | 1    |               | T            |
| PR11A             | D9             |              | 1    |               | T            |
| PR11C             | D10            |              | 1    |               | T            |
| PR2B              | C6             | 91           | 1    |               | C            |
| PR2D              | B6             | 89           | 1    |               | C            |
| PR3B              | B5             |              | 1    |               | C            |
| PR3D              | A5             | 87           | 1    |               | C            |
| PR4B              | D7             | 85           | 1    |               | C            |
| PR4D              | C7             |              | 1    |               | C            |
| PR6C              | B7             |              | 1    |               | T            |
| PR6D              | A7             |              | 1    |               | C            |
| PR7B              | D8             |              | 1    |               | C            |
| PR8A              | C8             |              | 1    |               | T            |
| PR8C              | B8             |              | 1    |               | T            |
| PR9B              | A9             |              | 1    |               | C            |
| PT2B              | F4             | 123          | 0    |               | C            |
| PT2C              | E3             |              | 0    |               | T            |
| PT2E              | E4             |              | 0    |               | T            |
| PT2F              | E2             | 121          | 0    |               | C            |
| PT3B              | E1             |              | 0    |               | C            |

**Pin Descriptions and Logic Signal Connections (Cont.)**

| Ball/Pin Function   | 208-Ball ftBGA | 128-Pin TQFP    | Bank | Dual Function        | Differential |
|---------------------|----------------|-----------------|------|----------------------|--------------|
| PT3C                | D3             | 119             | 0    |                      | T            |
| PT3E                | D2             |                 | 0    |                      | T            |
| PT3F                | D1             | 115             | 0    |                      | C            |
| PT4B                | C3             |                 | 0    |                      | C            |
| PT4C                | C2             |                 | 0    |                      | T            |
| PT4E                | B1             |                 | 0    |                      | T            |
| PT5A                | B2             |                 | 0    |                      | T            |
| PT5B                | A2             | 112             | 0    | PCLK0_0 <sup>1</sup> | C            |
| PT6A                | D4             |                 | 0    |                      | T            |
| PT6B                | D5             | 110             | 0    | PCLK0_1 <sup>1</sup> | C            |
| PT6C                | C4             |                 | 0    |                      | T            |
| PT7A                | B3             | 108             | 0    |                      | T            |
| PT7E                | A3             | 106             | 0    |                      | T            |
| PT8A                | B4             |                 | 0    |                      | T            |
| PT8C                |                | 104             | 0    |                      | T            |
| PT9A                | D6             | 102             | 0    |                      | T            |
| PT9C                |                | 100             | 0    |                      | T            |
| PT9E                | C5             | 98              | 0    |                      | T            |
| FTCK                | L4             | 37              |      |                      |              |
| FTDI                | N4             | 46              |      |                      |              |
| FTDO                | M4             | 44              |      |                      |              |
| FTMS                | K4             | 34              |      |                      |              |
| VCC <sup>3</sup>    | H8, H9         | 17, 48, 82, 114 |      |                      |              |
| VCCAUX <sup>3</sup> | N5             | 50, 113         |      |                      |              |
| VCCIO0              | G7, H7, C1     | 97, 125         | 0    |                      |              |
| VCCIO1              | G10, H10, A6   | 66, 93          | 1    |                      |              |
| VCCIO2              | K9, T8, K10    | 33, 62          | 2    |                      |              |
| VCCIO3              | K8, N1, K7     | 1, 30           | 3    |                      |              |
| APS                 | M14            | 49              |      |                      |              |
| PVCCA <sup>4</sup>  | H13            | 76              |      |                      |              |
| PVCCD <sup>4</sup>  | N14, D12, P14  | 16, 47, 120     |      |                      |              |
| PVCCINP             | G14            | 7               |      |                      |              |
| PVCCJ               | N11            | 41              |      |                      |              |
| CPLDCLK             | C11            | 122             |      |                      |              |
| MCLK                | B11            | 124             |      |                      |              |
| RESETB              | C12            | 116             |      |                      |              |
| RESERVED            | H14            | 75              |      |                      |              |
| SCL                 | B12            | 117             |      |                      |              |
| SDA                 | A12            | 118             |      |                      |              |
| IN1                 | A11            | 126             |      |                      |              |
| IN2                 | C10            | 2               |      |                      |              |
| IN3                 | B10            | 4               |      |                      |              |
| IN4                 | A10            | 5               |      |                      |              |
| HVOUT1              | F13            | 111             |      |                      |              |

**Pin Descriptions and Logic Signal Connections (Cont.)**

| Ball/Pin Function       | 208-Ball ftBGA | 128-Pin TQFP | Bank | Dual Function | Differential |
|-------------------------|----------------|--------------|------|---------------|--------------|
| HVOUT2                  | E13            | 107          |      |               |              |
| HVOUT3                  | L13            | 55           |      |               |              |
| HVOUT4                  | K13            | 52           |      |               |              |
| SMBA_OUT5               | G13            | 10           |      |               |              |
| OUT6                    | T10            | 11           |      |               |              |
| OUT7                    | R10            | 12           |      |               |              |
| OUT8                    | T11            | 14           |      |               |              |
| OUT9                    | T12            | 19           |      |               |              |
| OUT10                   | R11            | 20           |      |               |              |
| OUT11                   | R12            | 15           |      |               |              |
| OUT12                   | P10            | 18           |      |               |              |
| OUT13                   | T13            | 22           |      |               |              |
| OUT14                   | P11            | 25           |      |               |              |
| OUT15                   | T14            | 29           |      |               |              |
| OUT16                   | R13            | 31           |      |               |              |
| PATDI <sup>5, 8</sup>   | R14            | 36           |      |               |              |
| PTCK                    | M13            | 45           |      |               |              |
| PTDI <sup>6, 8</sup>    | P13            | 38           |      |               |              |
| PTDISEL <sup>7, 8</sup> | T15            | 40           |      |               |              |
| PTDO                    | N13            | 42           |      |               |              |
| PTMS                    | P12            | 35           |      |               |              |
| TRIM1                   | A14            |              |      |               |              |
| TRIM2                   | A15            |              |      |               |              |
| TRIM3                   | B14            | 103          |      |               |              |
| TRIM4                   | B15            | 101          |      |               |              |
| TRIM5                   | B16            | 99           |      |               |              |
| TRIM6                   | C14            | 94           |      |               |              |
| TRIM7                   | C15            | 92           |      |               |              |
| TRIM8                   | C16            | 90           |      |               |              |
| VMON1GS                 | R15            |              |      |               |              |
| VMON1                   | R16            | 59           |      |               |              |
| VMON2GS                 | P15            | 61           |      |               |              |
| VMON2                   | P16            | 63           |      |               |              |
| VMON3GS                 | N15            | 65           |      |               |              |
| VMON3                   | N16            | 67           |      |               |              |
| VMON4GS                 | M15            | 68           |      |               |              |
| VMON4                   | M16            | 69           |      |               |              |
| VMON5GS                 | L15            | 70           |      |               |              |
| VMON5                   | L16            | 71           |      |               |              |
| VMON6GS                 | K15            | 72           |      |               |              |
| VMON6                   | K16            | 74           |      |               |              |
| VMON7GS                 | J15            | 77           |      |               |              |
| VMON7                   | J16            | 79           |      |               |              |
| VMON8GS                 | H15            | 80           |      |               |              |

## Pin Descriptions and Logic Signal Connections (Cont.)

| Ball/Pin Function | 208-Ball ftBGA | 128-Pin TQFP | Bank | Dual Function | Differential |
|-------------------|----------------|--------------|------|---------------|--------------|
| VMON8             | H16            | 81           |      |               |              |
| VMON9GS           | G15            |              |      |               |              |
| VMON9             | G16            | 83           |      |               |              |
| VMON10GS          | F15            |              |      |               |              |
| VMON10            | F16            | 84           |      |               |              |
| VMON11GS          | E15            |              |      |               |              |
| VMON11            | E16            | 86           |      |               |              |
| VMON12GS          | D15            |              |      |               |              |
| VMON12            | D16            | 88           |      |               |              |

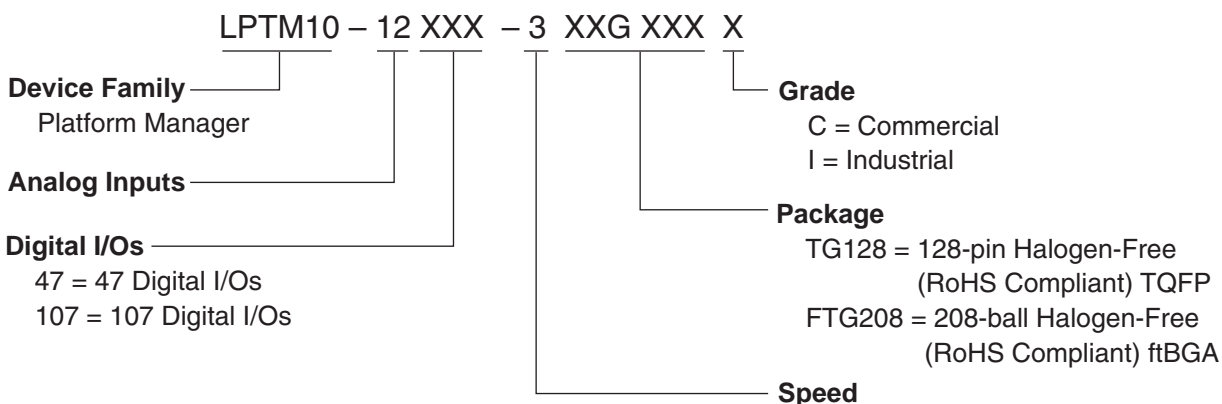
1. Primary clock inputs are single-ended.
2. Ensure that SLEEPN is tied to VCC via an external pull-up when the function will not be used or the Platform Manager FPGA section will not function correctly.
3. VCC and VCCAUX pins must be physically tied together for proper device operation.
4. PVCCA and PVCCD pins must be physically tied together for proper device operation.
5. PATDI pin is the alternate JTAG Test Data In, PTDISEL Pin = 0.
6. PTDI pin is the main JTAG Test Data In, PTDISEL Pin = 1.
7. This pin selects the JTAG Test Data Input pin PTDI/PATDI.
8. This pin has an internal pull-up.

## Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the [Thermal Management](#) document to find the device/package specific thermal values.



## Part Number Description



## Ordering Information

### Halogen-Free (RoHS Compliant) Packaging

| Part Number           | Package | Pins/Balls | Temp. |
|-----------------------|---------|------------|-------|
| LPTM10-1247-3TG128C   | TQFP    | 128        | COM   |
| LPTM10-1247-3TG128I   | TQFP    | 128        | IND   |
| LPTM10-12107-3FTG208C | ftBGA   | 208        | COM   |
| LPTM10-12107-3FTG208I | ftBGA   | 208        | IND   |

## For Further Information

For further information, refer to the following MachXO-specific literature which also applies to Platform Manager:

- TN1086, [MachXO JTAG Programming and Configuration User's Guide](#)
- TN1090, [Power Estimation and Management for MachXO™ Devices](#)
- TN1091, [MachXO sysIO Usage Guide](#)
  - Power Calculator tool included with the Platform Manager design tools, or as a standalone download from [www.latticesemi.com/software](http://www.latticesemi.com/software)
- TN1223, Using Platform Manager Successfully
  - Guidelines for practical circuits using Platform Manager

## Technical Support Assistance

Hotline: 1-800-LATTICE (North America)  
+1-503-268-8001 (Outside North America)  
e-mail: [isppacs@latticesemi.com](mailto:isppacs@latticesemi.com)  
Internet: [www.latticesemi.com](http://www.latticesemi.com)

## Revision History

| Date          | Version | Change Summary  |
|---------------|---------|---|
| October 2010  | 01.0    | Initial release.  |
| December 2010 | 01.1    | Typographical changes and clarifications.                                   |
| February 2012 | 01.2    | Added footnotes 5-8 to Pin Descriptions and Logic Signal Connections table. |
| February 2012 | 01.3    | Updated document with new corporate logo.                                   |

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