

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ max}$	$I_D \text{ max}$ $T_A = +25^\circ\text{C}$
30V	14mΩ @ $V_{GS} = 10\text{V}$	8.6A
	20mΩ @ $V_{GS} = 4.5\text{V}$	7.1A

Description

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

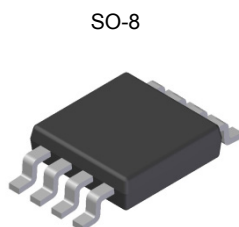
- Backlighting
- Power Management Functions
- DC-DC Converters

Features

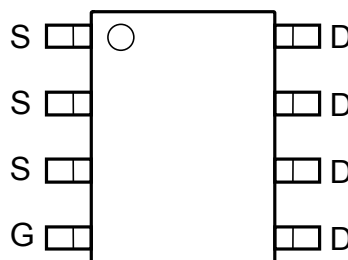
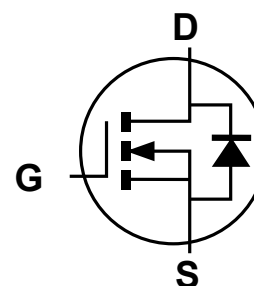
- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See Diagram
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208 ⁽³⁾
- Weight: 0.072g (approximate)



Top View


 Top View
Internal Schematic


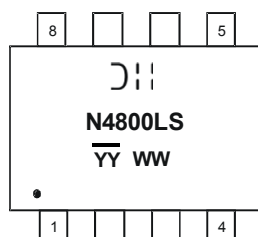
Equivalent circuit

Ordering Information (Note 4)

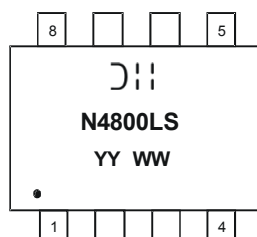
Part Number	Case	Packaging
DMN4800LSS-13	SO-8	2500/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



Chengdu A/T Site



Shanghai A/T Site

JII = Manufacturer's Marking
 N4800LS = Product Type Marking Code
 YYWW = Date Code Marking
 YY or YY = Year (ex: 13 = 2013)
 WW = Week (01 - 53)
 YY = Date Code Marking for SAT (Shanghai Assembly/ Test site)
 YY = Date Code Marking for CAT (Chengdu Assembly/ Test site)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V _{DSS}	30	V
Gate-Source Voltage			V _{GSS}	±25	V
Continuous Drain Current (Note 6) V _{GS} = 10V	Steady State	T _A = +25°C T _A = +70°C	I _D	8.6 6.3	A
	t < 10s	T _A = +25°C T _A = +70°C	I _D	11.8 9.0	A
Maximum Body Diode Forward Current (Note 6)			I _S	2.4	A
Pulsed Drain Current (Note 7)			I _{DM}	50	A

Thermal Characteristics

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)	T _A = +25°C	P _D	1.46	W
	T _A = +70°C		0.9	
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	R _{θJA}	86	°C/W
	t < 10s		46	
Total Power Dissipation (Note 6)	T _A = +25°C	P _D	1.7	W
	T _A = +70°C		1.0	
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	R _{θJA}	75	°C/W
	t < 10s		40	
Thermal Resistance, Junction to Case (Note 6)		R _{θJC}	15	
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV _{DSS}	30	—	—	V	V _{GS} = 0V, I _D = 250μA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	1	μA	V _{DS} = 30V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(th)}	0.8	1.2	1.6	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(on)}	—	11	14	mΩ	V _{GS} = 10V, I _D = 9A
			14	20		V _{GS} = 4.5V, I _D = 7A
Forward Transconductance	g _{fs}	—	8	—	S	V _{DS} = 10V, I _D = 9A
Diode Forward Voltage (Note 8)	V _{SD}	—	0.72	0.94	V	V _{GS} = 0V, I _S = 1A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iss}	—	798	—	pF	V _{DS} = 10V, V _{GS} = 0V f = 1.0MHz
Output Capacitance	C _{oss}	—	128	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	122	—	pF	
Gate Resistance	R _G	—	1.37	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1.0MHz
Total Gate Charge	Q _g	—	8.7	—	nC	V _{GS} = 5V, V _{DS} = 15V, I _D = 9A
Gate-Source Charge	Q _{gs}	—	1.7	—		
Gate-Drain Charge	Q _{gd}	—	2.4	—		
Turn-On Delay Time	t _{d(on)}	—	5.03	—	ns	V _{DD} = 15V, V _{GEN} = 10V, R _L = 15Ω, R _G = 6.0Ω, I _D = 1A
Rise Time	t _r	—	4.50	—		
Turn-Off Delay Time	t _{d(off)}	—	26.33	—		
Fall Time	t _f	—	8.55	—		

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper pad layout
 - Repetitive rating, pulse width limited by junction temperature.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing.

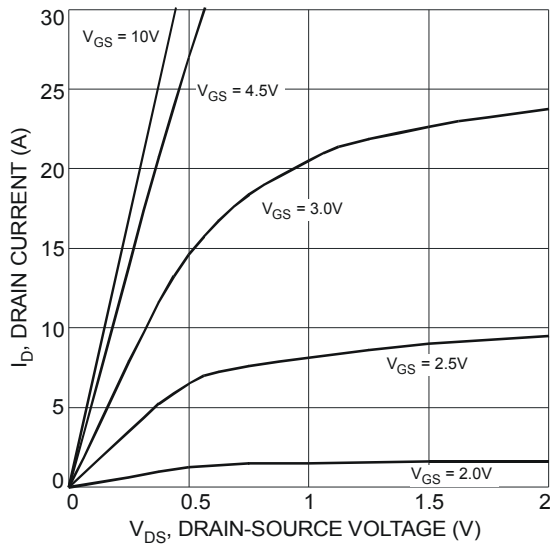


Fig. 1 Typical Output Characteristic

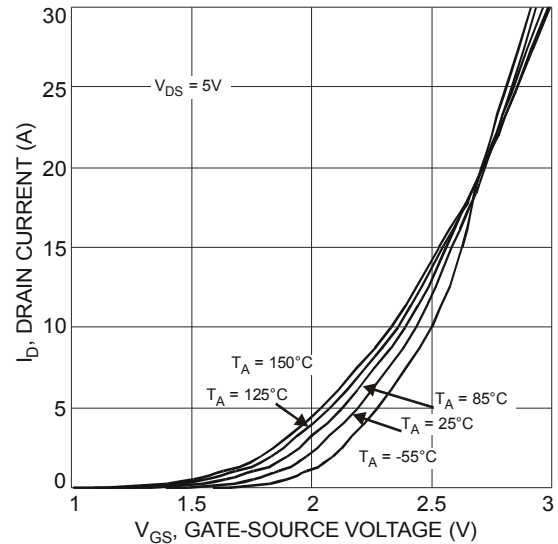


Fig. 2 Typical Transfer Characteristic

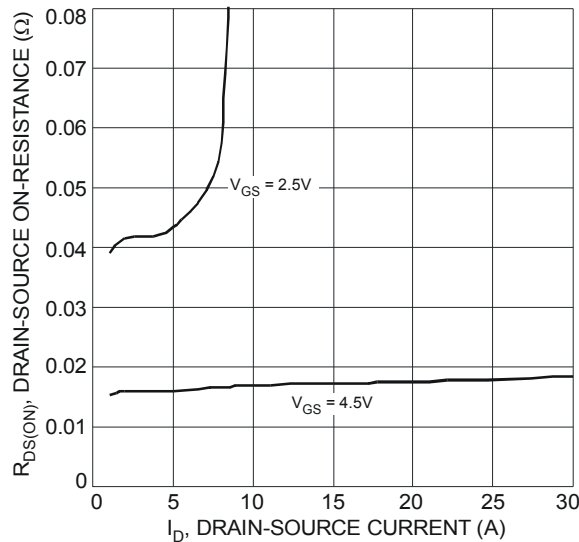


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

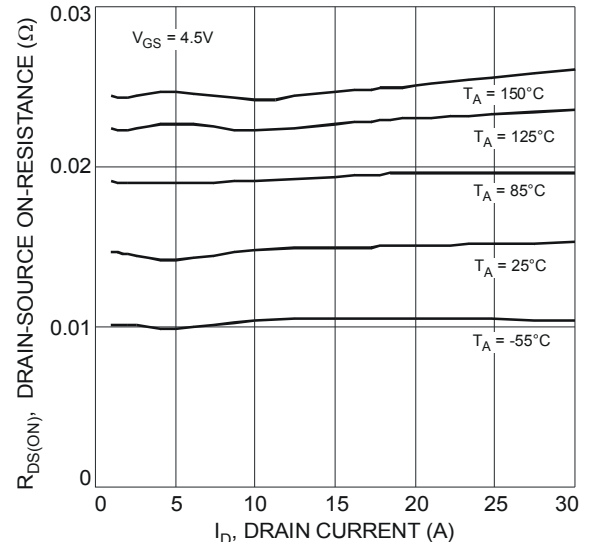


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

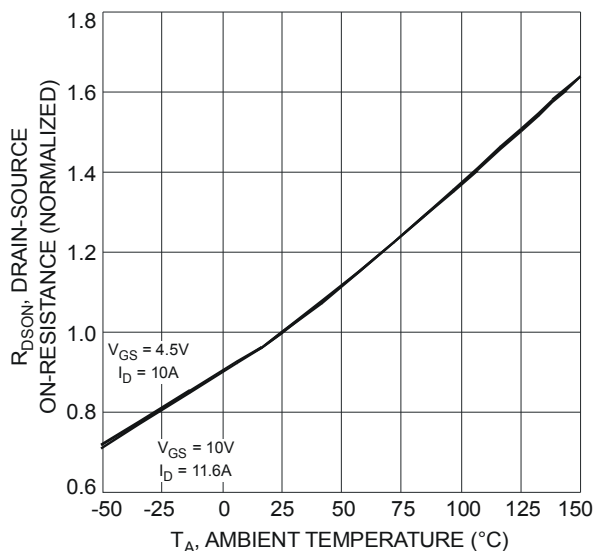


Fig. 5 On-Resistance Variation with Temperature

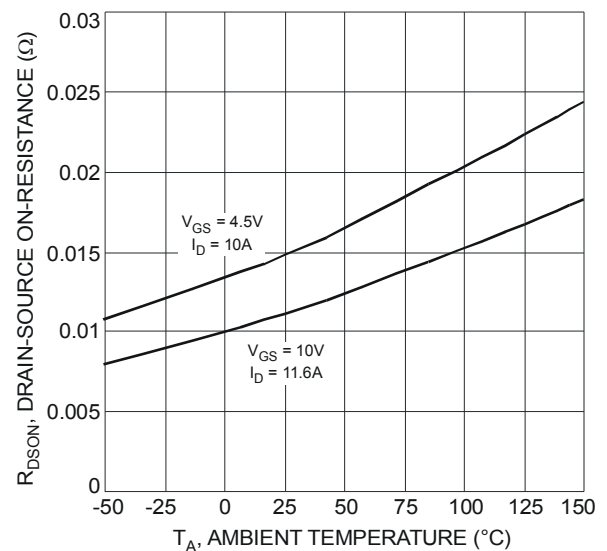


Fig. 6 On-Resistance Variation with Temperature

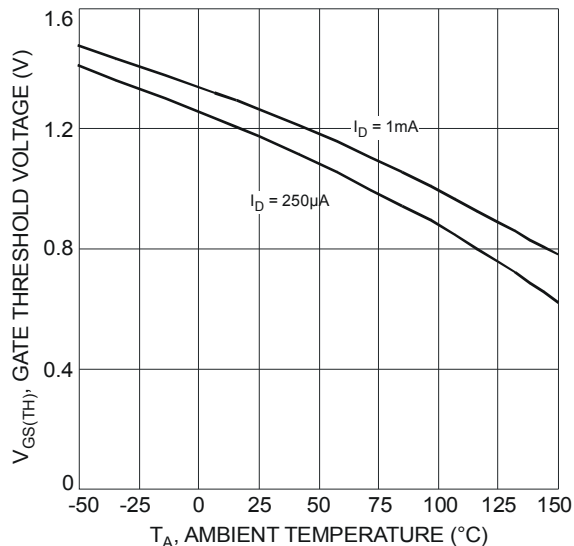


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

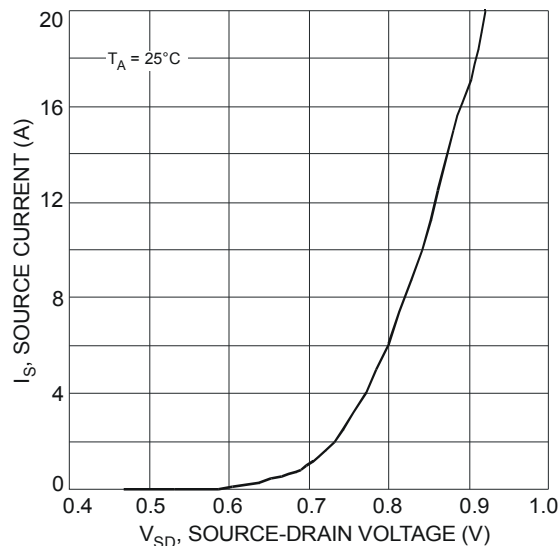


Fig. 8 Diode Forward Voltage vs. Current

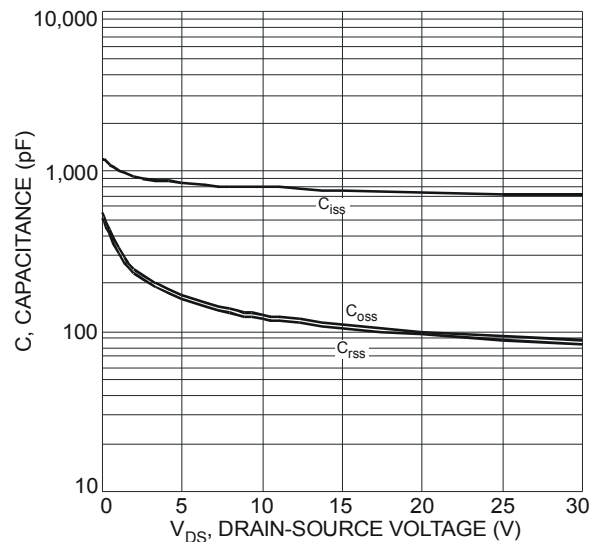


Fig. 9 Typical Total Capacitance

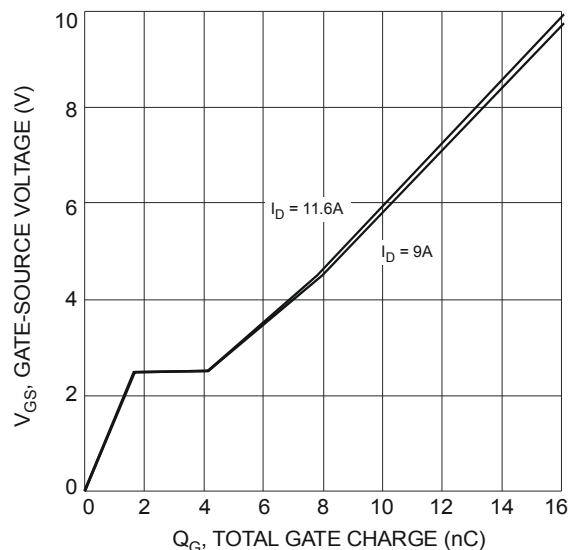


Fig. 10 Total Gate Charge

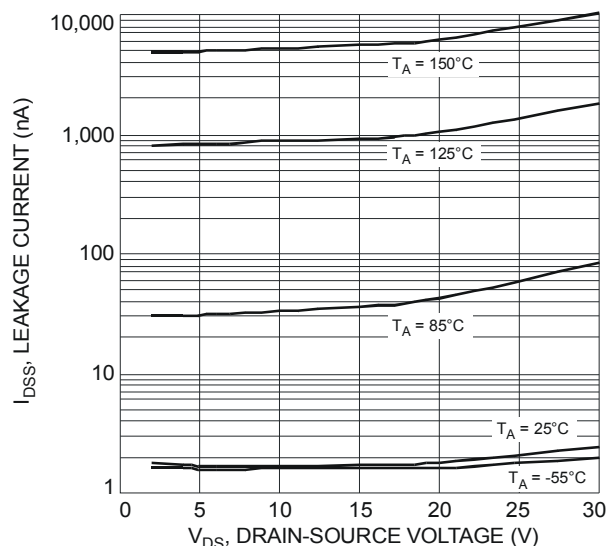


Fig. 11 Typical Leakage Current vs. Drain-Source Voltage

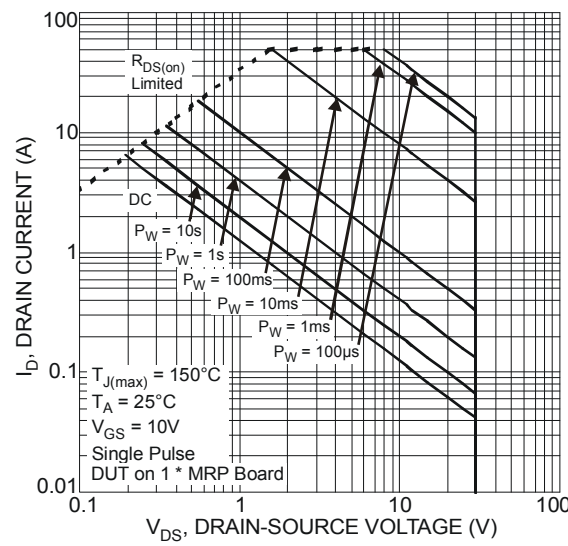


Fig. 12 SOA, Safe Operation Area

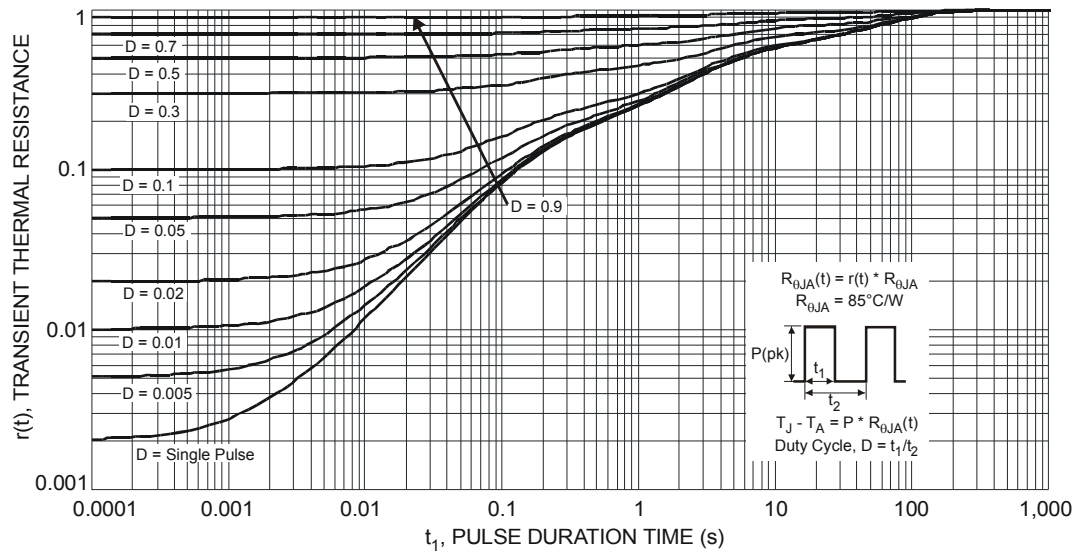
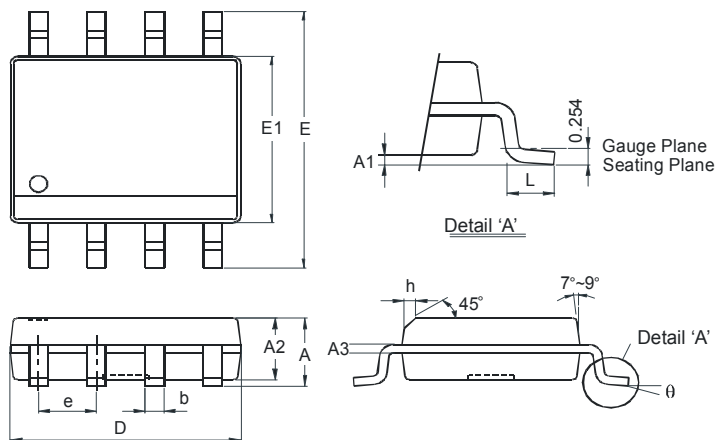


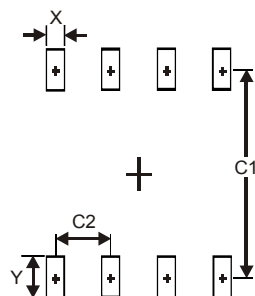
Fig. 13 Transient Thermal Response

Package Outline Dimensions



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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