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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FDD5612

## 60V N-Channel PowerTrench® MOSFET

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications. The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

Features

- 18 A, 60 V. $R_{DS(ON)}$ = 55 mΩ @ V_{GS} = 10 V
                 $R_{DS(ON)}$ = 64 mΩ @ V_{GS} = 6 V

- Optimized for use in high frequency DC/DC converters.

- Low gade charge.

- Very fast switching.

TO-252
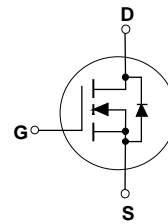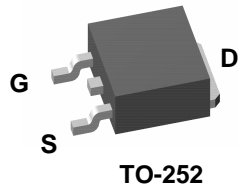
Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		60	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current – Continuous	(Note 1)	18	A
		(Note 1a)	5.4	
	Drain Current – Pulsed		100	
P_D	Maximum Power Dissipation	(Note 1)	42	W
		(Note 1a)	3.8	
		(Note 1b)	1.6	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +175	°C

Thermal Characteristics

Symbol	Parameter		Ratings	Units
$R_{θJC}$	Thermal Resistance, Junction-to-Case	(Note 1)	3.5	°C/W
$R_{θJA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	40	°C/W
		(Note 1b)	96	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDD5612	FDD5612	13''	16mm	2500 units

Electrical Characteristics

$T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Ratings (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 30$ V, $I_D = 5.4$ A			90	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				5.4	A
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ µA	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250$ µA, Referenced to 25°C		62		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 48$ V, $V_{GS} = 0$ V			1	µA
I_{GSSF}	Gate–Body Leakage, Forward	$V_{GS} = 20$ V, $V_{DS} = 0$ V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	$V_{GS} = -20$ V $V_{DS} = 0$ V			−100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250$ µA	1	2.4	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250$ µA, Referenced to 25°C		−6		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10$ V, $I_D = 5.4$ A $V_{GS} = 6$ V, $I_D = 5$ A $V_{GS} = 10$ V, $I_D = 5.4$ A, $T_J = 125°C$		36 42 64	55 64 103	mΩ
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 10$ V, $V_{DS} = 5$ V	20			A
g_{FS}	Forward Transconductance	$V_{DS} = 5$ V, $I_D = 5.4$ A		15		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 30$ V, $V_{GS} = 0$ V, f = 1.0 MHz		660		pF
C_{oss}	Output Capacitance			79		pF
C_{rss}	Reverse Transfer Capacitance			36		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 30$ V, $I_D = 1$ A, $V_{GS} = 10$ V, $R_{GEN} = 6$ Ω		8	16	ns
t_r	Turn–On Rise Time			4	8	ns
$t_{d(off)}$	Turn–Off Delay Time			24	38	ns
t_f	Turn–Off Fall Time			4	8	ns
Q_g	Total Gate Charge	$V_{DS} = 30$ V, $I_D = 5.4$ A, $V_{GS} = 10$ V		7.5	11	nC
Q_{gs}	Gate–Source Charge			2.5		nC
Q_{gd}	Gate–Drain Charge			3		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				2.7	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = 2.7$ A (Note 2)		0.8	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the drain tab.

   $R_{\theta JA}$ is the guaranteed design while RθJA is determined by the user's design. RθJA has been used to determine some of the maximum ratings.

a) $R_{\theta JA} = 40°C/W$ when mounted on a 1in^2 pad of 2oz copper.

b) $R_{\theta JA} = 96°C/W$ when mounted on a 0.076 in^2 pad of 2oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle ≤ 2.0%
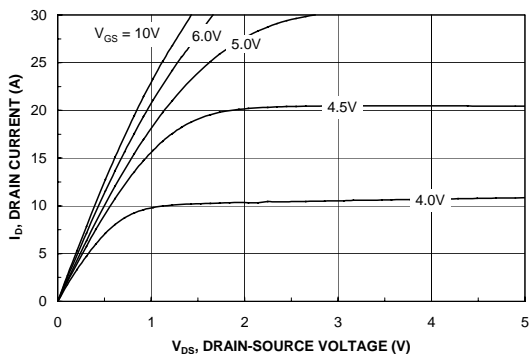
Typical Characteristics

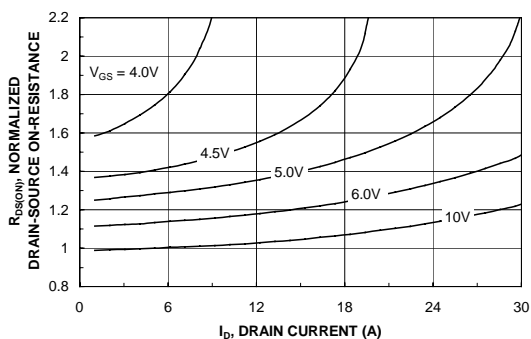**Figure 1. On-Region Characteristics.**

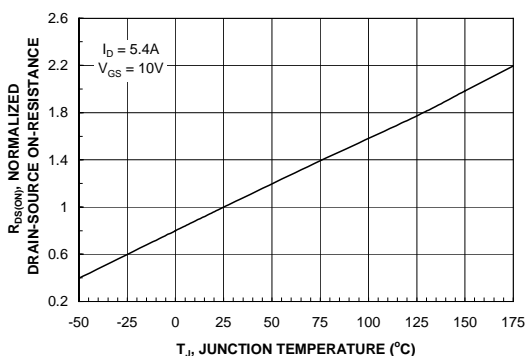**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

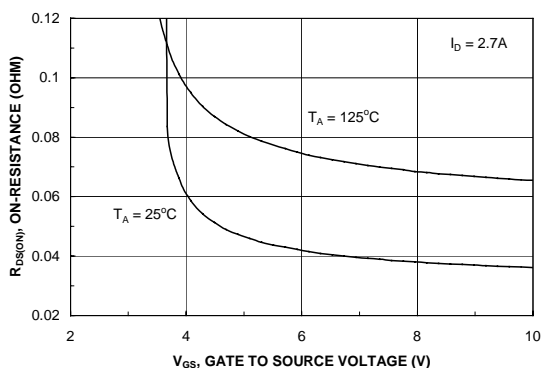**Figure 3. On-Resistance Variation with Temperature.**

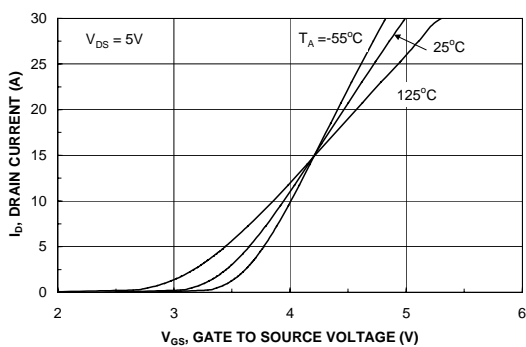**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**
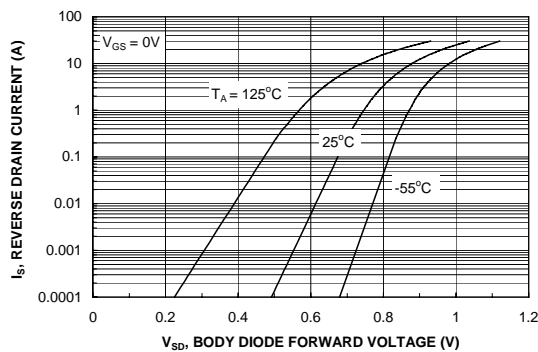

Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.
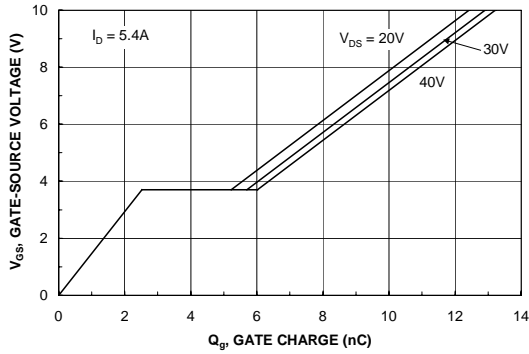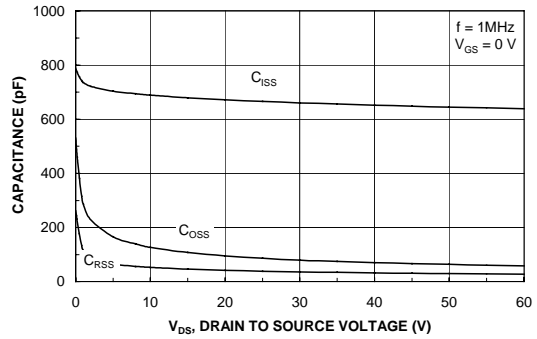
Typical Characteristics

Figure 7. Gate Charge Characteristics.

Figure 8. Capacitance Characteristics.
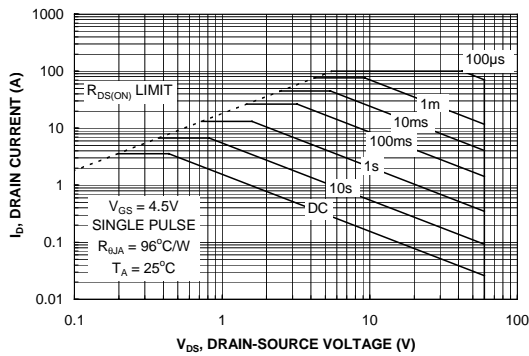
Figure 9. Maximum Safe Operating Area.
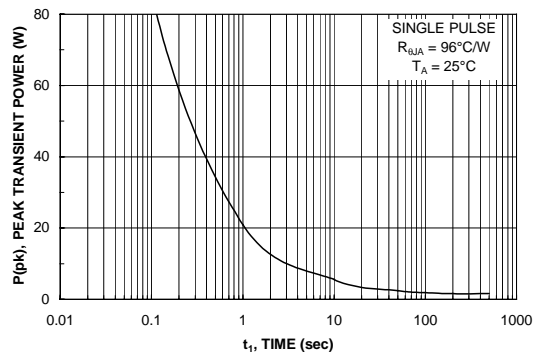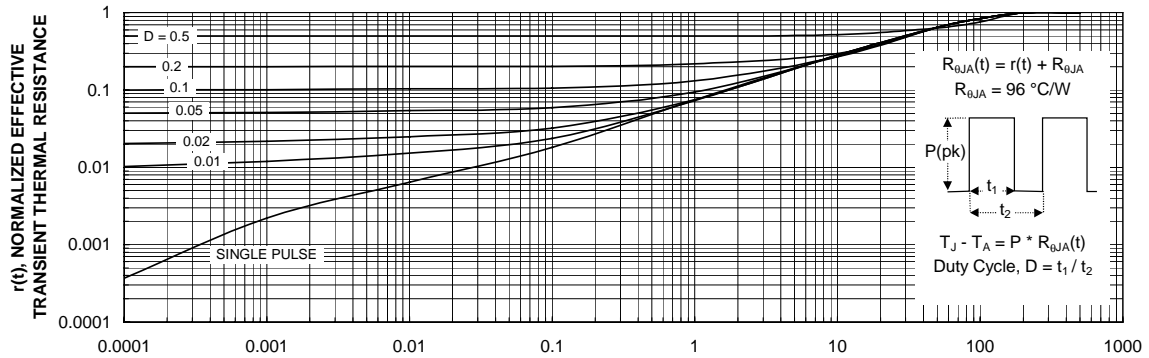

Figure 10. Single Pulse Maximum Power Dissipation.

$$R_{\theta JA}(t) = r(t) + R_{\theta JA}$$
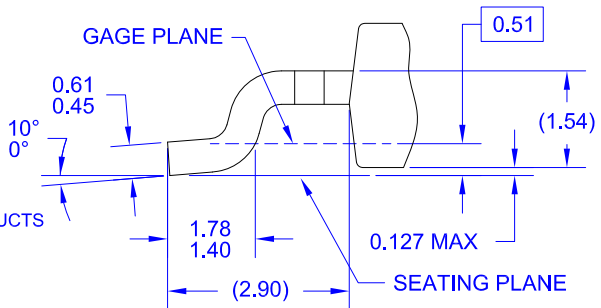$$R_{\theta JA} = 96\ °C/W$$

$$T_J - T_A = P * R_{\theta JA}(t)$$
Duty Cycle, $D = t_1 / t_2$

Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

6.73 / 6.35 ⟨A⟩

5.46 / 5.21

6.22 / 5.97

⟨C⟩

1.27 / 0.89

⟨E⟩ **1.02 MAX**

0.25 MAX

ISOLATED PLASTIC
BODY STUB

1   2   3

**DIODE
PRODUCTS VERSION**

(0.59)

1.14 / 0.76

0.89 / 0.64

2.29

| ⊕ | 0.25 Ⓜ | AⓂ | C |

4.57

1   2   3

**NON-DIODE
PRODUCTS VERSION**

5.55 MIN

4

6.40

6.50 MIN

1   3

2.85 MIN

1.25 MIN

2.28

4.56

**LAND PATTERN
RECOMMENDATION**

SEE
NOTE D

4.32 MIN   4

5.21 MIN

3   2 ⟨E⟩   1

**NON-DIODE
PRODUCTS VERSION**

3   2   1

**DIODE
PRODUCTS VERSION**

⟨B⟩

2.39 / 2.18

0.58 / 0.45

10.41 / 9.40

SEE DETAIL A

| ⌒ | 0.10 | B |

NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252,
ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER
ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED
CORNERS OR EDGE PROTRUSION.
⟨E⟩ TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSIVE OF BURS,
MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD
TO228P991X239-3N.
H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11

GAGE PLANE

0.51

0.61 / 0.45

10° / 0°

(1.54)

1.78 / 1.40

(2.90)

0.127 MAX

SEATING PLANE

DETAIL A
(ROTATED -90°)
SCALE: 12X

FAIRCHILD™

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