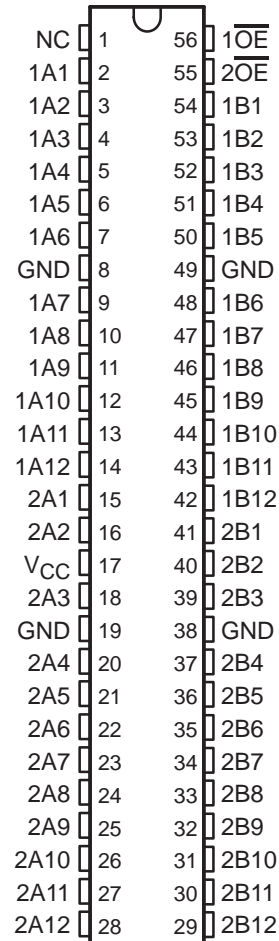- **Member of the Texas Instruments Widebus™ Family**

- **High-Bandwidth Data Path (Up To 500 MHz†)**

- **5-V Tolerant I/Os with Device Powered Up or Powered Down**

- **Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range (r_{on} = 5 Ω Typical)**

- **Rail-to-Rail Switching on Data I/O Ports**
  - **0-V to 5-V Switching With 3.3-V V_{CC}**
  - **0-V to 3.3-V Switching With 2.5-V V_{CC}**

- **Bidirectional Data Flow, With Near-Zero Propagation Delay**

- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 4 pF Typical)**

- **Fast Switching Frequency ($f_{\overline{OE}}$ = 20 MHz Max)**

- **Data and Control Inputs Provide Undershoot Clamp Diodes**

- **Low Power Consumption (I_{CC} = 1 mA Typical)**

- **V_{CC} Operating Range From 2.3 V to 3.6 V**

- **Data I/Os Support 0-V to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)**

- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**

- **I_{off} Supports Partial-Power-Down Mode Operation**

- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

- **Supports Both Digital and Analog Applications: PCI Interface, Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

† For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)

NC	1	56	1$\overline{OE}$
1A1	2	55	2$\overline{OE}$
1A2	3	54	1B1
1A3	4	53	1B2
1A4	5	52	1B3
1A5	6	51	1B4
1A6	7	50	1B5
GND	8	49	GND
1A7	9	48	1B6
1A8	10	47	1B7
1A9	11	46	1B8
1A10	12	45	1B9
1A11	13	44	1B10
1A12	14	43	1B11
2A1	15	42	1B12
2A2	16	41	2B1
V_{CC}	17	40	2B2
2A3	18	39	2B3
GND	19	38	GND
2A4	20	37	2B4
2A5	21	36	2B5
2A6	22	35	2B6
2A7	23	34	2B7
2A8	24	33	2B8
2A9	25	32	2B9
2A10	26	31	2B10
2A11	27	30	2B11
2A12	28	29	2B12

NC – No internal connection

Widebus is a trademark of Texas Instruments.

TEXAS INSTRUMENTS

SN74CB3Q16211
24-BIT SWITCH
2.5-V/3.3-V LOW-VOLTAGE FET BUS SWITCH

SCDS167 – MAY 2004

description/ordering information

The SN74CB3Q16211 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q16211 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q16211 is organized as two 12-bit bus switches with separate output-enable ($1\overline{OE}$, $2\overline{OE}$) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When $\overline{OE}$ is low, the associated 12-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 12-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP – DL	Tube	SN74CB3Q16211DL	CB3Q16211
		Tape and reel	SN74CB3Q16211DLR	
	TSSOP – DGG	Tape and reel	SN74CB3Q16211DGGR	CB3Q16211
	TVSOP – DGV	Tape and reel	SN74CB3Q16211DGVR	BW211
	VFBGA – GQL	Tape and reel	SN74CB3Q16211GQLR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
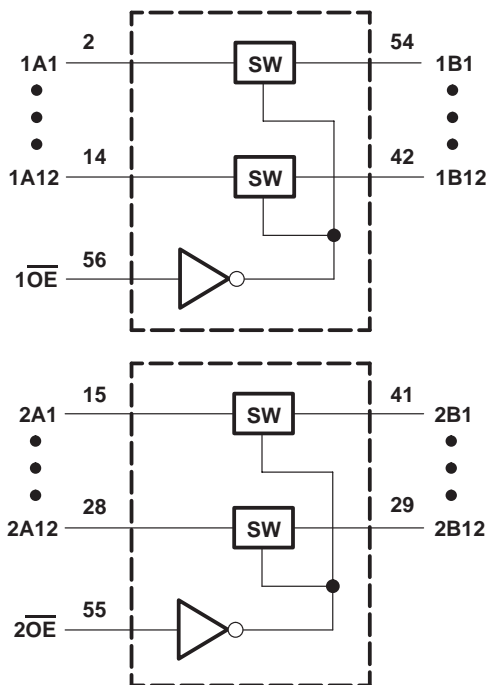
GQL PACKAGE
(TOP VIEW)
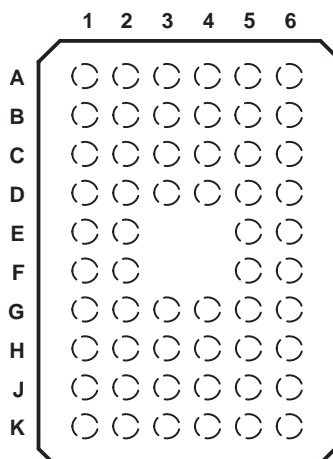
terminal assignments

	1	2	3	4	5	6
A	1A2	1A1	NC	$1\overline{OE}$	$2\overline{OE}$	1B1
B	1A5	1A4	1A3	1B2	1B3	1B4
C	1A7	GND	1A6	1B5	GND	1B6
D	1A10	1A8	1A9	1B8	1B7	1B9
E	1A12	1A11			1B10	1B11
F	2A1	2A2			2B1	1B12
G	V_{CC}	GND	2A3	2B3	GND	2B2
H	2A4	2A5	2A6	2B6	2B5	2B4
J	2A7	2A8	2A9	2B9	2B8	2B7
K	2A10	2A11	2A12	2B12	2B11	2B10

NC – No internal connection

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

FUNCTION TABLE
(each 12-bit bus switch)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)

Pin numbers shown are for the DGG, DGV, and DL packages.

simplified schematic, each FET switch (SW)
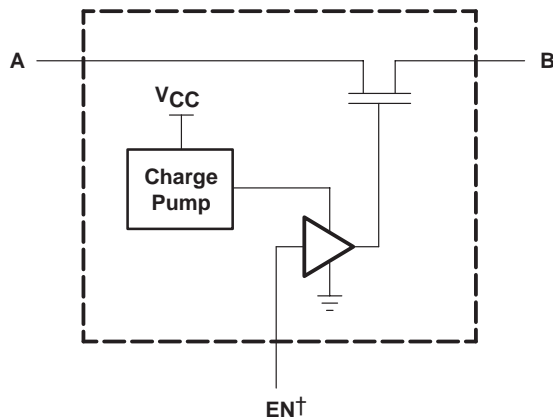
† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) .... –0.5 V to 4.6 V

Control input voltage range, V_{IN} (see Notes 1 and 2) .... –0.5 V to 7 V

Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) .... –0.5 V to 7 V

Control input clamp current, I_{IK} ($V_{IN} < 0$) .... –50 mA

I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$) .... –50 mA

ON-state switch current, $I_{I/O}$ (see Note 4) .... ±64 mA

Continuous current through V_{CC} or GND terminals .... ±100 mA

Package thermal impedance, θ_{JA} (see Note 5): DGG package .... 64°C/W

DGV package .... 48°C/W

DL package .... 56°C/W

GQL package .... 42°C/W

Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		–40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = −18 mA				−1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V				±1	µA
I_{OZ}[‡]		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±1	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			1	µA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND		1	3	mA
ΔI_{CC}[§]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			30	µA
I_{CCD}[¶]	Per control input	V_{CC} = 3.6 V,	A and B ports open, Control input switching at 50% duty cycle			0.15	0.25	mA/ MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0			3.5	5	pF
$C_{io(OFF)}$		V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		4	5	pF
$C_{io(ON)}$		V_{CC} = 3.3 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		10	12.5	pF
r_{on}[#]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0,	I_O = 30 mA		5	8	Ω
			V_I = 1.7 V,	I_O = −15 mA		5	9	
		V_{CC} = 3 V	V_I = 0,	I_O = 30 mA		5	6.5	
			V_I = 2.4 V,	I_O = −15 mA		5	8	

NOTE 7: V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.
[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
[¶] This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).
[#] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
$f_{\overline{OE}}$[‖]	$\overline{OE}$	A or B		10		20	MHz
t_{pd}[✶]	A or B	B or A		0.15		0.25	ns
t_{en}	$\overline{OE}$	A or B	1.5	8	1.5	8	ns
t_{dis}	$\overline{OE}$	A or B	1	7.5	1	7.5	ns

[‖] Maximum switching frequency for control input (V_O > V_{CC}, V_I = 5 V, R_L ≥ 1 MΩ, C_L = 0)
[✶] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
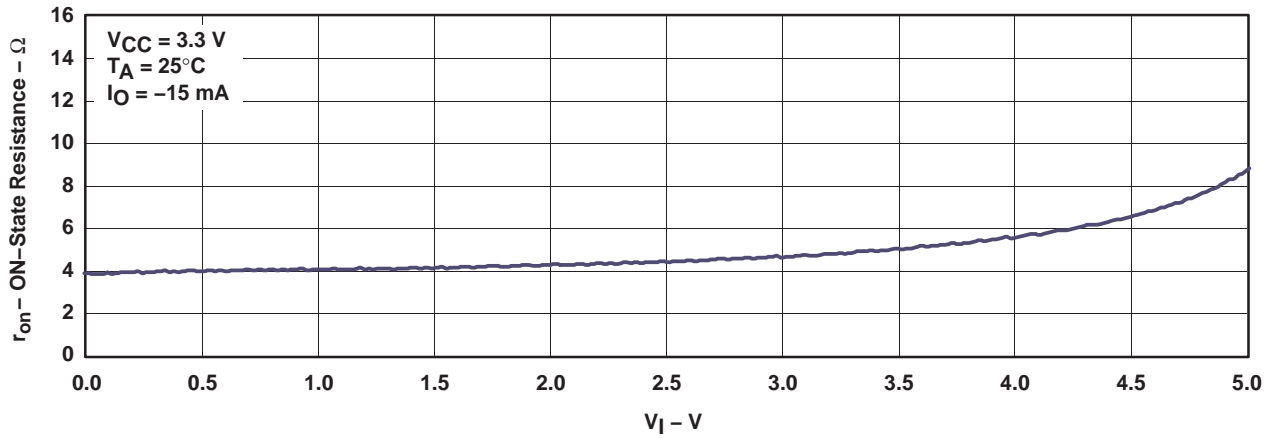
Figure 1. Typical r$_{on}$ vs V$_I$
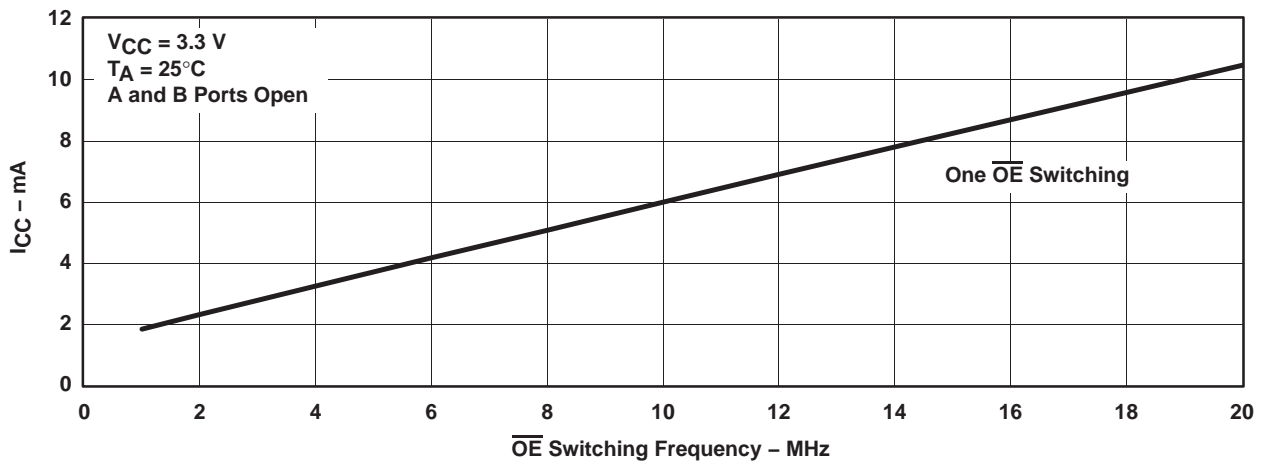
Figure 2. Typical I$_{CC}$ vs $\overline{\text{OE}}$ Switching Frequency

PARAMETER MEASUREMENT INFORMATION
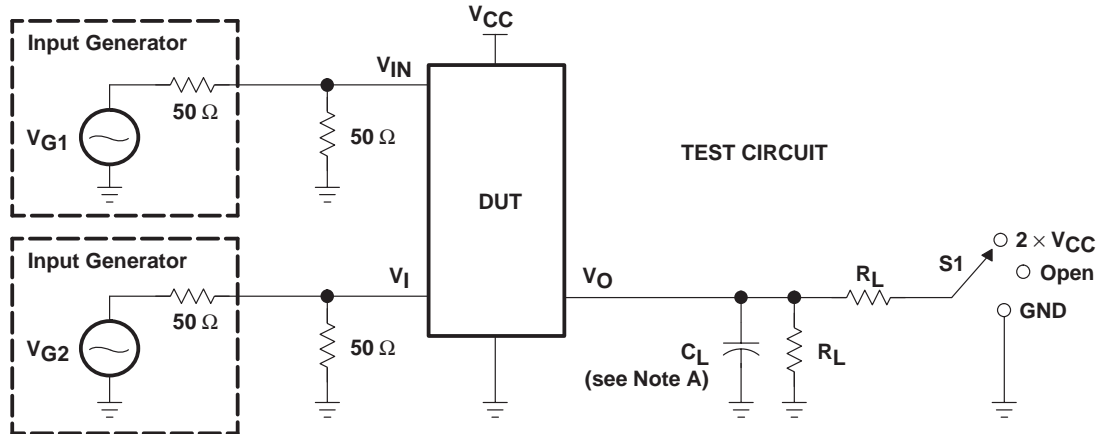
TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V	Open	500 Ω	V_{CC} or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	V_{CC} or GND	50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V	2 × V_{CC}	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V_{CC}	500 Ω	GND	50 pF	0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V	GND	500 Ω	V_{CC}	30 pF	0.15 V
	3.3 V ± 0.3 V	GND	500 Ω	V_{CC}	50 pF	0.3 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
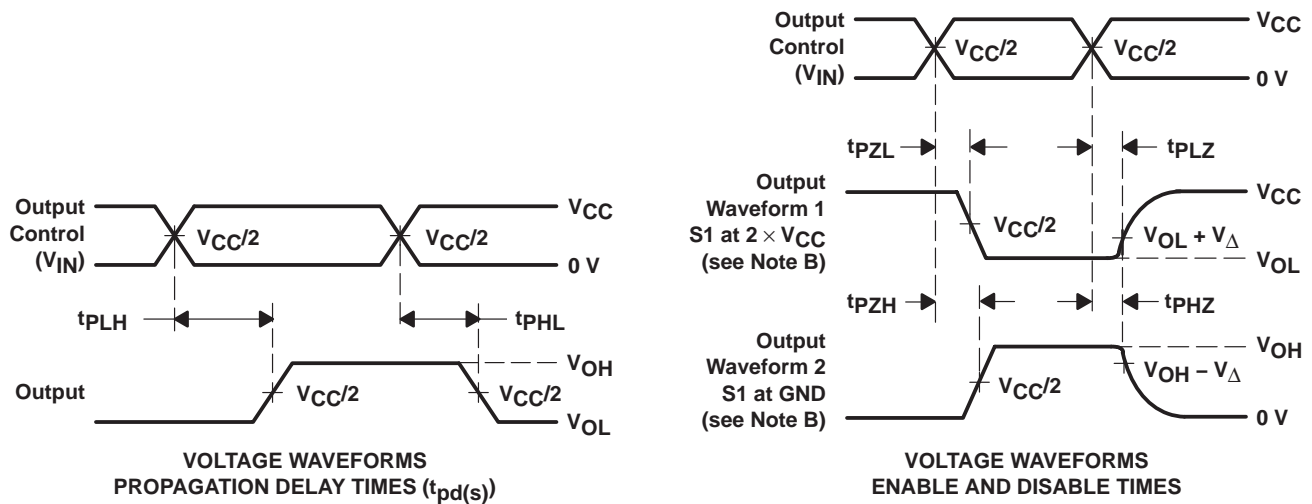
NOTES: A. C_L includes probe and jig capacitance.
  B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
  D. The outputs are measured one at a time, with one transition per measurement.
  E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
  F. t_{PZL} and t_{PZH} are the same as t_{en}.
  G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance
   of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

TEXAS
INSTRUMENTS

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CB3Q16211DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3Q16211	Samples
SN74CB3Q16211DGVR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BW211	Samples
SN74CB3Q16211DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3Q16211	Samples
SN74CB3Q16211DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3Q16211	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3Q16211DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74CB3Q16211DGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1
SN74CB3Q16211DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3Q16211DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74CB3Q16211DGVR	TVSOP	DGV	56	2000	367.0	367.0	45.0
SN74CB3Q16211DLR	SSOP	DL	56	1000	367.0	367.0	55.0

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

0,40

$\dfrac{0,23}{0,13}$ $\oplus$ 0,07 (M)

24   13

$\dfrac{4,50}{4,30}$ $\dfrac{6,60}{6,20}$

0,16 NOM

Gage Plane

0°–8°

0,25

1   12

A

$\dfrac{0,75}{0,50}$

1,20 MAX

$\dfrac{0,15}{0,05}$

Seating Plane

$\triangle$ 0,08

DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
           B. This drawing is subject to change without notice.
           C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
           D. Falls within JEDEC: 24/48 Pins – MO-153
                                 14/16/20/56 Pins – MO-194

DL (R−PDSO−G56)   PLASTIC SMALL−OUTLINE PACKAGE

0.025 (0,635)

0.0135 (0,343)
0.008 (0,203)

⊕ 0.005 (0,13) Ⓜ

56   29

0.420 (10,67)
0.395 (10,03)

0.010 (0,25)
0.005 (0,13)

0.299 (7,59)
0.291 (7,39)

Gage Plane

0.010 (0,25)

1   28

0°−8°

0.730 (18,54)
0.720 (18,29)

0.040 (1,02)
0.020 (0,51)

0.110 (2,79) MAX

0.008 (0,20) MIN

Seating Plane

0.004 (0,10)

4040048−4/F 05/13

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MO−118

PowerPAD is a trademark of Texas Instruments.

8.3
7.9 TYP

A

PIN 1 ID
AREA

1

54X 0.5

56

14.1
13.9
NOTE 3

2X
13.5

28

29

B

6.2
6.0

56X 0.27
0.17

⊕ 0.08 Ⓜ C AⓈ BⓈ

C

SEATING PLANE

⌒ 0.1 C

1.2 MAX

(0.15) TYP

SEE DETAIL A

0.25

GAGE PLANE

0° - 8°

0.75
0.50

0.15
0.05

DETAIL A
TYPICAL

4222167/A   07/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
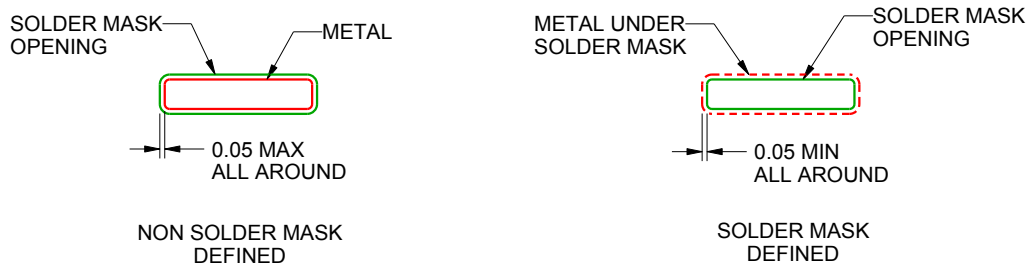4. Reference JEDEC registration MO-153.

56X (1.5)

1

56X (0.3)

54X (0.5)

(R0.05)
TYP

SYMM

56

28

29

SYMM

(7.5)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

0.05 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222167/A   07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

56X (1.5)
1
56X (0.3)
54X (0.5)
(R0.05) TYP
SYMM
56
SYMM
28
29
(7.5)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A   07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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