

DUAL SCHOTTKY DIODE BRIDGE

FEATURES

- **Monolithic Eight-Diode Array**
- **Exceptional Efficiency**
- **Low Forward Voltage**
- **Fast Recovery Time**
- **High Peak Current**
- **Small Size**

DESCRIPTION

This eight-diode array is designed for high-current, low duty-cycle applications typical of flyback voltage clamping for inductive loads. The dual bridge connection makes this device particularly applicable to bipolar driven stepper motors.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

This single monolithic chip is fabricated in both hermetic CERDIP and copper-leaded plastic packages. The UC1610 in ceramic is designed for -55°C to 125°C environments but with reduced peak current capability. The UC2610 in plastic and ceramic is designed for -25°C to 125°C environments also with reduced peak current capability; while the UC3610 in plastic has higher current rating over a 0°C to 70°C temperature range.

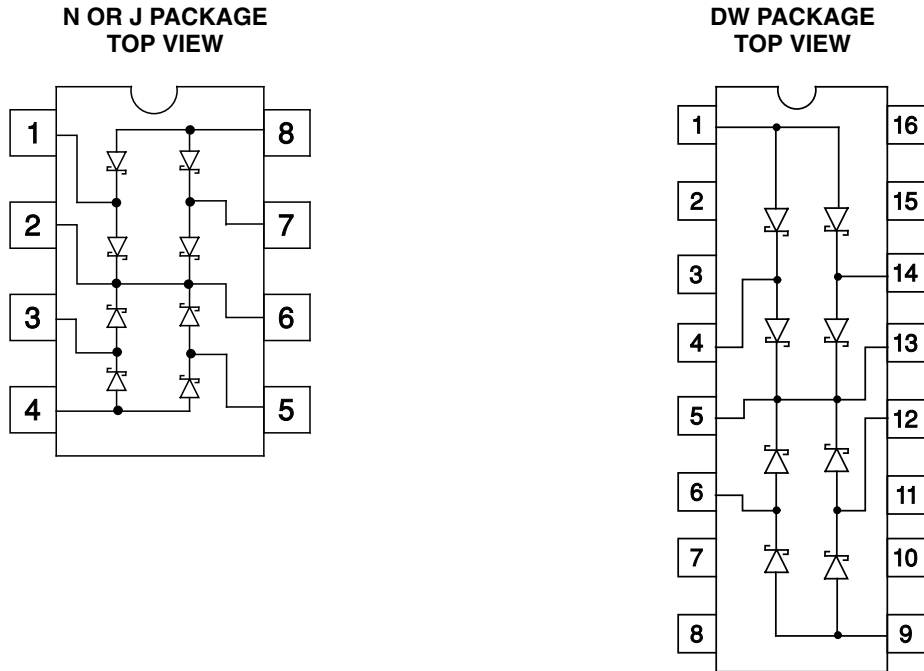
AVAILABLE OPTIONS

$T_A = T_J$	Packaged Devices		
	SOIC Wide (DW)	DIL (J)	DIL (N)
-55°C to 125°C	UC1610DW	UC1610J	UC1610N
-25°C to 125°C	UC2610DW	UC2610J	UC2610N
0°C to 70°C	UC3610DW	UC3610J	UC3610N

THERMAL INFORMATION

PACKAGE	θ_{ja}	θ_{jc}
SOIC (DW) 16 pin	50 – 100 ⁽¹⁾	27
DIP (J) 8 pin	125 – 160	20 ⁽²⁾
DIP (N) 8 pin	103 ⁽¹⁾	50

- NOTES:
1. Specified θ_{ja} (junction-to-ambient) is for devices mounted to 5-in² FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5-in² aluminum PC board. Test PWB was 0.062 in thick and typically used 0.635-mm trace widths for power packages and 1.3-mm trace widths for non-power packages with a 100-mil x 100-mil probe land area at the end of each trace.
 2. θ_{jc} data values stated were derived from MIL-STD-1835B. MIL-STD-1835B states that the baseline values shown are worst case (mean + 2s) for a 60-mil x 60-mil microcircuit device silicon die and applicable for devices with die sizes up to 14400 square mils. For device die sizes greater than 14400 square mils use the following values; dual-in-line, $11^{\circ}\text{C}/\text{W}$; flat pack, $10^{\circ}\text{C}/\text{W}$; pin grid array, $10^{\circ}\text{C}/\text{W}$.



absolute maximum ratings over operating free-air temperature (unless otherwise noted)^{†‡}

Peak inverse voltage (per diode)	50 V
Peak forward current	
UC1611	1 A
UC2610	1 A
UC3611	3 A
Power dissipation at $T_A = 70^\circ\text{C}$	1 W
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature (soldering, 10 seconds)	300°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] Consult packaging section of databook for thermal limitations and considerations of package.

electrical characteristics, all specifications apply to each individual diode, $T_J = 25^\circ\text{C}$, $T_A = T_J$, (except as noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward voltage drop	$I_F = 100 \text{ mA}$	0.35	0.5	0.7	V
	$I_F = 1 \text{ A}$	0.8	1.0	1.3	V
Leakage current	$V_R = 40 \text{ V}$		0.01	0.1	mA
	$V_R = 40 \text{ V}$, $T_J = 100^\circ\text{C}$		0.1	1.0	mA
Reverse recovery	0.5 A forward to 0.5 A reverse		15		ns
Forward recovery	1 A forward to 1.1 V recovery		30		ns
Junction capacitance	$V_R = 5 \text{ V}$		70		pF

NOTE: At forward currents of greater than 1.0 A, a parasitic current of approximately 10 mA may be collected by adjacent diodes.

APPLICATION INFORMATION

REVERSE CURRENT
vs
VOLTAGE

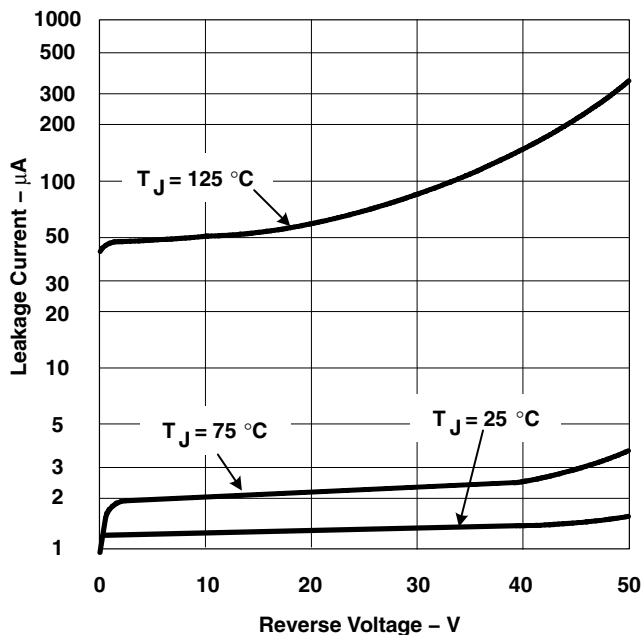


Figure 1

FORWARD CURRENT
vs
VOLTAGE

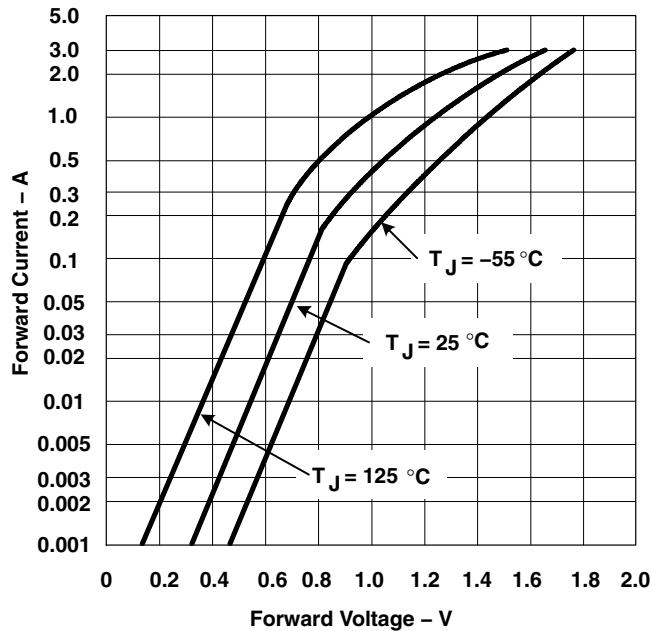


Figure 2

REVERSE RECOVERY CHARACTERISTICS

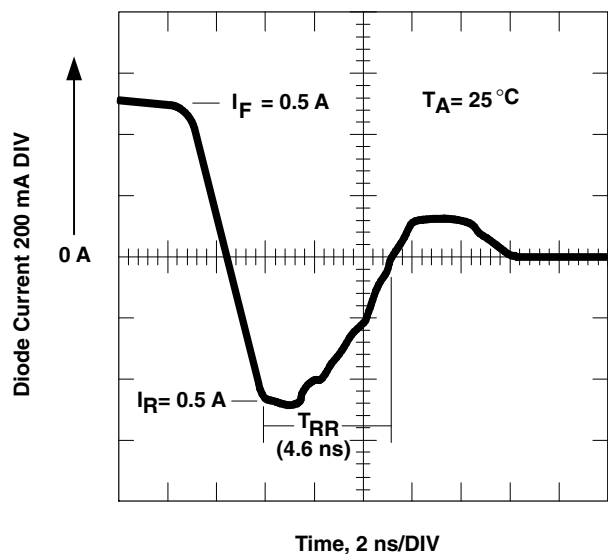


Figure 3

FORWARD RECOVERY CHARACTERISTICS

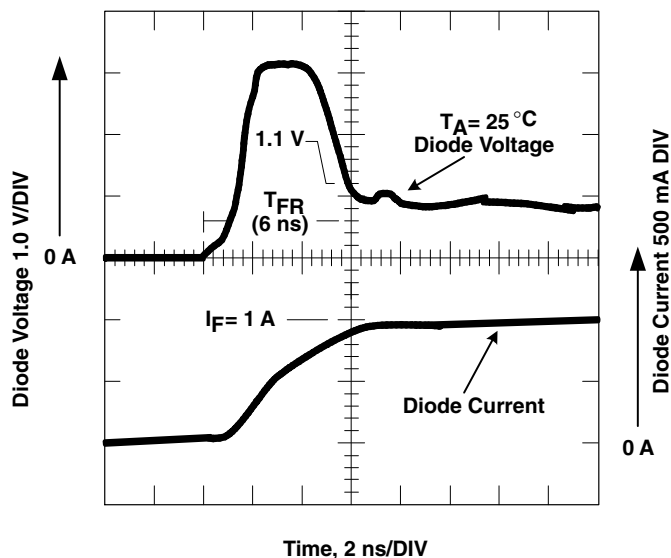


Figure 4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2610N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	UC2610N	Samples
UC3610DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3610DW	Samples
UC3610DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3610DW	Samples
UC3610N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	UC3610N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

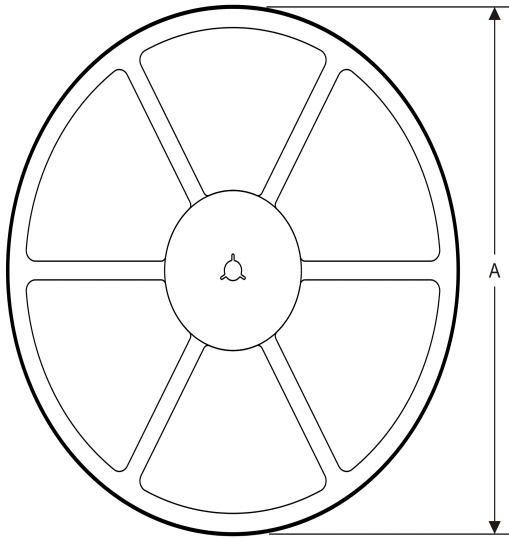
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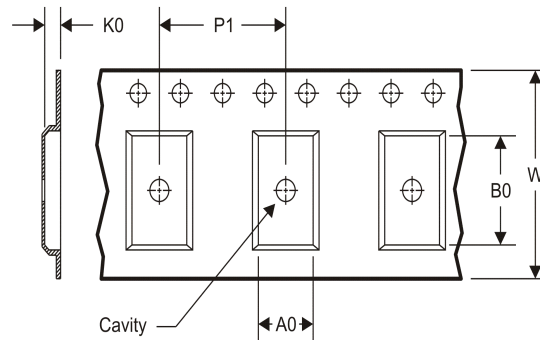
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC3610DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC3610DWTR	SOIC	DW	16	2000	367.0	367.0	38.0

GENERIC PACKAGE VIEW

DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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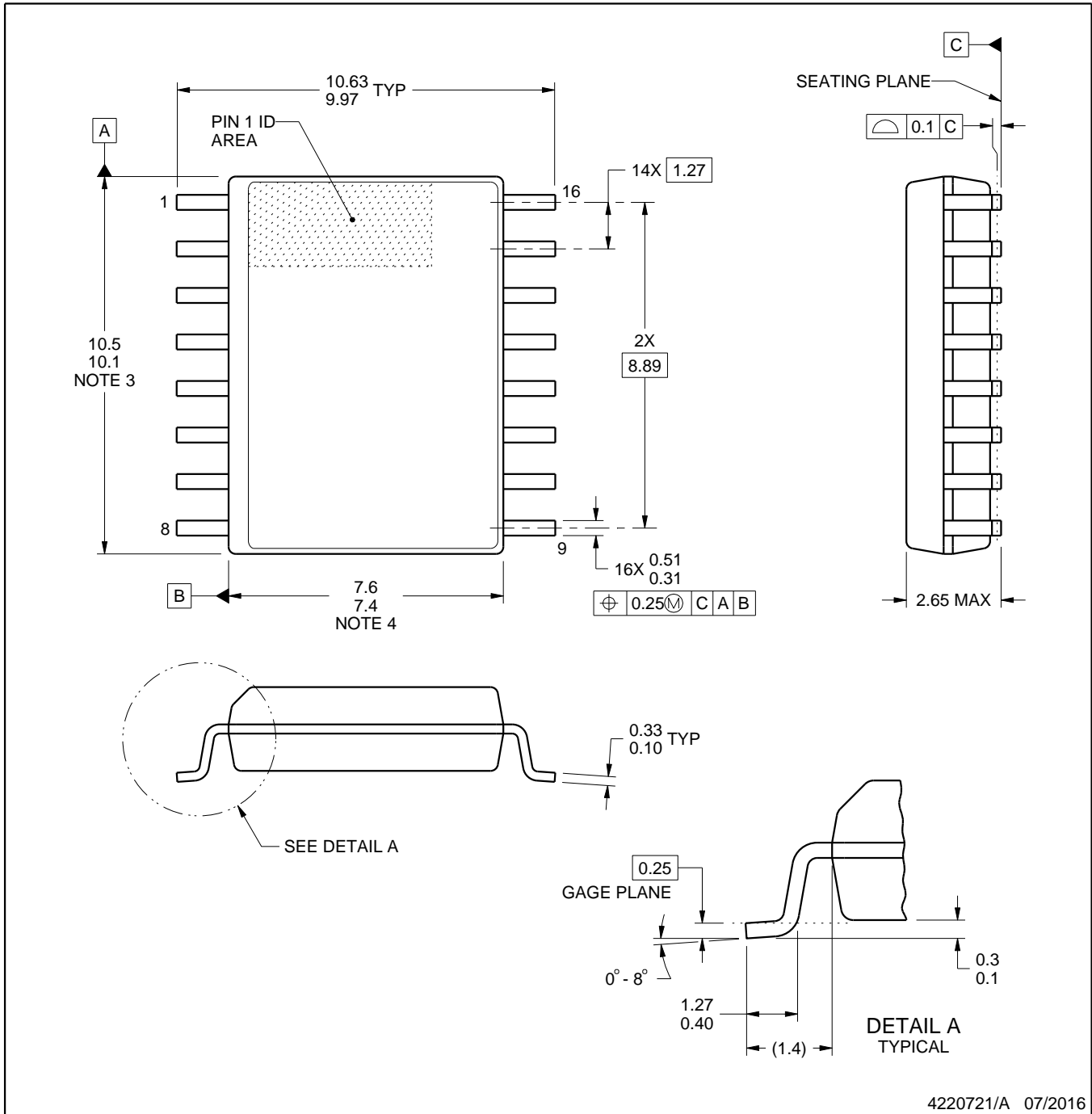


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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