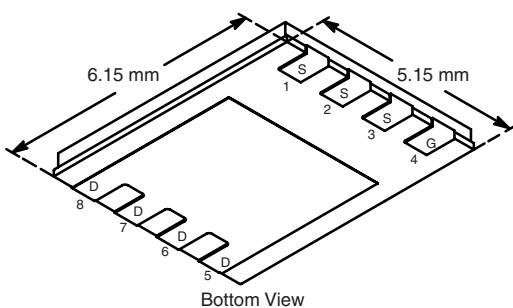


N-Channel 30-V (D-S) MOSFET with Schottky Diode

PRODUCT SUMMARY

| V_{DS} (V) | $R_{DS(on)}$ (Ω) | I_D (A) ^a | Q_g (Typ.) |
|--------------|---------------------------|------------------------|--------------|
| 30 | 0.0087 at $V_{GS} = 10$ V | 20 | 21 |
| | 0.010 at $V_{GS} = 4.5$ V | 20 | |

PowerPAK SO-8



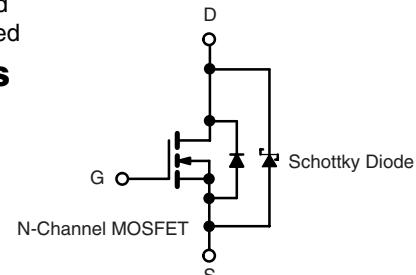
Ordering Information: Si7160DP-T1-E3 (Lead (Pb)-free)
Si7160DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- Ultra-Low On-Resistance Using High Density TrenchFET® Gen II Power MOSFET Technology
- Q_g Optimized
- New Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile
- 100 % R_g Tested
- 100 % UIS Tested

APPLICATIONS

- Notebook
- Logic DC/DC



ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

| Parameter | Symbol | Limit | Unit |
|--|----------------|----------------------|------|
| Drain-Source Voltage | V_{DS} | 30 | V |
| Gate-Source Voltage | V_{GS} | ± 16 | |
| Continuous Drain Current ($T_J = 150$ °C) | I_D | 20 ^a | |
| | | 20 ^a | |
| | | 17.8 ^{b, c} | |
| | | 14.2 ^{b, c} | |
| Pulsed Drain Current | I_{DM} | 60 | A |
| Continuous Source-Drain Diode Current | I_S | 20 ^a | |
| | | 4.5 ^{b, c} | |
| Avalanche Current | I_{AS} | 20 | |
| Single Pulse Avalanche Energy | E_{AS} | 20 | mJ |
| Maximum Power Dissipation | P_D | 27.7 | |
| | | 17.7 | |
| | | 5 ^{b, c} | |
| | | 3.2 ^{b, c} | |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | - 55 to 150 | °C |
| Soldering Recommendations (Peak Temperature) ^{d, e} | | 260 | |

THERMAL RESISTANCE RATINGS

| Parameter | Symbol | Typical | Maximum | Unit |
|---|------------|---------|---------|------|
| Maximum Junction-to-Ambient ^{b, f} | R_{thJA} | 20 | 25 | °C/W |
| Maximum Junction-to-Case (Drain) | R_{thJC} | 3.4 | 4.5 | |

Notes:

- Package Limited.
- Surface Mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- See Solder Profile (www.vishay.com/doc?73461). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 70 °C/W.



RoHS
COMPLIANT
HALOGEN
FREE
Available

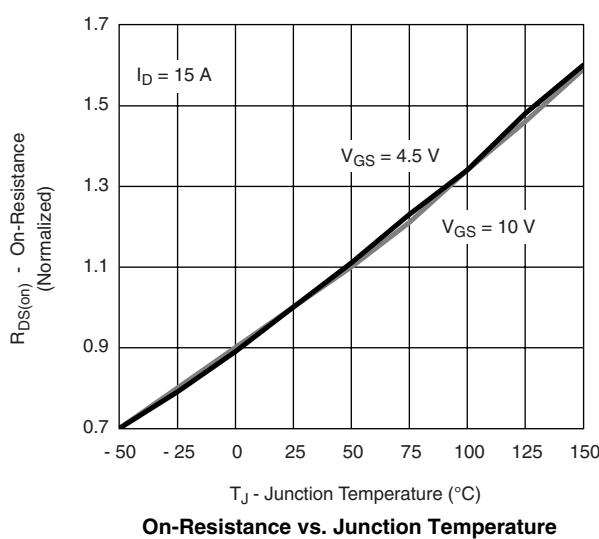
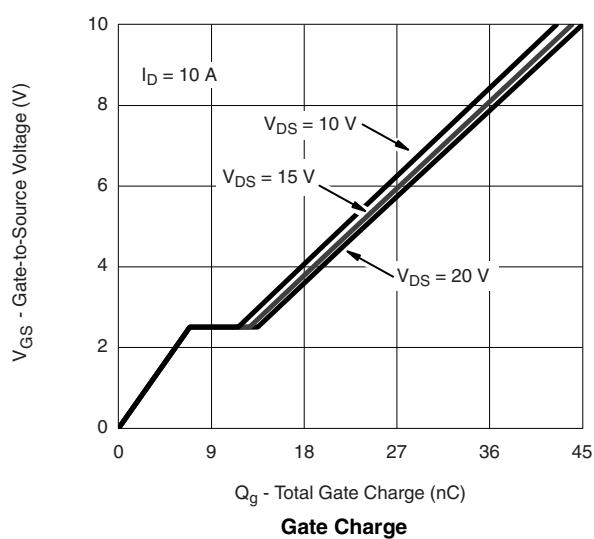
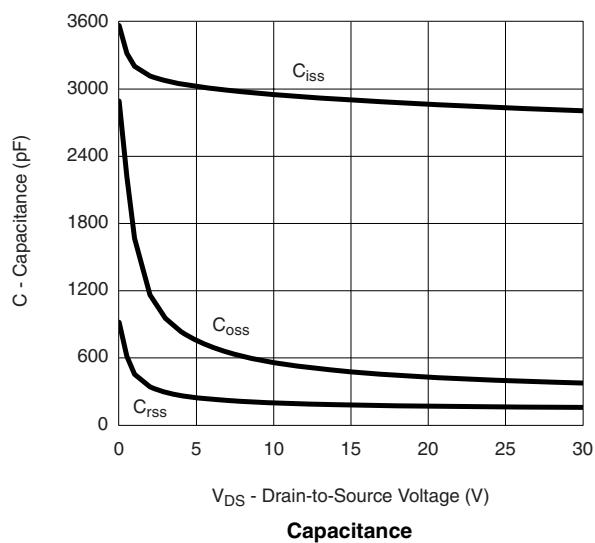
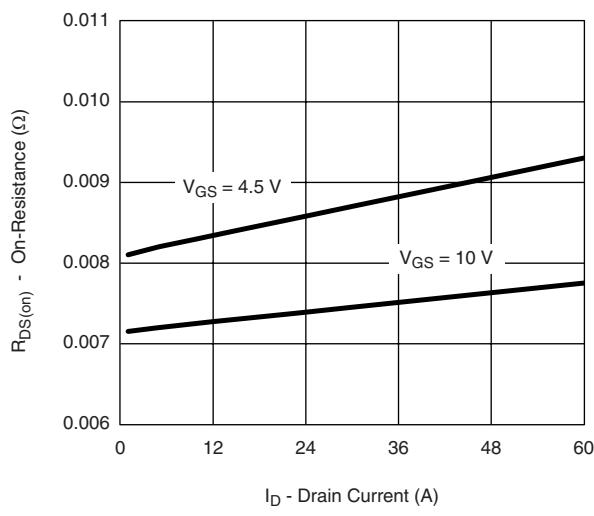
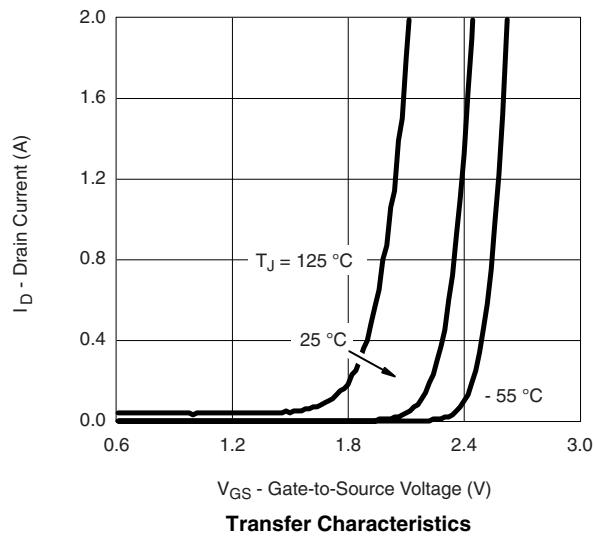
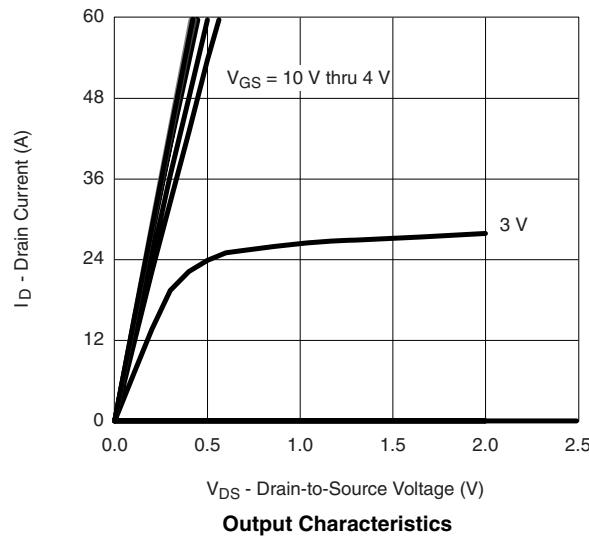
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

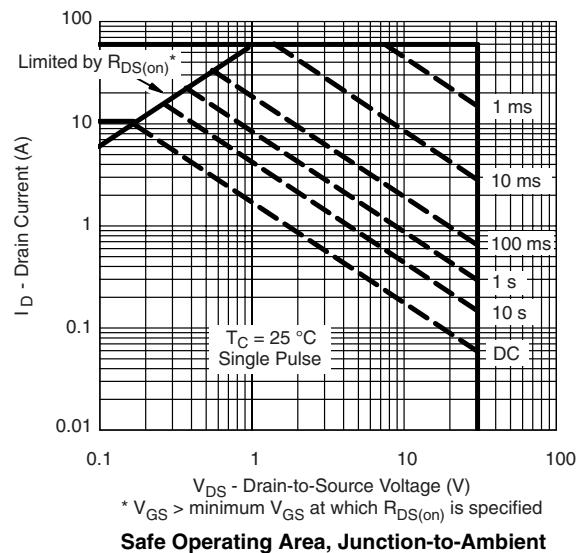
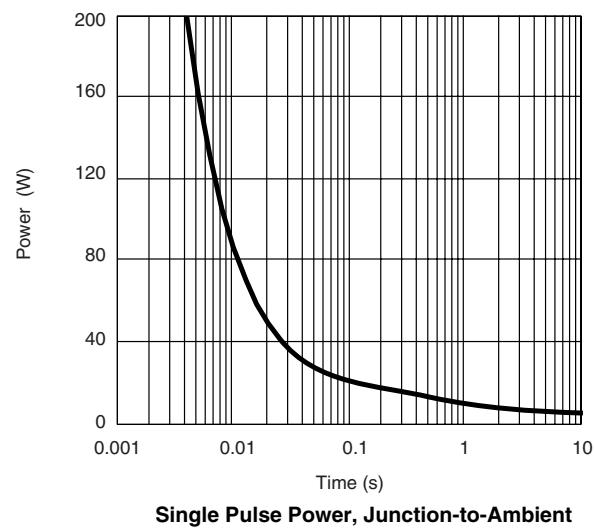
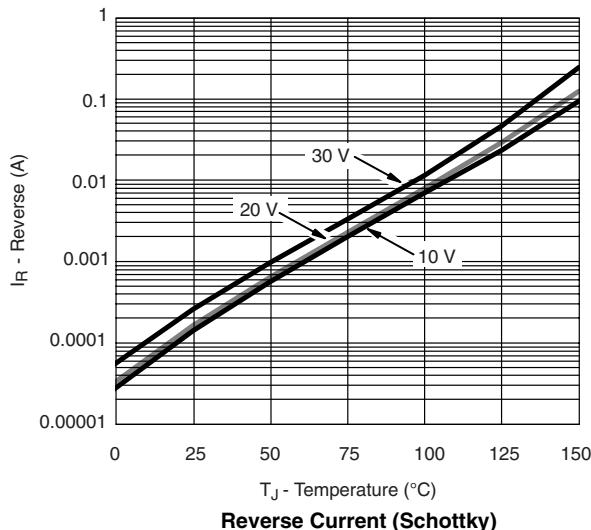
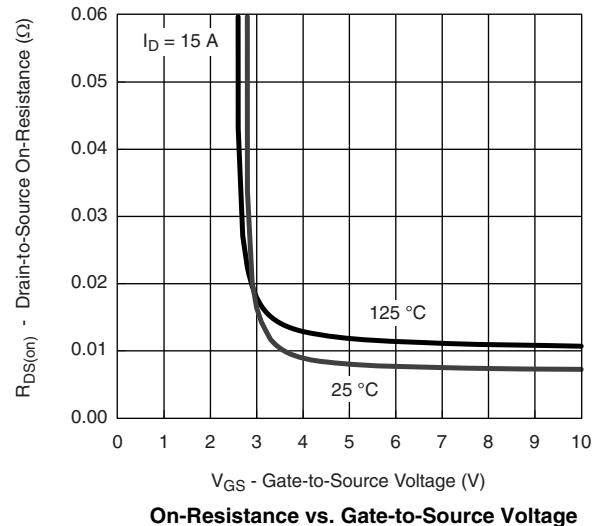
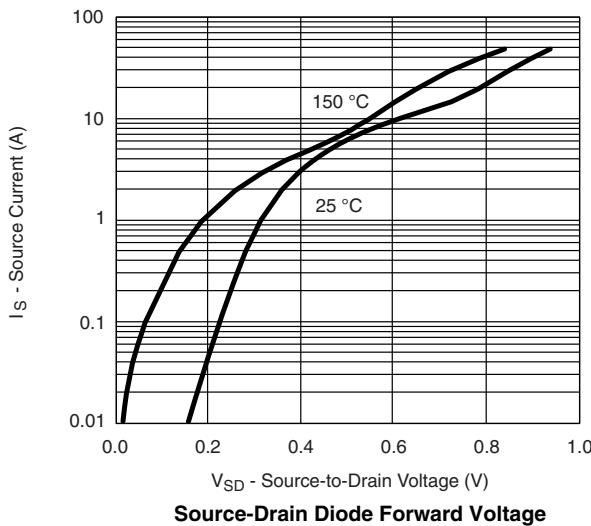
| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|--|---------------------|---|------|--------|-----------|----------|
| Static | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$ | 30 | | | V |
| Gate-Source Threshold Voltage | $V_{GS(\text{th})}$ | $V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$ | 1.0 | | 2.5 | V |
| Gate-Source Leakage | I_{GSS} | $V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 16 \text{ V}$ | | | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 30 \text{ V}$, $V_{GS} = 0 \text{ V}$ | | 0.26 | 1 | mA |
| | | $V_{DS} = 30 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 100^\circ\text{C}$ | | 12 | 100 | |
| On-State Drain Current ^a | $I_{D(\text{on})}$ | $V_{DS} \geq 5 \text{ V}$, $V_{GS} = 10 \text{ V}$ | 30 | | | A |
| Drain-Source On-State Resistance ^a | $R_{DS(\text{on})}$ | $V_{GS} = 10 \text{ V}$, $I_D = 15 \text{ A}$ | | 0.0072 | 0.0087 | Ω |
| | | $V_{GS} = 4.5 \text{ V}$, $I_D = 10 \text{ A}$ | | 0.0083 | 0.010 | |
| Forward Transconductance ^a | g_{fs} | $V_{DS} = 15 \text{ V}$, $I_D = 15 \text{ A}$ | | 60 | | S |
| Dynamic^b | | | | | | |
| Input Capacitance | C_{iss} | $V_{DS} = 15 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$ | | 2970 | | pF |
| Output Capacitance | C_{oss} | | | 475 | | |
| Reverse Transfer Capacitance | C_{rss} | | | 180 | | |
| Total Gate Charge | Q_g | $V_{DS} = 15 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 10 \text{ A}$ | | 44 | 66 | nC |
| | | | | 21 | 32 | |
| Gate-Source Charge | Q_{gs} | $V_{DS} = 15 \text{ V}$, $V_{GS} = 4.5 \text{ V}$, $I_D = 10 \text{ A}$ | | 6.9 | | |
| Gate-Drain Charge | Q_{gd} | | | 5.8 | | |
| Gate Resistance | R_g | $f = 1 \text{ MHz}$ | | 1.0 | 1.5 | Ω |
| Turn-On Delay Time | $t_{d(\text{on})}$ | | 29 | 45 | ns | |
| Rise Time | t_r | $V_{DD} = 15 \text{ V}$, $R_L = 1.5 \Omega$ $I_D \approx 10 \text{ A}$, $V_{GEN} = 4.5 \text{ V}$, $R_g = 1 \Omega$ | | 115 | | 175 |
| Turn-Off Delay Time | $t_{d(\text{off})}$ | | | 43 | | 65 |
| Fall Time | t_f | | | 21 | | 35 |
| Turn-On Delay Time | $t_{d(\text{on})}$ | | | 15 | | 25 |
| Rise Time | t_r | $V_{DD} = 15 \text{ V}$, $R_L = 1.5 \Omega$ $I_D \approx 10 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_g = 1 \Omega$ | | 12 | | 20 |
| Turn-Off Delay Time | $t_{d(\text{off})}$ | | | 33 | | 50 |
| Fall Time | t_f | | | 8 | | 15 |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous Source-Drain Diode Current | I_S | $T_C = 25^\circ\text{C}$ | | | 20 | A |
| Pulse Diode Forward Current ^a | I_{SM} | | | | 60 | |
| Body Diode Voltage | V_{SD} | $I_S = 2 \text{ A}$ | | 0.36 | 0.42 | V |
| Body Diode Reverse Recovery Time | t_{rr} | $I_F = 4 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$ | | 29 | 45 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | | 21 | 35 | nC |
| Reverse Recovery Fall Time | t_a | | | 15 | | ns |
| Reverse Recovery Rise Time | t_b | | | 14 | | |

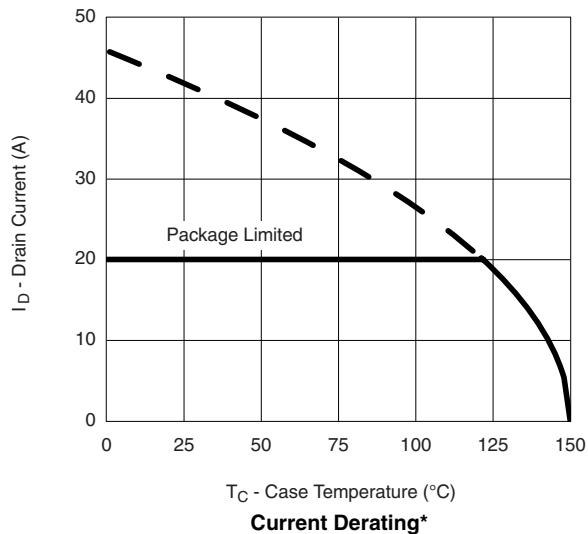
Notes:

a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

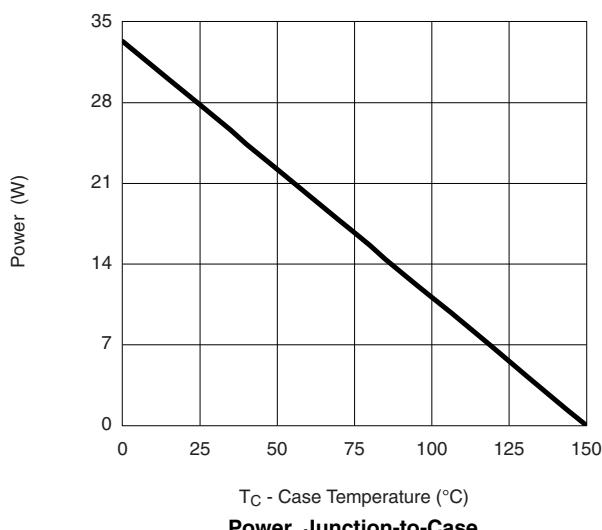
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


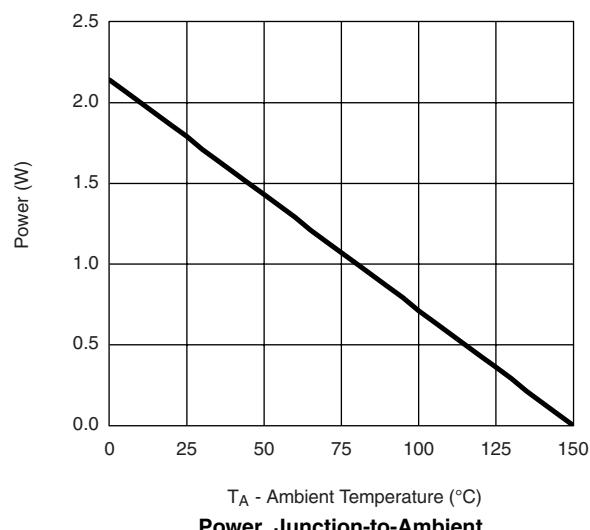
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

 T_C - Case Temperature (°C)

Current Derating*


 T_C - Case Temperature (°C)

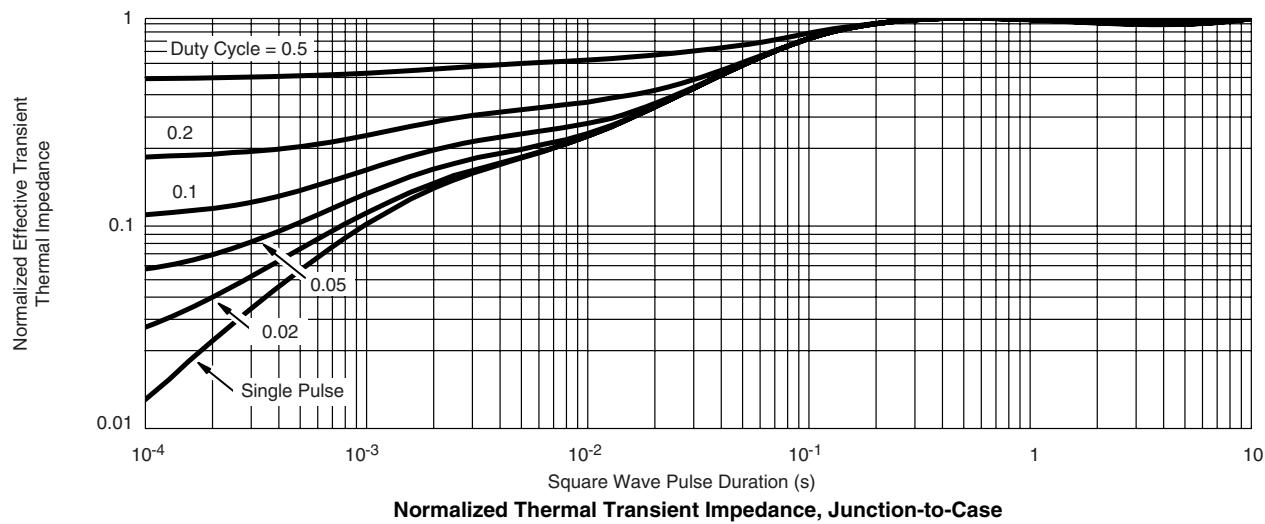
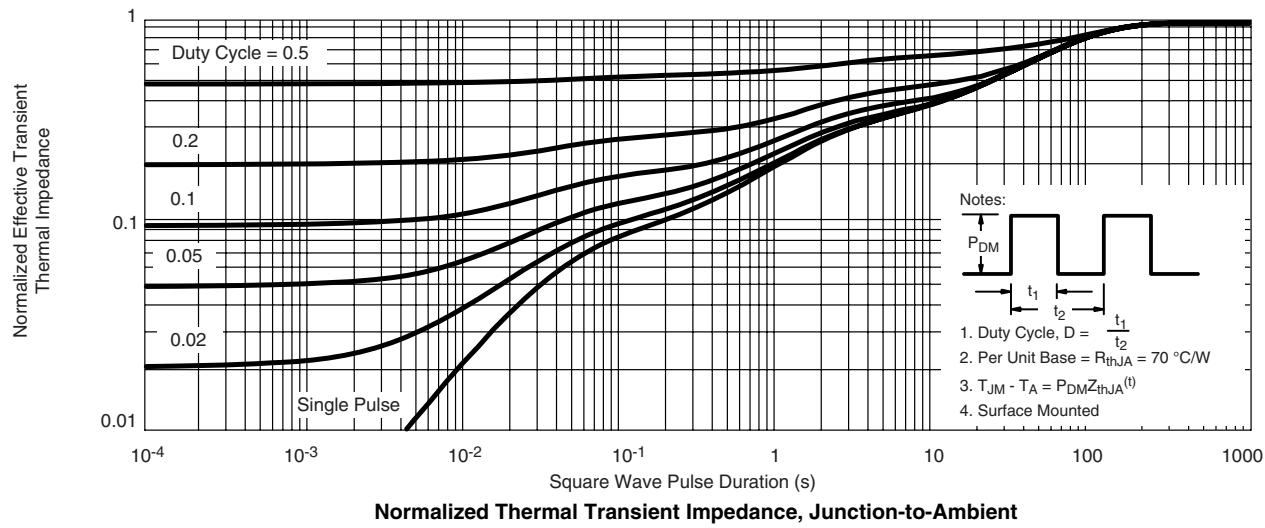
Power, Junction-to-Case


 T_A - Ambient Temperature (°C)

Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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