

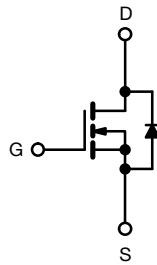
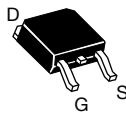
## D Series Power MOSFET



RoHS  
COMPLIANT  
HALOGEN  
**FREE**  
Available

PRODUCT SUMMARY		
$V_{DS}$ (V) at $T_J$ max.	550	
$R_{DS(on)}$ max. ( $\Omega$ ) at 25 °C	$V_{GS} = 10$ V	1.5
$Q_g$ max. (nC)	20	
$Q_{gs}$ (nC)	3	
$Q_{gd}$ (nC)	5	
Configuration	Single	

DPAK  
(TO-252)



N-Channel MOSFET

### FEATURES

- Optimal design
  - Low area specific on-resistance
  - Low input capacitance ( $C_{iss}$ )
  - Reduced capacitive switching losses
  - High body diode ruggedness
  - Avalanche energy rated (UIS)
- Optimal efficiency and operation
  - Low cost
  - Simple gate drive circuitry
  - Low figure-of-merit (FOM):  $R_{on} \times Q_g$
  - Fast switching
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

### APPLICATIONS

- Consumer electronics
  - Displays (LCD or plasma TV)
- Server and telecom power supplies
  - SMPS
- Industrial
  - Welding
  - Induction heating
  - Motor drives
- Battery chargers


ORDERING INFORMATION	
Package	DPAK (TO-252)
Lead (Pb)-free	SiHD5N50D-E3
Lead (Pb)-free and Halogen-free	SiHD5N50D-GE3
	SiHD5N50DT1-GE3
	SiHD5N50DT4-GE3
	SiHD5N50DT5-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$		500	V
Gate-Source Voltage	$V_{GS}$		$\pm 30$	
Gate-Source Voltage AC ( $f > 1$ Hz)			30	
Continuous Drain Current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$T_C = 25$ °C	5.3	A
		$T_C = 100$ °C	3.4	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$		10	
Linear Derating Factor			0.83	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$		28.8	mJ
Maximum Power Dissipation	$P_D$		104	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$		-55 to +150	°C
Drain-Source Voltage Slope	$T_J = 125$ °C		24	V/ns
Reverse Diode $dV/dt$ <sup>d</sup>	$dV/dt$		0.28	
Soldering Recommendations (Peak temperature) <sup>c</sup>	for 10 s		300	°C

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 2.3$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 5$  A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$ , starting  $T_J = 25$  °C.

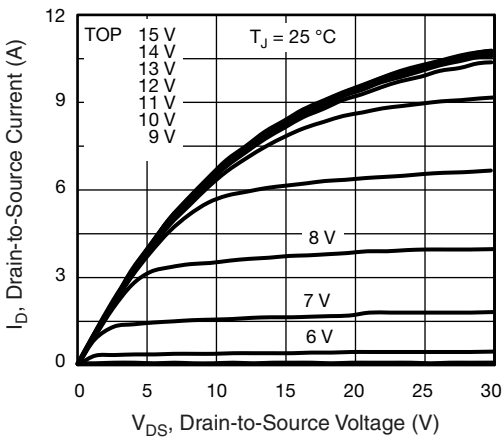
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.2	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	500	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 250\text{ }\mu\text{A}$	-	0.58	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	-	5	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 2.5\text{ A}$	-	1.2	1.5	$\Omega$
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 20\text{ V}, I_D = 2.5\text{ A}$	-	1.8	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$	-	325	-	pF
Output Capacitance	$C_{oss}$		-	34	-	
Reverse Transfer Capacitance	$C_{rss}$		-	6	-	
Effective Output Capacitance, Energy Related <sup>b</sup>	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	31	-	
Effective Output Capacitance, Time Related <sup>c</sup>	$C_{o(tr)}$		-	41	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}, I_D = 2.5\text{ A}, V_{DS} = 400\text{ V}$	-	10	20	nC
Gate-Source Charge	$Q_{gs}$		-	3	-	
Gate-Drain Charge	$Q_{gd}$		-	5	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400\text{ V}, I_D = 2.5\text{ A}, R_g = 9.1\text{ }\Omega, V_{GS} = 10\text{ V}$	-	12	24	ns
Rise Time	$t_r$		-	11	22	
Turn-Off Delay Time	$t_{d(off)}$		-	14	28	
Fall Time	$t_f$		-	11	22	
Gate Input Resistance	$R_g$	$f = 1\text{ MHz}, \text{open drain}$	-	1.7	-	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse P - N junction diode 	-	-	5	A
Pulsed Diode Forward Current	$I_{SM}$		-	-	20	
Diode Forward Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 4\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.2	V
Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 2.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_R = 20\text{ V}$	-	320	-	ns
Reverse Recovery Charge	$Q_{rr}$		-	1.2	-	$\mu\text{C}$
Reverse Recovery Current	$I_{RRM}$		-	8	-	A

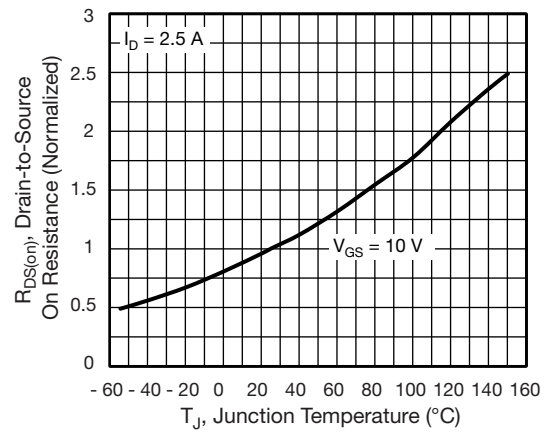
**Notes**

- Repetitive rating; pulse width limited by maximum junction temperature.
- $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .
- $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .

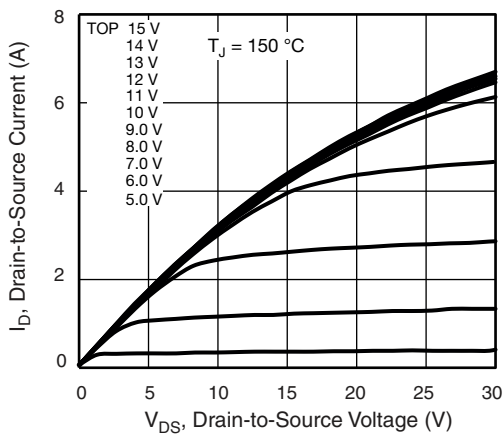
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



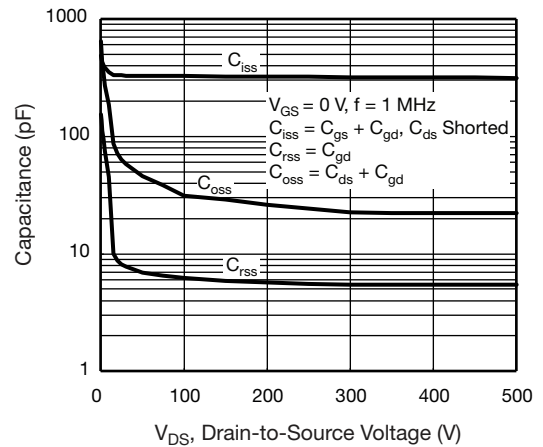
**Fig. 1 - Typical Output Characteristics**



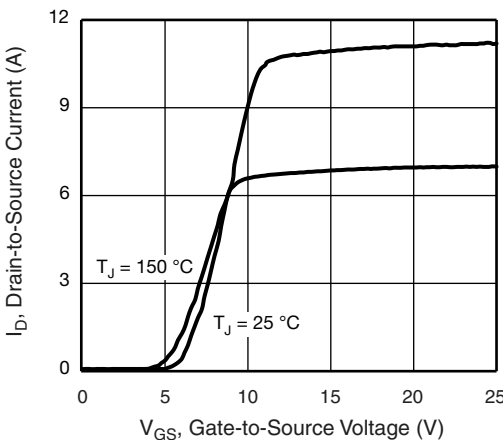
**Fig. 4 - Normalized On-Resistance vs. Temperature**



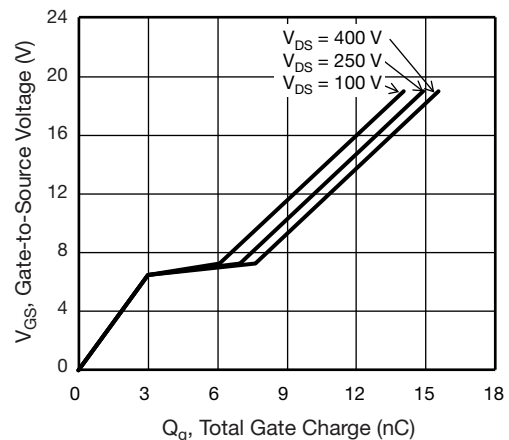
**Fig. 2 - Typical Output Characteristics**



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

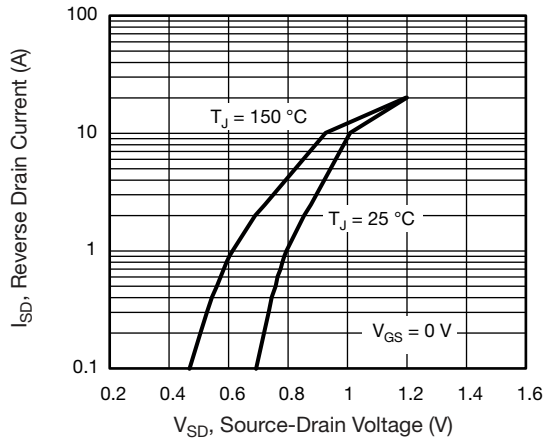


Fig. 7 - Typical Source-Drain Diode Forward Voltage

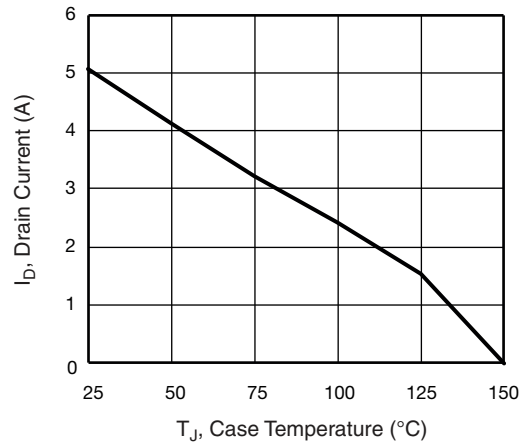


Fig. 9 - Maximum Drain Current vs. Case Temperature

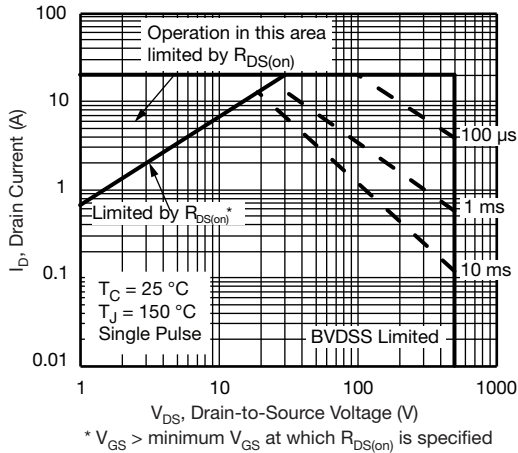


Fig. 8 - Maximum Safe Operating Area

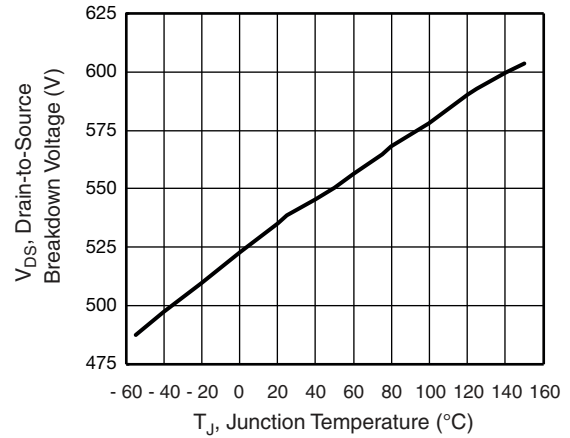


Fig. 10 - Typical Drain-to-Source Voltage vs. Temperature

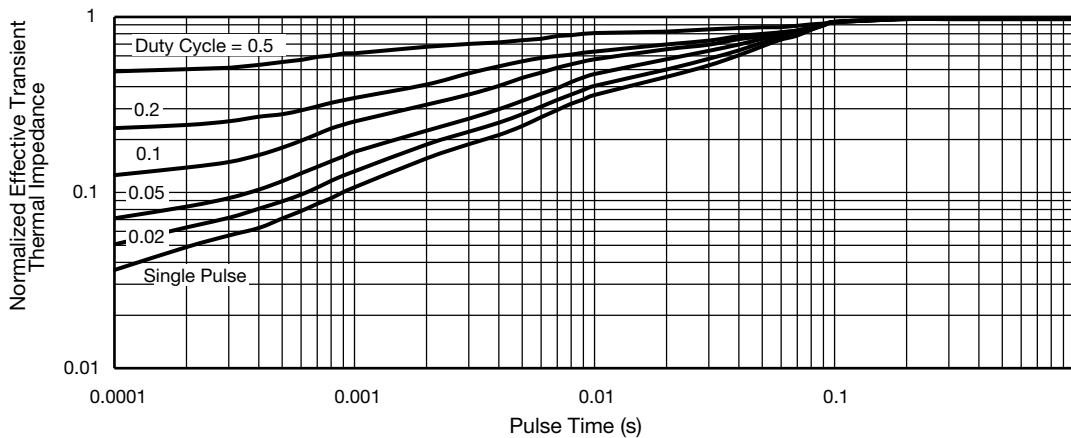


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case



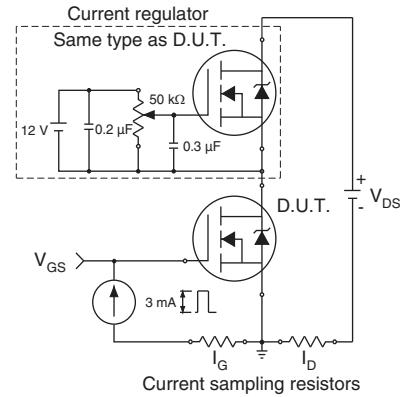
**Fig. 12 - Switching Time Test Circuit**



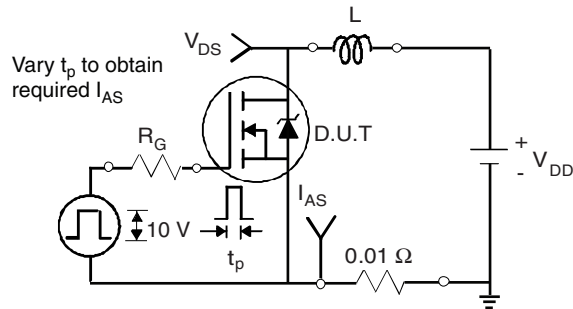
**Fig. 16 - Basic Gate Charge Waveform**



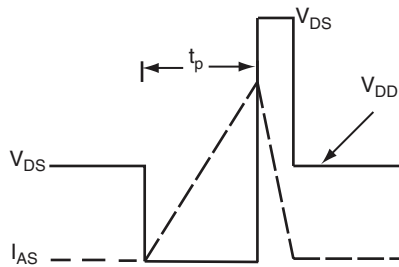
**Fig. 13 - Switching Time Waveforms**



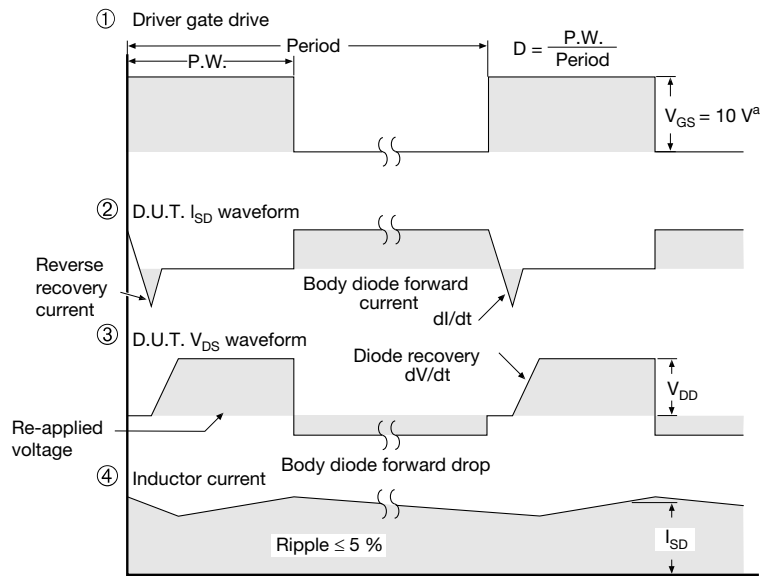
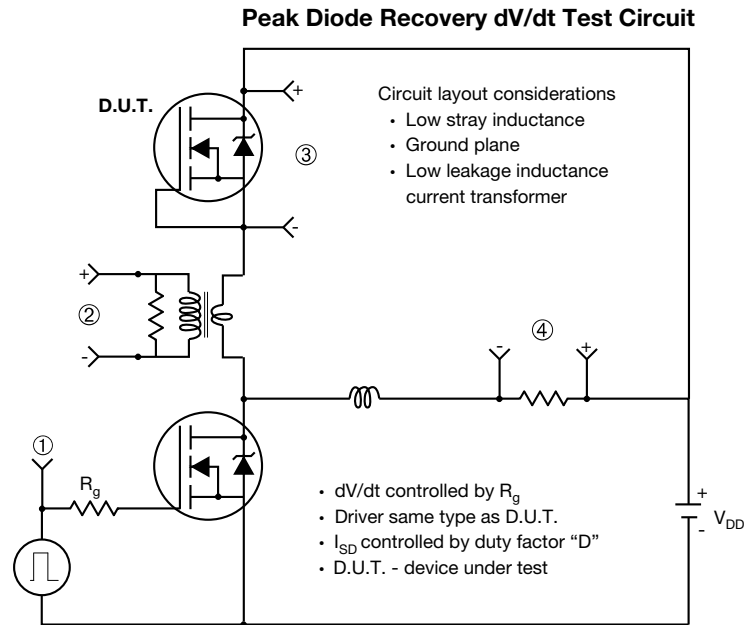
**Fig. 17 - Gate Charge Test Circuit**



**Fig. 14 - Unclamped Inductive Test Circuit**



**Fig. 15 - Unclamped Inductive Waveforms**



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 18 - For N-Channel**

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### TO-252AA Case Outline



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

**Notes**

- Dimension L3 is for reference only.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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