3.3V CMOS Static RAM 1 Meg (64K x 16-Bit)

71V016SA

Features

- **64K x 16 advanced high-speed CMOS Static RAM**
- **Equal access and cycle times**
  - *Commercial: 10/12/15/20ns*
  - *Industrial: 10/12/15/20ns*
- **One Chip Select plus one Output Enable pin**
- **Bidirectional data inputs and outputs directly LVTTL-compatible**
- **Low power consumption via chip deselect**
- **Upper and Lower Byte Enable Pins**
- **Single 3.3V power supply**
- **Available in 44-pin Plastic SOJ, 44-pin TSOP, and 48-Ball Plastic FBGA packages**
- **Industrial temperature range (–40°C to +85°C) is available for selected speeds**
- **Green parts available, see ordering information**

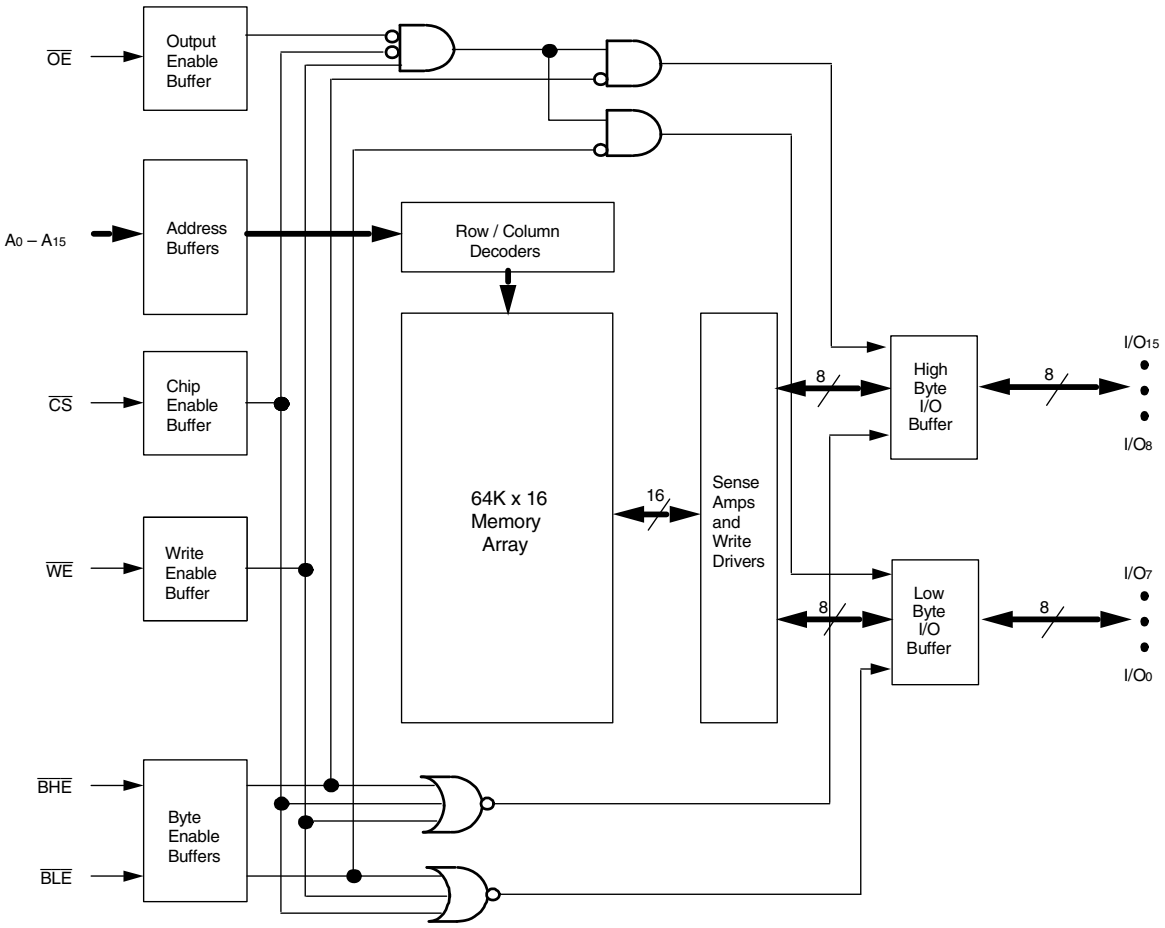
Description

The IDT71V016 is a 1,048,576-bit high-speed Static RAM organized as 64K x 16. It is fabricated using high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71V016 has an output enable pin which operates as fast as 5ns, with address access times as fast as 10ns. All bidirectional inputs and outputs of the IDT71V016 are LVTTL compatible and operation is from a single 3.3V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

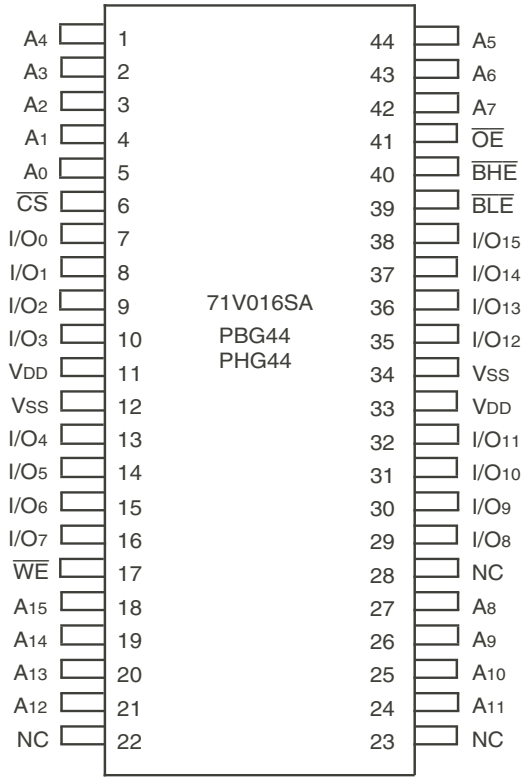
The IDT71V016 is packaged in a JEDEC standard 44-pin Plastic SOJ, a 44-pin TSOP Type II, and a 48-ball plastic 7 x 7 mm FBGA.

Functional Block Diagram



3834 drw 01

Pin Configurations - PBG44, PHG44[1]



3834 drw 02

SOJ/TSOP
Top View

NOTE:
1. This text does not indicate orientation of actual part-marking.

	1	2	3	4	5	6
A	$\overline{BLE}$	$\overline{OE}$	A_0	A_1	A_2	NC
B	I/O_8	$\overline{BHE}$	A_3	A_4	$\overline{CS}$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SS}	I/O_{11}	NC	A_7	I/O_3	V_{DD}
E	V_{DD}	I/O_{12}	NC	NC	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	NC	A_8	A_9	A_{10}	A_{11}	NC

3834 tbl 02a

FBGA (BF48, BFG48)[1]
Top View

NOTE:
1. This text does not indicate orientation of actual part-marking.

Pin Description

$A_0 - A_{15}$	Address Inputs	Input
$\overline{CS}$	Chip Select	Input
$\overline{WE}$	Write Enable	Input
$\overline{OE}$	Output Enable	Input
$\overline{BHE}$	High Byte Enable	Input
$\overline{BLE}$	Low Byte Enable	Input
$I/O_0 - I/O_{15}$	Data Input/Output	I/O
V_{DD}	3.3V Power	Power
V_{SS}	Ground	Gnd

3834 tbl 01

Truth Table[1]

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0-I/O_7	I/O_8-I/O_{15}	Function
H	X	X	X	X	High-Z	High-Z	Deselected – Standby
L	L	H	L	H	$DATA_{OUT}$	High-Z	Low Byte Read
L	L	H	H	L	High-Z	$DATA_{OUT}$	High Byte Read
L	L	H	L	L	$DATA_{OUT}$	$DATA_{OUT}$	Word Read
L	X	L	L	L	$DATA_{IN}$	$DATA_{IN}$	Word Write
L	X	L	L	H	$DATA_{IN}$	High-Z	Low Byte Write
L	X	L	H	L	High-Z	$DATA_{IN}$	High Byte Write
L	H	H	X	X	High-Z	High-Z	Outputs Disabled
L	X	X	H	H	High-Z	High-Z	Outputs Disabled

3834 tbl 02

NOTE:
1. H = V_{IH}, L = V_{IL}, X = Don't care.

Absolute Maximum Ratings(1)

Symbol	Rating	Value	Unit
V_{DD}	Supply Voltage Relative to V_{SS}	–0.5 to +4.6	V
V_{IN}, V_{OUT}	Terminal Voltage Relative to V_{SS}	–0.5 to V_{DD}+0.5	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.25	W
I_{OUT}	DC Output Current	50	mA

3834 tbl 03

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	6	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

3834 tbl 06

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	Vss	V_{DD}
Commercial	0°C to +70°C	0V	See Below
Industrial	-40°C to +85°C	0V	See Below

3834 tbl 04

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}(1)	Supply Voltage	3.15	3.3	3.6	V
V_{DD}(2)	Supply Voltage	3.0	3.3	3.6	V
Vss	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	V_{DD}+0.3(3)	V
V_{IL}	Input Low Voltage	–0.3(4)	—	0.8	V

3834 tbl 05

NOTES:
1. For 71V016SA10 only.
2. For all speed grades except 71V016SA10.
3. V_{IH} (max.) = V_{DD}+2V for pulse width less than 5ns, once per cycle.
4. V_{IL} (min.) = –2V for pulse width less than 5ns, once per cycle.

DC Electrical Characteristics

(V_{DD} = Min. to Max., Commercial and Industrial Temperature Ranges)

Symbol	Parameter	Test Condition	IDT71V016SA		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = V_{SS} to V_{DD}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{DD} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to V_{DD}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{DD} = Min.	2.4	—	V

3834 tbl 07

DC Electrical Characteristics(1,2)

(V_{DD} = Min. to Max., V_{LC} = 0.2V, V_{HC} = V_{DD} – 0.2V)

Symbol	Parameter		71V016SA10		71V016SA12		71V016SA15		71V016SA20		Unit
			Com'l	Ind'l	Com'l	Ind'l	Com'l	Ind'l	Com'l	Ind'l	
I_{CC}	Dynamic Operating Current $\overline{CS} \le V_{LC}$, Outputs Open, V_{DD} = Max., f = f_{MAX}(3)	Max.	160	170	150	160	130	130	120	120	mA
		Typ.(4)	65	--	60	--	55	--	50	--	
I_{SB}	Dynamic Standby Power Supply Current $\overline{CS} \ge V_{HC}$, Outputs Open, V_{DD} = Max., f = f_{MAX}(3)		45	50	40	45	35	35	30	30	mA
I_{SB1}	Full Standby Power Supply Current (static) $\overline{CS} \ge V_{HC}$, Outputs Open, V_{DD} = Max., f = 0(3)		10	10	10	10	10	10	10	10	mA

3834 tbl 08

NOTES:
1. All values are maximum guaranteed values.
2. All inputs switch between 0.2V (Low) and V_{DD} – 0.2V (High).
3. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing .
4. Typical values are based on characterization data for H step only measured at 3.3V, 25°C and with equal read and write cycles.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1.5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figure 1, 2 and 3

3834 tbl 09

AC Test Loads

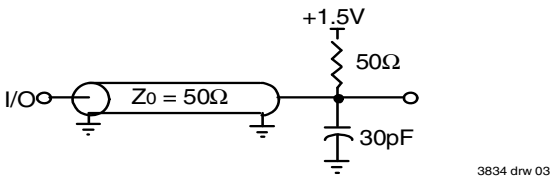
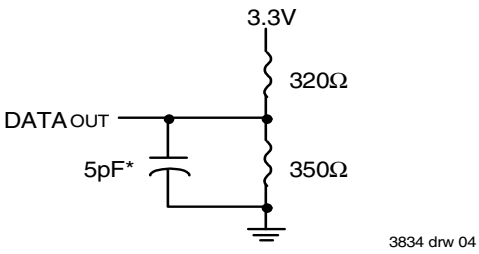


Figure 1. AC Test Load



*Including jig and scope capacitance.

Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

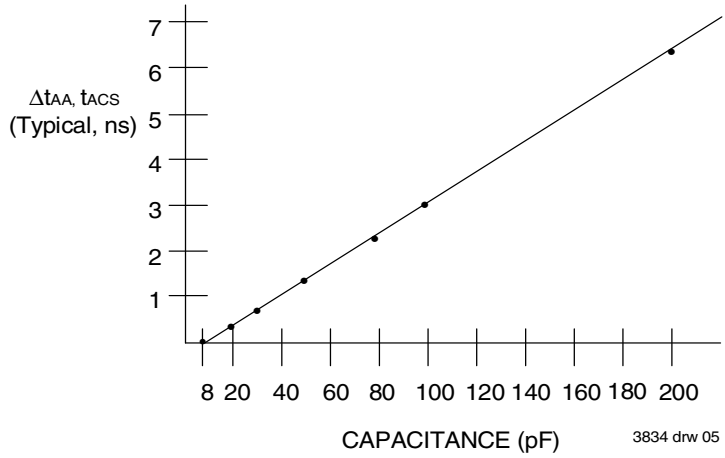


Figure 3. Output Capacitive Derating

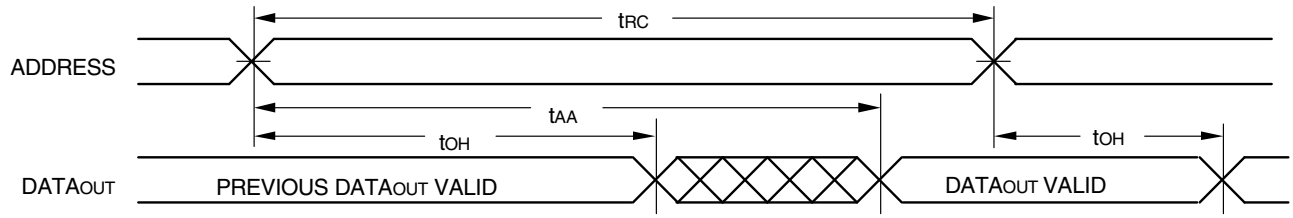
AC Electrical Characteristics (V_{DD} = Min. to Max., Commercial and Industrial Temperature Ranges)

Symbol	Parameter	71V016SA10		71V016SA12		71V016SA15		71V016SA20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	10	—	12	—	15	—	20	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	20	ns
t_{ACS}	Chip Select Access Time	—	10	—	12	—	15	—	20	ns
t_{CLZ}(1)	Chip Select Low to Output in Low-Z	4	—	4	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Select High to Output in High-Z	—	5	—	6	—	6	—	8	ns
t_{OE}	Output Enable Low to Output Valid	—	5	—	6	—	7	—	8	ns
t_{OLZ}(1)	Output Enable Low to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t_{OHZ}(1)	Output Enable High to Output in High-Z	—	5	—	6	—	6	—	8	ns
t_{OH}	Output Hold from Address Change	4	—	4	—	4	—	4	—	ns
t_{BE}	Byte Enable Low to Output Valid	—	5	—	6	—	7	—	8	ns
t_{BLZ}(1)	Byte Enable Low to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t_{BHZ}(1)	Byte Enable High to Output in High-Z	—	5	—	6	—	6	—	8	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	10	—	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End of Write	7	—	8	—	10	—	12	—	ns
t_{CW}	Chip Select Low to End of Write	7	—	8	—	10	—	12	—	ns
t_{BW}	Byte Enable Low to End of Write	7	—	8	—	10	—	12	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Address Hold from End of Write	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	7	—	8	—	10	—	12	—	ns
t_{DW}	Data Valid to End of Write	5	—	6	—	7	—	9	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{OW}(1)	Write Enable High to Output in Low-Z	3	—	3	—	3	—	3	—	ns
t_{WHZ}(1)	Write Enable Low to Output in High-Z	—	5	—	6	—	6	—	8	ns

NOTE:
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

3834 tbl 10

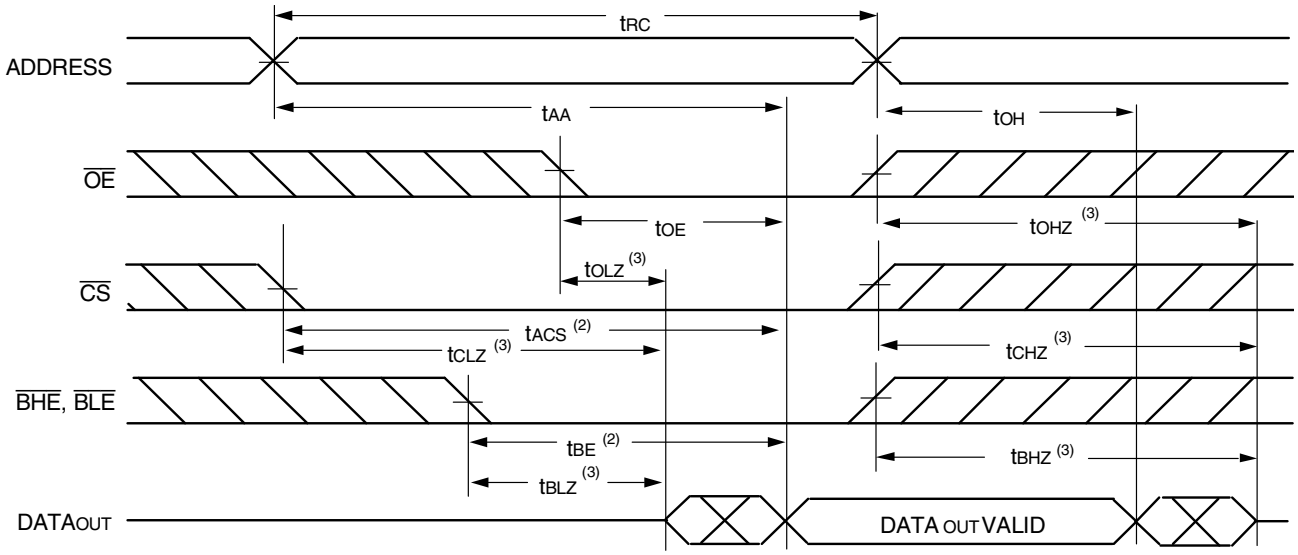
Timing Waveform of Read Cycle No. 1(1,2,3)



NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. $\overline{OE}$, $\overline{BHE}$, and $\overline{BLE}$ are LOW.

3834 drw 06

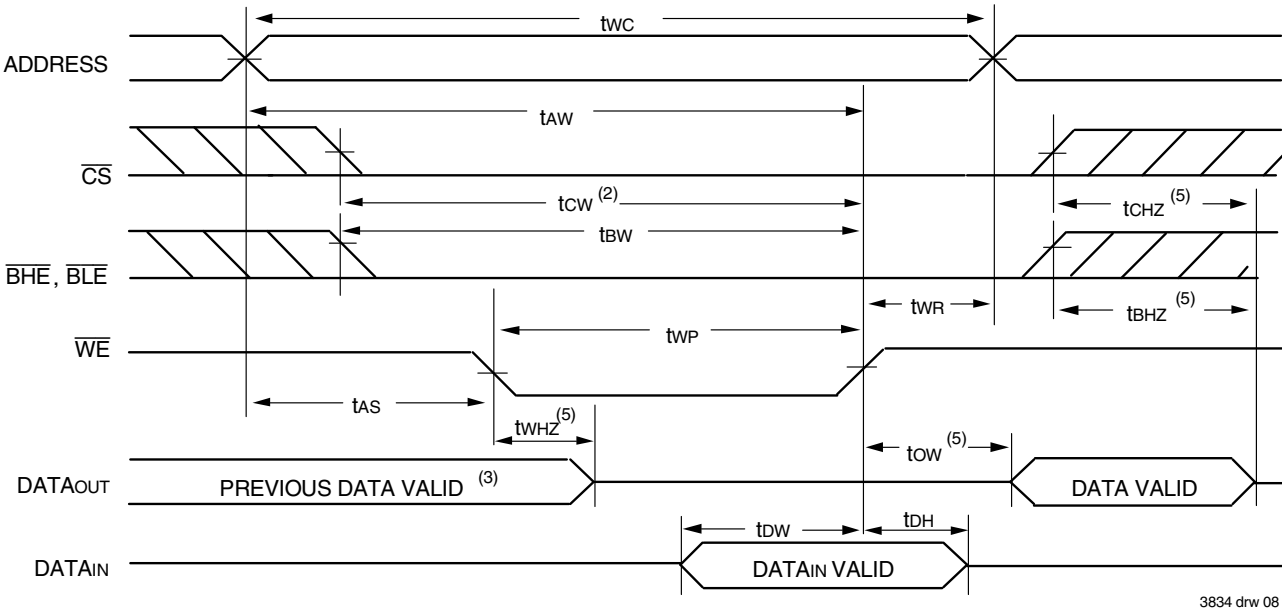
Timing Waveform of Read Cycle No. 2(1)



3834 drw 07

NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Address must be valid prior to or coincident with the later of $\overline{CS}$, $\overline{BHE}$, or $\overline{BLE}$ transition LOW; otherwise t_{AA} is the limiting parameter.
3. Transition is measured ±200mV from steady state.

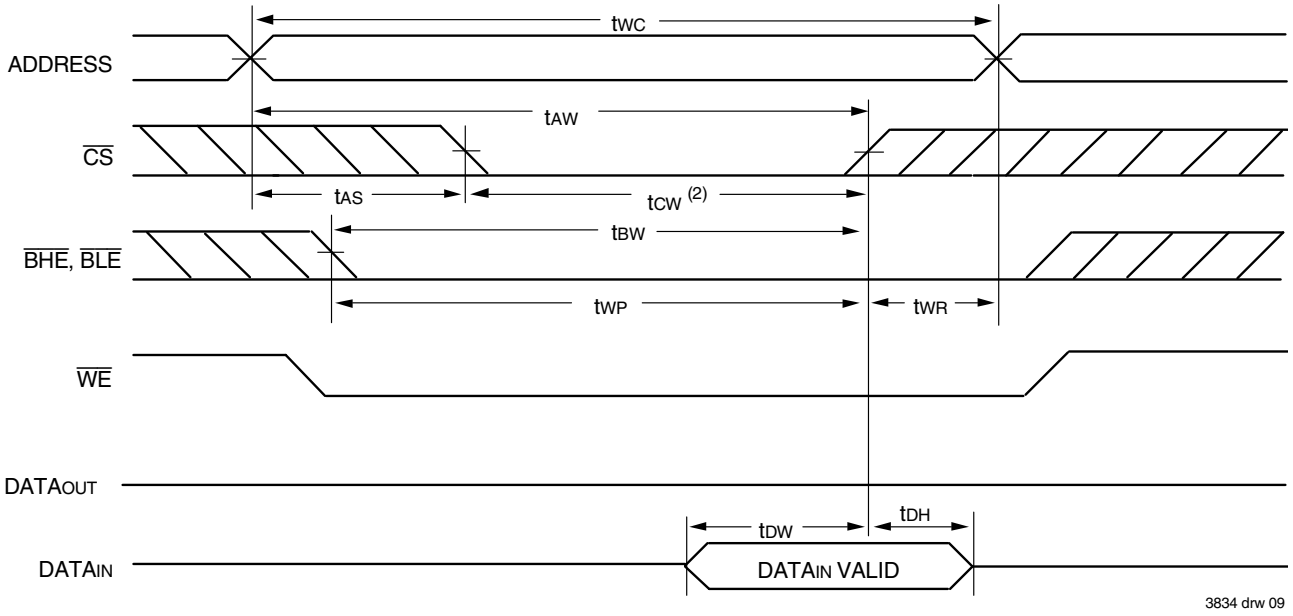
Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)(1,2,4)



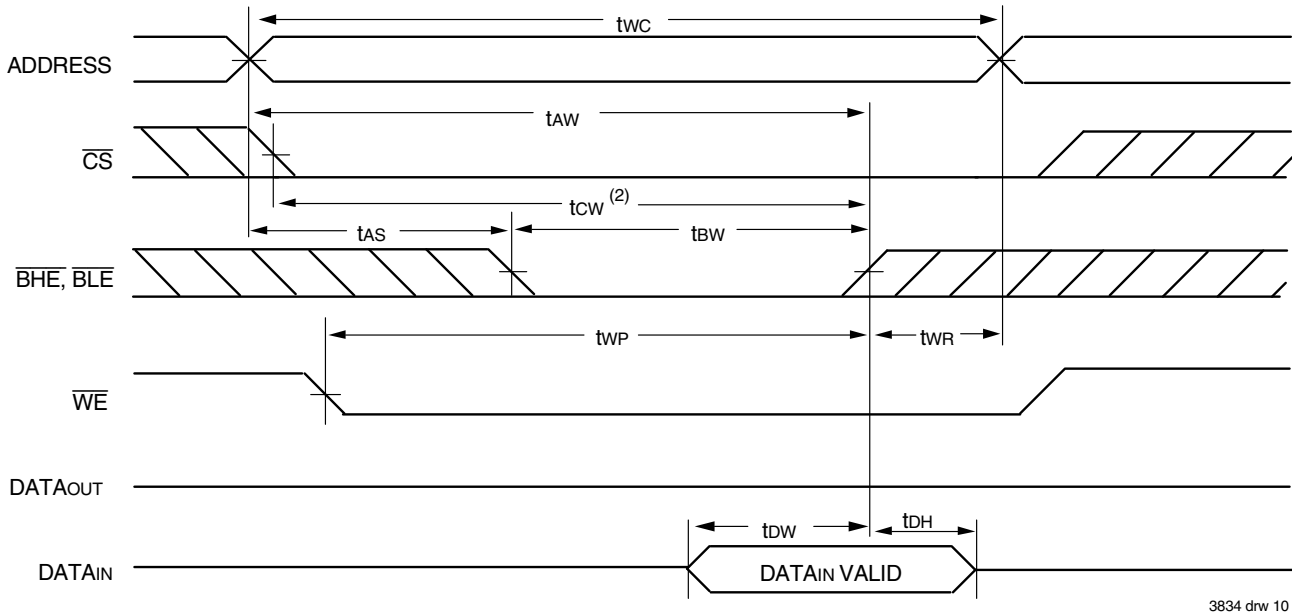
3834 drw 08

NOTES:
1. A write occurs during the overlap of a LOW $\overline{CS}$, LOW $\overline{BHE}$ or $\overline{BLE}$, and a LOW $\overline{WE}$.
2. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP}.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{CS}$ LOW or $\overline{BHE}$ and $\overline{BLE}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured ±200mV from steady state.

Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)(1,4)



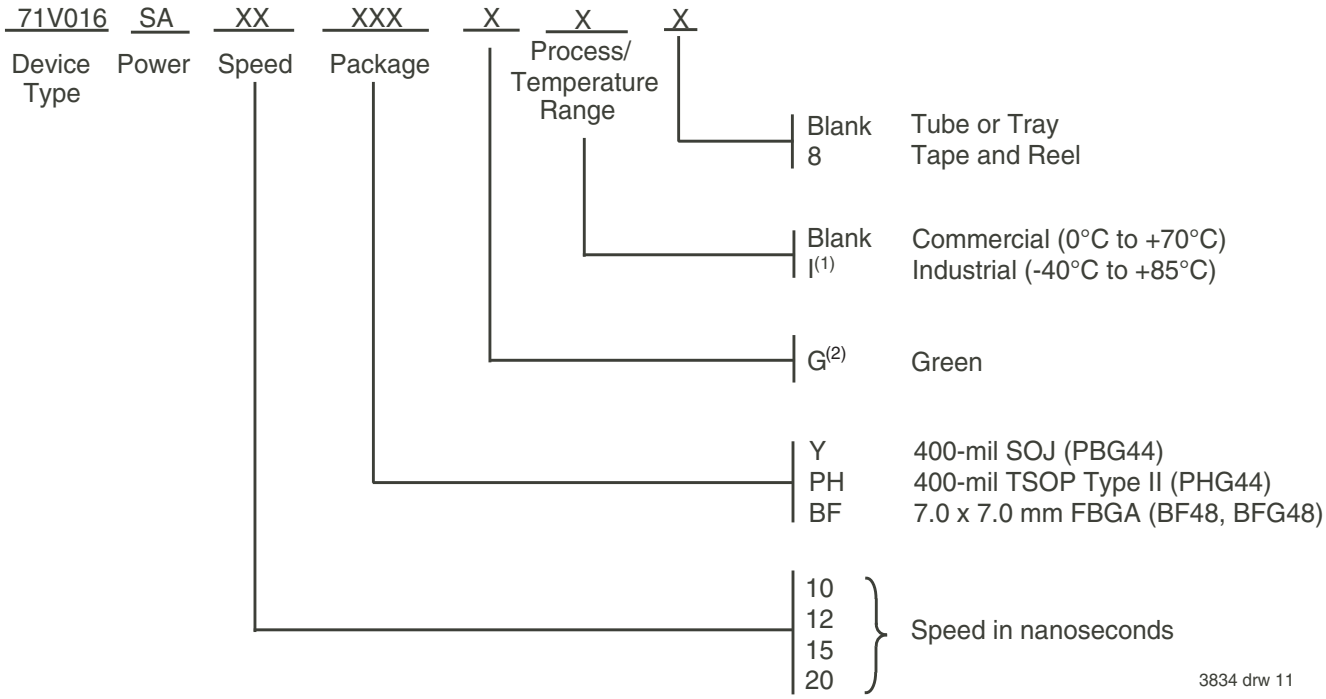
Timing Waveform of Write Cycle No. 3 ($\overline{BHE}$, $\overline{BLE}$ Controlled Timing)(1,4)



NOTES:

1. A write occurs during the overlap of a LOW $\overline{CS}$, LOW $\overline{BHE}$ or $\overline{BLE}$, and a LOW $\overline{WE}$.
2. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP}.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{CS}$ LOW or $\overline{BHE}$ and $\overline{BLE}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured ±200mV from steady state.

Ordering Information



NOTE:
1. Contact your local sales office for industrial temp. range for other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.

Note that information regarding recently obsoleted parts are included in this datasheet for customer convenience.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
10	71V016SA10BF	BF48	CABGA	C
	71V016SA10BF8	BF48	CABGA	C
	71V016SA10BFG	BFG48	CABGA	C
	71V016SA10BFG8	BFG48	CABGA	C
	71V016SA10BFGI	BFG48	CABGA	I
	71V016SA10BFGI8	BFG48	CABGA	I
	71V016SA10PHG	PHG44	TSOP	C
	71V016SA10PHG8	PHG44	TSOP	C
	71V016SA10PHGI	PHG44	TSOP	I
	71V016SA10PHGI8	PHG44	TSOP	I
	71V016SA10YG	PBG44	SOJ	C
	71V016SA10YG8	PBG44	SOJ	C
12	71V016SA12BF	BF48	CABGA	C
	71V016SA12BF8	BF48	CABGA	C
	71V016SA12BFG	BFG48	CABGA	C
	71V016SA12BFG8	BFG48	CABGA	C
	71V016SA12BFGI	BFG48	CABGA	I
	71V016SA12BFGI8	BFG48	CABGA	I
	71V016SA12BFI	BF48	CABGA	I
	71V016SA12BFI8	BF48	CABGA	I
	71V016SA12PHG	PHG44	TSOP	C
	71V016SA12PHG8	PHG44	TSOP	C
	71V016SA12PHGI	PHG44	TSOP	I
	71V016SA12PHGI8	PHG44	TSOP	I
	71V016SA12YG	PBG44	SOJ	C
	71V016SA12YG8	PBG44	SOJ	C
	71V016SA12YGI	PBG44	SOJ	I
	71V016SA12YGI8	PBG44	SOJ	I

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
15	71V016SA15BF	BF48	CABGA	C
	71V016SA15BF8	BF48	CABGA	C
	71V016SA15BFG	BFG48	CABGA	C
	71V016SA15BFG8	BFG48	CABGA	C
	71V016SA15BFGI	BFG48	CABGA	I
	71V016SA15BFGI8	BFG48	CABGA	I
	71V016SA15BFI	BF48	CABGA	I
	71V016SA15BFI8	BF48	CABGA	I
	71V016SA15PHG	PHG44	TSOP	C
	71V016SA15PHG8	PHG44	TSOP	C
	71V016SA15PHGI	PHG44	TSOP	I
	71V016SA15PHGI8	PHG44	TSOP	I
	71V016SA15YG	PBG44	SOJ	C
	71V016SA15YG8	PBG44	SOJ	C
	71V016SA15YGI	PBG44	SOJ	I
	71V016SA15YGI8	PBG44	SOJ	I
20	71V016SA20BF	BF48	CABGA	C
	71V016SA20BF8	BF48	CABGA	C
	71V016SA20BFG	BFG48	CABGA	C
	71V016SA20BFG8	BFG48	CABGA	C
	71V016SA20BFGI	BFG48	CABGA	I
	71V016SA20BFGI8	BFG48	CABGA	I
	71V016SA20BFI	BF48	CABGA	I
	71V016SA20BFI8	BF48	CABGA	I
	71V016SA20PHG	PHG44	TSOP	C
	71V016SA20PHG8	PHG44	TSOP	C
	71V016SA20PHGI	PHG44	TSOP	I
	71V016SA20PHGI8	PHG44	TSOP	I
	71V016SA20YG	PBG44	SOJ	C
	71V016SA20YG8	PBG44	SOJ	C
	71V016SA20YGI	PBG44	SOJ	I
	71V016SA20YGI8	PBG44	SOJ	I

Datasheet Document History

01/07/00		Updated to new format
	Pg. 1, 3, 5, 8	Added Industrial Temperature range offerings
	Pg. 2	Numbered I/Os and address pins on FBGA Top View
	Pg. 6	Revised footnotes on Write Cycle No. 1 diagram
	Pg. 7	Revised footnotes on Write Cycle No. 2 and No. 3 diagrams
	Pg. 9	Added Datasheet Document History
08/30/00	Pg. 3	Tighten I_{CC} and I_{SB}.
	Pg. 5	Tighten t_{CLZ}, t_{CHZ}, t_{OHZ}, t_{BHZ} and t_{WHZ}
08/22/01	Pg. 8	Removed footnote "available in 15ns and 20ns only"
06/20/02	Pg. 8	Added tape and reel field to ordering information
01/30/04	Pg. 8	Added "Restricted hazardous substance device" to ordering information.
09/27/06	Pg. 8	Corrected ordering information, changed position of I and G.
02/14/07	Pg.8	Added H step generation to data sheet ordering information.
06/26/07	Pg.3	Changed typical parameters for ICC, DC electrical characteristics table.
10/13/08	Pg.8	Removed "IDT" from orderable part number
10/11/11	Pg.1,8	Updated datasheet with removal of Obsolete HSA part number.
08/13/13	Pg.1,3,5,8	Added 10ns for Industrial Temperature range offerings.
06/23/20	Pg.1 - 9	Rebranded as Renesas datasheet
	Pg.1 & 8	Updated Industrial temp and Green availability
	Pg.2 & 8	Updated package codes
	Pg.9	Added Orderable Part Information tables

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.