# USB-to-UART Bridge Controller

## Features

- Universal Serial Bus (USB) Integration
  - Full-Speed USB peripheral compliant with USB2.0 specification
  - USB-IF certified with TID 40001425
  - Support for bus-powered and self-powered configurations
  - 3 endpoints (1 Interrupt IN, 1 Bulk OUT and 1 Bulk IN)
  - Integrated USB transceiver, 1.5 kΩ pull-up resistor on D+ line
- Universal Asynchronous Receiver Transmitter (UART)
  - Baud rate generation (300 to 230400)
  - Data format:
    - 8 data bits
    - 1 stop bit
    - No parity, even parity or odd parity
  - Support for Parity, Overrun and Framing errors
  - Supports flow control using CTS,RTS,DTR, DSR
  - LED signals to indicate activity on TxD and RxD lines

- Full device operation from a single voltage supply of 3.3 V or 5 V
- Low power consumption in suspend mode
  - 225 µA at 5 V operating voltage
  - 207 µA at 3.3 V operating voltage
- Integrated 24 MHz oscillator
- Integrated 3.3 V regulator
- Integrated flash to store device configuration
- Software support for ease of development
  - Configuration utility to program device parameters such as VID, PID and string descriptors.
  - Certified Cypress VCP driver for Windows (8 / 7 / Vista / XP)
  - Support for device drivers for Android, Mac, Linux, Window CE 4.2, 5.0, 6.0
- 28-pin SSOP 10 mm × 7.5 mm, RoHS compliant package
- Temperature grade
  - Commercial operating temperature range of 0 °C to +70 °C



Figure 1. CY7C64225 Block Diagram
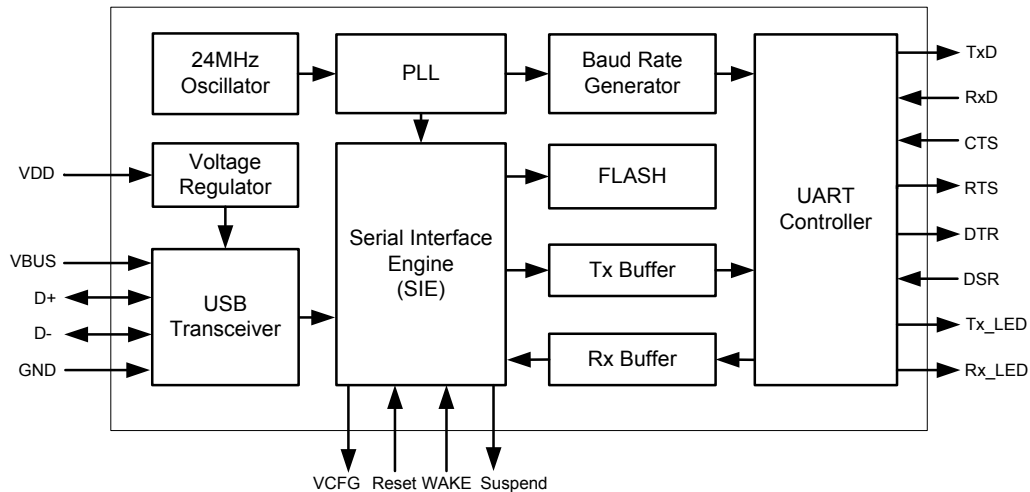
# More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the document USB-Serial Bridge Controller Product Overview.

■ Overview: USB Portfolio, USB Roadmap

■ USB 2.0 Product Selectors: USB-Serial Bridge Controller, USB to UART Controller (Gen I), enCoRe II, enCoRe III, enCoRe V

■ Knowledge Base Articles: Cypress offers a large number of USB knowledge base articles covering a broad range of topics, from basic to advanced level. Recommended knowledge base articles for getting started with USB to UART Controller (Gen I) are:

❏ KBA85920 – USB-UART and USB-Serial

❏ KBA85909 – Key Features of the Cypress® USB-Serial Bridge Controller

❏ KBA85921 – Replacing FT232R with CY7C65213 USB-UART LP Bridge Controller

❏ KBA85913 – Voltage supply range for USB-Serial

❏ KBA89355 – USB Serial Cypress Default VID and PID

❏ KBA92641 – USB-Serial Bridge Controller Managing I/Os using API

❏ KBA92442 – Non-Standard Baud Rates in USB-Serial Bridge Controllers

❏ KBA91366 – Binding a USB-Serial Device to a Microsoft® CDC Driver

❏ KBA92551 – Testing a USB-Serial Bridge Controller Configured as USB-UART with Linux®

For a complete list of knowledge base articles, click here.

■ Code Examples: USB Full-Speed

■ Development Kits:

❏ CYUSBS232, Cypress USB-UART LP Reference Design Kit

❏ CYUSBS234, Cypress USB-Serial (Single Channel) Development Kit

❏ CYUSBS236, Cypress USB-Serial (Dual Channel) Development Kit

■ Models: IBIS

Cypress USB-UART LP Reference Design Kit

The Cypress USB-UART LP Reference Design Kit is a complete development resource. It provides a platform to develop and test custom projects. The development kit contains collateral materials for the firmware, hardware, and software aspects of a design.

# Contents

## Applications

- Enable USB connectivity in legacy peripherals with UART

- Industrial and Metering devices

- Medical Devices

- Point of Sales (POS)

- USB-to-UART cables, USB to RS-232 cables

## Functional Description

### Introduction

Cypress's USB-to-UART bridge controller enables seamless PC connectivity for peripherals with UART interface. It integrates a USB 2.0 Full-Speed device controller, UART, voltage regulator, oscillator and flash memory for storing configuration parameters, offering a cost-effective solution. The controller supports bus-powered and self-powered modes, and enables efficient system power management with suspend and remote wake-up signals. It is available in 28-pin SSOP package.

## Functional Overview

### USB Interface

The USB-to-UART device supports Full-Speed USB operation and is compliant with USB 2.0 Specification. The integrated USB Serial Interface Engine (SIE) and USB transceiver manage the USB protocol and communication.

### UART Controller

The USB-to-UART device integrates a UART controller which supports the baud rates of 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600, 14400, 19200, 28800, 38400, 56000, 57600, 115200 and 230400* with even, odd or no parity.

*UART Flow Control*

USB-to-UART device supports UART hardware flow control using control signal pairs such as RTS (Request to Send) - CTS (Clear to Send) and DTR (Data Terminal Ready) - DSR (Data Set Ready). Data flow control is disabled by default. The hardware flow control is optional and can be selected from the host application software.

Following is the description of flow control signals:

CTS (input):

This signal can pause or resume data transmission over UART interface. Data transmission can be stopped by de-asserting the CTS signal and the data transmission can resume with CTS assertion. The pause and resume operation does not affect data integrity.

RTS (Output):

The receive buffer has a watermark level of 80%. Once the data in the receive buffer reaches that level, the RTS signal is de-asserted indicating the transmitting device to stop data transmission. Start of data consumption by application will reduce device data backlog and once it reaches 50% watermark level, RTS signal will be asserted to resume data reception.

DTR / DSR:

DTR / DSR signals are used to establish communication link with the UART. These signals complement each other in the functionality like RTS & CTS.

**Note:** Flow control is not supported when operating the device at 230400 Baud rate.

In applications where hardware flow control is desired, the CTS, RTS, DSR and DTR pins of the transmitting device have to be connected to RTS, CTS, DTR and DSR pins of USB-to-UART device respectively. In cases where DTR and DSR pins are not available on the transmitting device, the DTR and DSR pins of USB-to-UART device have to be connected. Please refer the circuit diagram shown in .

### Suspend and Resume

The USB-to-UART device drives the SUSPEND pin to logic low and enters into a low power mode whenever the USB bus goes into suspend state. This helps to meet the stringent suspend current requirement of the USB 2.0 specification, while using the device in bus powered mode. The device will resume from suspend state under any of the following conditions:

1. Any activity is detected on the USB bus

2. WAKE pin is asserted in order to generate Remote Wake-Up to the host.

### WAKE

WAKE pin is used to generate Remote Wake-Up signal on the USB bus. Remote Wake-Up signal is sent only if the host enables this feature through SET_FEATURE request. Support for Remote Wake-Up is intimated to the host from the device through configuration descriptor during the USB enumeration process. USB-to-UART device allows enabling/disabling the Remote Wake-Up feature through the configuration utility CyUsbUart.

### Reset

No Connect (NC)

### Activity Indicators

Tx_LED pin and Rx_LED pin are active low and sink a maximum current of 20 mA each.

### VCFG

An active low on the VCFG indicates that the VBUS is detected and the device is configured.

### VBUS

This pin is used for VBUS detection. A series resistor is required on this pin.

### Regulator

The USB-to-UART device integrates a 3.3 V voltage regulator which can be powered by the USB bus or an external power supply.

### Oscillator

The USB-to-UART device integrates a 24 MHz oscillator which is used as a reference clock for SIE and UART interface.

## Flash

The USB-to-UART device integrates a flash to store device parameters such as VID, PID, product string descriptor, manufacturer string descriptor and power mode (self-powered or bus-powered). Please refer Table 1 for the list of configurable parameters.

## Configurations

The internal flash can be used to configure the device parameters listed in Table 1.

**Table 1. Internal Flash Default Values**

| No. | Parameter | Default Value | Explanation |
|-----|-----------|---------------|-------------|
| 1 | VID / PID | 04B4 / 0008 | A 2-byte vendor ID and product ID must be set in hexadecimal format. The VID and PID options cannot be zero or empty. The Cypress VID/PID is programmed by default. |
| 2 | Manufacturer String Descriptor | 2012 Cypress Semiconductor | The Manufacturer string can be a value of up to 26 characters. |
| 3 | Product String Descriptor | Cypress-USB2UART-Ver1.0G | The Product string can be a value of up to 24 characters. |
| 4 | Bus/Self Powered | Self | The USB power mode can be set to either self-powered (input supply from external power supply) or bus-powered mode (input supply from VBUS) |
| 5 | Remote Wake-Up | Enabled | When enabled, this option can be used to wake up the USB host from suspend state remotely from the attached device. |
| 6 | Max. Power (mA) | 100 | The USB device current requirement value can be set by using this option. |

## Software and Driver Support

CyUsbUart configuration utility can be used to configure the parameters listed in Table 1. The configuration utility is available for download from http://www.cypress.com/?rID=61047.

The Cypress driver allows existing COM port based applications to communicate via USB to Cypress's USB-to-UART device.

The driver serves the following purposes:

■ Add UART port to PCs without UART port

■ Add an additional UART port to the PC

■ Facilitate easy migration for systems which have a free USB port and need an additional UART port

The driver is available for download from http://www.cypress.com/?rID=63794. This driver is WHQL certified for the default Cypress VID / PID of 0x04B4 / 0x0008.

## Pin Configuration

### 28-pin part pinout Description

The CY7C64225 USB-to-UART Bridge device is available in a 28-pin package as shown in Figure 2. The pin description is listed in Table 2.

**Table 2. 28-pin part pinout (SSOP)**

| Pin No. | Name | I/O | Description |
|---|---|---|---|
| 1 | GND | Power | Ground |
| 2 | Tx_LED | Output | Active low, UART Tx_LED, max current –20 mA |
| 3 | SUSPEND | Output | Active low indicates USB is suspended |
| 4 | TxD | Output | UART Data Transmit, Output |
| 5 | DTR | Output | Data Terminal Ready (DTR) Pin |
| 6 | RESET | Input | No Connect (NC) |
| 7 | VBUS | Input | Used for VBUS monitoring. This pin requires a series resistor when connected to VBUS. The recommended values are in the range of 1 k$\Omega$–10 k$\Omega$. |
| 8 | DSR | Input | Data Set Ready (DSR) pin |
| 13 | GND | Power | USB Ground |
| 14 | D+ | USB | USB D+ Line |
| 15 | D– | USB | USB D– Line |
| 16 | $V_{DD}$ | Power | Supply Voltage (3.3 V or 5 V) |
| 21 | CTS | Input | Clear to Send (CTS) input, handshake signal |
| 22 | WAKE | Input | Active high on this pin, generates Remote Wake-Up signal on the Bus |
| 23 | RxD | Input | UART Data Receive, Input |
| 24 | RTS | Output | Request to Sent (RTS) output, hand-shake signal |
| 26 | VCFG | Output | Active low indicates VBUS is detected and device is configured |
| 27 | Rx_LED | Output | Active low, UART Rx_LED, max current –20 mA |
| 28 | $V_{DD}$ | Power | Supply Voltage. 3.3 V or 5 V |
| 9 | NC | NC | No Connect |
| 10 | NC | NC | No Connect |
| 11 | NC | NC | No Connect |
| 12 | NC | NC | No Connect |
| 17 | NC | NC | No Connect |
| 18 | NC | NC | No Connect |
| 19 | NC | NC | No Connect |
| 20 | NC | NC | No Connect |
| 25 | NC | NC | No Connect |

**Figure 2. CY7C64225 USB-UART Bridge Device**
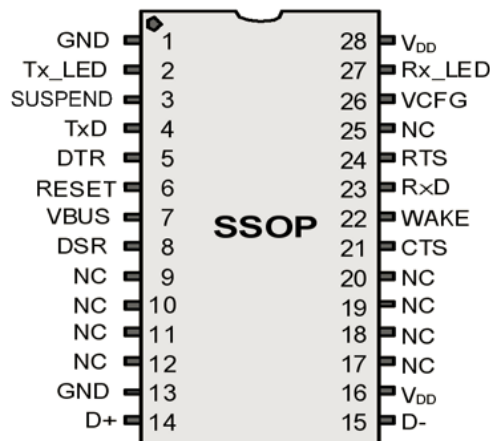
## Application Circuits

The following diagrams illustrates typical application schematics circuits.

### Bus Powered Design

The figure below illustrates the USB bus powered design using CY7C64225. The internal voltage regulator provides the 3.3 V required by the internal USB transceiver. The device parameters such as 'Power consumption' and 'Bus / Self Powered' in the internal flash can be modified as required by the application, using the configuration utility CyUsbUart.

A 1K series resistor is required for VBUS pin of CY7C64225 in this configuration.

**Figure 3.  Bus Powered Configuration**
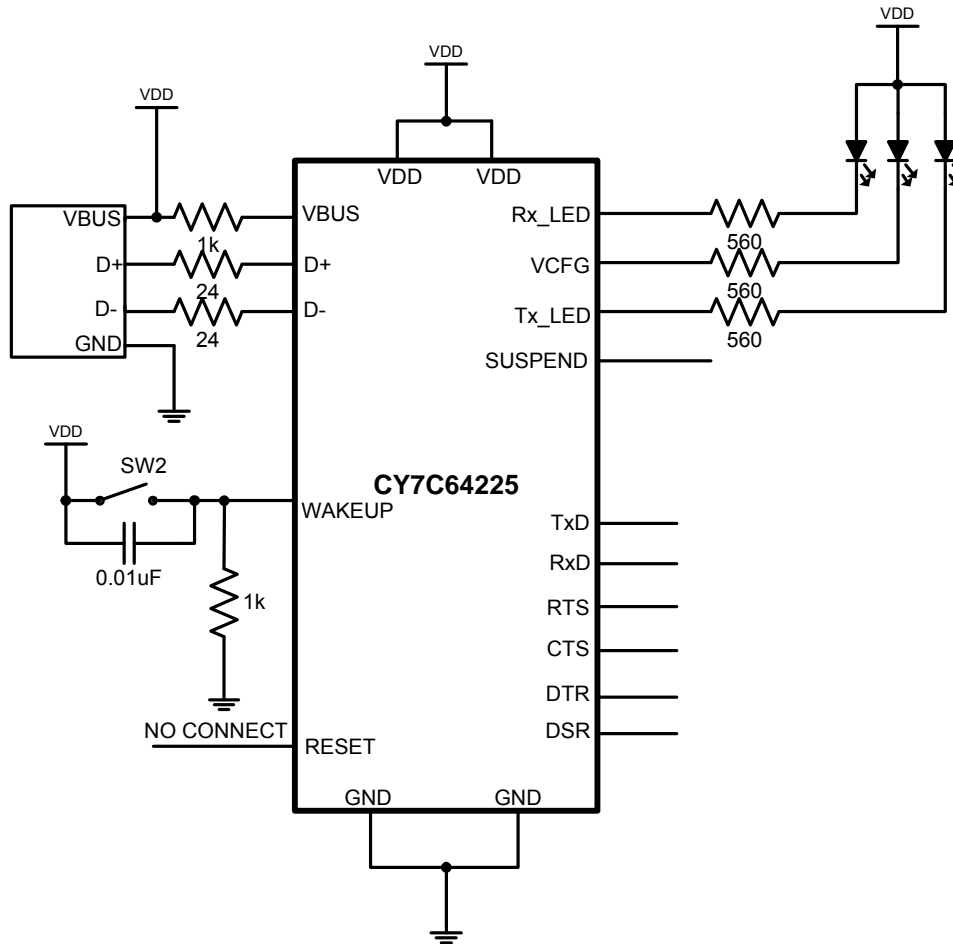
## Bus Powered Design using External Regulator

Figure 4 illustrates the use of CY7C64225 in bus powered mode but running at 3.3 V. This design can be adopted when the circuit operating at 3.3 V is desired (RX, TX, RTS, CTS, DSR, DTR at 3.3 V).

This design uses an external 5 V to 3.3 V regulator to supply the 3.3 V to CY7C64225 from VBUS. The 3.3 V to CY7C64225 can also be provided from a regulator which is already available on the circuit board, being used for other components on the board.

Since the circuit is operating at 3.3 V, a voltage divider is used to provide 3.3 V from VBUS of USB port to 'VBUS' pin of CY7C64225.

**Figure 4. Bus Powered Design using External Regulator**
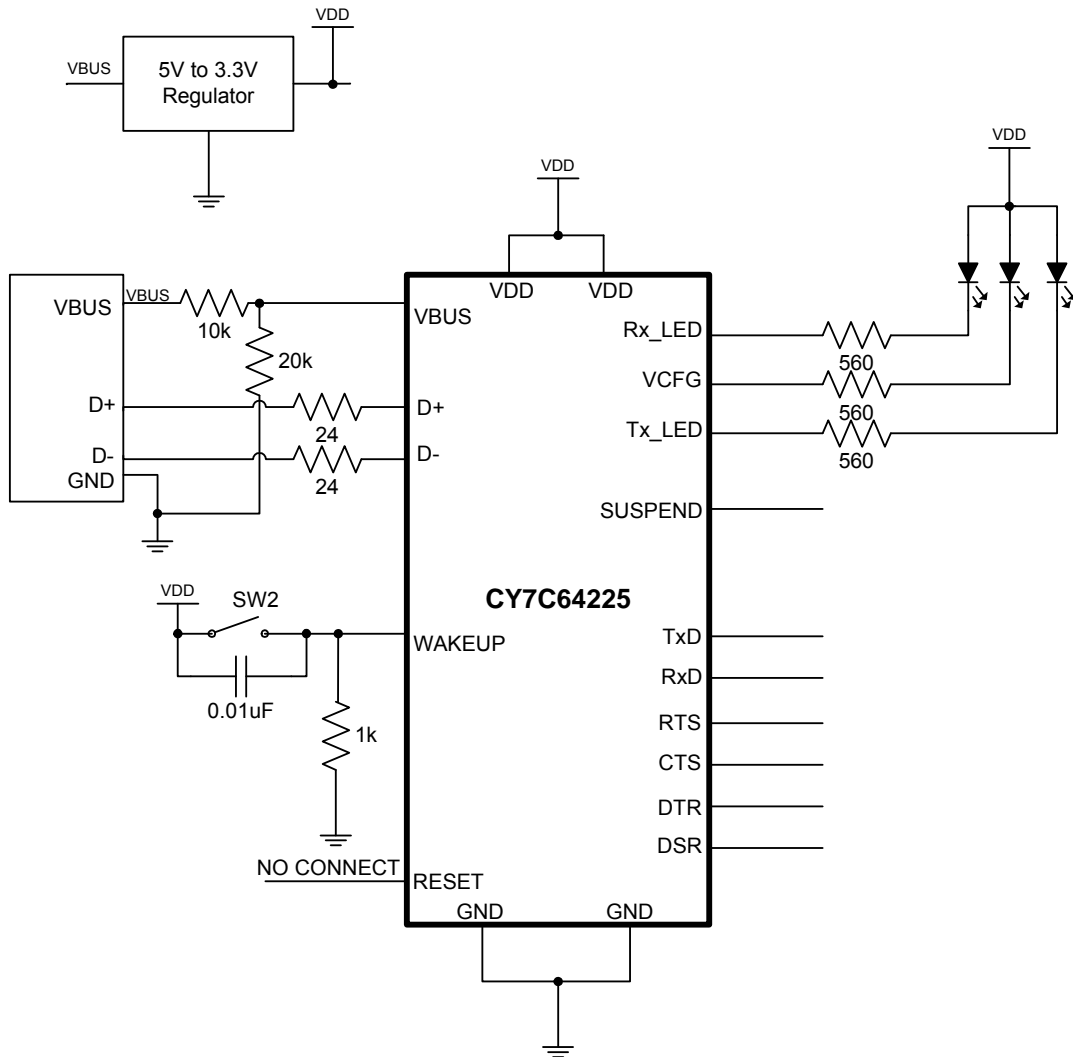
## Self Powered Design

Figure 5 illustrates the use of CY7C64225 in self powered mode operating at 3.3 V. VDD is obtained from an external power supply. As shown in Figure 5, a voltage divider circuit is used to provide 3.3 V from VBUS of USB port to VBUS pin of CY7C64225.

A self powered device can draw more current for its operation from external supply during USB active mode as well as suspend mode as this will not affect the operation of the USB.

**Figure 5. Self Powered Design (VDD = 3.3 V)**
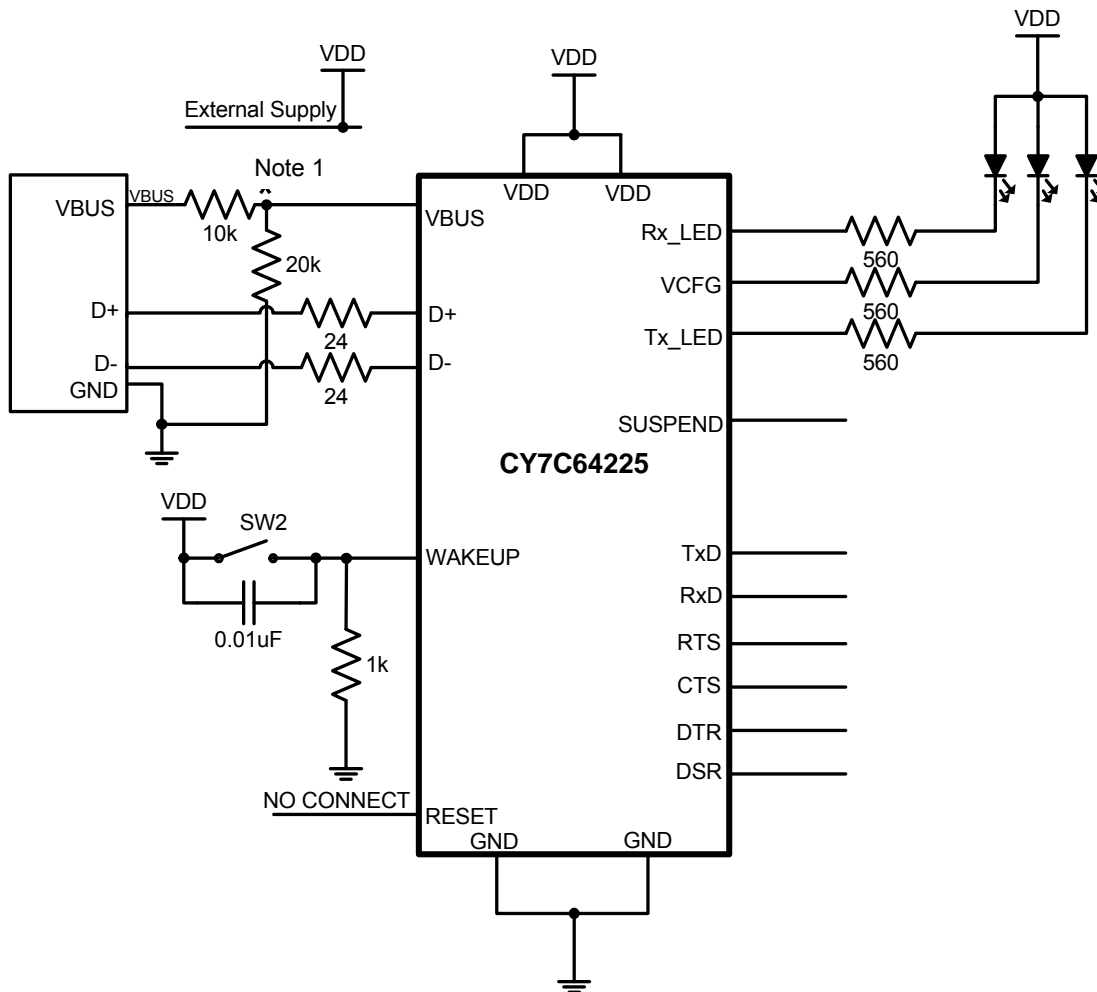


**Note**
1. Replace the voltage divider circuit (10K and 20K resistors) with 1K series resistor as shown in Figure 3, if 5 V is applied at VDD in this design.

## Application Diagram

### USB to RS-232 Converter

In this example the procedure of using the CY7C64225 as a USB to RS-232 converter is illustrated. In this application, a TTL to RS232 Level Converter IC is used on the serial UART interface of the CY7C74225 to convert the TTL levels of the CY7C64225 to RS-232 levels. RS-232 follows bipolar signaling i.e. the output signal toggles between negative and positive polarity. In RS-232, logic 1 is called Mark and is a –3 V input and logic 0 is called Space and is a +3 V input. The output voltage level of RS-232 is +/-5 V to +/-15 V. So there is not only an inversion in polarity but

also voltage level translation between the CY7C64225 UART interface and RS-232 signaling. So, RS-232 line driver/receiver is used for providing the necessary polarity inversion and level translation.

The connection between CY7C64225 and the RS-232 line driver/receiver is simple. The input lines (DSR, CTS and RX) of the UART interface should be connected to the logic outputs of the RS-232 line driver/receiver chip. The output lines (DTR, RTS and TX) of the UART interface should be connected to the logic inputs of the RS-232 line driver/receiver chip. The inverted, level-translated UART output will be sent through the line driver pins of the RS-232.
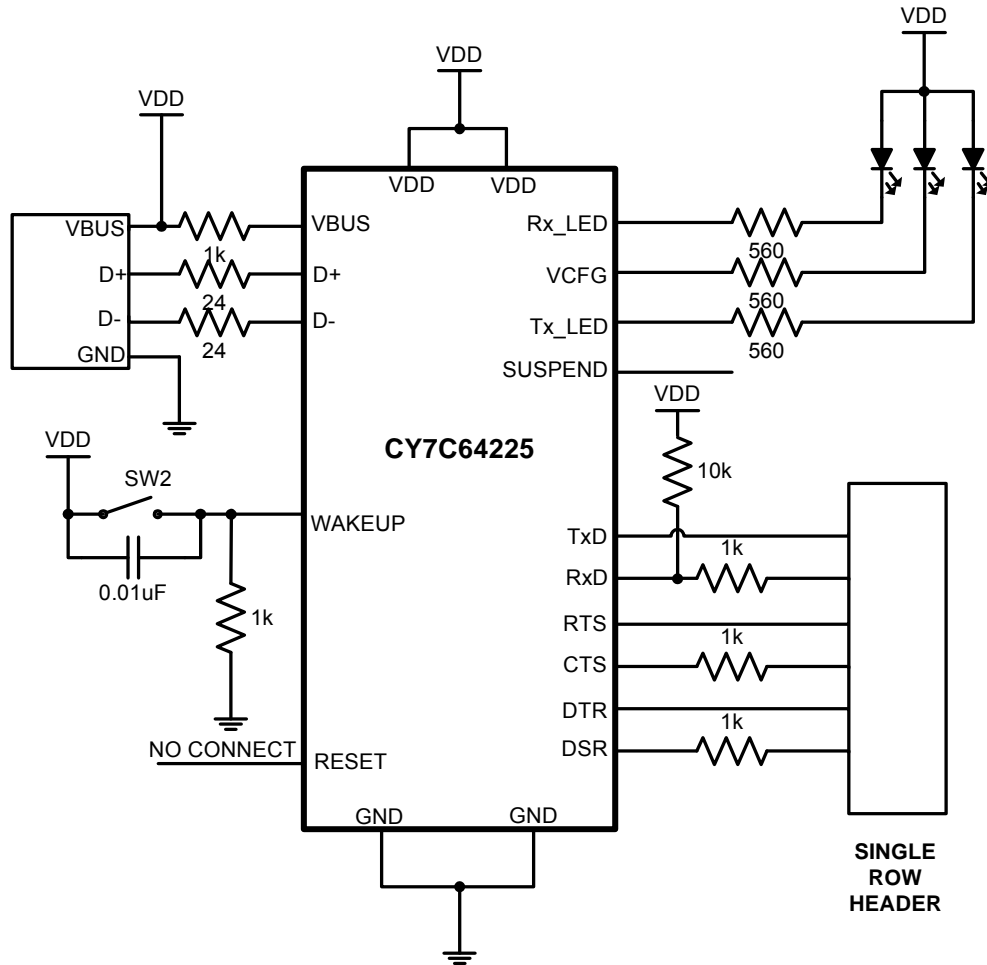
**Figure 6. USB to RS-232 Converter Configuration**
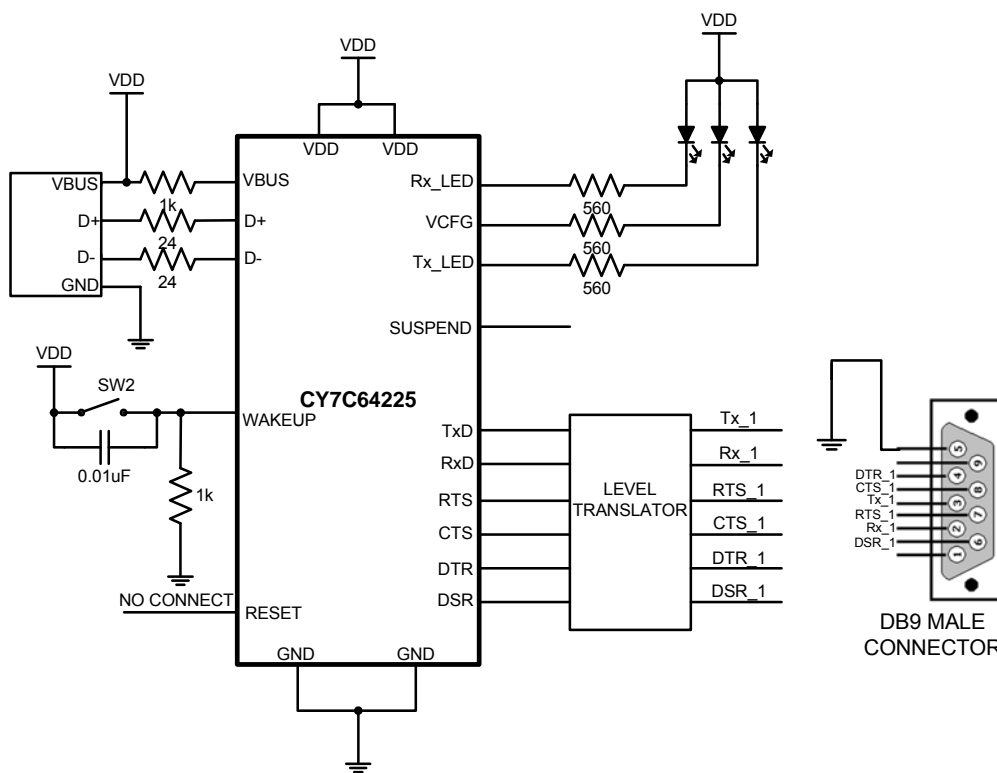
## USB to UART cable with TTL level UART signals

This example illustrates a USB to UART cable design with TTL Level UART Signals using CY7C64225. This design is based on bus powered configuration.
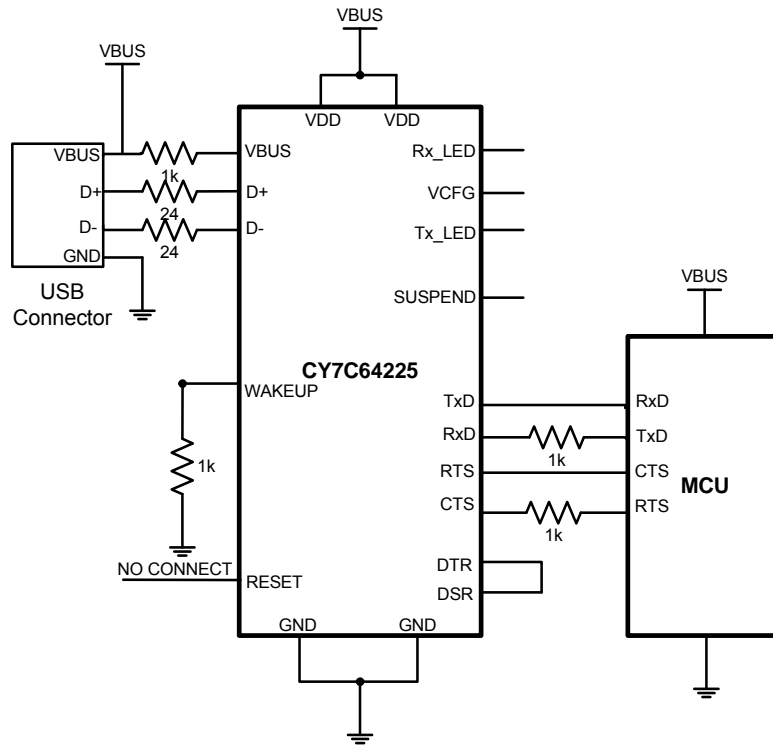
**Figure 7. USB to UART cable with TTL level UART signals**

## Interfacing CY7C64225 with Bus Powered Microcontroller

In this scenario both CY7C64225 and the microcontroller (MCU) are powered from VBUS. When the microcontroller and CY7C64225 controller are powered from different sources, 1K resistors are required on RXD and CTS lines of CY7C64225.

**Figure 8. Interfacing CY7C64225 with Bus Powered Microcontroller**

## Interfacing CY7C64225 with Self Powered Microcontroller

In this scenario CY7C64225 is powered from VBUS and the microcontroller is powered from an external supply.

If both CY7C64225 and the microcontroller (MCU) are operating at 3.3 V, connect a divider circuit to provide 3.3 V to VBUS pin of CY7C64225 from VBUS pin of USB port.

**Figure 9.  Interfacing CY7C64225 with Self Powered Microcontroller**
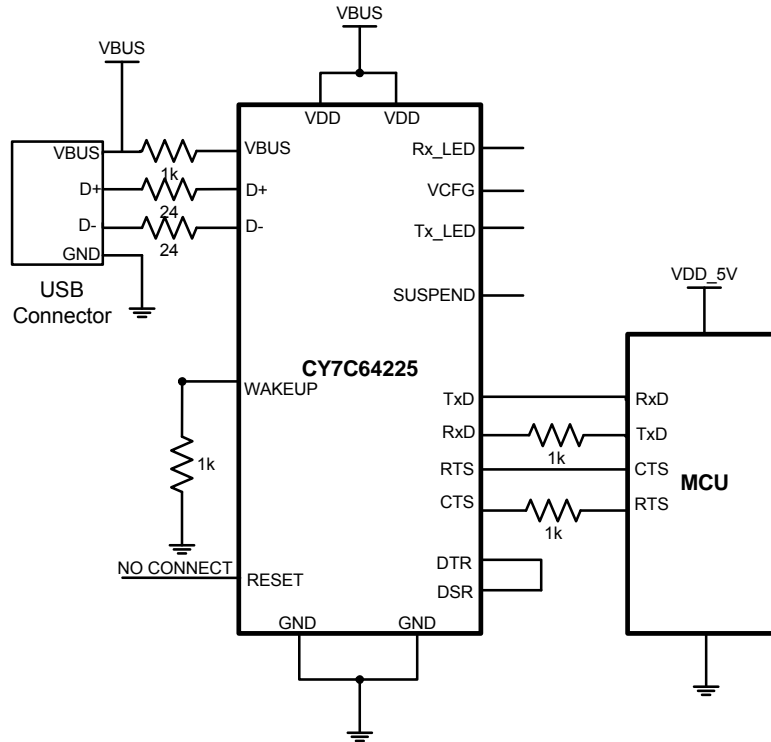
## Absolute Maximum Ratings

**Table 3. Absolute Maximum Ratings**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | –55 | – | +100 | °C | Higher storage temperatures reduces data retention time. |
| $T_{BAKETEMP}$ | Bake temperature | – | 125 | See package label | °C | – |
| $T_{BAKETIME}$ | Bake time | See package label | – | 72 | Hours | – |
| $T_A$ | Ambient temperature with power applied | 0 | – | +70 | °C | – |
| $V_{DD}$ | Supply voltage on $V_{DD}$ relative to $V_{SS}$ | –0.5 | – | +6.0 | V | – |
| $V_{IO}$ | DC input voltage | $V_{SS}$ – 0.5 | – | $V_{DD}$ + 0.5 | V | – |
| $I_{MIO}$ | Maximum current into any port pin | –25 | – | +50 | mA | – |
| ESD | Electrostatic discharge voltage | – | – | 2000 | V | Human body model ESD. |
| $Flash_{ENPB}$ | Flash endurance (per block) | 50,000[1] | – | – | – | Erase/write cycles per block. |
| $Flash_{ENT}$ | Flash endurance (total)[2] | 1,800,000 | – | – | – | Erase/write cycles. |
| $Flash_{DR}$ | Flash data retention | 10 | – | – | Years | – |

## Operating Temperature

**Table 4. Operating Temperature**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $T_{AC}$ | Commercial ambient temperature | 0 | – | +70 | °C | – |
| $T_J$ | Junction temperature | –40 | – | +100 | °C | The temperature rise from ambient to junction is package specific. See Thermal Impedance on page 17. The user must limit the power consumption to comply with this requirement. |

**Notes**
2. The 50,000 cycle Flash endurance per block will only be guaranteed if the Flash is operating within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.
3. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).

# DC Electrical Characteristics

## DC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and 0 °C $\leq T_A \leq$ 70 °C, or 3.15 V to 3.5 V and 0 °C $\leq T_A \leq$ 70 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

**Table 5. DC GPIO Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High output level | $V_{DD}$ – 1.0 | – | – | V | $I_{OH}$ = 10 mA, $V_{DD}$ = 4.75 to 5.25 V |
| $V_{OL}$ | Low output level | – | – | 0.75 | V | $I_{OL}$ = 25 mA, $V_{DD}$ = 4.75 to 5.25 V |
| $I_{OH}$ | High-level source current | 10 | – | – | mA | – |
| $I_{OL}$ | Low-level sink current | 25 | – | – | mA | – |
| $V_{IL}$ | Input low level | – | – | 0.8 | V | $V_{DD}$ = 3.15 to 5.25 V |
| $V_{IH}$ | Input high level | 2.1 | – | | V | $V_{DD}$ = 3.15 to 5.25 V |

## DC Full-Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges when the IMO is selected as system clock: 4.75 V to 5.25 V and 0 °C $\leq T_A \leq$ 70 °C, or 3.15 V to 3.5 V and 0 °C $\leq T_A \leq$ 70 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.
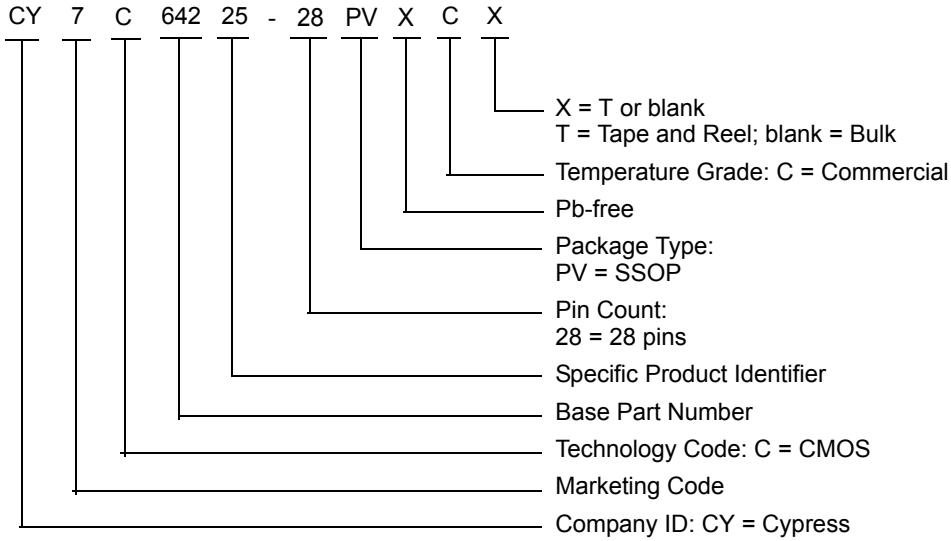
**Table 6. DC Full Speed (12 Mbps) USB Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| **USB Interface** | | | | | | |
| $V_{DI}$ | Differential input sensitivity | 0.2 | – | – | V | \| (D+) – (D–) \| |
| $V_{CM}$ | Differential input common mode range | 0.8 | – | 2.5 | V | – |
| $V_{SE}$ | Single-ended receiver threshold | 0.8 | – | 2.0 | V | – |
| $C_{IN}$ | Transceiver capacitance | – | – | 20 | pF | – |
| $I_{IO}$ | High Z state data line leakage | –10 | – | 10 | μA | 0 V < $V_{IN}$ < 3.3 V. |
| $R_{EXT}$ | External USB series resistor | 23 | – | 25 | Ω | In series with each USB pin. |
| $V_{UOH}$ | Static output high, driven | 2.8 | – | 3.6 | V | 15 kΩ ± 5% to ground. Internal pull-up enabled. |
| $V_{UOHI}$ | Static output high, idle | 2.7 | – | 3.6 | V | 15 kΩ ± 5% to ground. Internal pull-up enabled. |
| $V_{UOL}$ | Static output low | – | – | 0.3 | V | 15 kΩ ± 5% to ground. Internal pull-up enabled. |
| $Z_O$ | USB driver output impedance | 28 | – | 44 | Ω | Including $R_{EXT}$ resistor. |
| $V_{CRS}$ | D+/D– crossover voltage | 1.3 | – | 2.0 | V | – |

*DC Chip Level Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges when the IMO is selected as system clock: 4.75 V to 5.25 V and 0 °C $\leq T_A \leq$ 70 °C, or 3.15 V to 3.5 V and 0 °C $\leq T_A \leq$ 70 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

**Table 7. DC Chip-Level Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 3.0 | – | 5.25 | V | USB hardware is not functional when $V_{DD}$ is between 3.5 V to 4.35 V |
| $I_{DD5}$ | Supply current | – | 14 | 27 | mA | Conditions are $V_{DD}$ = 5.0 V, $T_A$ = 25 °C |
| $I_{DD3}$ | Supply current | – | 8 | 14 | mA | Conditions are $V_{DD}$ = 3.3 V, $T_A$ = 25 °C |
| $I_{SB}$ | Sleep (mode) current | – | 3 | 6.5 | μA | $V_{DD}$ = 3.3 V, 0 °C $\leq T_A \leq$ 55 °C |
| $I_{SBH}$ | Sleep (mode) current at high temperature. | – | 4 | 25 | μA | $V_{DD}$ = 3.3 V, 55 °C < $T_A \leq$ 70 °C |
| $I_{susp1}$ | USB suspend current | – | 225 | 285 | μA | For 5 V operating voltage range |
| $I_{susp2}$ | USB suspend current | – | 208 | 260 | μA | For 3.3 V operating voltage range |

## Ordering Information

| Package | Ordering Code | Temperature Range |
|---|---|---|
| 28-pin SSOP | CY7C64225-28PVXC | 0 °C to 70 °C |
| 28-pin SSOP (Tape and Reel) | CY7C64225-28PVXCT | 0 °C to 70 °C |

## Ordering Code Definitions

CY  7  C  642  25  -  28  PV  X  C  X

X = T or blank
T = Tape and Reel; blank = Bulk

Temperature Grade: C = Commercial

Pb-free

Package Type:
PV = SSOP

Pin Count:
28 = 28 pins

Specific Product Identifier

Base Part Number

Technology Code: C = CMOS

Marketing Code

Company ID: CY = Cypress

# Packaging Information

This section illustrates the package specification for the CY7C64225, along with the thermal impedance for the package.

## Package Diagrams

**Figure 10.  28-pin SSOP (210 Mils) O28.21 Package Outline, 51-85079**



51-85079 *F
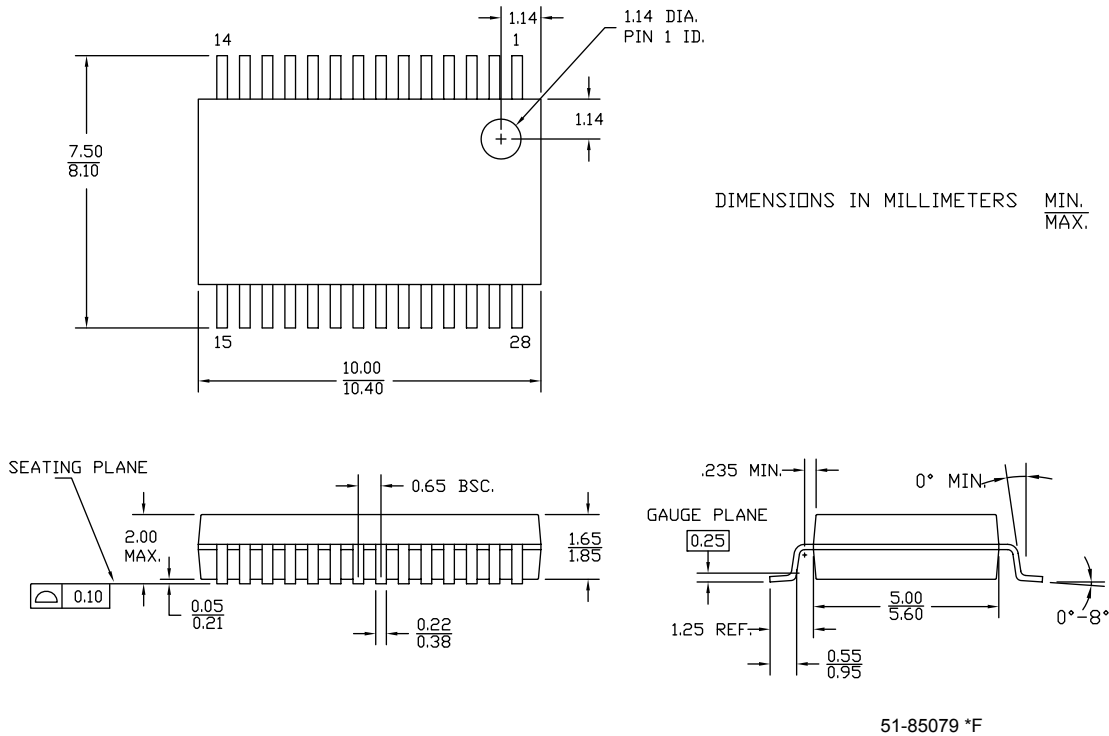
## Thermal Impedance

**Table 8.  Thermal Impedance for the Package**

| Package | Typical $\theta_{JA}$ |
|---|---|
| 28-pin SSOP | 96 °C/W |

**Note** Assumes 2-layer PCB

## Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

**Table 9.  Solder Reflow Peak Temperature**

| Package | Maximum Peak Temperature | Time at Maximum Peak Temperature |
|---|---|---|
| 28-pin SSOP | 260 °C | 20 s |

## Acronyms

The following table lists the acronyms used in this document.

| Acronym | Description |
|---------|-------------|
| DC | Direct Current |
| GPIO | General Purpose Input/Output |
| I/O | Input/Output |
| LED | Light Emitting Diode |
| PC | Personal Computer |
| SSOP | Shrink Small Outline Package |
| UART | Universal Asynchronous Receiver / Transmitter |
| USB | Universal Serial Bus |

## Reference Documents

USB 2.0 Specification

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| kΩ | kilohm |
| μA | microampere |
| mA | milliampere |
| Ω | ohm |
| % | percent |
| s | second |
| V | volt |
| W | watt |

## Glossary

| | |
|---|---|
| Asynchronous | A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal. |

Buffer
1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for I/O operations, into which data is read, or from which data is written.
2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device.
3. An amplifier used to lower the output impedance of a system.

Flash        Flash is a type of non-volatile memory used to store small amounts of data that must be saved when power is removed.

Reset        No Connect (NC)

$V_{DD}$        A name for a power net meaning "voltage drain" The most positive power supply signal. Usually 5 V or 3.3 V.

$V_{SS}$        A name for a power net meaning "voltage source" The most negative power supply signal.

Virtual COM Port   A USB virtual COM port is a software interface that enables applications to access a USB device as if it were a built-in serial port. Many USB virtual COM-port devices function as bridges that convert between USB and RS-232 or other asynchronous serial interfaces.

UART         A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.

## Document History Page

| Document Title: CY7C64225, USB-to-UART Bridge Controller Document Number: 001-76294 | | | | |
|---|---|---|---|---|

| Rev. | ECN No. | Submission Date | Orig. of Change | Description of Change |
|---|---|---|---|---|
| ** | 3533464 | 02/23/2012 | HBM | New data sheet. |
| *A | 3571321 | 05/15/2012 | AASI | Added Application Circuit Diagrams. Minor content edits to add clarity. Updated DC Chip Level Specifications and Table 6. |
| *B | 3931390 | 03/13/2013 | DTNK / NIKL | Updated Features.<br><br>Updated Figure 1 (CY7C64225 Block Diagram).<br><br>Updated Functional Description (Updated Introduction).<br><br>Renamed "Operational Details" as Functional Overview and updated the same section, also added sub-sections namely USB Interface, UART Controller, Regulator, Oscillator, Flash.<br><br>Updated Configurations (Updated Table 1).<br><br>Renamed "Driver" as Software and Driver Support and updated the same section.<br><br>Updated Application Circuits (Updated Bus Powered Design (Updated Figure 3), updated Bus Powered Design using External Regulator (Updated Figure 4), updated Self Powered Design (Updated description and Figure 5)).<br><br>Updated Application Diagram (Updated USB to RS-232 Converter (Updated Figure 6) and added sub-sections namely USB to UART cable with TTL level UART signals, Interfacing CY7C64225 with Bus Powered Microcontroller, Interfacing CY7C64225 with Self Powered Microcontroller).<br><br>Updated Absolute Maximum Ratings (Updated Table 3).<br><br>Replaced EEPROM with Flash in all instances across the document. |
| *C | 3979386 | 04/23/2013 | NIKL | Updated Functional Overview (Updated UART Controller (Updated UART Flow Control (Provided cross reference link to Figure 8))). |
| *D | 4296242 | 03/03/2014 | MVTA | Updated Configurations (Updated Table 1).<br><br>Updated to new template.<br><br>Completing Sunset Review. |
| *E | 4626645 | 01/16/2015 | MVTA | Added More Information. Updated Packaging Information: Updated Package Diagrams: spec 51-85079 – Changed revision from *E to *F. Updated to new template. Completing Sunset Review. |

## Document History Page *(continued)*

| Document Title: CY7C64225, USB-to-UART Bridge Controller | | | | |
|---|---|---|---|---|
| **Document Number: 001-76294** | | | | |
| **Rev.** | **ECN No.** | **Submission Date** | **Orig. of Change** | **Description of Change** |
| *F | 4952058 | 10/07/2015 | MVTA | Updated Functional Overview: <br> Updated Reset: <br> Updated description. <br><br> Updated Pin Configuration: <br> Updated 28-pin part pinout Description: <br> Updated Table 2: <br> Updated description of pin 6. <br><br> Updated Application Circuits: <br> Updated Bus Powered Design: <br> Updated Figure 3. <br> Updated Bus Powered Design using External Regulator: <br> Updated Figure 4. <br> Updated Self Powered Design: <br> Updated Figure 5. <br><br> Updated Application Diagram: <br> Updated USB to RS-232 Converter: <br> Updated Figure 6. <br> Updated USB to UART cable with TTL level UART signals: <br> Updated Figure 7. <br> Updated Interfacing CY7C64225 with Bus Powered Microcontroller: <br> Updated Figure 8. <br> Updated Interfacing CY7C64225 with Self Powered Microcontroller: <br> Updated Figure 9. <br><br> Updated Glossary: <br> Updated details corresponding to "Reset". |
| *G | 5687754 | 05/03/2017 | RUPA | Updated Cypress logo. <br> Updated Copyright information. |

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