# IXI858 / IXI859

## Gate Driver with VReg and Charge Pump Regulator

### Features:

- Logic Level Gate Drive Compatible
- 60mA Source / 120mA Sink Minimum Gate Drive
- 5.0V or 3.3V Voltage Regulator
- Charge Pump Regulator Stabilizes $V_{CC}$ Power Supply at 13V
- UVLO Protection

### Applications:

- µController based off-line applications
- Power Supply and Power Management
- Lighting Control

### General Description

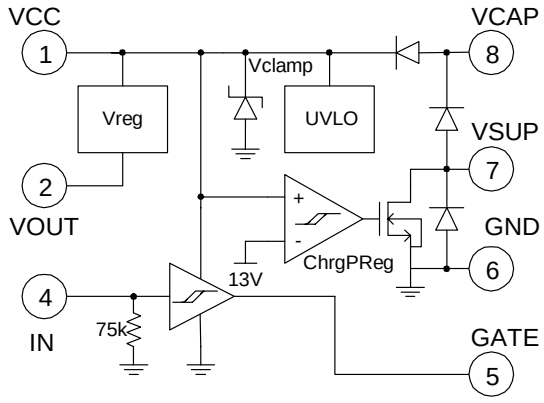
The IXI858 and IXI859 combine a power MOSFET driver, linear voltage regulator, and charge pump regulator for power supply generation in a single SOIC-8 package. The IXI858 features a 5.0V linear voltage regulator, and the IXI859 a 3.3V linear voltage regulator. These three power functions combined on the IXI858/859 target micro-controller based off-line applications.

The IXI858 and IXI859 are designed to operate over a temperature range of -25°C to +125°C, and are available in an 8 lead SOIC package.

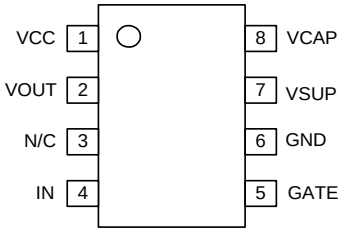
**ORDERING INFORMATION**

| Part No. | Description | Pack Quantity |
|---|---|---|
| IXI858S1 | 5.0V Version | 100 (Tube) |
| IXI858S1T/R | | 2500 (Tape & Reel) |
| IXI859S1 | 3.3V Version | 100 (Tube) |
| IXI859S1T/R | | 2500 (Tape & Reel) |

### Functional Block Diagram




### SOIC-8 Lead Configuration




8 - Lead SOIC

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### SOIC-8 Pin Description

| Pin No. | Pin Symbol | I/O | Description |
|---|---|---|---|
| 1 | VCC | Supply | Power input connects to a rectified high voltage source through a current limiting series resistor and filter capacitor to ground. Regulated 13 volt output when the charge pump is active. |
| 2 | VOUT | Output | Linear Regulator Output (IXI858 = 5.0V, IXI859 = 3.3V) |
| 3 | N/C | | No Connect |
| 4 | IN | Input | Gate Driver Input |
| 5 | GATE | Output | Gate Driver Output. Drives external power MOSFET. |
| 6 | GND | Ground | Ground Return |
| 7 | VSUP | I/O | Charge Pump Switch Input. Enables / disables the charge pump output. Requires a low ESR capacitor. |
| 8 | VCAP | I/O | Charge Pump Switch Output. Rectified charge pump output. Requires a low ESR capacitor. |

## Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | -0.4 | +20.0 | V |
| $V_{OUT}$ | Logic System Supply Voltage | -0.4 | +6.0 | V |
| $V_{IN}$ | Gate Input Voltage | -0.4 | +6.0 | V |
| $I_{SUP}$ | Continuous current into $V_{SUP}$ pin | -200 | +200 | mA |
| $I_{PEAK}$ | Peak Current into $V_{SUP}$ | -1 | +1 | A |
| $P_D$ | Power Dissipation | | 500 | mW |
| $T_J$ | Maximum Junction Temperature | | +150 | $^oC$ |
| $T_{STG}$ | Storage Temperature | -65 | +150 | $^oC$ |

*Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposure of the device to the absolute maximum ratings for an extended period may degrade the device and affect its reliability.*

### ESD Warning

ESD (electrostatic discharge) sensitive device. Although the IXI858 / IXI859 feature proprietary ESD protection circuitry, permanent damage may be sustained if subjected to high energy electrostatic discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## Operating Range

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | UVLO | +17 | V |
| $I_{SUP}$ | Continuous Current in $V_{SUP}$ Pin | 0 | 150 | mA |
| $I_{PEAK}$ | Peak Current in $V_{SUP}$ Pin ($t_P \leq 1\mu S$, $f \leq 150kHz$) | -750 | +750 | mA |

## Electrical Characteristics

$T_A$=25°C, $V_{CC}$=13V unless otherwise specified

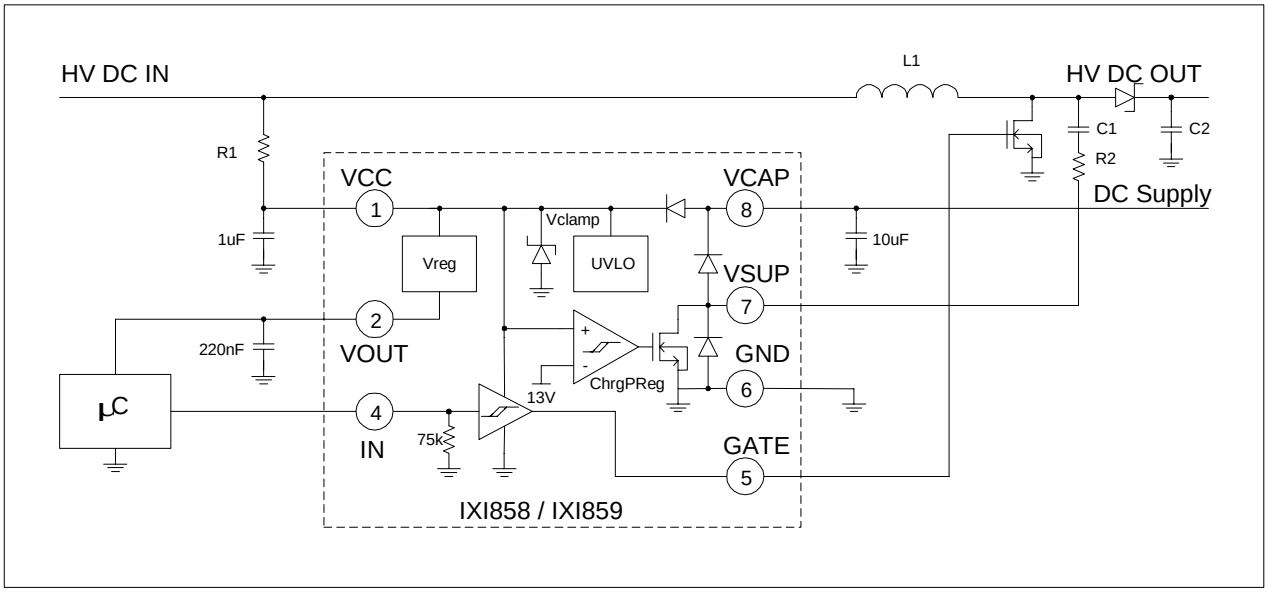
| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Supply (VCC)** | | | | | | |
| $I_{CC}$ | Supply Current | $V_{IN}$<1V, no load any pin | | 0.7 | 1.0 | mA |
| $I_{CC2}$ | Supply Current | 1nF GATE load, 300kHz IN signal | | 5 | | mA |
| $I_{STBY}$ | Standby Current | Undervoltage Detected | | 160 | | µA |
| $V_{CLAMP}$ | Clamp Voltage | $I_{CC}$ <5mA | | 17 | | V |
| **Input (IN)** | | | | | | |
| $V_{TON}$ | Turn-on Threshold Voltage | | | 1.95 | | V |
| $V_{TOFF}$ | Turn-off Threshold Voltage | | | 1.15 | | V |
| $V_H$ | Hysteresis | | 0.5 | | | V |
| $I_{INL}$ | Input Current Low | | | | 20 | µA |
| $I_{INH}$ | Input Current High | | | | 100 | µA |
| **Voltage Regulator (VOUT)** | | | | | | |
| $V_{OUT}$ | Voltage Reference | IXI859 $I_{OUT}$ = 10mA | 3.20 | 3.30 | 3.40 | V |
| | | IXI858 $I_{OUT}$ = 10mA | 4.85 | 5 | 5.15 | V |
| $Reg_{LOAD}$ | Load Regulation | $I_{OUT}$ change from 10mA to 25mA | | | 50 | mV |
| $I_{PEAK}$ | Peak Output Current | $V_{OUT}$ = 1V, IXI859 | 75 | | | mA |
| | | $V_{OUT}$ = 1V, IXI858 | 100 | | | |
| $dV_{OUT}$ | Temp Coefficient | $I_{OUT}$ = 10mA | | | 250 | ppm/°C |
| $C_{OUT}$ | Allowed Capacitive Load | $I_{OUT}$ = 10mA | 0.2 | | 2.2 | µF |
| $I_{LEAK}$ | Leakage current in UVLO state | $V_{OUT}$ = 1V | | | 10 | µA |
| $T_{STARTUP}$ | Startup Time ($V_{OUT}$ > 3.1V) | $C_{OUT}$ = 1uF | | | 0.1 | mS |
| $T_{SETTLE}$ | Settling Time | $C_{OUT}$ = 1 uF | | 2 | | mS |
| **Charge Pump Regulator** | | | | | | |
| $VCPR_{ON}$ | Turn-on Level | Measured at VCC | | 13.15 | | V |
| $VCPR_{OFF}$ | Turn-off Level | Measured at VCC | | 12.85 | | V |
| $VCPR_{HYS}$ | Hysteresis | | | 0.30 | | V |
| $VCPR_{FWD}$ | Forward Voltage | $I_{FWD}$ = 150mA (VSUP to VCAP) | | | 1.5 | V |

## Electrical Characteristics

$T_A$=25°C, $V_{CC}$=13V unless otherwise specified

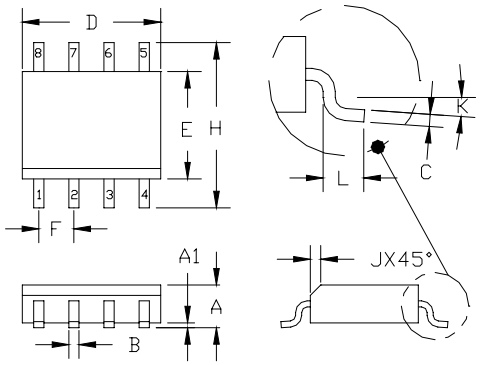
| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Gate Output (GATE)** | | | | | | |
| $V_{OL}$ | Output Low Voltage | $I_{GATE}$ = 10mA | | | 0.5 | V |
| $V_{OH}$ | Output High Voltage | $I_{GATE}$ = -10mA | 11 | | | V |
| $I_{SINK}$ | Output Sink Current | $V_{GATE}$ = 6V | 120 | | | mA |
| $I_{SRC}$ | Output Source Current | $V_{GATE}$ = 3V | 60 | | | mA |
| $V_{OL2}$ | Output Low Voltage in UVLO state | $V_{CC}$ = 6V, $I_{GATE}$ = 1mA | | 0.8 | | V |
| $t_{MINPW}$ | Minimum Output Pulse Width | $C_{GATE}$ = 10pF | 80 | | | nS |
| $t_{PD}$ | IN to GATE propagation delay | $C_{GATE}$ = 10pF | | 200 | | nS |
| **Under Voltage Lockout (VCC)** | | | | | | |
| $UVLO_H$ | UVLO Top Threshold Voltage | VCC Rising | | 14.1 | | V |
| $UVLO_L$ | UVLO Bottom Threshold Voltage | VCC Falling | | 8.2 | | V |
| $V_{HYS}$ | UVLO Hysteresis | | | 5.9 | | V |

## Typical Application Circuit



## Package Mechanical Data

8-LEAD SOIC




| DIMENSIONS (1) | | | | | |
|---|---|---|---|---|---|
| DIM. | INCH | | MM. | | NOTE |
| | MIN. | MAX. | MIN. | MAX. | |
| A | .0532 | .0688 | 1.35 | 1.75 | ---- |
| A1 | .0040 | .0098 | .10 | .25 | ---- |
| B | .013 | .020 | .33 | .51 | ---- |
| C | .0075 | .0098 | .19 | .25 | ---- |
| D | .1890 | .1968 | 4.80 | 5.00 | (2) |
| E | .1497 | .1574 | 3.80 | 4.00 | (2) |
| F | .050 BSC | | 1.27 BSC | | ---- |
| H | .2284 | .2440 | 5.80 | 6.20 | ---- |
| J | .0099 | .0196 | .25 | .50 | ---- |
| K | 0° | 8° | 0° | 8° | ---- |
| L | .016 | .050 | .40 | 1.27 | ---- |

3. MOLDED PACKAGE SHALL CONFORM TO JEDEC STANDARD CONFIGURATION MS-012 VARIATION AA.

(2) DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.

(1) CONTROLLING DIMENSIONS: MILLIMETERS.

NOTES: (UNLESS OTHERWISE SPECIFIED)

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