

GENERAL DESCRIPTION

The 843251I-14 is a 10Gb Ethernet Clock Generator. The 843251I-14 uses an 18pF parallel resonant crystal over the range of 22.4MHz - 27.2MHz. For Ethernet applications, a 25MHz crystal is used. The device has excellent <1ps phase jitter performance, over the 1.875MHz - 20MHz integration range. The 843251I-14 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space. NOTE: It is not recommended to overdrive the crystal input with an external clock.

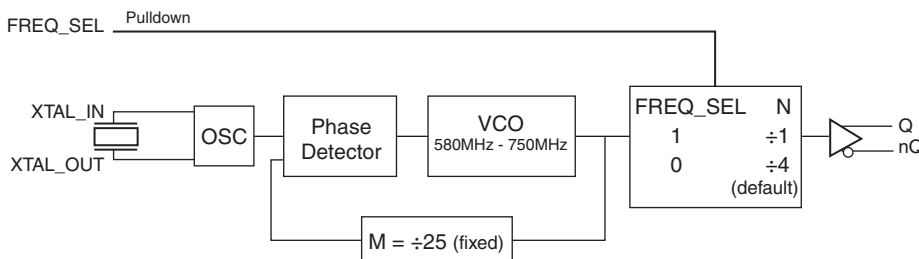
FEATURES

- One Differential LVPECL output
- Crystal oscillator interface, 18pF parallel resonant crystal (22.4MHz - 27.2MHz)
- Output frequency ranges:
FREQ_SEL = 1: 560MHz to 680MHz
FREQ_SEL = 0: 140MHz to 170MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.49ps (typical) @ 3.3V
- 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

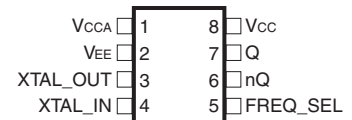
COMMON CONFIGURATION TABLE

| Crystal Frequency (MHz) | Inputs | | | Multiplication Value M/N | Output Frequency (MHz) |
|-------------------------|----------|----|---|--------------------------|------------------------|
| | FREQ_SEL | M | N | | |
| 25 | 1 | 25 | 1 | 25 | 625 |
| 26.67 | 1 | 25 | 1 | 25 | 666.67 |
| 25 | 0 | 25 | 4 | 6.25 | 156.25 (default) |

BLOCK DIAGRAM



PIN ASSIGNMENT



843251I-14

8-Lead TSSOP

4.4mm x 3.0mm x 0.925mm
package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|--------|----------------------|--------|----------|-----------------------------------------------------------------------------|
| 1 | V_{CCA} | Power | | Analog supply pin. |
| 2 | V_{EE} | Power | | Negative supply pin. |
| 3, 4 | XTAL_OUT, XTAL_IN | Input | | Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output. |
| 5 | FREQ_SEL | Input | Pulldown | Frequency select pin. LVCMOS/LVTTL interface levels. |
| 6, 7 | nQ, Q | Output | | Differential clock outputs. LVPECL interface levels. |
| 8 | V_{CC} | Power | | Core supply pin. |

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------|-------------------------|-----------------|---------|---------|---------|------------|
| C_{IN} | Input Capacitance | | | 4 | | pF |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | k Ω |

ABSOLUTE MAXIMUM RATINGS

| | |
|------------------------------------------|--------------------------|
| Supply Voltage, V_{CC} | 4.6V |
| Inputs, V_I | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, I_O | |
| Continuous Current | 50mA |
| Surge Current | 100mA |
| Package Thermal Impedance, θ_{JA} | 101.7°C/W (0 mps) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|-----------------|---------|----------|-------|
| V_{CC} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{CCA} | Analog Supply Voltage | | $V_{CC} - 0.15$ | 3.3 | V_{CC} | V |
| I_{CCA} | Analog Supply Current | | | | 15 | mA |
| I_{EE} | Power Supply Current | | | | 105 | mA |

TABLE 3B. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|-----------------|---------|----------|-------|
| V_{CC} | Core Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{CCA} | Analog Supply Voltage | | $V_{CC} - 0.12$ | 2.5 | V_{CC} | V |
| I_{CCA} | Analog Supply Current | | | | 12 | mA |
| I_{EE} | Power Supply Current | | | | 95 | mA |

TABLE 3C. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|-----------------------------------------------|---------|---------|----------------|---------------|
| V_{IH} | Input High Voltage | $V_{CC} = 3.3V$ | 2 | | $V_{CC} + 0.3$ | V |
| | | $V_{CC} = 2.5V$ | 1.7 | | $V_{CC} + 0.3$ | V |
| V_{IL} | Input Low Voltage | $V_{CC} = 3.3V$ | -0.3 | | 0.8 | V |
| | | $V_{CC} = 2.5V$ | -0.3 | | 0.7 | V |
| I_{IH} | Input High Current | $V_{CC} = V_{IN} = 3.465V$ or $2.625V$ | | | 150 | μA |
| I_{IL} | Input Low Current | $V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$ | -5 | | | μA |

TABLE 3D. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------------|-----------------|----------------|---------|----------------|-------|
| V_{OH} | Output High Voltage; NOTE 1 | | $V_{CC} - 1.4$ | | $V_{CC} - 0.9$ | V |
| V_{OL} | Output Low Voltage; NOTE 1 | | $V_{CC} - 2.0$ | | $V_{CC} - 1.7$ | V |
| V_{SWING} | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CC} - 2V$.

TABLE 4. CRYSTAL CHARACTERISTICS

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------------|-------------|---------|---------|---------------|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | 22.4 | | 27.2 | MHz |
| Equivalent Series Resistance (ESR) | | | | 40 | Ω |
| Shunt Capacitance | | | | 7 | pF |
| Drive Level | | | | 300 | μW |

NOTE: It is not recommended to overdrive the crystal input with an external clock.

TABLE 5A. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|---------------------------------------|----------------------------------------------------|---------|---------|---------|-------|
| f_{OUT} | Output Frequency | F_SEL = 0 | 140 | | 170 | MHz |
| | | F_SEL = 1 | 560 | | 680 | MHz |
| $t_{jit}(\emptyset)$ | RMS Phase Jitter (Random); NOTE 1 | 156.25MHz @ Integration Range: 1.875MHz - 20MHz | | 0.49 | | ps |
| | | 625MHz @ Integration Range: 1.875MHz - 20MHz | | 0.40 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 150 | | 500 | ps |
| odc | Output Duty Cycle | F_SEL = 0 | 48 | | 52 | % |
| | | F_SEL = 1 | 45 | | 55 | % |

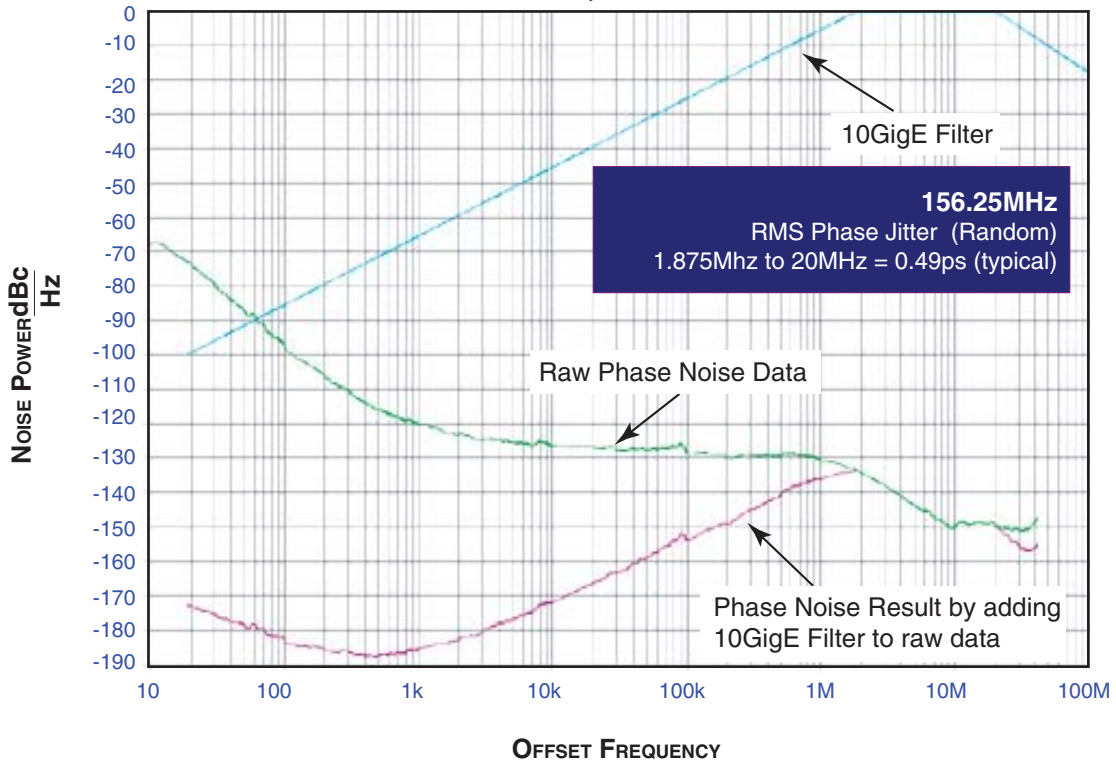
NOTE 1: Please refer to the Phase Noise Plots following this section.

TABLE 5B. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

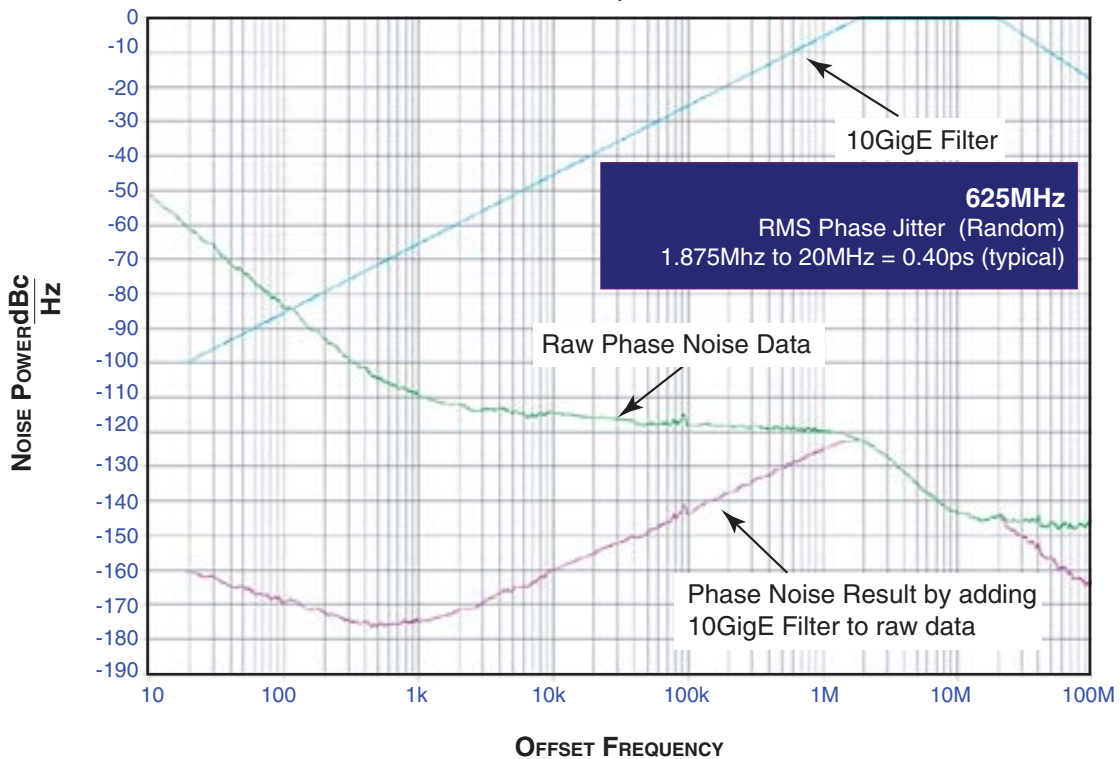
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|---------------------------------------|----------------------------------------------------|---------|---------|---------|-------|
| f_{OUT} | Output Frequency | F_SEL = 0 | 140 | | 170 | MHz |
| | | F_SEL = 1 | 560 | | 680 | MHz |
| $t_{jit}(\emptyset)$ | RMS Phase Jitter (Random); NOTE 1 | 156.25MHz @ Integration Range: 1.875MHz - 20MHz | | 0.52 | | ps |
| | | 625MHz @ Integration Range: 1.875MHz - 20MHz | | 0.44 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 150 | | 500 | ps |
| odc | Output Duty Cycle | F_SEL = 0 | 48 | | 52 | % |
| | | F_SEL = 1 | 45 | | 55 | % |

NOTE 1: Please refer to the Phase Noise Plots following this section.

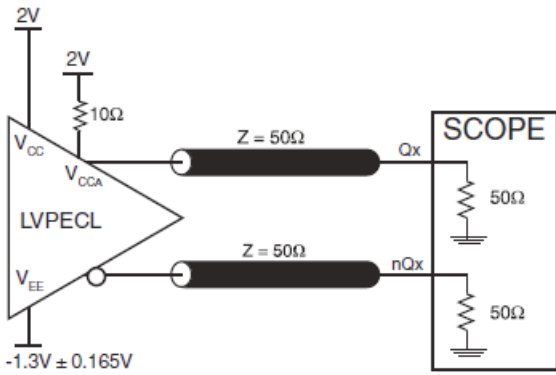
TYPICAL PHASE NOISE, 156.25MHz @ 3.3V



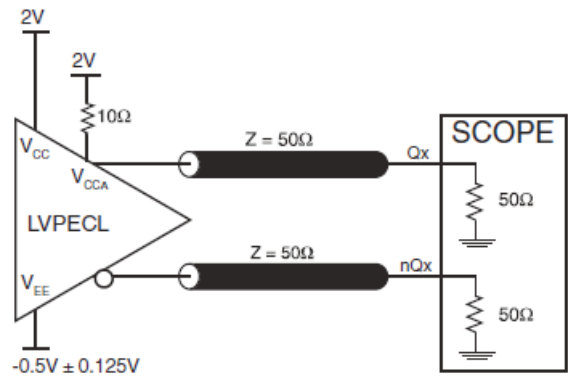
TYPICAL PHASE NOISE, 625MHz @ 3.3V



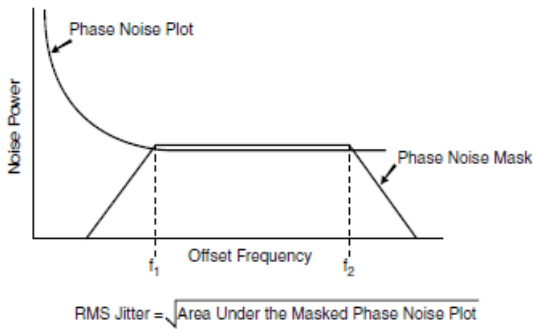
PARAMETER MEASUREMENT INFORMATION



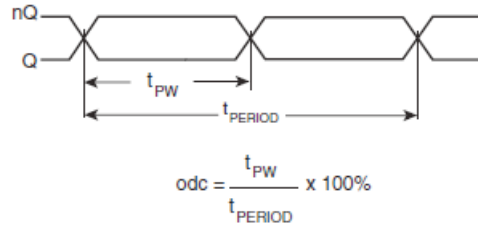
LVPECL 3.3V OUTPUT LOAD AC TEST CIRCUIT



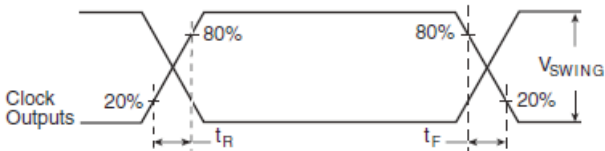
LVPECL 2.5V OUTPUT LOAD AC TEST CIRCUIT



RMS PHASE JITTER



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 8432511-14 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} and V_{CCA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a $10\mu\text{F}$ and a $.01\mu\text{F}$ bypass capacitor should be connected to each V_{CCA} pin.

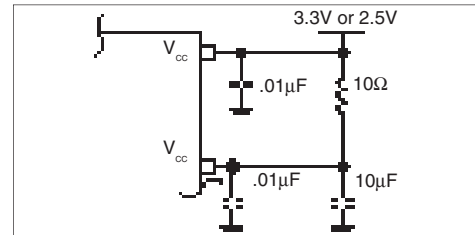


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The 8432511-14 has been characterized with 18pF parallel resonant crystals. The capacitor values, $C1$ and $C2$, shown in *Figure 2* below were determined using a 25MHz , 18pF parallel

resonant crystal and were chosen to minimize the ppm error. The optimum $C1$ and $C2$ values can be slightly adjusted for different board layouts.

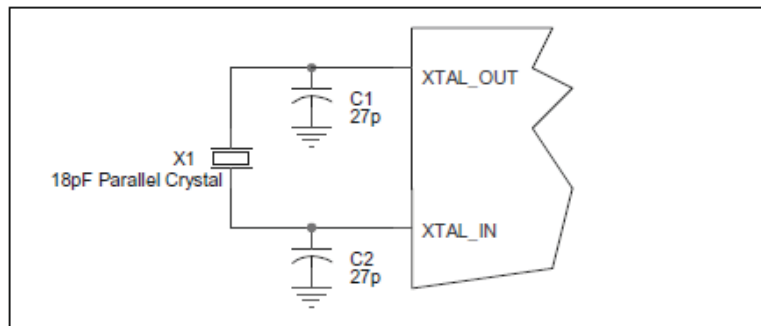


Figure 2. CRYSTAL INPUT INTERFACE

TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission

lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

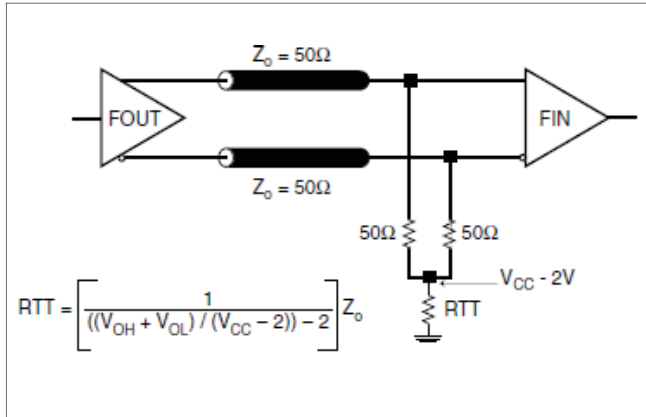


FIGURE 4A. LVPECL OUTPUT TERMINATION

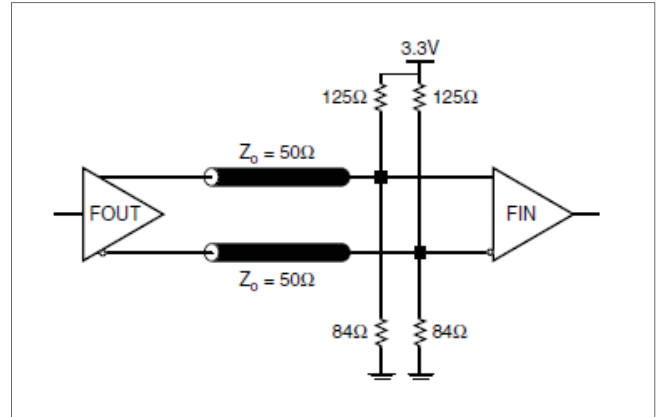


FIGURE 4B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 5A and Figure 5B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{cc} - 2V$. For $V_{cc} = 2.5V$, the $V_{cc} - 2V$ is very close to ground

level. The R3 in Figure 5B can be eliminated and the termination is shown in Figure 5C.

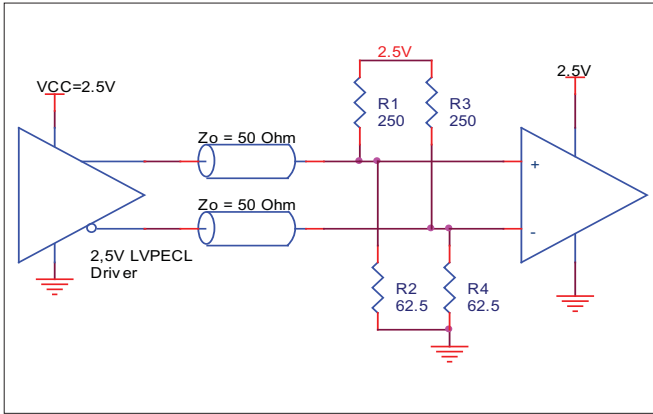


FIGURE 5A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

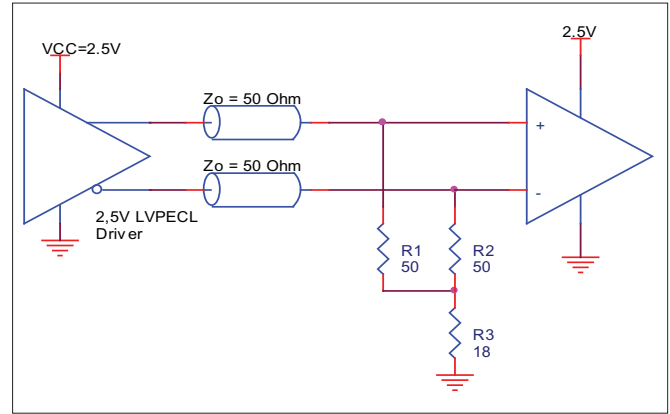


FIGURE 5B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

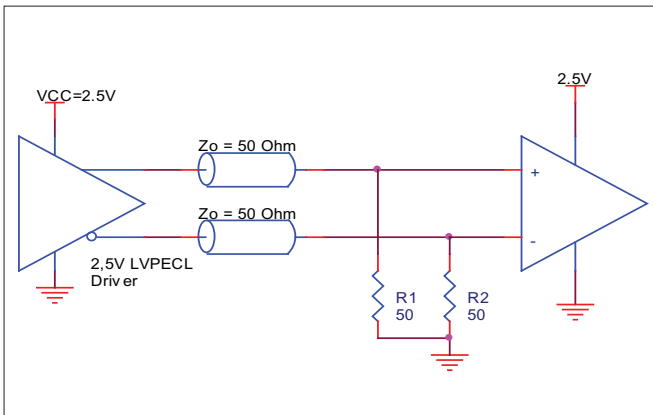


FIGURE 5C. 2.5V LVPECL TERMINATION EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 8432511-14. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8432511-14 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.465V * 105mA = 363.8mW$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**

Total Power_{MAX} (3.465V, with all outputs switching) = $363.8mW + 30mW = 393.8mW$

2. Junction Temperature.

Junction temperature, T_j, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_{total} = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 90.5°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$85^\circ C + 0.394W * 90.5^\circ C/W = 120.6^\circ C$. This is below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 8-PIN TSSOP, FORCED CONVECTION

| θ_{JA} by Velocity (Meter per Second) | | | |
|----------------------------------------------|-----------|----------|----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 101.7°C/W | 90.5°C/W | 89.8°C/W |

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in Figure 6.

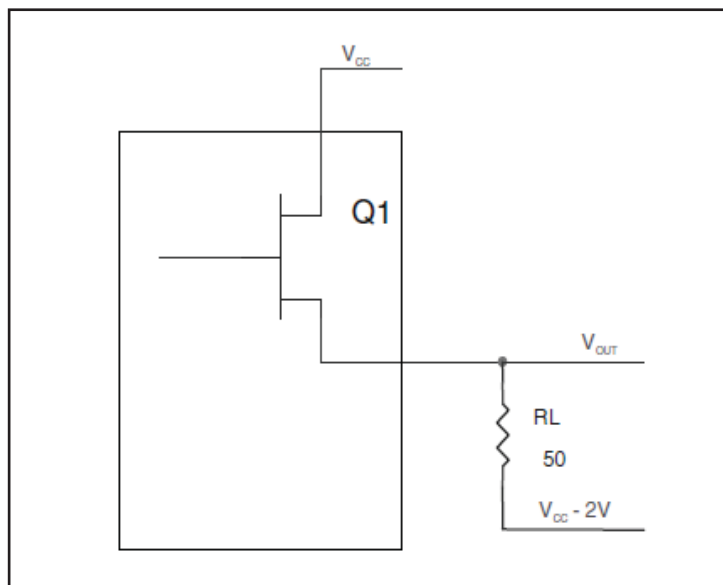


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CC_MAX} - 0.9V$

$$(V_{CC_MAX} - V_{OH_MAX}) = 0.9V$$

- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CC_MAX} - 1.7V$

$$(V_{CC_MAX} - V_{OL_MAX}) = 1.7V$$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = 30mW$$

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

| θ_{JA} by Velocity (Meters per Second) | | | |
|-----------------------------------------------|-----------|----------|----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 101.7°C/W | 90.5°C/W | 89.8°C/W |

TRANSISTOR COUNT

The transistor count for 843251I-14 is: 2377

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

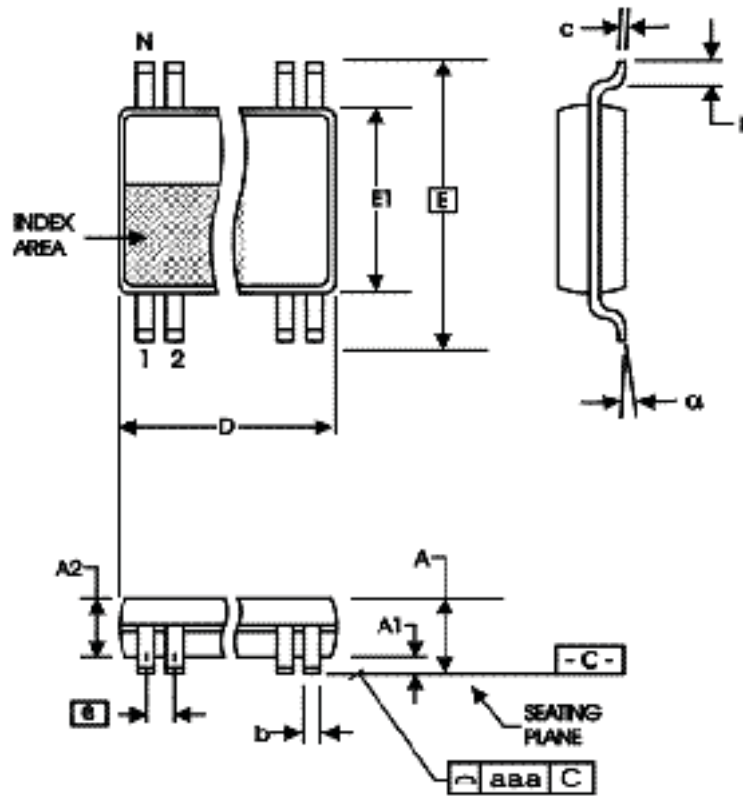


TABLE 8. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|----------|-------------|---------|
| | Minimum | Maximum |
| N | 8 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 2.90 | 3.10 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|--------------------|---------|--------------------------|--------------------|---------------|
| ICS843251AGI-14LF | AI14L | 8 Lead "Lead-Free" TSSOP | tube | -40°C to 85°C |
| ICS843251AGI-14LFT | AI14L | 8 Lead "Lead-Free" TSSOP | tape & reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

| REVISION HISTORY SHEET | | | | |
|------------------------|-------|-----------------------------------------------------|------------------------------------------------------------------------------|----------|
| Rev | Table | Page | Description of Change | Date |
| A | T4 | 1 | Deleted HiPerClockS references. | 10/22/12 |
| | | 4 | Crystal Characteristics Table - added note. | |
| | 8 | Deleted application note, LVCMOS to XTAL Interface. | | |
| | 14 | Deleted quantity from tape and reel | | |
| A | T9 | 14 | Ordering Information - removed leaded devices. Updated data sheet format. | 10/23/15 |
| | | | | |

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