TEXAS INSTRUMENTS

# TPS75525EVM

## Voltage Regulator Evaluation Module

# User's Guide

November 2001

Power Management Products Low Power

SLVU062

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## DYNAMIC WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.8–5.5 V and the output current range of 0 mA to 5 mA.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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# Preface

## About This Manual

This user's guide describes the TPS75525EVM LDO regulator evaluation module. Each EVM contains a SLVP190 test board with one TPS75525KTT 5-A, 2.5-V linear regulator and one TPS75733KTT 3-A, 3.3-V linear regulator as well as supporting passive components. The EVM provides a convenient method of evaluating the performance of the TPS755xx and TPS757xx linear regulator families.

## How to Use This Manual

- Chapter 1—Introduction
- Chapter 2—EVM Test Setup
- Chapter 3—Test Results

## Trademarks

PowerFlex is a trademark of Texas Instruments.

## Related Documentation From Texas Instruments

- TPS755xx data sheet (literature number SLVS293)
- TPS757xx data sheet (literature number SLVS306)

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Chapter 1

# Introduction

This user's guide describes the TPS75525EVM LDO regulator evaluation module. Each EVM contains an SLVP190 test board with one TPS75525KTT 5-A, 2.5-V linear regulator and one TPS75733KTT 3-A, 3.3-V linear regulator, as well as supporting passive components. Although other configurations are possible through jumper selection, this EVM is configured to perform power-up sequencing, i.e., the 2.5-V regulator powers up before the 3.3-V regulator. This type of power-up sequencing is recommended when powering the 2.5-V core voltage and 3.3-V I/O voltage power supply rails in many DSP, microcontroller, and FPGA applications.

**Topic** **Page**

## 1.1 TPS755xx and TPS757xx Families of LDO Regulators

Like all LDO linear regulators, the TPS755xx and TPS757xx families of LDO regulators use a series pass element and feedback network, including an error amplifier and voltage reference, to provide a regulated output voltage from a slightly higher, possibly varying input voltage. The distinguishing characteristics of these regulators include high current output, low dropout and integrated power good. Specific capabilities of these regulators include:

- 5-A (TPS755xx) and 3-A (TPS757xx) maximum load current
- Both families are available in 1.5-V, 1.8-V, 2.5-V, 3.3-V, and adjustable with active low enable ($\overline{EN}$)
- Very low dropout voltage (250 mV at 5 A for the TPS75533)
- Active low power good ($\overline{PG}$) signal
- Available in either TO-220 or TO-263 packages for maximum power dissipation capability

## 1.2 EVM Design Strategy

Power-up sequencing is recommended when powering the core and I/O power supply rails in many DSP, microcontroller, and FPGA applications. Designing a system without proper sequencing can result in two types of faults. The first type represents a threat to the long-term reliability of the dual voltage device. The second can cause faults in and possible permanent damage to the I/O ports of the processor or the supporting system devices. Through jumper selections, the two regulators on this EVM have been configured to perform power-up sequencing. The active low power good ($\overline{PG}$) output of the TPS75525 2.5-V regulator has been tied to the active low enable ($\overline{EN}$) input of the TPS75733 3.3-V regulator. Therefore, the 3.3-V regulator will not be enabled until the 2.5-V regulator is within approximately 90% of its regulated voltage. A high current Schottky diode has been placed between the two voltage rails so that the 2.5-V rail will pull the 3.3-V rail up to 2.5 V until the 3.3-V regulator is enabled.

The EVM board can be used to perform other tests. The jumpers can be changed as indicated in Table 1–1 so that each regulator can be separately enabled and/or disabled. U1 and U2 can be replaced with any of the TPS755xx, TPS756xx, TPS757xx, TPS758xx, and TPS759xx fixed regulator options. As per Table 1–1, changing JP4 causes resistors R4 and R5 to become usable and U1 can be replaced with one of TPS75x01 adjustable voltage option regulators. Note that diode D1 may need to be removed if the output voltage of U1 is larger than the output voltage of U3 by more than 0.3 V.

The board has been designed to accommodate either the TO-220 (KC) and TO-263 PowerFlex™ (KTT) packages, but not both at the same time. The TO-263 packages have been installed on this EVM and soldered to the ground plane area on both the top and bottom layers of the board for heat sinking. Refer to the TPS755xx and TPS757xx data sheets for the maximum power dissipation capabilities of the TO-263 packages. If the TO-263 packages are replaced with TO-220 packages, appropriate heat sinks will have to be attached to the TO-220 packages to achieve comparable power dissipation.

## 1.3 Adjustment by Jumper and Switch

The schematic for the EVM is provided in Figure 1–1.

*Table 1–1. TPS75525EVM Jumper Explanations*

| Jumper or Switch | Status | Description |
|---|---|---|
| JP1 | Open (Default) | Pin 3 of JP3 is pulled high to VIN. If pins 2–3 of JP3 are shorted, then U2 $\overline{EN}$ is pulled high to $V_I$ thereby disabling U2. If pins 1–2 of JP3 are shorted, JP1 has no effect. |
| | Short | Pin 3 of JP3 is tied low to GND. If pins 2–3 of JP3 are shorted, then U2 $\overline{EN}$ is tied low to GND thereby enabling U2. If pins 1–2 of JP3 are shorted, JP1 has no effect. |
| JP2 | Open | U1 $\overline{EN}$ pulled high to $V_I$ thereby disabling U1. |
| | Short (Default) | U1 $\overline{EN}$ tied low to GND thereby enabling U1. |
| JP3 | Short 1-2 (Default) | $\overline{EN}$ of U2 is tied to pin 1 of JP4. If pins 1–2 of JP4 are shorted, then U1 $\overline{PG}$ drives U2 $\overline{EN}$ for power up sequencing. If pins 2–3 of JP4 are shorted, then changing JP3 has no effect. |
| | Short 2–3 | U2 $\overline{EN}$ independent of U1. U2 status is controlled by JP1 |
| JP4 | Short 1–2 (Default) | $\overline{PG}$ of U1 is tied to pin 1 of JP3. If pins 1–2 of JP3 are shorted, then U1 $\overline{PG}$ drives U2 $\overline{EN}$ for power up sequencing. If pins 2–3 of JP4 are shorted, then changing JP3 has no effect. |
| | Short 2–3 | U1 can accommodate the TPS75x01 adjustable option regulator using resistors R4 and R5. |

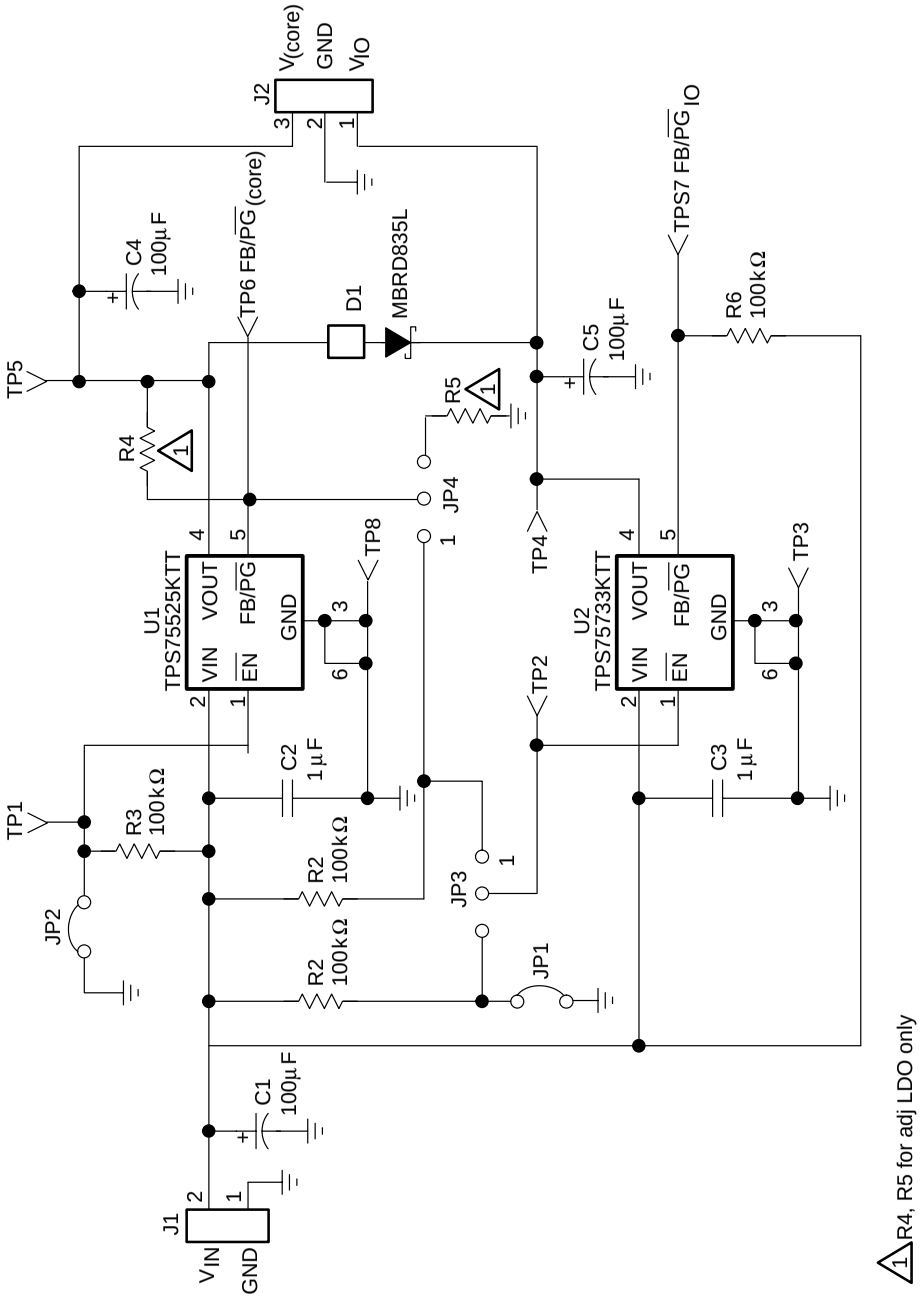
*Table 1–2. TPS75525EVM Recommended Jumper Settings*

| JP1 | JP2 | JP3 | JP4 | Description |
|---|---|---|---|---|
| Open | Open | Short 1–2 | Short 1–2 | Recommended setup for power up sequencing when JP2 is connected to a function generator. |
| Open | Short | Short 1–2 | Short 1–2 | |
| Short | Short | Short 2–3 | Short 1–2 | Recommended setup for dc operation. |
| Short | Short | Short 2–3 | Short 2–3 | Recommended setup when replacing U2 with TPS75x01 adjustable option. |

## 1.4 Schematic

Figure 1-1 shows the TPS75525EVM schematic diagram.

*Figure 1–1. TPS75525EVM Schematic Diagram*



## 1.5 Bill of Materials

Table 1–3 lists materials required for the TPS75525 EVMs.

*Table 1–3. TPS75525EVM Bill of Materials*

| Qty | Ref Des | Description | Size | MFR | Part Number |
|---|---|---|---|---|---|
| 3 | C1, C4, C5 | Capacitor, tantalum, 100 μF, 10 V, 20% | 7343 (D) | Sprague | 293D107X0010D2T |
| 2 | C2, C3 | Capacitor, ceramic, 1-μF, 16 V, X7R, 10% | 805 | Murata | GRM40X7R105K16 |
| 1 | D1 | Diode, Schottky, 8.0-A, 35 V | TO-252AA | On Semi | MBRD835L |
| 1 | J1 | Terminal block, 2 pin, 15 A, 5,1 mm | 148830 | OST | ED1609 |
| 1 | J2 | Terminal block, 3 pin, 15 A, 5,1 mm | 221430 | OST | ED1610 |
| 2 | JP1, JP2 | Header, 2 pin, 100 mil spacing, (36-pin strip) | 0.100 × 2 | Sullins | PTC36SAAN |
| 2 | JP3, JP4 | Header, 3 pin, 100 mil spacing, (36-pin strip) | 0.100 × 3 | Sullins | PTC36SAAN |
| 4 | R1, R2, R3, R6 | Resistor, chip, 100 kΩ, 1/10 W, 1% | 805 | Std | Std |
| 0 | R4, R5 | | 805 | — | — |
| 6 | TP1, TP2, TP4 – TP7 | Test point, red, 1 mm | 0.038 | Farnell | 240–345 |
| 2 | TP3, TP8 | Test point, black, 1 mm | 0.038 | Farnell | 240–333 |
| 1 | U1 | IC, voltage regulator, LDO, 2.5 V, 5 A | 267750 | TI | TPS75525KTT |
| 1 | U2 | IC, voltage regulator, LDO, 3.3 V, 5 A | 267750 | TI | TPS75733KTT |
| 4 | — | Shunt, 100 mil, black | 0.1 | 3M | 929950–00 |
| 1 | — | PCB, 2.7 in × 2.59 in × 0.062 in | | Any | SLVP190 |

## 1.6 Board Layout

Figures 1–2 and 1-3 show the board layout for the TPS75525EVM

*Figure 1–2. Top Layer*

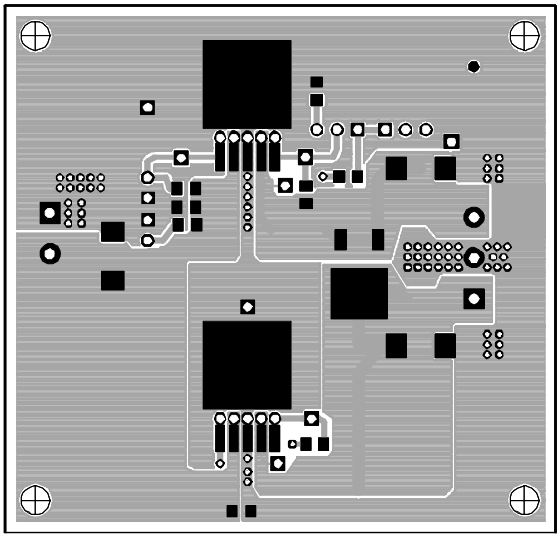


*Figure 1–3. Bottom Layer (top view)*

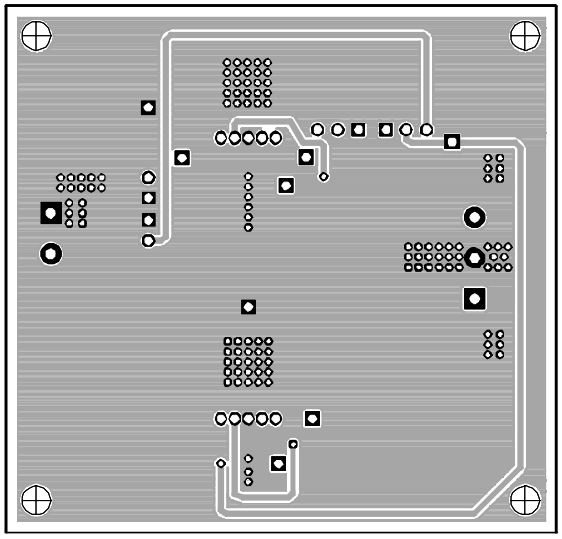
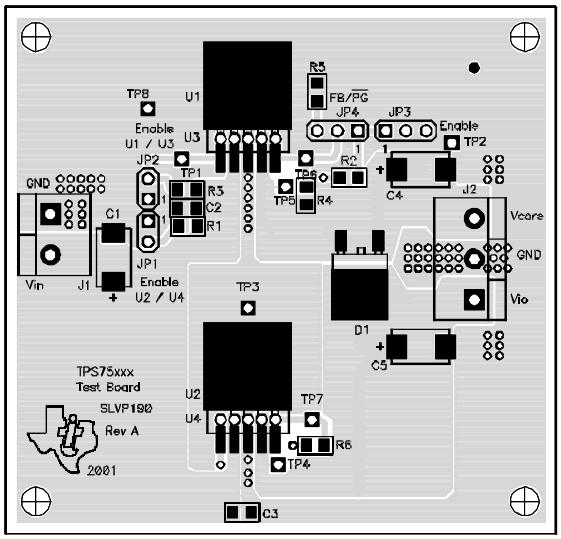


*Figure 1–4. Assembly Drawing*

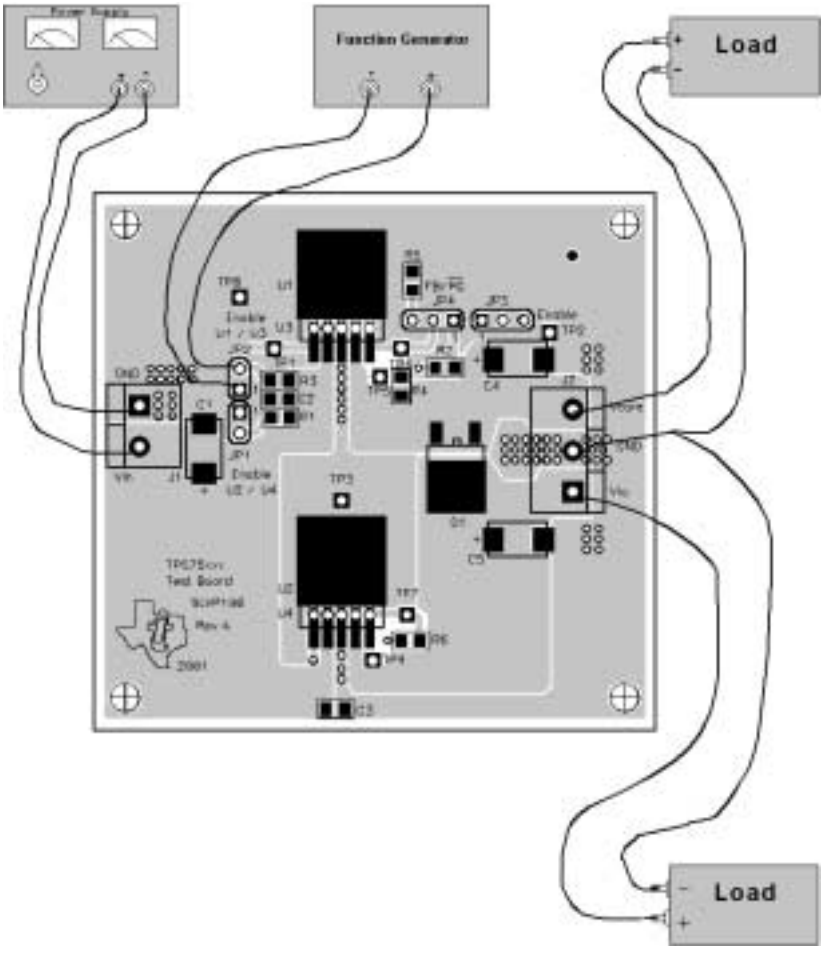


Chapter 2

# EVM Test Setup

This chapter provides recommended test equipment and procedures for evaluating the power up sequencing capability of the TPS75525EVM. Figure 2–1 shows the test setup.

*Figure 2–1. Recommended TPS75525EVM Test Setup*



The following is a list of recommended equipment.

- ❑ Power supply with 5-V and 8-A current limit connected to $V_I$ and GND.
- ❑ Oscilloscope set to 100 µs/div and triggering off the falling edge of channel 1.
  - Channel 1—set to 5 V/div, position at 2 V, and connected to TP1
  - Channel 2—set to 1 V/div, position at –1 V, measure high or max, and connected to TP5 (U1)
  - Channel 3—set to 1 V/div, position at –4 V, measure high or max, and connected to TP4 (U2)
- ❑ Set the function generator to 1 Hz, 25% duty cycle, 0-V to 5-V amplitude (may require a setting of 2.5-V square wave and 2.5-V dc offset) square wave and connected across JP2 (per the schematic in Figure 1–1).
- ❑ A variable resistance or electronic load capable of dissipating 10 W on J2 between $V_{(CORE)}$ and GND and a similar variable resistance, or an electronic load capable of dissipating 10 W on J2 between $V_{IO}$ and GND.

The following steps are recommended for evaluating the power-up sequencing of the two devices:

1) Turn on the power supply, then the function generator.
2) Set each variable resistance or electronic load so that each regulator will provide the desired current. Do not exceed the maximum current of each device.
3) Verify on the oscilloscope that the voltage on channel 2 ramps up to 2.5 V before the voltage on channel 3 ramps up to 3.3 V.
4) Turn off the function generator then the power supply. Disconnect the function generator.

Other test setups are possible by changing the jumpers.

**When performing tests that require the devices to provide large dc currents, the test board, regulators, and loads will get hot. It is the user's responsibility to ensure that the test board and load resistors can handle the power dissipation.**

Refer to the TPS755xx and TPS757xx datasheets for the maximum power dissipation capabilities of the TO–263 and TO-220 packages. Additional air flow may be required to achieve the desired power dissipation. If the junction temperature of the device exceeds 125°C, the device may attempt to protect itself from damage by entering a thermal shutdown mode. The device will have to cool down before it can be restarted.

# Chapter 3

# Test Results

This chapter presents laboratory test results of the TPS75525EVM obtained for the recommended test procedures in Chapter 2.

Figure 3–1 shows the power up sequencing capability of the EVM. Channel 1 is $\overline{\text{ENABLE}}$. Channel 2 is $V_{(CORE)}$. Channel 3 is $V_{IO}$.

*Figure 3–1. Power-Up Sequencing Capability*