

# 3.3V ZERO DELAY CLOCK BUFFER

IDT2305A

### **FEATURES:**

- · Phase-Lock Loop Clock Distribution
- 10MHz to 133MHz operating frequency
- · Distributes one clock input to one bank of five outputs
- · Zero Input-Output Delay
- Output Skew < 250ps
- Low jitter <200 ps cycle-to-cycle
- · IDT2305A-1 for Standard Drive
- IDT2305A-1H for High Drive
- · No external RC network required
- Operates at 3.3V VDD
- · Power down mode
- Available in SOIC package

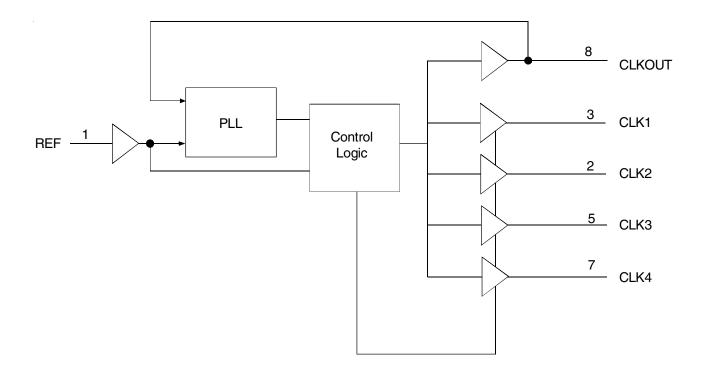
### **DESCRIPTION:**

The IDT2305A is a high-speed phase-lock loop (PLL) clock buffer, designed to address high-speed clock distribution applications. The zero delay is achieved by aligning the phase between the incoming clock and the output clock, operable within the range of 10 to 133MHz.

The IDT2305A is an 8-pin version of the IDT2309A. IDT2305A accepts one reference input, and drives out five low skew clocks. The -1H version of this device operates up to 133MHz frequency and has a higher drive than the -1 device. All parts have on-chip PLLs which lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad. In the absence of an input clock, the IDT2305A enters power down. In this mode, the device will draw less than  $12\mu A$  for Commercial Temperature range and less than  $25\mu A$  for Industrial temperature range, the outputs are tri-stated, and the PLL is not running, resulting in a significant reduction of power.

The IDT2305A is characterized for both Industrial and Commercial operation.

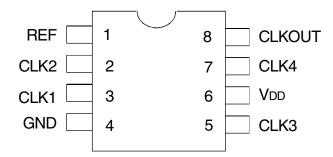
## **FUNCTIONAL BLOCK DIAGRAM**



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**AUGUST 2012** 

## **PINCONFIGURATION**



SOIC TOP VIEW

## **APPLICATIONS:**

- SDRAM
- · Telecom
- · Datacom
- · PC Motherboards/Workstations
- · Critical Path Delay Designs

## ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max.	Unit
VDD	Supply Voltage Range	-0.5 to +4.6	V
VI <sup>(2)</sup>	Input Voltage Range (REF)	-0.5 to +5.5	V
VI	Input Voltage Range	-0.5 to	V
	(except REF)	VDD+0.5	
IIK (VI < 0)	Input Clamp Current	-50	mA
Io (Vo = 0 to VDD)	Continuous Output Current	±50	mA
VDD or GND	Continuous Current	±100	mA
TA = 55°C	Maximum Power Dissipation	0.7	W
(in still air) <sup>(3)</sup>			
Tstg	Storage Temperature Range	-65 to +150	°C
Operating	Commercial Temperature	0 to +70	°C
Temperature	Range		
Operating	Industrial Temperature	-40 to +85	°C
Temperature	Range		

## NOTES:

- 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

### **PINDESCRIPTION**

Pin Name	Pin Number	Туре	Functional Description
REF	1	IN	Input reference clock, 5 Volt tolerant input
CLK2 <sup>(1)</sup>	2	Out	Output clock
CLK1 <sup>(1)</sup>	3	Out	Output clock
GND	4	Ground	Ground
CLK3 <sup>(1)</sup>	5	Out	Output clock
VDD	6	PWR	3.3V Supply
CLK4 <sup>(1)</sup>	7	Out	Output clock
CLKOUT <sup>(1)</sup>	8	Out	Output clock, internal feedback on this pin

#### NOTES:

1. Weak pull down on all outputs.

## **OPERATING CONDITIONS-COMMERCIAL**

Symbol	nbol Parameter		Max.	Unit
VDD	VDD Supply Voltage		3.6	V
TA	Operating Temperature (Ambient Temperature)	0	70	°C
CL	Load Capacitance < 100MHz		30	pF
	Load Capacitance 100MHz - 133MHz	_	10	
CIN	InputCapacitance	_	7	pF

## DC ELECTRICAL CHARACTERISTICS-COMMERCIAL

Symbol	Parameter	C	Conditions		Max.	Unit
VIL	Input LOW Voltage Level			_	0.8	V
Vih	Input HIGH Voltage Level			2	_	V
lıL	Input LOW Current	VIN = 0V		_	50	μΑ
lін	Input HIGH Current	VIN = VDD	VIN = VDD		100	μΑ
Vol	Output LOW Voltage	Standard Drive	IoL = 8mA	_	0.4	V
		High Drive	IoL = 12mA (-1H)			
Voн	Output HIGH Voltage	Standard Drive	Iон = -8mA	2.4	_	V
		High Drive	Iон = -12mA (-1H)			
ldd_pd	Power Down Current	REF = 0MHz		_	12	μΑ
ldd	Supply Current	Unloaded Outputs at 66.	Unloaded Outputs at 66.66MHz		32	mA

## SWITCHING CHARACTERISTICS (2305A-1)-COMMERCIAL (1,2)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
tı	Output Frequency	10pFLoad	10	_	133	MHz
		30pF Load	10	_	100	
	Duty Cycle = t2 ÷ t1	Measured at 1.4V, Fout = 66.66MHz	40	50	60	%
ts	Rise Time	Measured between 0.8V and 2V	-	_	2.5	ns
t4	FallTime	Measured between 0.8V and 2V	1	_	2.5	ns
t5	Output to Output Skew	All outputs equally loaded	1	_	250	ps
t6	Delay, REF Rising Edge to CLKOUT Rising Edge	Measured at VDD/2	-	0	±350	ps
t7	Device-to-Device Skew	Measured at VDD/2 on the CLKOUT pins of devices	1	0	700	ps
tı	Cycle-to-Cycle Jitter, pk - pk	Measured at 54-81MHz, loaded outputs	1	_	170	ps
		Otherfrequencies, loaded outputs			200	ps
tLOCK	PLL Lock Time	Stable power supply, valid clock presented on REF pin	_	_	1	ms

#### NOTES

- 1. REF Input has a threshold voltage of VDD/2.
- 2. All parameters specified with loaded outputs.

## SWITCHING CHARACTERISTICS (2305A-1H)-COMMERCIAL (1,2)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
t1	Output Frequency	10pFLoad	10	_	133	MHz
		30pF Load	10	_	100	
	Duty Cycle = t2 ÷ t1	Measured at 1.4V, Fout = 66.66MHz	40	50	60	%
	Duty Cycle = t2 ÷ t1	Measured at 1.4V, Fout <50MHz	45	50	55	%
t3	Rise Time	Measured between 0.8V and 2V	_	_	1.5	ns
t4	Fall Time	Measured between 0.8V and 2V	_	_	1.5	ns
t5	Output to Output Skew	All outputs equally loaded	_	_	250	ps
t6	Delay, REF Rising Edge to CLKOUT Rising Edge	Measured at VDD/2	_	0	±350	ps
t7	Device-to-Device Skew	Measured at VDD/2 on the CLKOUT pins of devices	_	0	700	ps
t8	Output Slew Rate	Measured between 0.8V and 2V using Test Circuit #2	1	_	_	V/ns
tı	Cycle-to-Cycle Jitter, pk - pk	Measured at 54-81MHz, loaded outputs		_	170	ps
		Other frequencies, loaded outputs			200	ps
tLOCK	PLL Lock Time	Stable power supply, valid clock presented on REF pin	_	_	1	ms

#### NOTES:

- 1. REF Input has a threshold voltage of VDD/2.
- 2. All parameters specified with loaded outputs.

## **OPERATING CONDITIONS-INDUSTRIAL**

Symbol	Parameter	Min.	Max.	Unit
VDD	Supply Voltage	3	3.6	V
TA	Operating Temperature (Ambient Temperature)	-40	+85	°C
CL	Load Capacitance < 100MHz		30	pF
	Load Capacitance 100MHz - 133MHz	_	10	
CIN	InputCapacitance	_	7	pF

## DC ELECTRICAL CHARACTERISTICS-INDUSTRIAL

Symbol	Parameter	C	Conditions	Min.	Max.	Unit
VIL	Input LOW Voltage Level			_	0.8	V
ViH	Input HIGH Voltage Level			2	_	V
lıL	Input LOW Current	VIN = 0V		_	50	μA
Iн	Input HIGH Current	VIN = VDD	VIN = VDD		100	μA
Vol	Output LOW Voltage	Standard Drive	IOL = 8mA	_	0.4	V
		High Drive	IOL = 12mA (-1H)			
Vон	Output HIGH Voltage	Standard Drive	Iон = -8mA	2.4	_	V
		High Drive	Iон = -12mA (-1H)			
IDD_PD	Power Down Current	REF = 0MHz		_	25	μA
ldd	Supply Current	Unloaded Outputs at 66.	66MHz	_	35	mA

## SWITCHING CHARACTERISTICS (2305A-1) - INDUSTRIAL (1,2)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
t1	Output Frequency	10pFLoad	10	_	133	MHz
		30pFLoad	10	_	100	
	Duty Cycle = t2 ÷ t1	Measured at 1.4V, FOUT = 66.66MHz	40	50	60	%
t3	Rise Time	Measured between 0.8V and 2V	1	_	2.5	ns
t4	FallTime	Measured between 0.8V and 2V	1	_	2.5	ns
t5	Output to Output Skew	All outputs equally loaded	-	_	250	ps
t6	Delay, REF Rising Edge to CLKOUT Rising Edge	Measured at VDD/2	1	0	±350	ps
t7	Device-to-Device Skew	Measured at VDD/2 on the CLKOUT pins of devices	1	0	700	ps
tu	Cycle-to-Cycle Jitter, pk - pk	Measured at 54-81MHz, loaded outputs	1	_	170	ps
		Other frequencies, loaded outputs			200	ps
tLOCK	PLL Lock Time	Stable power supply, valid clock presented on REF pin	_	_	1	ms

#### NOTES:

- 1. REF Input has a threshold voltage of VDD/2.
- 2. All parameters specified with loaded outputs.

## SWITCHING CHARACTERISTICS (2305A-1H)-INDUSTRIAL (1,2)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
t1	Output Frequency	10pFLoad		_	133	MHz
		30pFLoad	10	_	100	
	Duty Cycle = t2 ÷ t1	Measured at 1.4V, Fout = 66.66MHz	40	50	60	%
	Duty Cycle = t2 ÷ t1	Measured at 1.4V, Fout <50MHz	45	50	55	%
t3	Rise Time	Measured between 0.8V and 2V	_	_	1.5	ns
t4	Fall Time	Measured between 0.8V and 2V		_	1.5	ns
t5	Output to Output Skew	All outputs equally loaded		_	250	ps
t6	Delay, REF Rising Edge to CLKOUT Rising Edge	Measured at VDD/2	_	0	±350	ps
t7	Device-to-Device Skew	Measured at VDD/2 on the CLKOUT pins of devices	-	0	700	ps
t8	Output Slew Rate	Measured between 0.8V and 2V using Test Circuit #2	1	_	_	V/ns
tu	Cycle-to-Cycle Jitter, pk - pk	Measured at 54-81MHz, loaded outputs	_	_	170	ps
		Other frequencies, loaded outputs			200	ps
tLOCK	PLL Lock Time	Stable power supply, valid clock presented on REF pin	_	_	1	ms

#### NOTES:

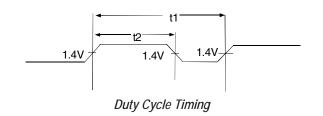
- 1. REF Input has a threshold voltage of VDD/2.
- 2. All parameters specified with loaded outputs.

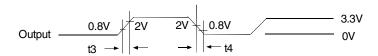
### ZERO DELAY AND SKEW CONTROL

All outputs should be uniformly loaded in order to achieve Zero I/O Delay. Since the CLKOUT pin is the internal feedback for the PLL, its relative loading can affect and adjust the input/output delay.

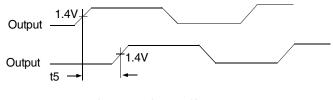
For designs utilizing zero I/O Delay, all outputs including CLKOUT must be equally loaded. Even if the output is not used, it must have a capacitive load equal to that on the other outputs in order to obtain true zero I/O Delay. If I/O Delay adjustments are needed, use the Output Load Difference diagram to calculate loading differences between the CLKOUT pin and other outputs. For zero output-to-output skew, all outputs must be loaded equally.

## **SWITCHING WAVEFORMS**

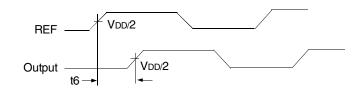




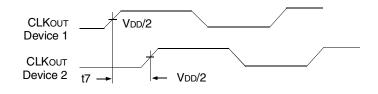
All Outputs Rise/Fall Time



Output to Output Skew

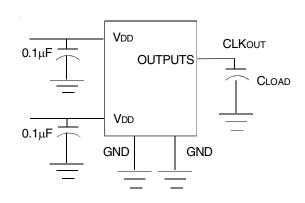


Input to Output Propagation Delay

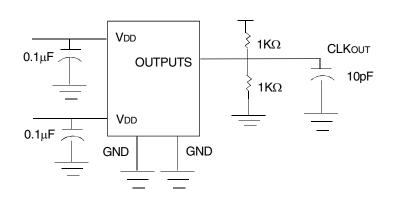


Device to Device Skew

## **TEST CIRCUITS**

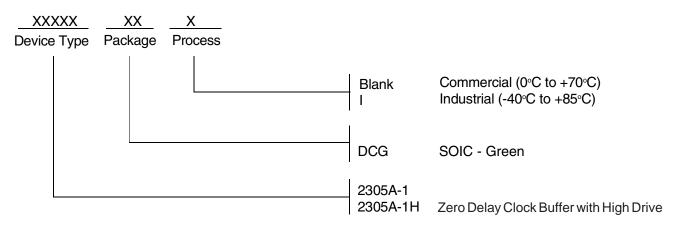


Test Circuit 1 (all Parameters Except t8)



Test Circuit 2 (t8, Output Slew Rate On -1H Devices)

## **ORDERING INFORMATION**



Ordering Code	Package Type Package Type	Operating Range
2305A-1DCG8 (tape and reel)	8-Pin SOIC	Commercial
2305A-1DCG	8-Pin SOIC	Commercial
2305A-1DCGI	8-Pin SOIC	Industrial
2305A-1DCGI8 (tape and reel)	8-Pin SOIC	Industrial
2305A-1HDCG8 (tape and reel)	8-Pin SOIC	Commercial
2305A-1HDCG	8-Pin SOIC	Commercial
2305A-1HDCGI	8-Pin SOIC	Industrial
2305A-1HDCGI8 (tape and reel)	8-Pin SOIC	Industrial

G denotes Pb-free, RoHS complaint package; "8" denotes tape and reel



## **Mouser Electronics**

**Authorized Distributor** 

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IDT (Integrated Device Technology):

<u>2305A-1DCGI8</u> <u>2305A-1DCG</u> <u>2305A-1DCG8</u> <u>2305A-1DCG8</u> <u>2305A-1HDCGI8</u> <u>2305A-1HDCGI</u> <u>2305A-1HDCGI</u> <u>2305A-1DCGI</u>