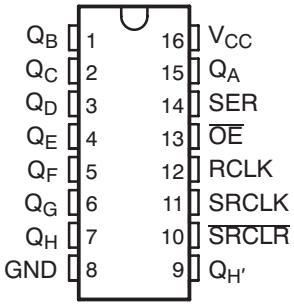
8-BIT SHIFT REGISTER WITH 3-STATE OUTPUT REGISTERS

Check for Samples: SN74LV595A-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval**
- **2-V to 5.5-V V_{CC} Operation**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2.3 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Supports Mixed-Mode Voltage Operation on All Ports**
- **8-Bit Serial-In, Parallel-Out Shift**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Shift Register Has Direct Clear**



DESCRIPTION

The SN74LV595A is an 8-bit shift register designed for 2-V to 5.5-V V_{CC} operation.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear ($\overline{SRCLR}$) input, serial (SER) input, and a serial output for cascading. When the output-enable ($\overline{OE}$) input is high, all outputs except $Q_{H'}$ are in the high-impedance state.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION(1)

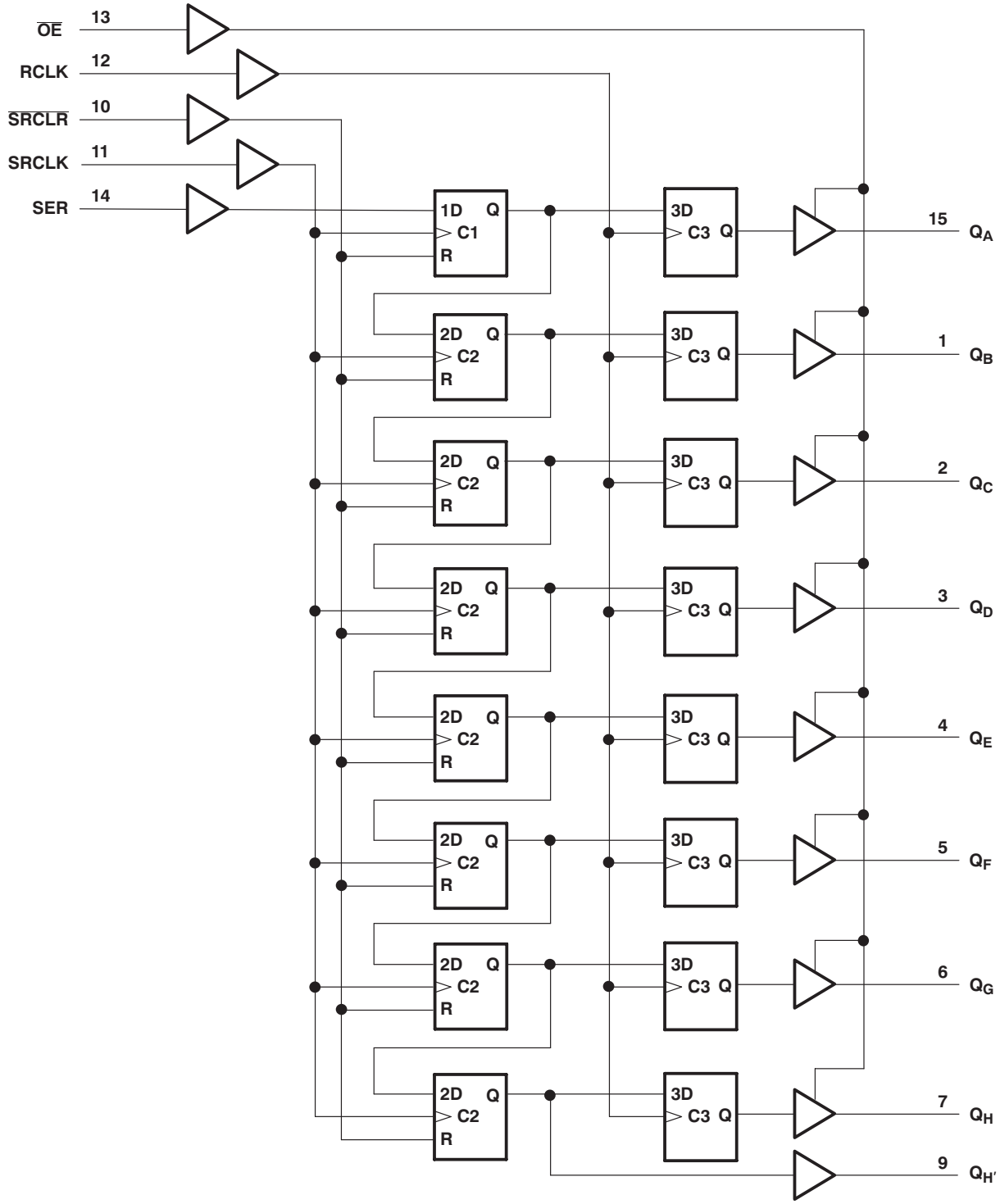
T_A	PACKAGE (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP − PW	Reel of 2000	SN74LV595AIPWRQ1	LV595AI
–40°C to 125°C	TSSOP − PW	Reel of 2000	SN74LV595AQPWRQ1	LV595AQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

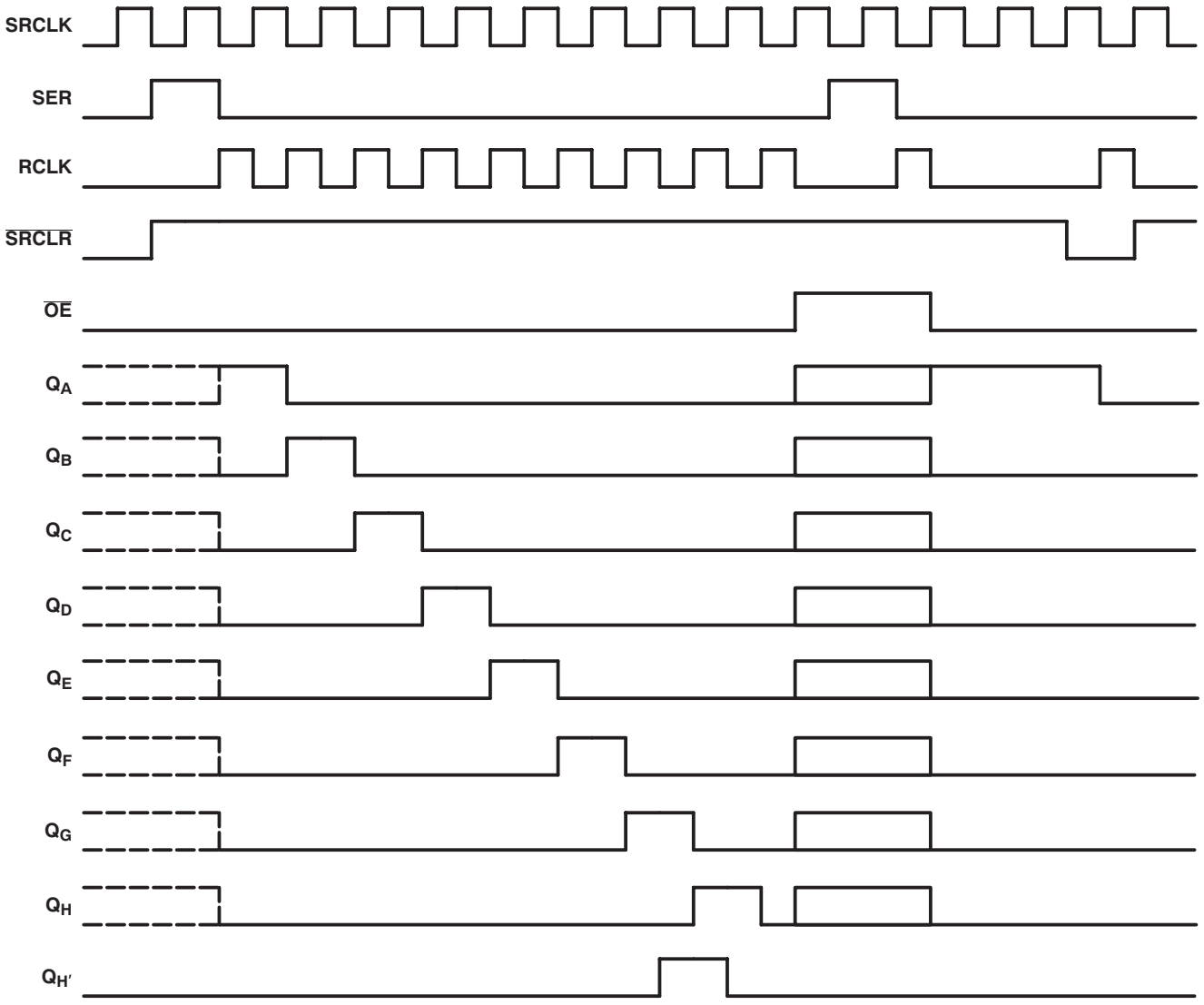
Table 1. FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{OE}}$	
X	X	X	X	H	Outputs Q_A–Q_H are disabled.
X	X	X	X	L	Outputs Q_A–Q_H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored in the storage register.

LOGIC DIAGRAM (POSITIVE LOGIC)



TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage range		−0.5 V to 7 V
V_I	Input voltage range(2)		−0.5 V to 7 V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		−0.5 V to 7 V
V_O	Output voltage range applied in the high or low state(2) (3)		−0.5 V to V_{CC} + 0.5 V
I_{IK}	Input clamp current(2)	V_I < 0	–20 mA
I_{OK}	Output clamp current(2)	V_O < 0	–50 mA
I_O	Continuous output current	V_O = 0 to V_{CC}	±35 mA
	Continuous current through V_{CC} or GND		±70 mA
θ_{JA}	Package thermal impedance(4)		108°C/W
T_{stg}	Storage temperature range		−65°C to 150°C
ESD	Electrostatic discharge rating	Human-body model (HBM)	2000 V
		Machine model (MM)	200 V
		Charged-device model (CDM)	1000 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High level output current	V_{CC} = 2 V		–50	µA
		V_{CC} = 2.3 V to 2.7 V		–2	mA
		V_{CC} = 3 V to 3.6 V		–8	
		V_{CC} = 4.5 V to 5.5 V		–16	
I_{OL}	Low level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		8	
		V_{CC} = 4.5 V to 5.5 V		16	
Δt/Δv	Input transition rise/fall time	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature	SN74LV595AIPWRQ1	–40	85	°C
		SN74LV595AQPWRQ1	–40	125	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = −40°C TO 85°C			T_A = −40°C TO 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}		I_{OH} = −50 µA	2 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1			V
		I_{OH} = −2 mA	2.3 V	2			2			
	$Q_{H'}$	I_{OH} = −6 mA	3 V	2.48			2.45			
	Q_A–Q_H	I_{OH} = −8 mA		2.48			2.45			
	$Q_{H'}$	I_{OH} = −12 mA	4.5 V	3.8			3.7			
	Q_A–Q_H	I_{OH} = −16 mA		3.8			3.7			
V_{OL}		I_{OL} = 50 µA	2 V to 5.5 V			0.1			0.1	V
		I_{OH} = 2 mA	2.3 V			0.4			0.45	
	$Q_{H'}$	I_{OH} = 6 mA	3 V			0.44			0.5	
	Q_A–Q_H	I_{OH} = 8 mA				0.44			0.5	
	$Q_{H'}$	I_{OH} = 12 mA	4.5 V			0.55			0.65	
	Q_A–Q_H	I_{OH} = 16 mA				0.55			0.65	
I_I		V_I = 5.5 V or GND	0 V to 5.5 V			±1			±1	nA
I_{OZ}	Q_A–Q_H	V_O = V_{CC} or GND	5.5 V			±5			±10	µA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			20			40	µA
I_{off}		V_I or V_O = 0 to 5.5 V	0			5(1)			10	µA
C_i		V_I = V_{CC} or GND	3.3 V		3.5			3.5		pF

(1) I_{off} does not apply to pin 9.

TIMING REQUIREMENTS

over operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

			T_A = 25°C		T_A = −40°C TO 85°C		T_A = −40°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	SRCLK high or low	7		7.5		8.5		ns
		RCLK high or low	7		7.5		8.5		
		$\overline{SRCLR}$ low	6		6.5		7.5		
t_{su}	Setup time	SER before SRCLK↑	5.5		5.5		6.5		ns
		SRCLK↑ before RCLK↑(1)	8		9		10		
		$\overline{SRCLR}$ low before RCLK↑	8.5		9.5		10.5		
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	4		4		5		
t_h	Hold time	SER after SRCLK↑	1.5		1.5		2.5		ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

TIMING REQUIREMENTS

over operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

			T_A = 25°C		T_A = −40°C TO 85°C		T_A = −40°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	SRCLK high or low	5.5		5.5		6.5		ns
		RCLK high or low	5.5		5.5		6.5		
		$\overline{SRCLR}$ low	5		5		6		
t_{su}	Setup time	SER before SRCLK↑	3.5		3.5		4.5		ns
		SRCLK↑ before RCLK↑(1)	8		8.5		9.5		
		$\overline{SRCLR}$ low before RCLK↑	8		9		10		
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	3		3		4		
t_h	Hold time	SER after SRCLK↑	1.5		1.5		2.5		ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

TIMING REQUIREMENTS

over operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

			T_A = 25°C		T_A = −40°C TO 85°C		T_A = −40°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	SRCLK high or low	5		5		6		ns
		RCLK high or low	5		5		6		
		$\overline{SRCLR}$ low	5.2		5.2		6.2		
t_{su}	Setup time	SER before SRCLK↑	3		3		4		ns
		SRCLK↑ before RCLK↑(1)	5		5		6		
		$\overline{SRCLR}$ low before RCLK↑	5		5		6		
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	2.5		2.5		3.5		
t_h	Hold time	SER after SRCLK↑	2		2		3		ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V, C_L = 50 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			T_A = −40°C TO 85°C		T_A = −40°C TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			60	70		40		30		MHz
t_{PLH}	RCLK	Q_A–Q_H		11.2	17.2	1	19.3	1	22.3	ns
t_{PHL}				11.2	17.2	1	19.3	1	22.3	ns
t_{PLH}	SRCLK	$Q_{H'}$		13.1	22.5	1	25.5	1	28.5	ns
t_{PHL}				13.1	22.5	1	25.5	1	28.5	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$		12.4	18.8	1	21.1	1	24.1	ns
t_{PZH}	$\overline{OE}$	Q_A–Q_H		10.8	17	1	18.3	1	21.3	ns
t_{PZL}				13.4	21	1	23	1	26	ns
t_{PHZ}	$\overline{OE}$	Q_A–Q_H		12.2	18.3	1	19.5	1	22.5	ns
t_{PLZ}				14	20.9	1	22.6	1	25.6	ns

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, C_L = 50 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			T_A = −40°C TO 85°C		T_A = −40°C TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			55	105		50		40		MHz
t_{PLH}	RCLK	Q_A–Q_H		7.9	15.4	1	17	1	20	ns
t_{PHL}				7.9	15.4	1	17	1	20	ns
t_{PLH}	SRCLK	$Q_{H'}$		9.2	16.5	1	18.5	1	21.5	ns
t_{PHL}				9.2	16.5	1	18.5	1	21.5	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$		9	16.3	1	17.2	1	20.2	ns
t_{PZH}	$\overline{OE}$	Q_A–Q_H		7.8	15	1	17	1	20	ns
t_{PZL}				9.6	15	1	17	1	20	ns
t_{PHZ}	$\overline{OE}$	Q_A–Q_H		8.1	15.7	1	16.2	1	19.2	ns
t_{PLZ}				9.3	15.7	1	16.2	1	19.2	ns

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V, C_L = 50 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			T_A = −40°C TO 85°C		T_A = −40°C TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			95	140		85		75		MHz
t_{PLH}	RCLK	Q_A–Q_H		5.6	9.4	1	10.5	1	13.5	ns
t_{PHL}				5.6	9.4	1	10.5	1	13.5	ns
t_{PLH}	SRCLK	$Q_{H'}$		6.4	10.2	1	11.4	1	14.4	ns
t_{PHL}				6.4	10.2	1	11.4	1	14.4	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$		6.4	10	1	11.1	1	14.1	ns
t_{PZH}	$\overline{OE}$	Q_A–Q_H		5.7	10.6	1	12	1	15	ns
t_{PZL}				6.8	10.6	1	12	1	15	ns
t_{PHZ}	$\overline{OE}$	Q_A–Q_H		3.5	10.3	1	11	1	14	ns
t_{PLZ}				3.4	10.3	1	11	1	14	ns

NOISE CHARACTERISTICS(1)

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.2		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.8		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

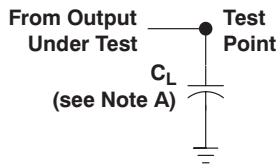
(1) Characteristics are for surface-mount packages only.

OPERATING CHARACTERISTICS

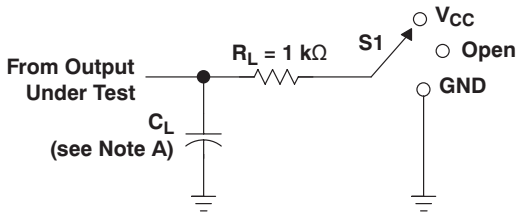
T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	V_{CC} = 3.3 V	111	pF
			V_{CC} = 5 V	114	

PARAMETER MEASUREMENT INFORMATION

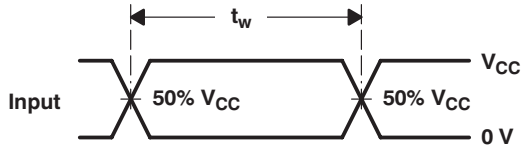


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

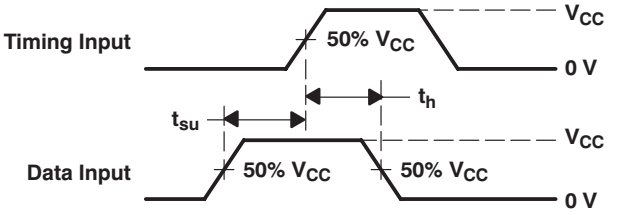


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

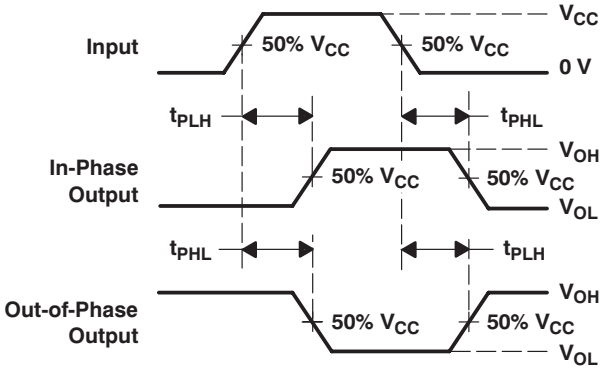
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



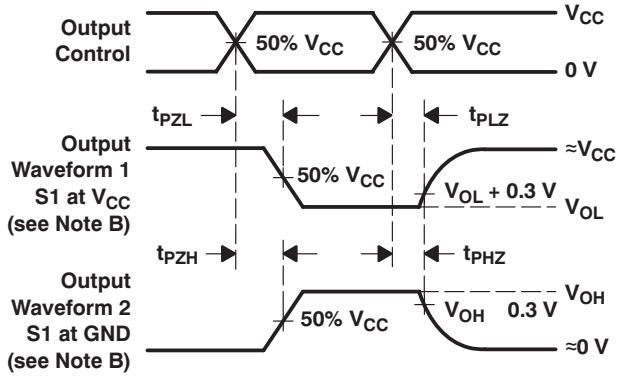
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74LV595AIPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV595AI	Samples
SN74LV595AIPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	LV595AI	Samples
SN74LV595AQPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV595AQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF SN74LV595A-Q1 :

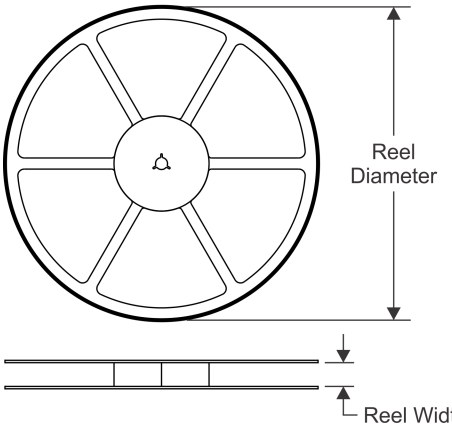
- Catalog: SN74LV595A
- Enhanced Product: SN74LV595A-EP

NOTE: Qualified Version Definitions:

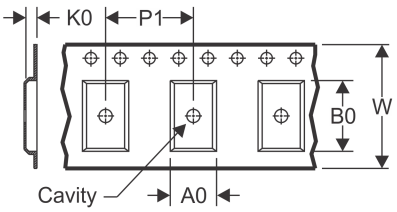
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

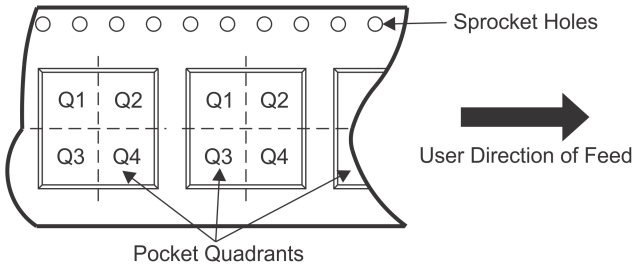


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

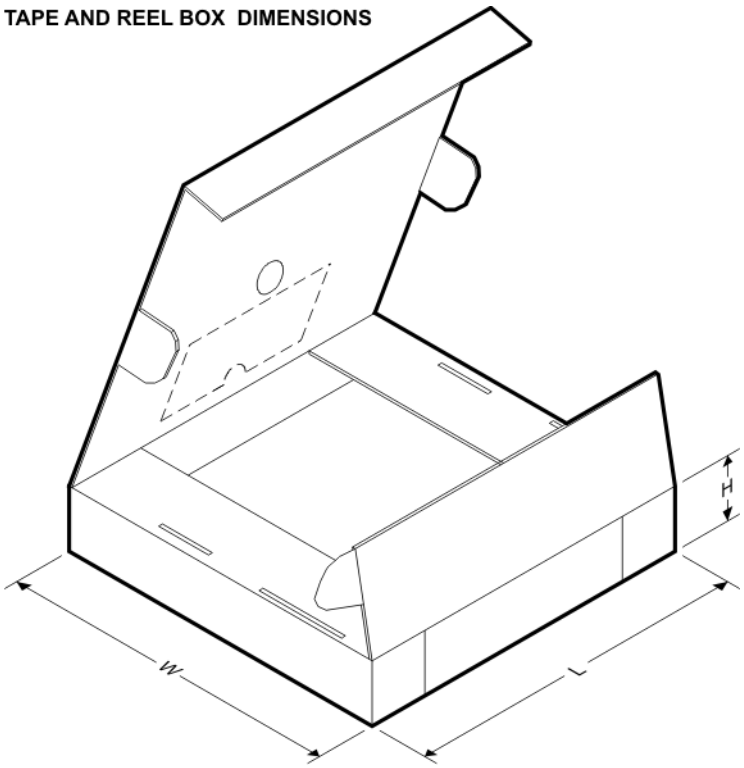
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV595AIPWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV595AIPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV595AQPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

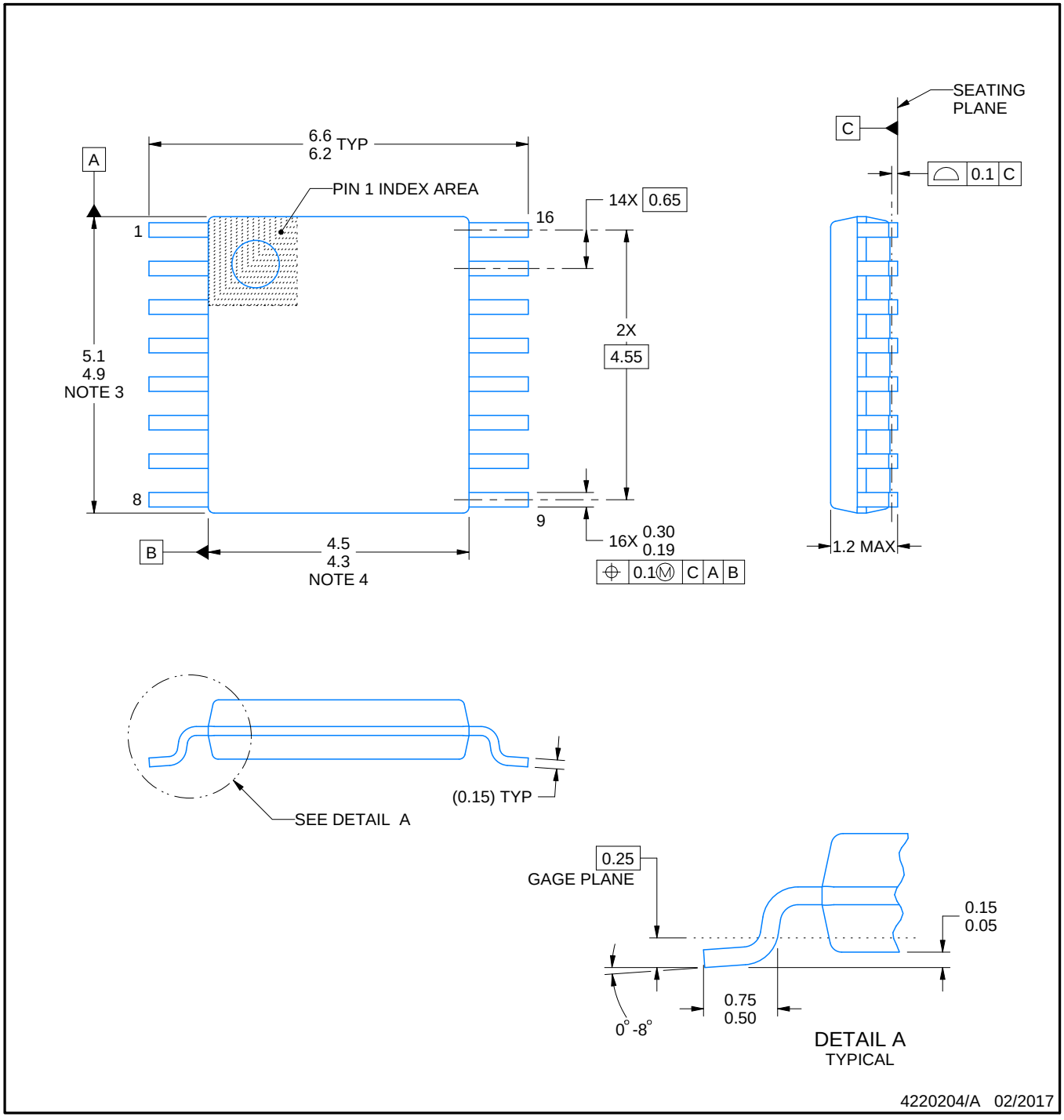
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV595AIPWRG4Q1	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV595AIPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV595AQPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0

PACKAGE OUTLINE

PW0016A

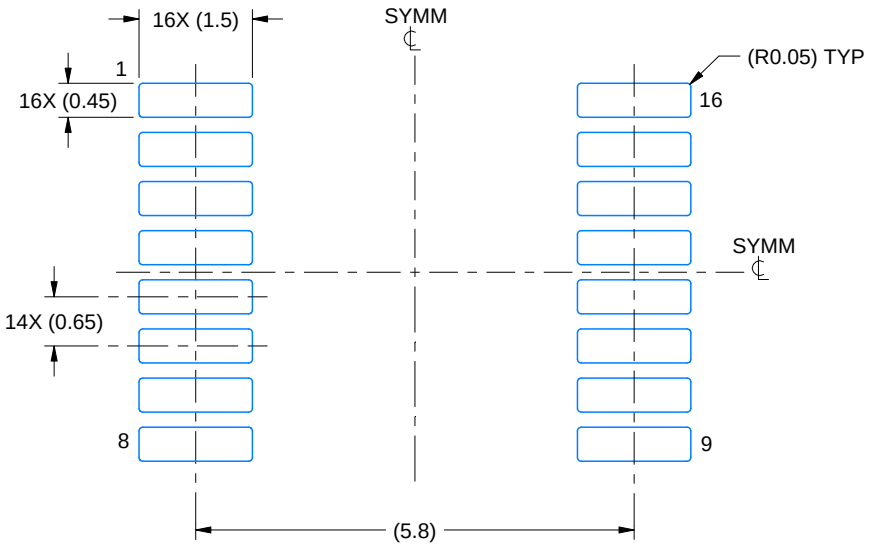
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

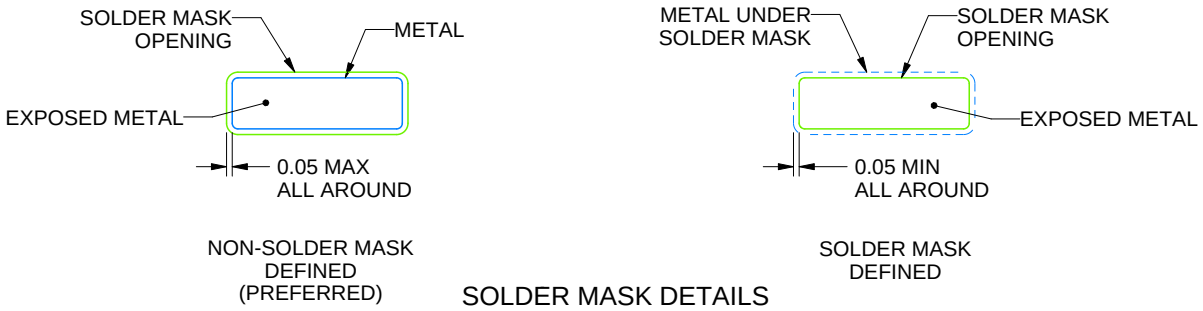


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

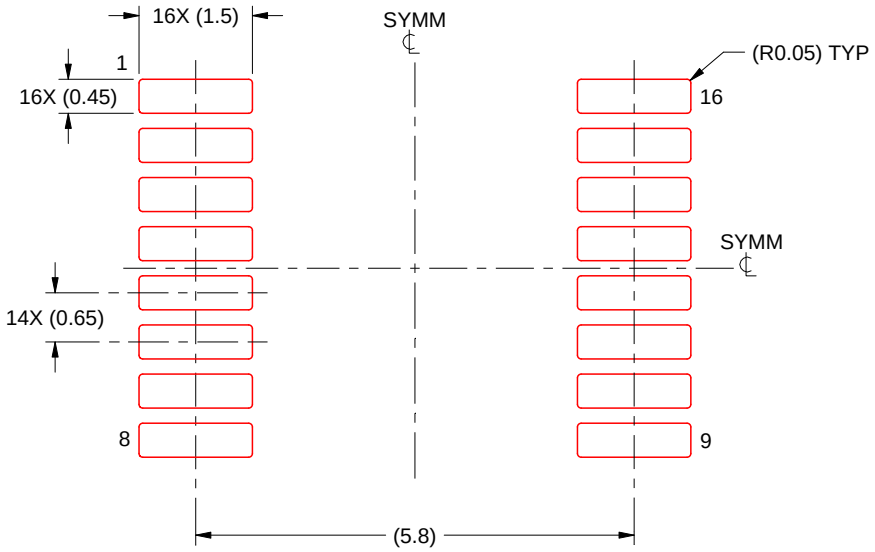


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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