

FEATURES:

- Up to 64 serial input and output streams
- Maximum 16,384 x 16,384 channel non-blocking switching
- Accepts data streams at 2.048Mb/s, 4.096Mb/s, 8.192Mb/s, 16.384Mb/s or 32.768Mb/s
- Rate matching capability: rate selectable on both RX and TX in eight groups of 8 streams
- Optional Output Enable Indication Pins for external driver High-Z control
- Per-channel Variable Delay Mode for low-latency applications
- Per-channel Constant Delay Mode for frame integrity applications
- Enhanced Block programming capabilities
- TX/RX Internal Bypass
- Automatic identification of ST-BUS® and GCI serial streams
- Per-stream frame delay offset programming
- Per-channel High-Impedance output control
- Per-channel processor mode to allow microprocessor writes to TX streams
- Bit Error Rate Testing (BERT) for testing
- Direct microprocessor access to all internal memories

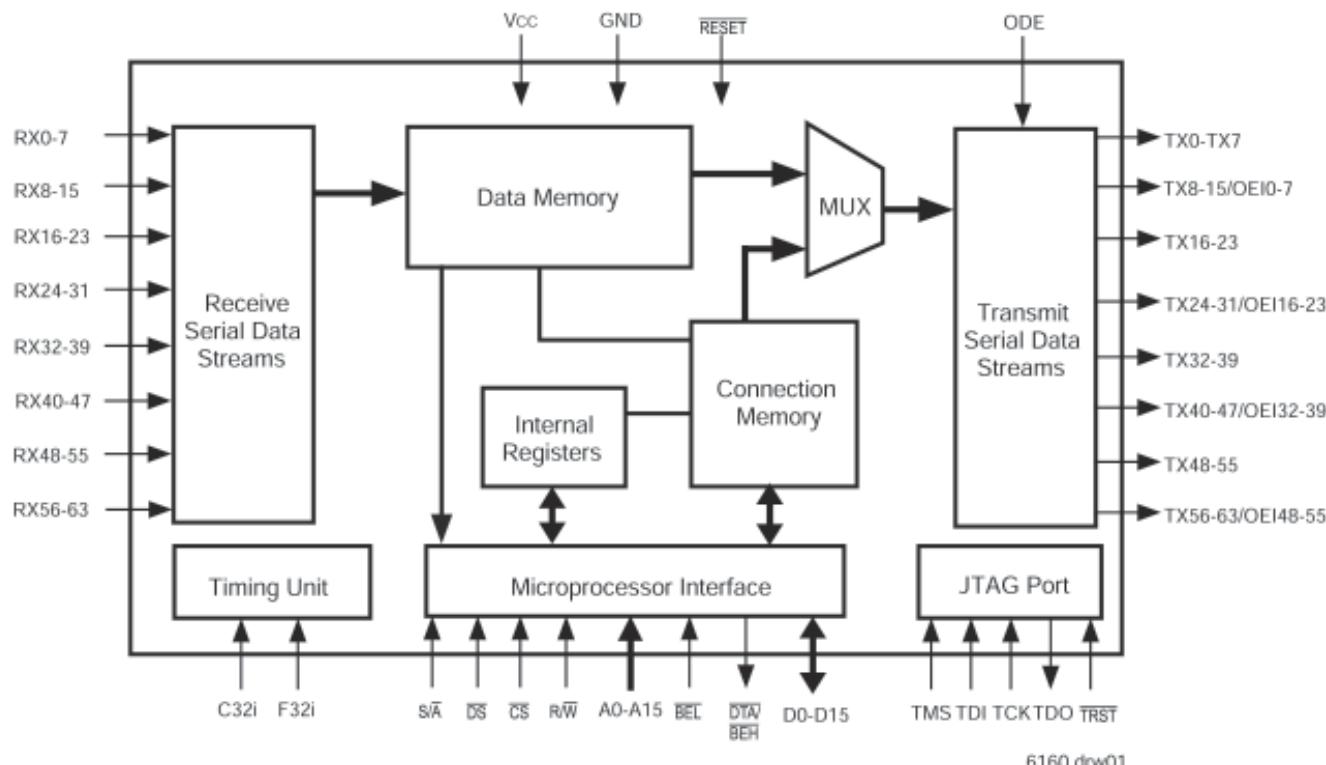
- Selectable Synchronous and Asynchronous Microprocessor bus timing modes
- IEEE-1149.1 (JTAG) Test Port
- Available in 208-pin (17mm x 17mm) Plastic Ball Grid Array (PBGA)
- Operating Temperature Range -40°C to +85°C

DESCRIPTION:

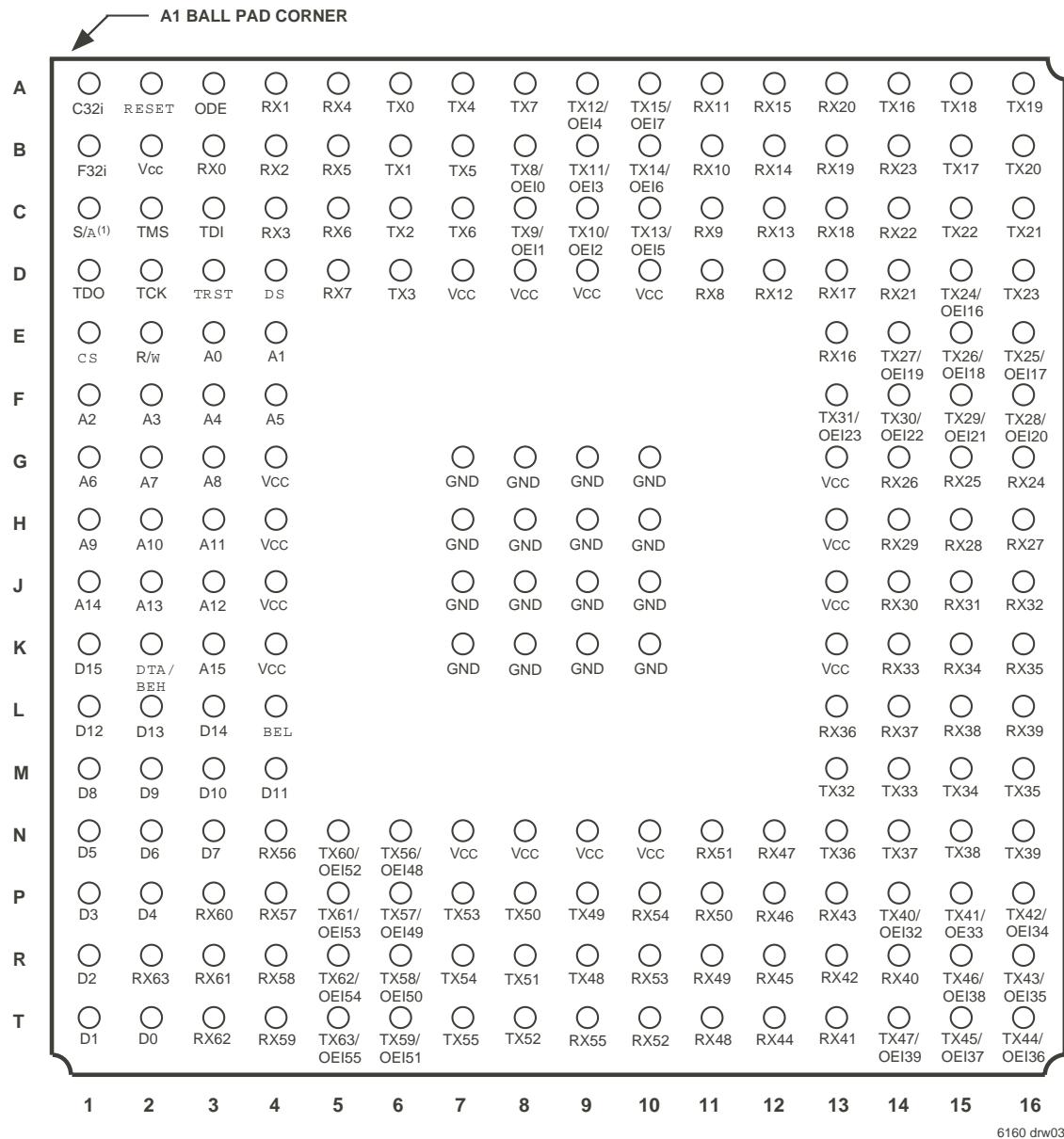
The IDT72V73263 has a non-blocking switch capacity of 16,384 x 16,384 channels at 32.768Mb/s. With 64 inputs and 64 outputs, programmable per stream control, and a variety of operating modes the IDT72V73263 is designed for the TDM time slot interchange function in either voice or data applications.

Some of the main features of the IDT72V73263 are LOW power 3.3 Volt operation, automatic ST-BUS®/GCI sensing, memory block programming, simple microprocessor interface, JTAG Test Access Port (TAP) and per stream programmable input offset delay, variable or constant throughput modes, output enable and processor mode, BER testing, bypass mode, and advanced block programming.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



NOTE:

1. S/A should be tied directly to VCC or GND for proper operation.

PBGA: 1mm pitch, 17mm x 17mm (BB208-1 order code: BB)
TOP VIEW

PIN DESCRIPTION

| SYMBOL | NAME | I/O | PBGA PIN NO. | DESCRIPTION |
|---------|--|-----|-----------------------|---|
| A0-A15 | Address 0-15 | I | *See PBGA Table Below | These address lines access all internal memories. |
| BEL | Byte Enable LOW | I | L4 | In synchronous mode, this input will enable the lower byte (D0-7) on to the data bus. |
| C32i | Clock | I | A1 | Serial clock for shifting data in/out on the serial data streams. This input accepts a 32.768MHz clock. |
| CS | Chip Select | I | E1 | Active LOW input used by a microprocessor to activate the microprocessor port of the device. |
| D0-15 | Data Bus 0-15 | I/O | *See PBGA Table Below | These pins are the data bus of the microprocessor port. |
| DS | Data Strobe | I | D4 | This active LOW input works in conjunction with CS to enable the read and write operations. This active LOW input sets the data bus lines (D0-D15). |
| DTA/BEH | Data Transfer Acknowledgment Active LOW Output | I/O | K2 | In asynchronous mode this pin indicates that a data bus transfer is complete. When the bus cycle ends, this pin drives HIGH and then High-Z allowing for faster bus cycles with a weaker pull-up resistor. A pull-up resistor is required to hold a HIGH level when the pin is High-Z. When the device is in /Byte Enable HIGH synchronous bus mode, this pin acts as an input and will enable the upper byte (D8-15) on to the data bus. |
| F32i | Frame Pulse | I | B1 | This input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS® and GCI specifications. |
| GND | | | *See PBGA Table Below | Ground. |
| ODE | Output Drive Enable | I | A3 | This is the output enable control for the TX serial outputs. When ODE input is LOW and the OSB bit of the CR register is LOW, all TX outputs are in a High-Impedance state. If this input is HIGH, the TX output drivers are enabled. However, each channel may still be put into a High-Impedance state by using the per channel control bits in the Connection Memory HIGH. |
| RX0-63 | RX Input 0 to 63 | I | *See PBGA Table Below | Serial data Input Stream. These streams may have data rates of 2.048Mb/s, 4.096Mb/s, 8.192Mb/s, 16.384Mb/s, or 32.768Mb/s depending upon the selection in Receive Data Rate Selection Register (RDRSR). |
| RESET | Device Reset: | I | A2 | This input (active LOW) puts the device in its reset state that clears the device internal counters, registers and brings TX0-63 and microport data outputs to a High-Impedance state. The RESET pin must be held LOW for a minimum of 20ns to reset the device. |
| R/W | Read/Write | I | E2 | This input controls the direction of the data bus lines (D0-D15) during a microprocessor access. |
| S/A | Synchronous/Asynchronous Bus Mode | I | C1 | This input will select between asynchronous microprocessor bus timing and synchronous microprocessor bus timing. In synchronous mode, DTA/BEH acts as the BEH input and is used in conjunction with BEL to output data on the data bus. In asynchronous bus mode, BEL is tied LOW and DTA/BEH acts as the DTA, data bus acknowledgment output. |
| TCK | Test Clock | I | D2 | Provides the clock to the JTAG test logic. |
| TDI | Test Serial Data In | I | C3 | JTAG serial test instructions and data are shifted in on this pin. This pin is pulled HIGH by an internal pull-up when not driven. |
| TDO | Test Serial Data Out | O | D1 | JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in High-Impedance state when JTAG scan is not enabled. |
| TMS | Test Mode Select | I | C2 | JTAG signal that controls the state transitions of the TAP controller. This pin is pulled HIGH by an internal pull-up when not driven. |
| TRST | TestReset | I | D3 | Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin is pulled by an internal pull-up when not driven. This pin should be pulsed LOW on power-up, or held LOW, to ensure that the device is in the normal functional mode. |

PIN DESCRIPTION (CONTINUED)

| SYMBOL | NAME | I/O | PBGA PIN NO. | DESCRIPTION |
|---|---------------------------------------|-----|--------------------------|---|
| TX0-7 TX16-23 TX32-39 TX48-55 | TXOutput | O | *See PBGA Table Below | Serial data Output Stream. These streams may have data rates of 2.048Mb/s, 4.096Mb/s, 8.192Mb/s, 16.384Mb/s, or 32.768Mb/s depending upon the selection in Transmit Data Rate Selection Register (TDRSR). If G0/G2/G4/G6 are programmed to 32.768Mb/s mode the corresponding odd group is unavailable (G1/G3/G5G7). |
| TX8-15/OEI0-7 TX24-31/OEI16-23 TX40-47/OEI32-39 TX56-63/OEI48-55 | TX Output/Output Enable Indication | O | *See PBGA Table Below | When output streams are selected via TDRSR, these pins are the TX output streams. When output enable indication function is selected, these pins reflect the active or High-Z impedance status for the corresponding TX output stream. |
| Vcc | | | *See PBGA Table Below | +3.3 Volt Power Supply. |

PBGA PIN NUMBER TABLE

| SYMBOL | NAME | I/O | PIN NUMBER |
|---|------------------|-----|--|
| A0-A15 | Address A0-15 | I | E3, E4, F1, F2, F3, F4, G1, G2, G3, H1, H2, H3, J3, J2, J1, K3. |
| D0-D15 | Data Bus 0-15 | I/O | T2, T1, R1, P1, P2, N1, N2, N3, M1, M2, M3, M4, L1, L2, L3, K1. |
| GND | Ground | | G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, |
| RX0-63 | RX Input 0 to 63 | I | B3, A4, B4, C4, A5, B5, C5, D5, D11, C11, B11, A11, D12, C12, B12, A12, E13, D13, C13, B13, A13, D14, C14, B14, G16, G15, G14, H16, H15, H14, J14, J15, J16, K14, K15, K16, L13, L14, L15, L16, R14, T13, R13, P13, T12, R12, P12, N12, T11, R11, P11, N11, T10, R10, P10, T9, N4, P4, R4, T4, P3, R3, T3, R2. |
| TX0-TX7 TX16-23 TX32-39 TX48-55 | TXOutput | O | A6, B6, C6, D6, A7, B7, C7, A8 A14, B15, A15, A16, B16, C16, C15, D16 M13, M14, M15, M16, N13, N14, N15, N16 R9, P9, P8, R8, T8, P7, R7, T7 |
| TX8-15/OEI0-7 TX24-31/OEI16-23 TX40-47/OEI32-39 TX56-63/OEI48-55 | TX Output/Output | O | B8, C8, C9, B9, A9, C10, B10, A10. D15, E16, E15, E14, F16, F15, F14, F13. P14, P15, P16, R16, T16, T15, R15, T14. N6, P6, R6, T6, N5, P5, R5, T5. |
| Vcc | | | B2, D7, D8, D9, D10, G4, G13, H4, H13, J4, J13, K4, K13, N7, N8, N9, N10. |

DESCRIPTION (CONTINUED):

The IDT72V73263 is capable of switching up to 16,384 x 16,384 channels without blocking. Designed to switch 64 Kbit/s PCM or N x 64 Kbit/s data, the device maintains frame integrity in data applications and minimizes throughput delay for voice applications on a per-channel basis.

The 64 serial input streams (RX) of the IDT72V73263 can be run at 2.048Mb/s, 4.096Mb/s, 8.192Mb/s, 16.384Mb/s or 32.768Mb/s allowing 32, 64, 128, 256 or 512 channels per 125 μ s frame. The data rates on the output streams can independently be programmed to run at any of these data rates.

With two main operating modes, Processor Mode and Connection Mode, the IDT72V73263 can easily switch data from incoming serial streams (Data Memory) or from the controlling microprocessor via Connection Memory.

As control and status information is critical in data transmission, the Processor Mode is especially useful when there are multiple devices sharing the input and output streams.

With data coming from multiple sources and through different paths, data entering the device is often delayed. To handle this problem, the IDT72V73263 has a Frame Offset feature to allow individual streams to be offset from the frame pulse in half clock-cycle intervals up to +7.5 clock cycles.

The IDT72V73263 also provides a JTAG test access port, memory block programming, Group Block Programming, RX/TX internal bypass, a simple microprocessor interface and automatic ST-BUS®/GCI sensing to shorten setup time, aid in debugging and ease use of the device without sacrificing capabilities.

FUNCTIONAL DESCRIPTION

DATA AND CONNECTION MEMORY

All data that comes in through the RX inputs go through a serial-to-parallel conversion before being stored into internal Data Memory. The 8 KHz frame pulse (F32i) is used to mark the 125 μ s frame boundaries and to sequentially address the input channels in Data Memory.

Data output on the TX streams may come from either the serial input streams (Data Memory) or from the Connection Memory via the microprocessor or in the case that RX input data is to be output, the addresses in Connection Memory are used to specify a stream and channel of the input. The Connection Memory is setup in such a way that each location corresponds to an output channel for each particular stream. In that way, more than one channel can output the same data. In Processor Mode, the microprocessor writes data to the Connection Memory locations corresponding to the stream and channel that is to be output. The lower half (8 least significant bits) of the Connection Memory LOW is output every frame until the microprocessor changes the data or mode of the channels. By using this Processor Mode capability, the microprocessor can access input and output time-slots on a per-channel basis.

The three least significant bits of the Connection Memory HIGH are used to control per-channel mode of the output streams. The MOD2-0 bits are used to select Processor Mode, Constant or Variable Delay Mode, Bit Error Rate, and the High-Impedance state of output drivers. If the MOD2-0 bits are set to 1-1-1 accordingly, only that particular output channel (8 bits) will be in the High-Impedance state. If the MOD2-0 bits are set to 1-0-0 accordingly, that particular channel will be in Processor Mode. If the MOD2-0 bits are set to 1-0-1 a Bit Error Rate Test pattern will be transmitted for that time slot. See BERT section. If the

MOD2-0 bits are set to 0-0-1 accordingly, that particular channel will be in Constant Delay Mode. Finally, if the MOD2-0 bits are set to 0-0-0, that particular channel will be in Variable Delay Mode.

SERIAL DATA INTERFACE TIMING

The master clock frequency of the IDT72V73263 is 32.768MHz, C32i. For 32.768Mb/s data rates, this results in a single-bit per clock. For 16.384Mb/s, 8.192Mb/s, 4.096Mb/s, and 2.048Mb/s this will result in two, four, eight, and sixteen clocks per bit, respectively. The IDT72V73263 provides two different interface timing modes, ST-BUS® or GCI. The IDT72V73263 automatically detects the polarity of an input frame pulse and identifies it as either ST-BUS® or GCI.

For 32.768Mb/s, in ST-BUS® Mode, data is clocked out on a falling edge and is clocked in on the subsequent rising-edge. For 16.384Mb/s, 8.192Mb/s, 4.096Mb/s, and 2.048Mb/s however there is not the typical associated clock since the IDT72V73263 accepts only a 32.768MHz clock. As a result there will be 2, 4, 8, and 16 clock between the 32.768Mb/s transmit edge and the subsequently transmit edges. Although in this is the case, the IDT72V73263 will appropriately transmit and sample on the proper edge as if the respective clock were present. See ST-BUS® Timing for detail.

For 32.768Mb/s, in GCI Mode, data is clocked out on a rising edge and is clocked in on the subsequent falling-edge. For 16.384Mb/s, 8.192Mb/s, 4.096Mb/s, and 2.048Mb/s however, again there is not the typical associated clock since the IDT72V73263 accepts only a 32.768MHz clock. As a result there will be 2, 4, 8, and 16 clocks between the 32.768Mb/s transmit edge and the other transmit edges. Although this is the case, the IDT72V73263 will appropriately transmit and sample on the proper edge as if the respective clock were present. See GCI Bus Timing for detail.

DELAY THROUGH THE IDT72V73263

The switching of information from the input serial streams to the output serial streams results in a throughput delay. The device can be programmed to perform time-slot interchange functions with different throughput delay capabilities on a per-channel basis. For voice applications, variable throughput delay is best as it ensures minimum delay between input and output data. In wideband data applications, constant throughput delay is best as the frame integrity of the information is maintained through the switch.

The delay through the device varies according to the type of throughput delay selected in the MOD bits of the Connection Memory.

VARIABLE DELAY MODE (MOD2-0 = 0-0-0)

In this mode, mostly for voice applications where minimum throughput delay is desired, delay is dependent on the combination of source and destination channels. The minimum delay achievable is a 3 channel periods of the slower data rate.

CONSTANT DELAY MODE (MOD2-0 = 0-0-1)

In this mode, frame integrity is maintained in all switching configurations by making use of a multiple data memory buffer. Input channel data is written into the data memory buffers during frame n and will be read out during frame n+2. In the IDT72V73263, the minimum throughput delay achievable in Constant Delay mode will be one frame plus one channel. See Table 14.

MICROPROCESSOR INTERFACE

The IDT72V73263's microprocessor interface looks like a standard RAM interface to improve integration into a system. With a 16-bit address bus and a 16-bit data bus all memories can be accessed. Using the TSI microprocessor interface, reads and writes are mapped into Data and Connection memories. By allowing the internal memories to be randomly accessed, the controlling microprocessor has more time to manage other peripheral devices and can more easily and quickly gather information and setup the switch paths. Table 1 shows the mapping of the addresses into internal memory blocks. In order to minimize the amount of memory mapped space however, the Memory Select (MS1-0) bits in the Control Register must be written to first to select between the Connection Memory HIGH, the Connection Memory LOW, or Data Memory. Effectively, the Memory Select bits act as an internal mux to select between the Data Memory, Connection Memory HIGH, and Connection Memory LOW.

MEMORY MAPPING

The address bus on the microprocessor interface selects the internal registers and memories of the IDT72V73263. The most significant bit of the address select between the registers and internal memories. See Table 1 for mappings.

As explained in the Initialization section, after system power-up, the TDRSR and RDRSR, should be programmed immediately to establish the desired switching configuration.

The data in the Control Register consists of the Software Reset, RX/TX Bypass, Output Enable Polarity, All Output Enable, Full Block Programming, Block Programming Data, Begin Block Programming Enable, Reset Connection Memory LOW in Block Programming, Output Standby, and Memory Select.

SOFTWARE RESET

The Software Reset serves the same function as the hardware reset. As with the hard reset, the Software Reset must also be set HIGH for 20ns before bringing the Software Reset LOW again for normal operation. Once the Software Reset is LOW, internal registers and other memories may be read or written. During Software Reset, the microprocessor port is still able to read from all

internal memories. The only write operation allowed during a Software Reset is to the Software Reset bit in the Control Register to complete the Software Reset.

CONNECTION MEMORY CONTROL

If the ODE pin and the Output Standby bit are LOW, all output channels will be in three-state. See Table 2 for detail.

If MOD2-0 of the Connection Memory HIGH is 1-0-0 accordingly, the output channel will be in Processor Mode. In this case the lower eight bits of the Connection Memory LOW are output each frame until the MOD2-0 bits are changed. If MOD2-0 of the Connection Memory HIGH are 0-0-1 accordingly, the channel will be in Constant Delay Mode and bits 14-0 are used to address a location in Data Memory. If MOD2-0 of the Connection Memory HIGH are 0-0-0, the channel will be in Variable Delay Mode and bits 14-0 are used to address a location in Data Memory. If MOD2-0 of the Connection Memory HIGH are 1-1-1, the channel will be in High-Impedance mode and that channel will be in three-state.

RX/TX INTERNAL BYPASS

When the Bypass bit of control registers is 1, all RX streams will be "shorted" to TX in effect bypassing all internal circuitry of the TSI. This effectively sets the TSI to a 1-to-1 switch mode with minimal I/O delay. A zero can be written to allow normal operation. The intention of this mode is to minimize the delay from the RX input to the TX output making the TSI "invisible".

INITIALIZATION OF THE IDT72V73263

After power up, the state of the Connection Memory is unknown. As such, the outputs should be put in High-Impedance by holding the ODE pin LOW. While the ODE is LOW, the microprocessor can initialize the device by using the Block Programming feature and program the active paths via the microprocessor bus. Once the device is configured, the ODE pin (or Output Standby bit depending on initialization) can be switched to enable the TSI switch.

TABLE 1—ADDRESS MAPPING

| A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W | Location | Hex Value |
|-----|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|--|-----------------|
| 1 | STA5 | STA4 | STA3 | STA2 | STA1 | STA0 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 | R/W | Internal memory (CM, DM (read only) ⁽¹⁾) | 0x8000-0xFFFF |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | X | X | X | X | X | X | R/W | Control | 0x00XX Register |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | X | X | X | X | X | X | R/W | TDRSR0 | 0x02XX |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | X | X | X | X | X | X | X | X | X | R/W | TDRSR1 | 0x04XX |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | X | X | X | X | X | X | X | X | X | R/W | RDRSR0 | 0x06XX |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | R/W | RDRSR1 | 0x08XX |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | X | X | X | X | X | X | X | X | X | R/W | BPSA | 0x0AXX |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | X | X | X | X | X | X | X | X | X | R/W | BPEA | 0x0CXX |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | X | X | X | X | X | X | X | X | X | R/W | BIS | 0x0EXX |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | X | X | X | X | X | X | X | X | X | R/W | BER | 0x10XX |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | X | X | X | X | X | X | X | X | X | R/W | FOR0 | 0x20XX |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | X | X | X | X | X | X | X | X | X | R/W | FOR1 | 0x22XX |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | X | X | X | X | X | X | X | X | X | R/W | FOR2 | 0x24XX |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | X | X | X | X | X | X | X | X | X | R/W | FOR3 | 0x26XX |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | R/W | FOR4 | 0x28XX |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | X | X | X | X | X | X | X | X | X | R/W | FOR5 | 0x2AXX |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | X | X | X | X | X | X | X | X | X | R/W | FOR6 | 0x2CXX |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | X | X | X | X | X | X | X | X | X | R/W | FOR7 | 0x2EXX |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | X | X | X | X | X | X | X | X | X | R/W | FOR8 | 0x30XX |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | X | X | X | X | X | X | X | X | X | R/W | FOR9 | 0x32XX |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | X | X | X | X | X | X | X | X | X | R/W | FOR10 | 0x34XX |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | X | X | X | X | X | X | X | X | X | R/W | FOR11 | 0x36XX |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | R/W | FOR12 | 0x38XX |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | X | X | X | X | X | X | X | X | X | R/W | FOR13 | 0x3AXX |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | X | X | X | X | X | X | X | X | X | R/W | FOR14 | 0x3CXX |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | X | X | X | X | X | X | X | X | X | R/W | FOR15 | 0x3EXX |

NOTE:

1) Select Connection Memory High, Connection Memory Low, or Data Memory by setting the MS1-0 bits in the Control Register.

TABLE 2—OUTPUT HIGH-IMPEDANCE CONTROL

| MOD2-0 BITS IN CONNECTION MEMORY HIGH | OE X BIT OF TDRSR CONTROL REGISTER | ODE PIN | OSB BIT IN | OUTPUT DRIVER STATUS |
|---------------------------------------|------------------------------------|---------|------------|-------------------------------------|
| 1-1-1 | 1 | X | X | Per Channel High-Impedance |
| Any, other than 1-1-1 | 1 | 0 | 0 | All TX in High-Impedance |
| Any, other than 1-1-1 | 1 | 0 | 1 | Enable |
| Any, other than 1-1-1 | 1 | 1 | 0 | Enable |
| Any, other than 1-1-1 | 1 | 1 | 1 | Enable |
| Any, other than 1-1-1 | 0 | X | X | Group x of OEx is in High-Impedance |

NOTE:

X = Don't Care.

TABLE 3—CONTROL REGISTER (CR) BITS

| Reset Value: 0000H | | | | | | | | | | | | | | | | |
|--------------------|-----|-------|-----|------|------|------|-----|------|------|------|-----|------|-----|-----|-----|--|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| SRS | BYP | OEPOL | AOE | PRST | CBER | SBER | FBP | BPD2 | BPD1 | BPD0 | BPE | RCML | OSB | MS1 | MS0 | |

| BIT | NAME | DESCRIPTION |
|-----|--|--|
| 15 | SRS (Software Reset) | A one will reset the device and have the same effect as the RESET pin. Must be zero for normal operation. |
| 14 | BYP (RX/TX Bypass) | When the Bypass bit is 1, all RX streams will be "shorted" to TX—in effect bypassing all internal circuitry of the TSI. This effectively sets the TSI to a 1-to-1 switch mode with almost only a few nanoseconds of delay. A zero can be written to allow normal operation. The intention of this mode is to minimize the delay from the RX input to the TX output making the TSI "invisible". Any offset values in the FOR register will be required. |
| 13 | OEPOL (Output Enable Polarity) | When 1, a one on OEI pin denotes an active state on the output data stream; zero on OEI pin denotes High-Impedance state. When 0, a one denotes High-Impedance and a zero denotes an active state. OEI mode is entered on a per-group basis in the DRSR. |
| 12 | AOE (All Output Enable) | When 1, all output stream pins (TXn) become OEI to allow for a two-chip solution for a larger switching matrix with OEI pins. When in AOE the DRS must be set to the corresponding data rate of the other device. |
| 11 | PRST (PRBS Reset) | When HIGH, the PRBS transmitter output will be initialized. |
| 10 | CBER (Clear Bit Error Rate) | A low to high transition of this bit clears the BER register (BERR). |
| 9 | SBER (Start Bit Error Rate) | A low to high transition in this bit starts the bit error rate test. The bit error test results is kept in the BER register (BERR). |
| 8 | FBP (Full Block Programming) | When 1, this bit overrides the BPSA and BPEA registers and programs the full Connection Memory space. When 0, the BPSA and BPEA determine the Connection Memory space to be programmed. |
| 7-5 | BPD2-0 (Block Programming Data) | These bits carry the value to be loaded into the Connection Memory block whenever the Connection Memory block programming features is activated. After the BPE bit is set to 1 from 0, the contents of the bits BPD1-0 are loaded into bit 1 and 0 (MOD2-0) of the Connection Memory HIGH. |
| 4 | BPE (Begin Block Programming Enable) | A zero to one transition of this bit enables the Connection Memory block programming feature delimited by the BPSA and BPEA registers as well as for a full block program. Once the BPE bit is set HIGH, the device will program the Connection Memory block as fast as if the user manually programmed each Connection Memory location through the microprocessor. After the programming function has finished, the BPE bit returns to zero to indicate the operation is completed. When the BPE = 1, the BPE bit can be set to 0 to abort block programming. |
| 3 | RCML (Reset Connection Memory LOW in Block Programming) | When RCML = 1, all bits 14-0 in Connection Memory LOW will be reset to zero during block programming; when RCML = 0, bits 14-0 in Connection Memory LOW will retain their original values during block programming. |
| 2 | OSB (Output Standby) | When ODE = 0 and OSB = 0, the output drivers of transmit serial streams are in High-Impedance mode. When either ODE = 1 or OSB = 1, the output serial stream drivers function normally. |
| 1-0 | MS1-0 (Memory Select) | These two bits decide which memory to be accessed via microprocessor port. 00 -- Connection Memory LOW 01 -- Connection Memory HIGH 10 -- Data Memory 11 -- Reserved |

MEMORY BLOCK PROGRAMMING

The IDT72V73263 provides users with the capability of initializing the entire Connection Memory block in two frames. To set bits 2,1 and 0 of every Connection Memory HIGH location, set the Full Block Program to 1, write the desired pattern in to the Block Programming Data Bits (BPD 2). All of the block programming control can be found in the Control Register and enable the Block Program Enable bit.

Enabled by setting the Block Program Enable bit of the Control Register HIGH. When the Block Programming Enable bit of the Control Register is set to HIGH, the Block Programming data will be loaded into the bits 2,1 and 0 of every Connection Memory HIGH location regardless of the selected data rate for the group. The Connection Memory LOW bits will be loaded with zeros when the Reset Connection Memory LOW(RCML) bit is enabled and is otherwise left untouched. When the memory block programming is complete, the device resets the Block Programming Enable and the BPD 2-0 bits to zero.

The IDT72V73263 also incorporates a feature termed Group Block Programming. Group Block Programming, allows subsections of the Connection Memory to be block programmed as if the microprocessor were accessing the Connection Memory HIGH locations in a back-to-back fashion. The results in one connection memory high location being programmed for each C32i clock cycle. By having the TSI perform this function it allows the controlling

microprocessor more time to perform other functions. Also, the TSI can be more efficient in programming the locations since one CMH location is programmed every 32i clock cycles. The group block programming function programs "channel n" for all streams delineated by the group before going to "channel n+1". A C-cycle representation is shown below. The Group Block Programming feature is composed of the Block Programming Start Address(BPSA), the Block Programming End Address(BPEA), and the BPE and BPD bits in the Control Register. The BPSA contains a start address for the block programming and BPEA contains an end address. The block programming will start at the start address and program until the end address even if the end address is "less" than the start address. In other words there is no mechanism to prevent a start address that is larger than the end address. If this occurs, the inverse CM locations in the given group are programmed resulting in a "wrap around" effect. This "wrap around" effect is independent for both the stream and channel addresses. This is illustrated in the Group Block Programming diagram See Figure 1 Group Block Programming Feature. Users must not initiate a block program too close (ahead) of the present transmit location. If this is done the TSI may simultaneously access the CM location that is being modified and unpredictable data on TX outputs may occur. It should be noted however, in order to enable the Group Block Programming the Full Block Program (FBP) must be 0.

TABLE 4—BLOCK PROGRAMMING STARTING ADDRESS (BPSA) REGISTER

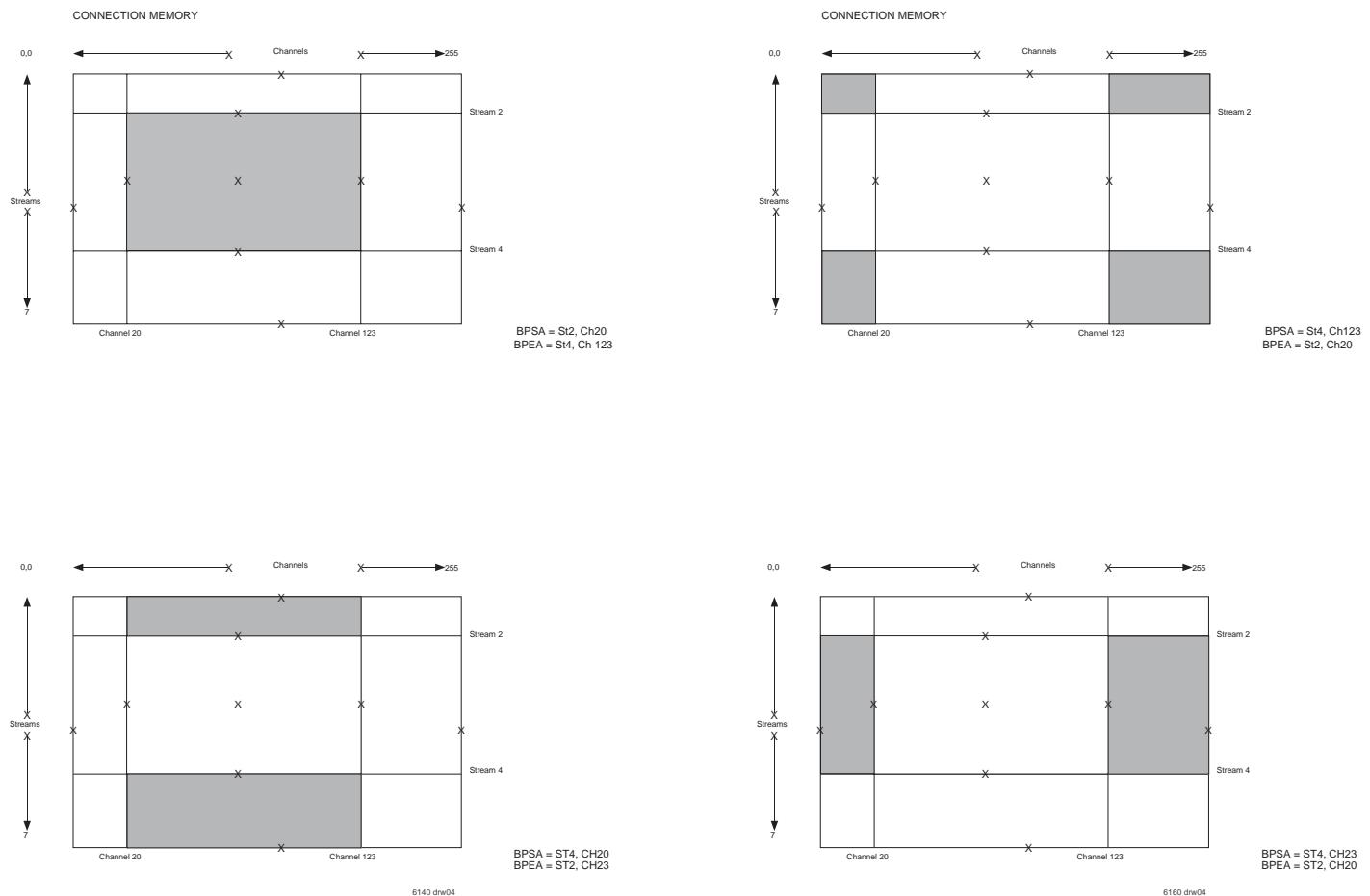
| Reset Value: 0000H | | | | | | | | | | | | | | | | |
|--------------------|----|----|----|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|--|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0 | G2 | G1 | G0 | STA2 | STA1 | STA0 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 | |

| BIT | NAME | DESCRIPTION |
|-------|---|--|
| 15 | Unused | Must be zero for normal operation. |
| 14-12 | G2-0 (Group Address bits 2-0) | These bits are used to select which group will be block programmed |
| 11-9 | STA2-0 (Stream Address bits 2-0) | These bits are used to select starting stream number for block programming. |
| 8-0 | CHA8-0 (Channel Address bits 8-0) | These bits are used to select starting channel number for block programming. |

TABLE 5—BLOCK PROGRAMMING ENDING ADDRESS (BPEA) REGISTER

| Reset Value: FFFFH | | | | | | | | | | | | | | | | |
|--------------------|----|----|----|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|--|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 1 | 1 | 1 | 1 | STA2 | STA1 | STA0 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 | |

| BIT | NAME | DESCRIPTION |
|-------|---|--|
| 15-12 | Unused | Must be one for normal operation. |
| 11-9 | STA2-0 (Stream Address bits 2-0) | These bits are used to select ending stream number for burst programming. |
| 8-0 | CHA8-0 (Channel Address bits 8-0) | These bits are used to select starting channel number for burst programming. |



NOTE:

The group number is defined by the stream address in the BPSA.

Figure 1. Group Block Programming

```

int ST, CH
for (CH = StartChannel; CH <= EndChannel; CH++) {
    for (ST = StartStream; ST <= EndStream; ST++) {
        CMH[ST][CH] = BPD;
    }
}

```

NOTE:

This code is for illustration purposes only. The IDT72V73263 is a HW instantiation of this kind of software.

Figure 2. "Basic Instantiation"

```

/* GroupNum is 0-7 */
/* GroupDataRate = 2, 4, 8, 16. or 32 (2Mb/s, 4Mb/s, 8Mb/s, 16Mb/s, 32Mb/s) */
functional BlockProgram (int GroupNum; int GroupDataRate) {
    int ST, CH;
    int MaxStream = ((GroupNum * 8) + 7);
    int MaxChannel = (((GroupDataRate/2) * 32) - 1);
    /* StartChannel <= EndChannel */
    if (StartChannel <= EndChannel) {
        for (CH = StartChannel; CH <= EndChannel; CH++) {
            /* StartStream <= EndStream and StartChannel <= EndChannel */
            if (StartStream <= EndStream) {
                for (ST = StartStream; ST <= EndStream; ST++) {
                    CMH[ST][CH] = BPD;
                }
            }
            /* StartStream > EndStream and StartChannel <= EndChannel */
            else {
                for (ST = EndStream; ST <= MaxStream; ST++) {
                    CMH[ST][CH] = BPD;
                }
                for (ST = (GroupNum*7); ST <= StartStream; ST++) {
                    CMH[ST][CH] = BPD;
                }
            }
        }
    }
    /* End > Start Channel */
    else {
        /* The last part to be programmed */
        for (CH = EndChannel; CH <= MaxChannel; CH++) {
            /* StartStream > EndStream and StartChannel > EndChannel */
            if (StartStream <= EndStream) {
                for (ST = StartStream; ST <= EndStream; ST++) {
                    CMH[ST][CH] = BPD;
                }
            }
            /* StartStream > EndStream and StartChannel > EndChannel */
            else {
                for (ST = EndStream; ST <= MaxStream; ST++) {
                    CMH[ST][CH] = BPD;
                }
                for (ST = (GroupNum*7); ST <= StartStream; ST++) {
                    CMH[ST][CH] = BPD;
                }
            }
        }
    }
    /* The first part to be programmed */
    for (CH = 0; CH <= StartChannel; CH++) {
        /* StartStream > EndStream and StartChannel > EndChannel */
        if (StartStream <= EndStream) {
            for (ST = StartStream; ST <= EndStream; ST++) {
                CMH[ST][CH] = BPD;
            }
        }
        /* StartStream > EndStream and StartChannel . EndChannel */
        else {
            for (ST = EndStream; ST <= MaxStream; ST++) {
                CMH[ST][CH] = BPD;
            }
            for (ST = (GroupNum*7); ST <= StartStream; ST++) {
                CMH[ST][CH] = BPD;
            }
        }
    }
}

```

NOTE:

This code is for illustration purposes only. The IDT72V73263 is a HW instantiation of this kind of software.

Figure 3. "Real" Instantiation of Memory Block Programming

BIT ERROR RATE

Pseudo-Random Bit Sequences (PRBS) can be independently transmitted and received. By setting the connection memory high bits to the BER transmit mode, that particular channel will transmit a BER pattern of the form $2^{16}-1$. For the receiver only one channel can be specified and monitored at a given time. By setting the BER Input Selection (BIS) to a given channel, every error in the BER sequence will be incremented by one.

If the more than $2^{16}-1$ errors are encountered the BERR register will automatically overflow and be reset to zero. It is important to note that no interrupt or warning will be issued in this case. It is recommended that this register be

polled periodically and reset to prevent an overflow condition. To reset the Pseudo-random bit sequence and the error count registers set the PRST, CBER, and SBER, of the Control Register to high. See the Control Register for details.

Following a write to the BERR register a read of the BERR will result in the present value of the BERR data. Likewise, when the Clear Bit Error Rate bit (CBER) in the control register is activated, this will clear the internal BERR (iBERR).

As a general rule, a read of BERR should be proceeded by a write to BERR. Again, it should be noted that the write to the BERR register will actually initiate a transfer from the iBERR to the BERR while the microprocessor data is ignored.

TABLE 6 — BER INPUT SELECTION REGISTER (BIS)

| Reset Value: Unknown (must be programmed) | | | | | | | | | | | | | | | | |
|---|---|--|-----|------|------|------|------|------|------|------|------|------|------|------|------|--|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0 | BG2 | BG1 | BG0 | BSA2 | BSA1 | BSA0 | BCA8 | BCA7 | BCA6 | BCA5 | BCA4 | BCA3 | BCA2 | BCA1 | BCA0 | |
| BIT NAME DESCRIPTION | | | | | | | | | | | | | | | | |
| 15 | Unused | Must be zero for normal operation | | | | | | | | | | | | | | |
| 14-12 | BG2-BG0 (BER Input Group Address Bits) | These bits refer to the input data group which receives the BER data. | | | | | | | | | | | | | | |
| 11-9 | BSA2-BSA0 (BER Input Stream Address Bits) | These bits refer to the input data stream which receives the BER data. | | | | | | | | | | | | | | |
| 8-0 | BCA8-BCA0 (Local BER Input Channel Address Bits) | These bits refer to the input channel which receives the BER data. | | | | | | | | | | | | | | |

TABLE 7 — BIT ERROR RATE REGISTER (BERR)

| Reset Value: Unknown (must be programmed) | | | | | | | | | | | | | | | | |
|---|---|---|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|--|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| BER15 | BER14 | BER13 | BER12 | BER11 | BER10 | BER9 | BER8 | BER7 | BER6 | BER5 | BER4 | BER3 | BER2 | BER1 | BER0 | |
| BIT NAME DESCRIPTION | | | | | | | | | | | | | | | | |
| 15-0 | BER15-BER0 (Local Bit Error Rate Count Bits) | These bits refer to the local bit error counts. | | | | | | | | | | | | | | |

NOTE:

Before a read of the BERR, a write to the BERR is necessary. As a read only register the write will have no effect. See the Bit Error Rate section for more details.

INPUT FRAME OFFSET SELECTION

Input frame offset selection allows the channel alignment of individual input streams to be offset with respect to the output stream channel alignment. Although all input data comes in at the same speed, delays can be caused by variable path serial backplanes and variable path lengths which may be implemented in large centralized and distributed switching systems. Because data is often

delayed, this feature is useful in compensating for the skew between input streams.

Each input stream can have its own delay offset value by programming the frame input offset registers (FOR, Table 8). The maximum allowable skew is +7.5 clock periods forward with a resolution of $\frac{1}{2}$ clock period, see Table 9. The output streams cannot be adjusted.

TABLE 8 — FRAME INPUT OFFSET REGISTER (FOR) BITS

| Register | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| FOR0 Register | OF32 | OF31 | OF30 | DLE3 | OF22 | OF21 | OF20 | DLE2 | OF12 | OF11 | OF10 | DLE1 | OF02 | OF01 | OF00 | DLE0 |
| FOR1 Register | OF72 | OF71 | OF70 | DLE7 | OF62 | OF61 | OF60 | DLE6 | OF52 | OF51 | OF50 | DLE5 | OF42 | OF41 | OF40 | DLE4 |
| FOR2 Register | OF112 | OF111 | OF110 | DLE11 | OF102 | OF101 | OF100 | DLE10 | OF92 | OF91 | OF90 | DLE9 | OF82 | OF81 | OF80 | DLE8 |
| FOR3 Register | OF152 | OF151 | OF150 | DLE15 | OF142 | OF141 | OF140 | DLE14 | OF132 | OF131 | OF130 | DLE13 | OF122 | OF121 | OF120 | DLE12 |
| FOR4 Register | OF192 | OF191 | OF190 | DLE19 | OF182 | OF181 | OF180 | DLE18 | OF172 | OF171 | OF170 | DLE17 | OF162 | OF161 | OF160 | DLE16 |
| FOR5 Register | OF232 | OF231 | OF230 | DLE23 | OF222 | OF221 | OF220 | DLE22 | OF212 | OF211 | OF210 | DLE21 | OF202 | OF201 | OF200 | DLE20 |
| FOR6 Register | OF272 | OF271 | OF270 | DLE27 | OF262 | OF261 | OF260 | DLE26 | OF252 | OF251 | OF250 | DLE25 | OF242 | OF241 | OF240 | DLE24 |
| FOR7 Register | OF312 | OF311 | OF310 | DLE31 | OF302 | OF301 | OF300 | DLE30 | OF292 | OF291 | OF290 | DLE29 | OF282 | OF281 | OF280 | DLE28 |
| FOR8 Register | OF352 | OF351 | OF350 | DLE35 | OF342 | OF341 | OF340 | DLE34 | OF332 | OF331 | OF330 | DLE33 | OF322 | OF321 | OF320 | DLE32 |
| FOR9 Register | OF392 | OF391 | OF390 | DLE39 | OF382 | OF381 | OF380 | DLE38 | OF372 | OF371 | OF370 | DLE37 | OF362 | OF361 | OF360 | DLE36 |
| FOR10 Register | OF432 | OF431 | OF430 | DLE43 | OF422 | OF421 | OF420 | DLE42 | OF412 | OF411 | OF410 | DLE41 | OF402 | OF401 | OF400 | DLE40 |
| FOR11 Register | OF472 | OF471 | OF470 | DLE47 | OF462 | OF461 | OF460 | DLE46 | OF452 | OF451 | OF450 | DLE45 | OF442 | OF441 | OF440 | DLE44 |
| FOR12 Register | OF512 | OF511 | OF510 | DLE51 | OF502 | OF501 | OF500 | DLE50 | OF492 | OF491 | OF490 | DLE49 | OF482 | OF481 | OF480 | DLE48 |
| FOR13 Register | OF552 | OF551 | OF550 | DLE55 | OF542 | OF541 | OF540 | DLE54 | OF532 | OF531 | OF530 | DLE53 | OF522 | OF521 | OF520 | DLE52 |
| FOR14 Register | OF592 | OF591 | OF590 | DLE59 | OF582 | OF581 | OF580 | DLE58 | OF572 | OF571 | OF570 | DLE57 | OF562 | OF561 | OF560 | DLE56 |
| FOR15 Register | OF632 | OF631 | OF630 | DLE63 | OF622 | OF621 | OF620 | DLE62 | OF612 | OF611 | OF610 | DLE61 | OF602 | OF601 | OF600 | DLE60 |

| NAME | DESCRIPTION | |
|--|---|--|
| OFn2, OFn1, OFn0 (Offset Bits 2, 1 & 0) | These three bits define how long the serial interface receiver takes to recognize and store bit 0 from the RX input pin: i.e., to start a new frame. The input frame offset can be selected to +7.5 clock periods from the point where the external frame pulse input signal is applied to the FOi input of the device. | |
| DLEn (DataLatch Edge) | ST-BUS® and DLEn = 0, offset is on the clock boundary. GCI mode: DLEn = 1, offset is a half cycle off of the clock boundary. | |

TABLE 9 — OFFSET BITS (OFN2, OFN1, OFN0, DLEN) & FRAME DELAY BITS (FD11, FD2-0)

| INPUT STREAM OFFSET CLOCK PERIOD SHIFT BASED ON 32.768MHZ CLOCK | | | | | CORRESPONDING OFFSET BITS | | | | |
|--|------------|-----------|-----------|-----------|------------------------------|------|------|------|--|
| 32.768Mb/s | 16.384Mb/s | 8.192Mb/s | 4.096Mb/s | 2.048Mb/s | OFn2 | OFn1 | OFn0 | DLEn | |
| None | None | None | None | None | 0 | 0 | 0 | 0 | |
| + 0.5 | + 1.0 | + 1.0 | + 2.0 | + 4.0 | 0 | 0 | 0 | 1 | |
| + 1.0 | + 2.0 | + 2.0 | + 4.0 | + 8.0 | 0 | 0 | 1 | 0 | |
| + 1.5 | + 3.0 | + 3.0 | + 6.0 | + 12.0 | 0 | 0 | 1 | 1 | |
| + 2.0 | + 4.0 | + 4.0 | + 8.0 | + 16.0 | 0 | 1 | 0 | 0 | |
| + 2.5 | + 5.0 | + 5.0 | + 10.0 | + 20.0 | 0 | 1 | 0 | 1 | |
| + 3.0 | + 6.0 | + 6.0 | + 12.0 | + 24.0 | 0 | 1 | 1 | 0 | |
| + 3.5 | + 7.0 | + 7.0 | + 14.0 | + 28.0 | 0 | 1 | 1 | 1 | |
| • • • • • | | | | | | | | | |
| + 7.5 | + 15.0 | + 15.0 | + 30.0 | + 60.0 | 1 | 1 | 1 | 1 | |

Examples for Input Offset Delay Timing

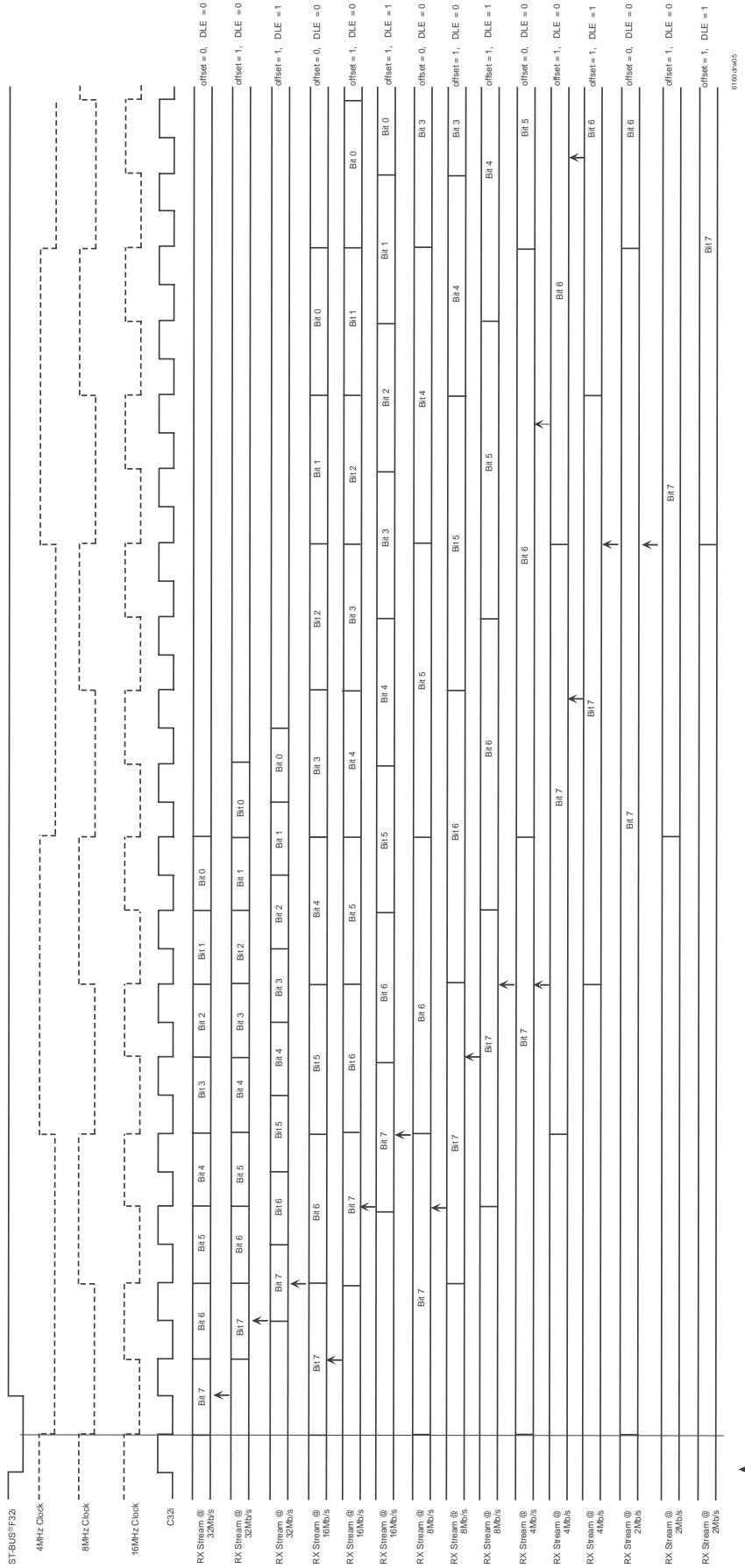


Figure 4. ST-BUS® Offset Timing

↑ NOTE: denotes sample point of RX Data

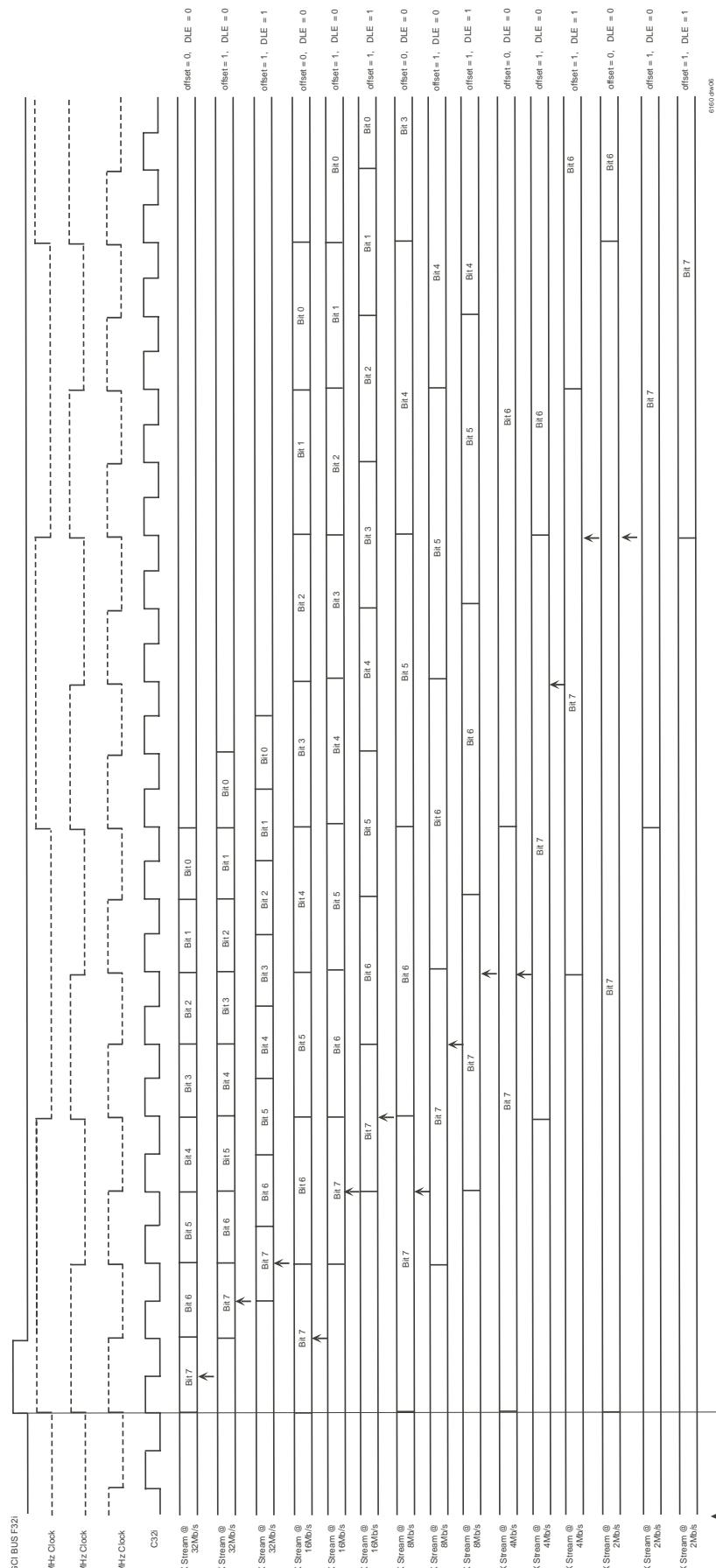
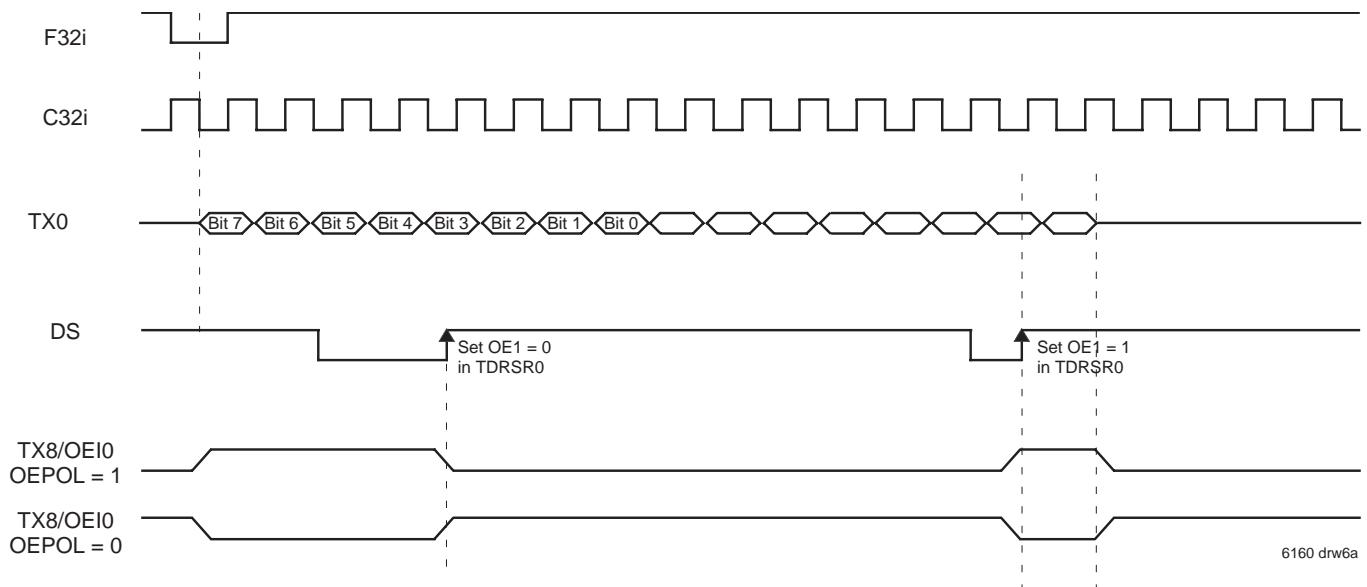


Figure 5. GC/Offset Timing

OUTPUT ENABLE INDICATION

The IDT72V73263 has the capability to indicate the state of the outputs (active or three-state) by enabling the Output Enable Indication in the DRSR. In the

Output Enable Indication mode however, those output streams cannot be used to transmit CM or DM data only OE data. In the diagram below notice how the transmitting stream, TX0 is unaffected by the enabling and disabling of the OE stream (TX8).



NOTE:

The TX0-7 pins are unaffected by the OE1 Change.

Figure 6. The Effect of Enabling and Disabling of the OE Bit in TDRSR

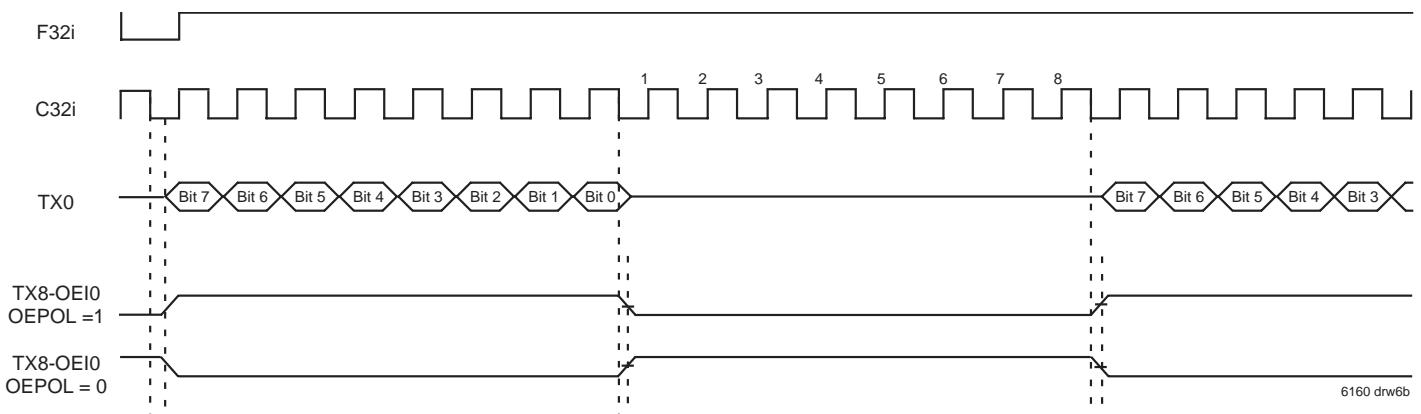


Figure 7. OEI Function

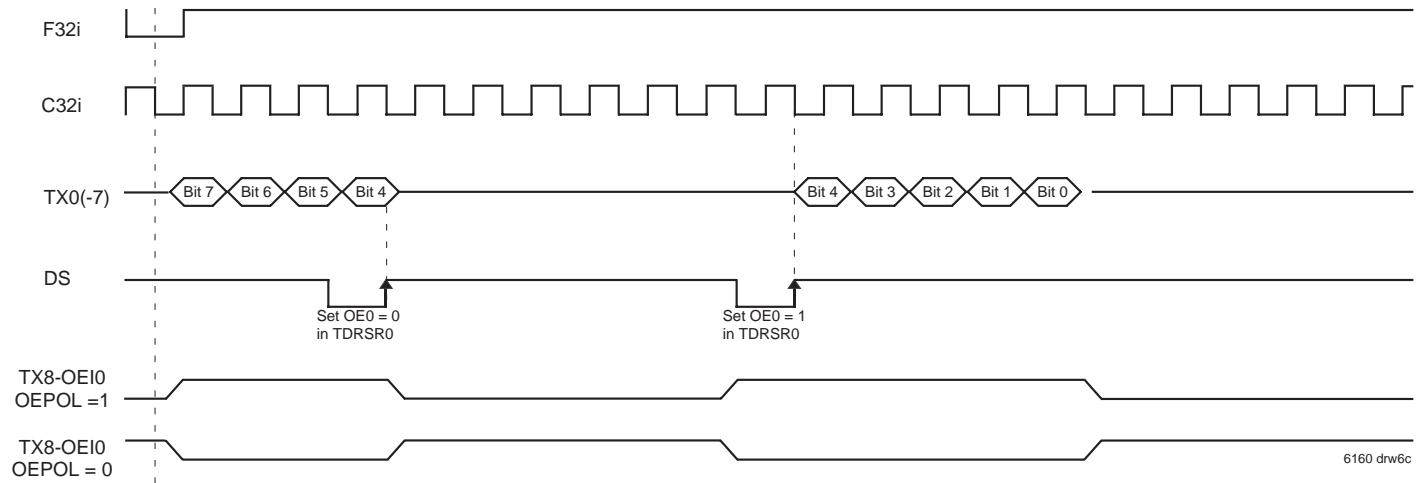


Figure 8. Group OE Operation

TABLE 10 — TRANSMIT DATA RATE SELECTION REGISTER (TDRSR)

| | | | | | | | | | | | | | | | |
|------------------|-------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Reset Value: | 0000H | | | | | | | | | | | | | | |
| TX DRSR 1 | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OE7 | G72 | G71 | G70 | OE6 | G62 | G61 | G60 | OE5 | G52 | G52 | G51 | OE4 | G42 | G41 | G40 |
| TX DRSR 0 | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OE3 | G32 | G31 | G30 | OE2 | G22 | G21 | G20 | OE1 | G12 | G11 | G10 | OE0 | G02 | G01 | G00 |

| | | | | |
|--------------------|--|--------------------|-------------------------|--|
| OEx | These bits can be used to High-Z the entire associated group. If OEx = 0 the group will be in High-Z. If OEx =1, the group is in Low-Z (active state). | | | |
| Gx2-Gx0 | These three group bits are used to select the transmit data rates for the eight groups of eight streams. See table 11 for data rates. | | | |
| Gx2 ⁽¹⁾ | Gx1 ⁽¹⁾ | Gx0 ⁽¹⁾ | Data Rate | |
| 0 | 0 | 0 | 2.048Mb/s | |
| 0 | 0 | 1 | 4.096Mb/s | |
| 0 | 1 | 0 | 8.192Mb/s | |
| 0 | 1 | 1 | 16.384Mb/s | |
| 1 | 0 | 0 | 32.768Mb/s | |
| 1 | 0 | 1 | Reserved ⁽²⁾ | |
| 1 | 1 | 0 | Reserved ⁽²⁾ | |
| 1 | 1 | 1 | OE ⁽³⁾ | |

If G0/G2/G4/G6 are programmed to be run at 32.768Mb/s, then G1/G3/G5/G7 will be unavailable, respectively, except for OEI purposes. In other words if G0 is programmed for 32.768Mb/s, G1 will only be available for OEI.

NOTES:

1. "x" corresponds to groups 0-7 (8 Data streams per group).
2. If the Gx2-0 are programmed to the reserved values the device will operate in the default 2.048Mb/s mode.
3. Only odd groups can be programmed for OEI. The OEI rate corresponds it's associated even group.

TABLE 11 — TX GROUPING AND DATA RATES

| GROUP NUMBER | STREAMS | SPEED | WITH OEI=1 |
|--------------|---------|----------------------|----------------------|
| G0 | 0-7 | 2.048Mb/s-32.768Mb/s | 2.048Mb/s-32.768Mb/s |
| G1 | 8-15 | 2.048Mb/s-32.768Mb/s | OEI<0-7> |
| G2 | 16-23 | 2.048Mb/s-32.768Mb/s | 2.048Mb/s-32.768Mb/s |
| G3 | 24-31 | 2.048Mb/s-32.768Mb/s | OEI<16-23> |
| G4 | 32-39 | 2.048Mb/s-32.768Mb/s | 2.048Mb/s-32.768Mb/s |
| G5 | 40-47 | 2.048Mb/s-32.768Mb/s | OEI<32-39> |
| G6 | 48-55 | 2.048Mb/s-32.768Mb/s | 2.048Mb/s-32.768Mb/s |
| G7 | 56-63 | 2.048Mb/s-32.768Mb/s | OEI<48-55> |

TABLE 12— RECEIVE DATA RATE SELECTION REGISTER(RDRSR)

| | | | | | | | | | | | | | | | |
|------------------|-------|-----|-----|----|-----|-----|-----|---|-----|-----|-----|---|-----|-----|-----|
| Reset Value: | 0000H | | | | | | | | | | | | | | |
| RX DRSR 1 | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | G72 | G71 | G70 | 0 | G62 | G61 | G60 | 0 | G52 | G51 | G50 | 0 | G42 | G41 | G40 |
| RX DRSR 0 | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | G32 | G31 | G30 | 0 | G22 | G21 | G20 | 0 | G12 | G11 | G10 | 0 | G02 | G01 | G00 |

| Gx0-Gx2 | These three group bits are used to select the receive data rates for the eight groups of eight streams. See table 13 for data rates. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------------|--|--------------------|-------------------------|--------------------|-----------|---|---|---|-----------|---|---|---|-----------|---|---|---|-----------|---|---|---|------------|---|---|---|------------|---|---|---|-------------------------|---|---|---|-------------------------|---|---|---|-------------------------|
| | <table> <thead> <tr> <th>Gx2⁽¹⁾</th> <th>Gx1⁽¹⁾</th> <th>Gx0⁽¹⁾</th> <th>Data Rate</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>2.048Mb/s</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>4.096Mb/s</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>8.192Mb/s</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>16.384Mb/s</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>32.768Mb/s</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Reserved⁽²⁾</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Reserved⁽²⁾</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Reserved⁽²⁾</td> </tr> </tbody> </table> | Gx2 ⁽¹⁾ | Gx1 ⁽¹⁾ | Gx0 ⁽¹⁾ | Data Rate | 0 | 0 | 0 | 2.048Mb/s | 0 | 0 | 1 | 4.096Mb/s | 0 | 1 | 0 | 8.192Mb/s | 0 | 1 | 1 | 16.384Mb/s | 1 | 0 | 0 | 32.768Mb/s | 1 | 0 | 1 | Reserved ⁽²⁾ | 1 | 1 | 0 | Reserved ⁽²⁾ | 1 | 1 | 1 | Reserved ⁽²⁾ |
| Gx2 ⁽¹⁾ | Gx1 ⁽¹⁾ | Gx0 ⁽¹⁾ | Data Rate | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 2.048Mb/s | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 4.096Mb/s | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 8.192Mb/s | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 16.384Mb/s | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 32.768Mb/s | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | Reserved ⁽²⁾ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | Reserved ⁽²⁾ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | Reserved ⁽²⁾ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

If G0/G2/G4/G6 are programmed to be run at 32.768Mb/s, then G1/G3/G5/G7 will be unavailable, respectively, except for OEI purposes. In other words if G0 is programmed for 32.768Mb/s, G1 will only be available for OEI.

NOTES:

1. "x" corresponds to groups 0-7 (8 Data streams per group).
2. If the Gx2-0 are programmed to the reserved values the device will operate in the default 2.048Mb/s mode.
3. Only odd groups can be programmed for OEI. The OEI rate corresponds to it's associated even group.

TABLE 13— RX GROUPING AND DATA RATES

| GROUP NUMBER | STREAMS | SPEED |
|--------------|---------|----------------------|
| G0 | 0-7 | 2.048Mb/s-32.768Mb/s |
| G1 | 8-15 | 2.048Mb/s-32.768Mb/s |
| G2 | 16-23 | 2.048Mb/s-32.768Mb/s |
| G3 | 24-31 | 2.048Mb/s-32.768Mb/s |
| G4 | 32-39 | 2.048Mb/s-32.768Mb/s |
| G5 | 40-47 | 2.048Mb/s-32.768Mb/s |
| G6 | 48-55 | 2.048Mb/s-32.768Mb/s |
| G7 | 56-63 | 2.048Mb/s-32.768Mb/s |

TABLE 14— CONNECTION MEMORY HIGH

| Reset Value: Unknown (must be programmed) | | | | | | | | | | | | | | | | |
|---|----|----|----|----|----|---|---|---|---|---|---|---|------|------|------|--|
| | | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MOD2 | MOD1 | MOD0 | |

| BIT | NAME | DESCRIPTION | | | |
|------|--------|------------------------------------|------|------|---------------------|
| 15-3 | Unused | Must be zero for normal operation. | | | |
| 2-0 | MOD2-0 | MOD2 | MOD1 | MOD0 | MODE |
| | | 0 | 0 | 0 | Variable Delay Mode |
| | | 0 | 0 | 1 | Constant Delay Mode |
| | | 0 | 1 | 0 | Reserved |
| | | 0 | 1 | 1 | Reserved |
| | | 1 | 0 | 0 | Processor Mode |
| | | 1 | 0 | 1 | Bit Error Rate Test |
| | | 1 | 1 | 0 | Reserved |
| | | 1 | 1 | 1 | High-Impedance |

TABLE 15— CONNECTION MEMORY LOW

| Reset Value: Unknown (must be programmed) | | | | | | | | | | | | | | | | |
|---|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|--|
| | | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0 | SAB5 | SAB4 | SAB3 | SAB2 | SAB1 | SAB0 | CAB8 | CAB7 | CAB6 | CAB5 | CAB4 | CAB3 | CAB2 | CAB1 | CAB0 | |

| BIT | NAME | DESCRIPTION | | | |
|------|---|---|--|--|--|
| 15 | Unused | Must be zero for normal operation | | | |
| 14-9 | SAB5-0 (Source Stream Address Bits) | The binary value is the number of the data stream for the source of the connection. | | | |
| 8-0 | CAB8-0 (Source Channel Address Bits) | The binary value is the number of the channel for the source of the connection. | | | |

NOTES:

1. When running the device at lower bit rates (i.e. 2, 4, 8, or 16.384Mb/s), make sure the bits corresponding to the unused channels are set to 0.
2. When G0/G2/G4/G6 are programmed for 32.768Mb/s operation its corresponding group G1/G3/G5/F7 will be unavailable.
3. In processor mode, data in the lower byte (bits0-7) of the Connection Memory LOW will be output to the TX streams. The order in which the data are output will be starting from the LSB (Bit 0) to the MSB (Bit 7) of the lower byte. The figure below illustrates the sequence:

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | H | G | F | E | D | C | B | A |

Figure 9. Processor Mode Bit Sequencing

TABLE 16 — BOUNDARY SCAN REGISTER BITS

| Device Pin | Boundary Scan Bit 0 to 267 | | |
|------------|----------------------------|------------------|---------------------|
| | Input Scan Cell | Output Scan Cell | Three-state Control |
| ODE | 0 | | |
| RESET | 1 | | |
| C32i | 2 | | |
| F32i | 3 | | |
| S/A | 4 | | |
| DS | 5 | | |
| CS | 6 | | |
| R/W | 7 | | |
| A0 | 8 | | |
| A1 | 9 | | |
| A2 | 10 | | |
| A3 | 11 | | |
| A4 | 12 | | |
| A5 | 13 | | |
| A6 | 14 | | |
| A7 | 15 | | |
| A8 | 16 | | |
| A9 | 17 | | |
| A10 | 18 | | |
| A11 | 19 | | |
| A12 | 20 | | |
| A13 | 21 | | |
| A14 | 22 | | |
| A15 | 23 | | |
| BEL | 24 | | |
| DTA/BEH | 25 | 26 | 27 |
| D15 | 28 | 29 | 30 |
| D14 | 31 | 32 | 33 |
| D13 | 34 | 35 | 36 |
| D12 | 37 | 38 | 39 |
| D11 | 40 | 41 | 42 |
| D10 | 43 | 44 | 45 |
| D9 | 46 | 47 | 48 |
| D8 | 49 | 50 | 51 |
| D7 | 52 | 53 | 54 |
| D6 | 55 | 56 | 57 |
| D5 | 58 | 59 | 60 |
| D4 | 61 | 62 | 63 |
| D3 | 64 | 65 | 66 |
| D2 | 67 | 68 | 69 |
| D1 | 70 | 71 | 72 |
| D0 | 73 | 74 | 75 |
| RX63 | 76 | | |
| RX62 | 77 | | |
| RX61 | 78 | | |

| Device Pin | Boundary Scan Bit 0 to 267 | | |
|------------|----------------------------|------------------|---------------------|
| | Input Scan Cell | Output Scan Cell | Three-state Control |
| RX60 | 79 | | |
| RX59 | 80 | | |
| RX58 | 81 | | |
| RX57 | 82 | | |
| RX56 | 83 | | |
| TX63/OEI31 | | 84 | 85 |
| TX62/OEI30 | | 86 | 87 |
| TX61/OEI29 | | 88 | 89 |
| TX60/OEI28 | | 90 | 91 |
| TX59/OEI27 | | 92 | 93 |
| TX58/OEI26 | | 94 | 95 |
| TX57/OEI25 | | 96 | 97 |
| TX56/OEI24 | | 98 | 99 |
| TX55/OEI23 | | 100 | 101 |
| TX54/OEI22 | | 102 | 103 |
| TX53/OEI21 | | 104 | 105 |
| TX52/OEI20 | | 106 | 107 |
| TX51/OEI19 | | 108 | 109 |
| TX50/OEI18 | | 110 | 111 |
| TX49/OEI17 | | 112 | 113 |
| TX48/OEI16 | | 114 | 115 |
| RX55 | 116 | | |
| RX54 | 117 | | |
| RX53 | 118 | | |
| RX52 | 119 | | |
| RX51 | 120 | | |
| RX50 | 121 | | |
| RX49 | 122 | | |
| RX48 | 123 | | |
| RX47 | 124 | | |
| RX46 | 125 | | |
| RX45 | 126 | | |
| RX44 | 127 | | |
| RX43 | 128 | | |
| RX42 | 129 | | |
| RX41 | 130 | | |
| RX40 | 131 | | |
| TX47/OEI15 | | 132 | 133 |
| TX46/OEI14 | | 134 | 135 |
| TX45/OEI13 | | 136 | 137 |
| TX44/OEI12 | | 138 | 139 |
| TX43/OEI11 | | 140 | 141 |
| TX42/OEI10 | | 142 | 143 |
| TX41/OEI9 | | 144 | 145 |
| TX40/OEI8 | | 146 | 147 |

TABLE 16 — BOUNDARY SCAN REGISTER BITS (CONTINUED)

| Device Pin | Boundary Scan Bit 0 to 267 | | |
|------------|----------------------------|------------------|---------------------|
| | Input Scan Cell | Output Scan Cell | Three-state Control |
| TX39/OEI7 | | 148 | 149 |
| TX38/OEI6 | | 150 | 151 |
| TX37/OEI5 | | 152 | 153 |
| TX36/OEI4 | | 154 | 155 |
| TX35/OEI3 | | 156 | 157 |
| TX34/OEI2 | | 158 | 159 |
| TX33/OEI1 | | 160 | 161 |
| TX32/OEI0 | | 162 | 163 |
| RX39 | 164 | | |
| RX38 | 165 | | |
| RX37 | 166 | | |
| RX36 | 167 | | |
| RX35 | 168 | | |
| RX34 | 169 | | |
| RX33 | 170 | | |
| RX32 | 171 | | |
| RX31 | 172 | | |
| RX30 | 173 | | |
| RX29 | 174 | | |
| RX28 | 175 | | |
| RX27 | 176 | | |
| RX26 | 177 | | |
| RX25 | 178 | | |
| RX24 | 179 | | |
| TX31 | | 180 | 181 |
| TX30 | | 182 | 183 |
| TX29 | | 184 | 185 |
| TX28 | | 186 | 187 |
| TX27 | | 188 | 189 |
| TX26 | | 190 | 191 |
| TX25 | | 192 | 193 |
| TX24 | | 194 | 195 |
| TX23 | | 196 | 197 |
| TX22 | | 198 | 199 |
| TX21 | | 200 | 201 |
| TX20 | | 202 | 203 |
| TX19 | | 204 | 205 |
| TX18 | | 206 | 207 |
| TX17 | | 208 | 209 |
| TX16 | | 210 | 211 |
| RX23 | 212 | | |
| RX22 | 213 | | |
| RX21 | 214 | | |
| RX20 | 215 | | |

| Device Pin | Boundary Scan Bit 0 to 267 | | |
|------------|----------------------------|------------------|---------------------|
| | Input Scan Cell | Output Scan Cell | Three-state Control |
| RX19 | 216 | | |
| RX18 | 217 | | |
| RX17 | 218 | | |
| RX16 | 219 | | |
| RX15 | 220 | | |
| RX14 | 221 | | |
| RX13 | 222 | | |
| RX12 | 223 | | |
| RX11 | 224 | | |
| RX10 | 225 | | |
| RX9 | 226 | | |
| RX8 | 227 | | |
| TX15 | | 228 | 229 |
| TX14 | | 230 | 231 |
| TX13 | | 232 | 233 |
| TX12 | | 234 | 235 |
| TX11 | | 236 | 237 |
| TX10 | | 238 | 239 |
| TX9 | | 240 | 241 |
| TX8 | | 242 | 243 |
| TX7 | | 244 | 245 |
| TX6 | | 246 | 247 |
| TX5 | | 248 | 249 |
| TX4 | | 250 | 251 |
| TX3 | | 252 | 253 |
| TX2 | | 254 | 255 |
| TX1 | | 256 | 257 |
| TX0 | | 258 | 259 |
| RX7 | 260 | | |
| RX6 | 261 | | |
| RX5 | 262 | | |
| RX4 | 263 | | |
| RX3 | 264 | | |
| RX2 | 265 | | |
| RX1 | 266 | | |
| RX0 | 267 | | |

JTAG SUPPORT

The IDT72V73263 JTAG interface conforms to the Boundary-Scan standard IEEE-1149.1. This standard specifies a design-for-testability technique called Boundary-Scan test (BST). The operation of the boundary-scan circuitry is controlled by an external test access port (TAP) Controller.

TEST ACCESS PORT (TAP)

The Test Access Port (TAP) provides access to the test functions of the IDT72V73263. It consists of three input pins and one output pin.

- Test Clock Input (TCK)

TCK provides the clock for the test logic. The TCK does not interfere with any on-chip clock and thus remains independent. The TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrently with the operation of the device and without interfering with the on-chip logic.

- Test Mode Select Input (TMS)

The logic signals received at the TMS input are interpreted by the TAP Controller to control the test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to VCC when it is not driven from an external source.

- Test Data Input (TDI)

Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. Both registers are described in a subsequent section. The received input data is sampled at the rising edge of TCK pulses. This pin is internally pulled to VCC when it is not driven from an external source.

- Test Data Output (TDO)

Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or data register are serially shifted out through the TDO pin on the falling edge of each TCK pulse. When no data is shifted through the boundary scan cells, the TDO driver is set to a High-Impedance state.

- Test Reset (TRST)

Reset the JTAG scan structure. This pin is internally pulled to VCC when it is not driven from an external source.

INSTRUCTION REGISTER

In accordance with the IEEE-1149.1 standard, the IDT72V73263 uses public instructions. The IDT72V73263 JTAG interface contains a four-bit instruction register. Instructions are serially loaded into the instruction register from the TDI when the TAP Controller is in its shift-IR state. Subsequently, the instructions are decoded to achieve two basic functions: to select the test data register that may operate while the instruction is current, and to define the serial test data register path, which is used to shift data between TDI and TDO during data register scanning. See Table 12 for Instruction decoding.

TEST DATA REGISTER

As specified in IEEE-1149.1, the IDT72V73263 JTAG Interface contains two test data registers:

- The Boundary-Scan register

The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of the IDT72V73263 core logic.

- The Bypass Register

The Bypass register is a single stage shift register that provides a one-bit path from TDI to TDO. The IDT72V73263 boundary scan register bits are shown in Table 14. Bit 0 is the first bit clocked out. All three-state enable bits are active HIGH.

ID CODE REGISTER

As specified in IEEE-1149.1, this instruction loads the IDR with the Revision Number, Device ID, JEDEC ID, and ID Register Indicator Bit. See Table 10.

TABLE 17—IDENTIFICATION REGISTER DEFINITIONS

| INSTRUCTION FIELD | VALUE | DESCRIPTION |
|-----------------------------------|--------|--|
| Revision Number (31:28) | 0x0 | Reserved for version number |
| IDT Device ID (27:12) | 0x0430 | Defines IDT part number |
| IDT JEDEC ID (11:1) | 0x33 | Allows unique identification of device vendor as IDT |
| ID Register Indicator Bit (Bit 0) | 1 | Indicates the presence of an ID register |

TABLE 18—SCAN REGISTER SIZES

| REGISTER NAME | BIT SIZE |
|----------------------|----------|
| Instruction (IR) | 4 |
| Bypass (BYR) | 1 |
| Identification (IDR) | 32 |
| Boundary Scan (BSR) | Note(1) |

NOTE:

1. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website (www.idt.com), or by contacting your local IDT sales representative.

TABLE 19—SYSTEM INTERFACE PARAMETERS

| INSTRUCTION | CODE | DESCRIPTION |
|----------------|-----------------|---|
| EXTEST | 0000 | Forces contents of the boundary scan cells onto the device outputs ⁽¹⁾ . Places the boundary scan register (BSR) between TDI and TDO. |
| BYPASS | 1111 | Places the bypass register (BYR) between TDI and TDO. |
| IDCODE | 0010 | Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO. |
| HIGH-Z | 0011 | Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state. |
| SAMPLE/PRELOAD | 0001 | Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs ⁽²⁾ and outputs ⁽¹⁾ to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI. |
| RESERVED | All other codes | Several combinations are reserved. Do not use other codes than those identified above. |

NOTES:

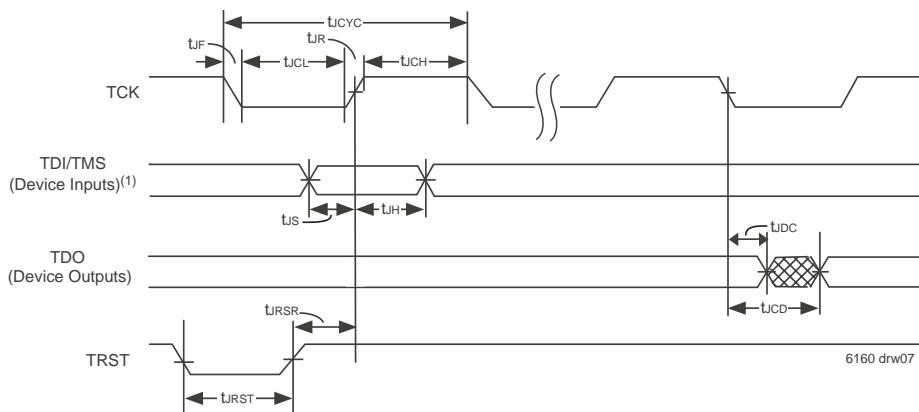
1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS and TRST.

TABLE 20—JTAG AC ELECTRICAL CHARACTERISTICS (1,2,3,4)

| SYMBOL | PARAMETER | MIN. | MAX. | UNITS |
|-------------------|-------------------------|------|------------------|-------|
| t _{JCYC} | JTAG Clock Input Period | 100 | — | ns |
| t _{JCH} | JTAG Clock HIGH | 40 | — | ns |
| t _{JCL} | JTAG Clock LOW | 40 | — | ns |
| t _{JR} | JTAG Clock Rise Time | — | 3 ⁽¹⁾ | ns |
| t _{JF} | JTAG Clock Fall Time | — | 3 ⁽¹⁾ | ns |
| t _{JRST} | JTAG Reset | 50 | — | ns |
| t _{JRSR} | JTAG Reset Recovery | 50 | — | ns |
| t _{JCD} | JTAG Data Output | — | 25 | ns |
| t _{JDC} | JTAG Data Output Hold | 0 | — | ns |
| t _{JS} | JTAG Setup | 15 | — | ns |
| t _{JH} | JTAG Hold | 15 | — | ns |

NOTES:

1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.



NOTES:

1. Device inputs = All device inputs except TDI, TMS and TRST.

Figure 10. JTAG Timing Specifications

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Min. | Max. | Unit |
|-----------------|----------------------------|----------|----------------------|------|
| V _{CC} | Supply Voltage | -0.5 | +4.0 | V |
| V _I | Voltage on Digital Inputs | GND -0.3 | V _{CC} +0.3 | V |
| I _O | Current at Digital Outputs | -50 | 50 | mA |
| T _S | Storage Temperature | -55 | +125 | °C |
| P _D | Package Power Dissipation | — | 2 | W |

NOTE:

1. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------------------------------|--------------------|------|------|-----------------|------|
| V _{CC} | Positive Supply | 3.0 | 3.3 | 3.6 | V |
| V _{IH} ⁽¹⁾ | Input HIGH Voltage | 2.0 | — | V _{CC} | V |
| V _{IL} | Input LOW Voltage | -0.3 | — | 0.8 | V |

NOTES:

1. Inputs/Outputs are not 5V tolerant
2. Voltages are with respect to ground (GND) unless otherwise stated.

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|----------------------------------|----------------------------|------|------|------|-------|
| I _{CC} ⁽²⁾ | Supply Current | — | — | 380 | mA |
| I _{IL} ^(3,4) | Input Leakage (input pins) | — | — | 60 | µA |
| I _{BL} ^(3,4) | Input Leakage (I/O pins) | — | — | 60 | µA |
| I _{OZ} ^(3,4) | High-Impedance Leakage | — | — | 60 | µA |
| V _{OH} ⁽⁵⁾ | Output HIGH Voltage | 2.4 | — | — | V |
| V _{OL} ⁽⁶⁾ | Output LOW Voltage | — | — | 0.4 | V |

NOTES:

1. Voltages are with respect to ground (GND) unless otherwise stated.
2. Outputs unloaded.
3. $0 \leq V \leq V_{CC}$.
4. Maximum leakage on pins (output or I/O pins in High-Impedance state) is over an applied voltage (V).
5. IOH = 10 mA.
6. IOL = 10 mA.

AC ELECTRICAL CHARACTERISTICS - TIMING PARAMETER MEASUREMENT VOLTAGE LEVELS

| Symbol | Rating | Level | Unit |
|-------------------------------|--------------------------------------|-------|------|
| V _{TT} | TTL Threshold | 1.5 | V |
| V _{HM} | TTL Rise/Fall Threshold Voltage HIGH | 2.0 | V |
| V _{LM} | TTL Rise/Fall Threshold Voltage LOW | 0.8 | V |
| | Input Pulse Levels | — | V |
| t _{r,tf} | Input Rise/Fall Times | 1 | ns |
| | Input Timing Reference Levels | — | V |
| | Output Reference Levels | — | V |
| C _L ⁽¹⁾ | Output Load | 50 | pF |

NOTE:

1. JTAG CL is 30pF

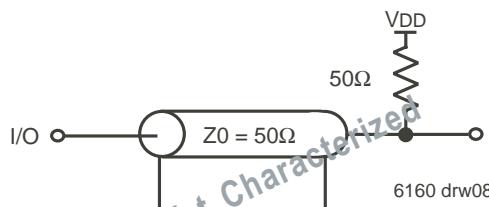


Figure 11. AC Termination

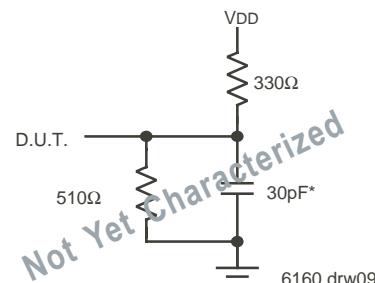


Figure 12. AC Test Load

AC ELECTRICAL CHARACTERISTICS - RESET AND ODE TIMING

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|-------------|-------------------------------------|------|------|------|-------|
| t_{RZ} | Active to High-Z on Master Reset | — | — | 12 | ns |
| t_{RS} | Reset Pulse Width | 20 | — | — | ns |
| t_{ODELZ} | Output Driver Enable (ODE) to Low-Z | 6 | — | — | ns |

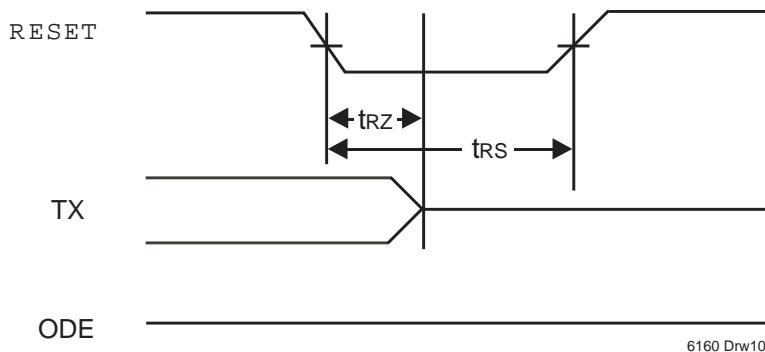


Figure 13. Reset and ODE Timing

AC ELECTRICAL CHARACTERISTICS - C32i AND ODE TO HIGH-Z TIMING AND C32i AND ODE TO LOW-Z TIMING

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|-----------------|--------------------------------------|------|------|------|-------|
| $t_{CLZ}^{(1)}$ | Clock to Low-Z | 3 | — | — | ns |
| $t_{CHZ}^{(1)}$ | Clock to High-Z | — | — | 9 | ns |
| t_{ODEA} | ODE to Valid Data | 6 | — | — | ns |
| t_{ODEHZ} | Output Driver Enable (ODE) to High-Z | 3 | — | 9 | ns |
| t_{ODELZ} | Output Driver Enable (ODE) to Low-Z | 4 | — | — | ns |
| $t_{SIH}^{(1)}$ | RX Hold Time | 4 | — | — | ns |
| t_{SOD} | Clock to Valid Data | 3 | 7 | 9 | ns |

NOTE:

1. $C_L = 30\text{pF}$.

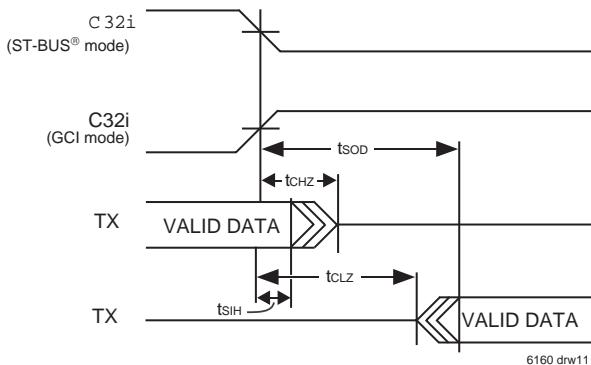


Figure 14. Serial Output and External Control

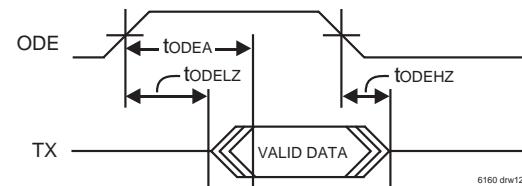


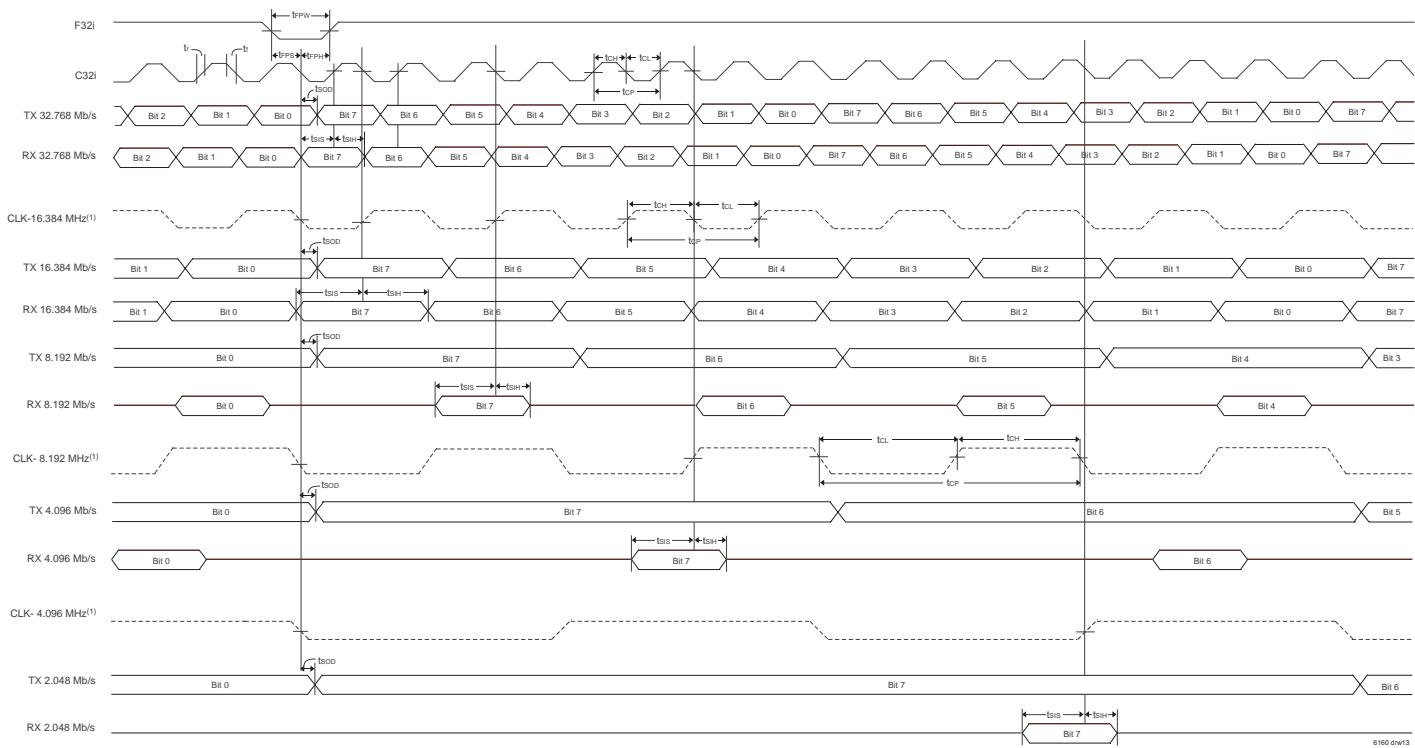
Figure 15. Output Driver Enable (ODE)

AC ELECTRICAL CHARACTERISTICS - ST-BUS® TIMING

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|------------------|---|------|-------|------|-------|
| t_{CH} | C32i Pulse Width HIGH Clock rate = 32.768Mb/s | 13 | 15.25 | 17 | ns |
| t_{CL} | C32i Pulse Width LOW Clock rate = 32.768Mb/s | 13 | 15.25 | 17 | ns |
| t_{CP} | C32i Period Clock rate = 32.768Mb/s | 29 | 30.5 | 35 | ns |
| t_{FPH} | Frame Pulse Hold Time from C32i falling (ST-BUS® or GCI) | 5 | — | — | ns |
| t_{FPS} | Frame Pulse Setup Time from C32i falling *ST-BUS® or GCI) | 5 | — | — | ns |
| t_{FPW} | Frame Pulse Width (ST-BUS®, GCI) Clock rate = 32.768Mb/s | 13 | — | 31 | ns |
| $t_r, t_f^{(1)}$ | Clock Rise/Fall Time | — | 1 | — | ns |
| t_{SIH} | RX Hold Time | 4 | — | — | ns |
| t_{SIS} | RX Setup Time | 2 | — | — | ns |
| t_{SOD} | Clock to Valid Data | 3 | 7 | 9 | ns |

NOTE:

1. Parameters verified under test conditions.



NOTE:

1. These clocks are for reference purposes only.
The TSI only accepts a 32.768MHz clock.

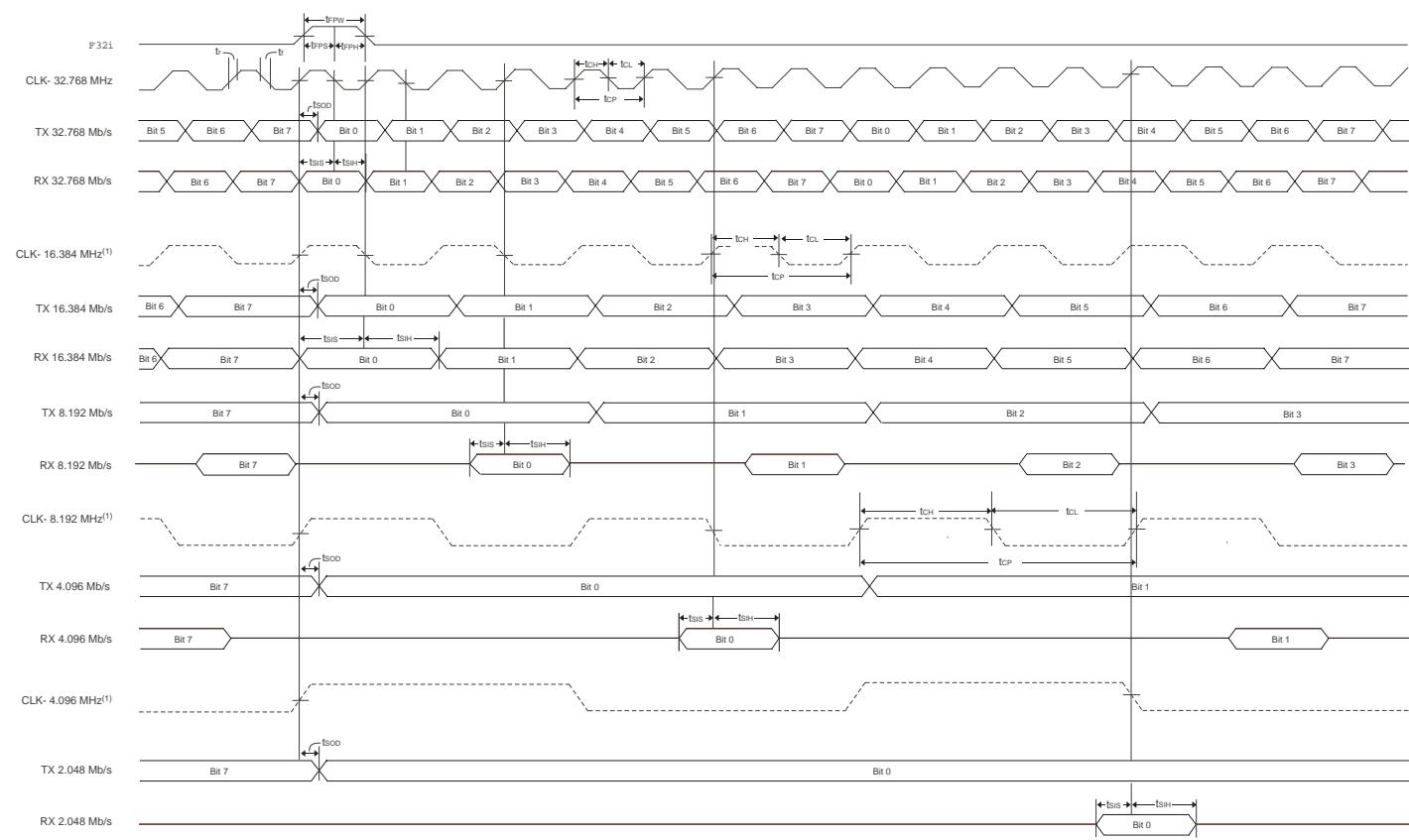
Figure 16. ST-BUS® Timing

AC ELECTRICAL CHARACTERISTICS - GCI BUS TIMING

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|--------------------------|---|------|-------|------|-------|
| t_{CH} | C32i Pulse Width HIGH Clock rate = 32.768Mb/s | 13 | 15.25 | 17 | ns |
| t_{CL} | C32i Pulse Width Clock rate = 32.768Mb/s | 13 | 15.25 | 17 | ns |
| t_{CP} | C32i Period Clock rate = 32.768Mb/s | 29 | 30.5 | 35 | ns |
| t_{FPH} | Frame Pulse Hold Time from C32i falling (ST-BUS® or GCI) | 5 | — | — | ns |
| t_{FPS} | Frame Pulse Setup Time before C32i falling (ST-BUS® or GCI) | 5 | — | — | ns |
| t_{FPW} | Frame Pulse Width (ST-BUS® or GCI) Clock rate = 32.768Mb/s | 13 | — | 31 | ns |
| $t_{R,F}$ ⁽¹⁾ | Clock Rise/Fall Time | — | 1 | — | ns |
| t_{SIH} | RX Hold Time | 4 | — | — | ns |
| t_{SIS} | RX Setup Time | 2 | — | — | ns |
| t_{SOD} | Clock to Valid Data | 3 | 7 | 9 | ns |

NOTE:

1. Parameters verified under test conditions.



NOTE:

1. These clocks are for reference purposes only.
The TSI only accepts a 32.768MHz clock.

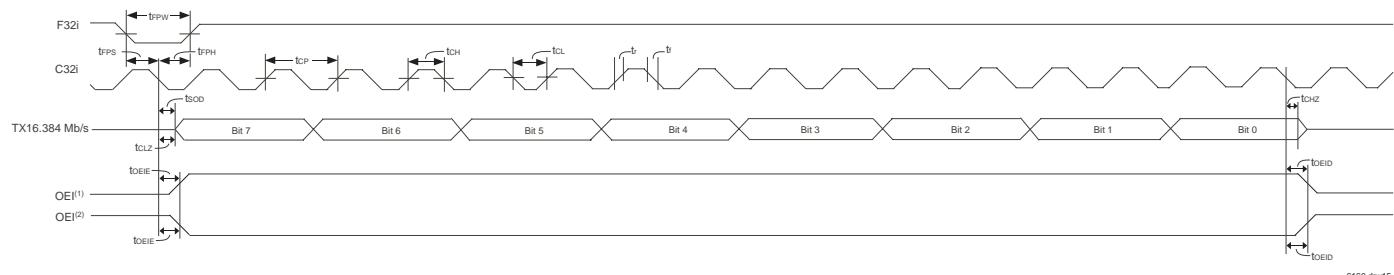
Figure 17. GCI Bus Timing

AC ELECTRICAL CHARACTERISTICS - OEI BUS TIMING IN ST-BUS® MODE

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|-----------------|---|------|-------|------|-------|
| t_{CH} | C32i Pulse Width HIGH Clock rate = 32.768Mb/s | 13 | 15.25 | 17 | ns |
| $t_{CHZ}^{(2)}$ | Clock to High-Z | — | — | 9 | ns |
| t_{CL} | C32i Pulse Width Clock rate = 32.768Mb/s | 13 | 15.25 | 17 | ns |
| $t_{CLZ}^{(2)}$ | Clock to Low-Z | 3 | — | — | ns |
| t_{CP} | C32i Period Clock rate = 32.768Mb/s | 29 | 30.5 | 35 | ns |
| t_{FPH} | Frame Pulse Hold Time from C32i falling (ST-BUS® or GCI) | 5 | — | — | ns |
| t_{FPS} | Frame Pulse Setup Time before C32i falling (ST-BUS® or GCI) | 5 | — | — | ns |
| t_{FPW} | Frame Pulse Width (ST-BUS® or GCI) Clock rate = 32.768Mb/s | 13 | — | 31 | ns |
| t_{OEIE} | Clock to OEI Enable | 3 | — | 9 | ns |
| t_{OEID} | Clock to OEI Disable | 3 | — | 9 | ns |
| $t_{r,f}^{(1)}$ | Clock Rise/Fall Time | — | 1 | — | ns |
| t_{SOD} | Clock to Valid Data | 3 | 7 | 9 | ns |

NOTE:

1. Parameters verified under test conditions.
2. $C_L = 300\text{pF}$



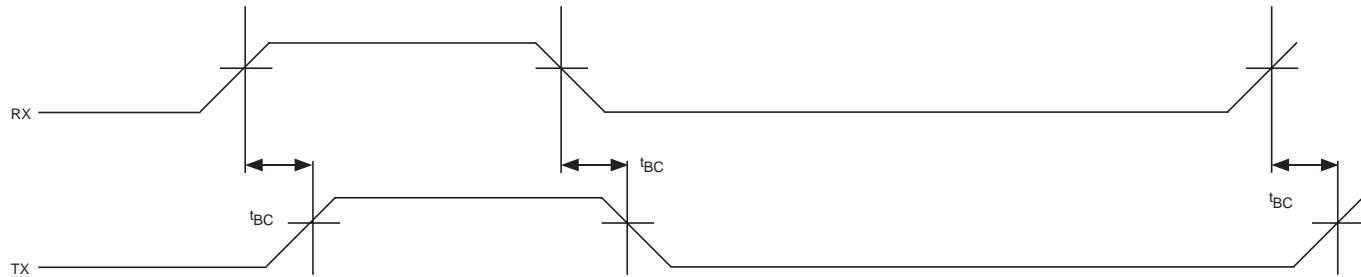
NOTES:

- 1) OEPOL = 1
- 2) OEPOL = 0

Figure 18. OEI Bus Timing in ST-BUS® Mode

AC ELECTRICAL CHARACTERISTICS - RX TO TX INTERNAL BYPASS BIT

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNITS |
|----------|-----------|------|------|------|-------|
| t_{BC} | | 2 | 8 | 12 | ns |



6160 drw16

t_{BC} = end to end chip delay

Figure 19. RX to TX Internal Bypass Bit

AC ELECTRICAL CHARACTERISTICS - MOTOROLA NON-MULTIPLEXED BUS ASYNCHRONOUS TIMING MEMORY ACCESS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNITS |
|-----------------------|--|------|------|------|-------|
| tADH | Address Hold after DS Rising | 2 | — | — | ns |
| tADS | Address Setup from DS Falling | 2 | — | — | ns |
| tAKD ⁽¹⁾ | AcknowledgmentDelay: Reading/Writing Memory | — | — | 30 | ns |
| tAKH ^(2,3) | AcknowledgmentHold Time | — | — | 10 | ns |
| tCSH | CS Hold Time after DS Rising | 0 | — | — | ns |
| tCSS | CS Setup from DS Falling | 0 | — | — | ns |
| tDDR ⁽⁴⁾ | Data Setup from DTA LOW on Read | 2 | — | — | ns |
| tDHR ⁽⁵⁾ | Data Hold On Read | 10 | 15 | 25 | ns |
| tDHW | Data Hold on Read | 5 | — | — | ns |
| tDSS | Data Strobe Setup Time | 2 | — | — | ns |
| tDSPW | Data Strobe on Write | 6 | — | — | ns |
| tRWH | R/W Hold after DS Rising | 3 | — | — | ns |
| tRWS | R/W Setup from DS Falling | 3 | — | — | ns |
| tSWD | Valid Data Delay on Write | 2 | — | — | ns |

NOTES:

1. $C_L = 30\text{pF}$
2. $R_L = 1\text{K}$
3. High-Impedance is measured by pulling to the appropriate rail with R_L , with timing corrected to cancel time taken to discharge C_L .
4. To achieve on clock cycle fast memory access, this setup time, tDSS should be met. Otherwise, worst-case memory access operation is determined by tAKD.

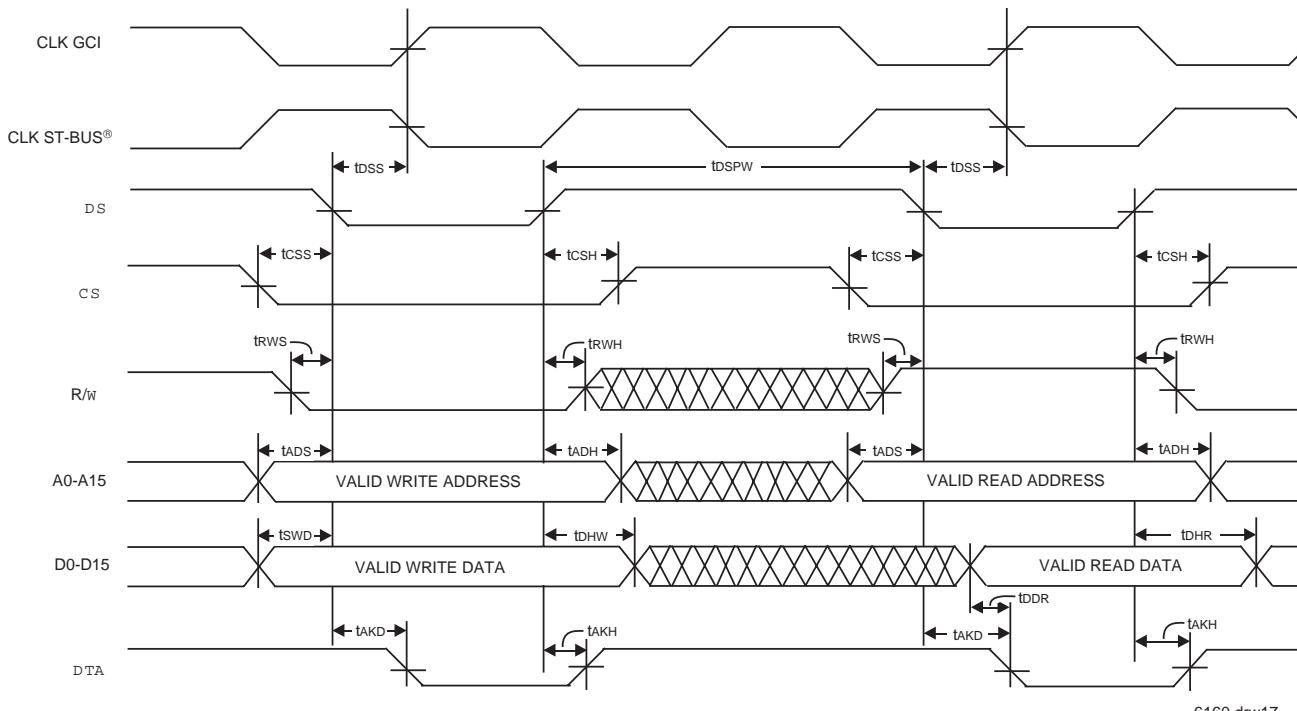


Figure 20. Motorola Non-Multiplexed Bus Asynchronous Memory Access

AC ELECTRICAL CHARACTERISTICS - MOTOROLA NON-MULTIPLEXED BUS ASYNCRONOUS TIMING REGISTER ACCESS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNITS |
|-------------------------|--|------|------|------|-------|
| tADH | Address Hold after DS Rising | 2 | — | — | ns |
| tADS | Address Setup from DS Falling | 2 | — | — | ns |
| tAKD ⁽¹⁾ | Acknowledgment Delay: Reading/Writing Registers | — | — | 40 | ns |
| tAKH ^(1,2,3) | Acknowledgment Hold Time | — | — | 20 | ns |
| tCSH | CS Hold Time after DS Rising | 0 | — | — | ns |
| tCSS | CS Setup from DS Falling | 0 | — | — | ns |
| tDDR ⁽¹⁾ | Data Setup from DTA LOW on Read | 2 | — | — | ns |
| tDHR ⁽¹⁾ | Data Hold On Read | 10 | 15 | 25 | ns |
| tDHW | Data Hold on Read | 5 | — | — | ns |
| tDSPW | Data Strobe on Write | 6 | — | — | ns |
| tDSW | Data Setup on Write | 10 | — | — | ns |
| tRWH | R/W Hold after DS Rising | 3 | — | — | ns |
| tSWD | R/W Setup from DS Falling | 3 | — | — | ns |

NOTES:

1. $C_L = 30\text{pF}$
2. $R_L = 1\text{K}$
3. High-Impedance is measured by pulling to the appropriate rail with R_L , with timing corrected to cancel time taken to discharge C_L .
4. To achieve on clock cycle fast memory access, this setup time, tDSS should be met. Otherwise, worst-case memory access operation is determined by tAKD.

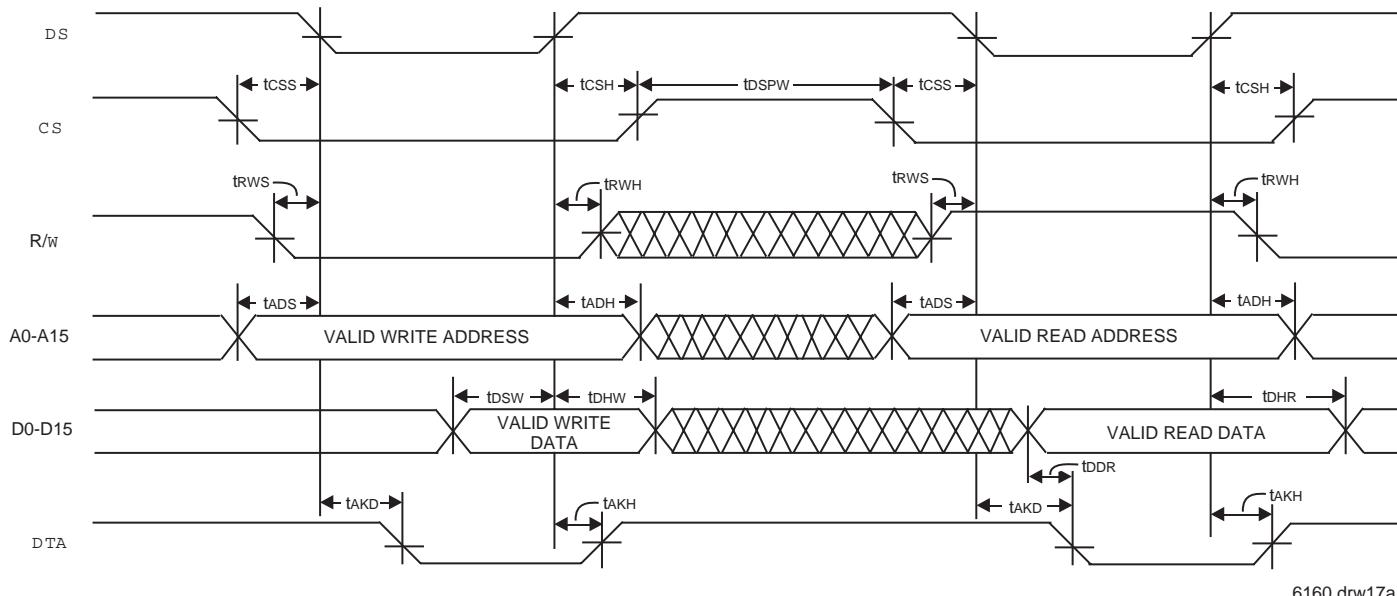


Figure 21. Motorola Non-Multiplexed Bus Asynchronous Timing Register Access

AC ELECTRICAL CHARACTERISTICS - SYNCHRONOUS BUS TIMING

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNITS |
|-------------------|---------------------|------|------|------|-------|
| t_{ADH} | Address Hold | 3 | — | — | ns |
| t_{ADS} | Address Setup | 3 | — | — | ns |
| t_{BEH} | Byte Enable Hold | 3 | — | — | ns |
| t_{BES} | Byte Enable Setup | 3 | — | — | ns |
| t_{CD} | Clock to Data | — | — | 20 | ns |
| $t_{DHR}^{(2,3)}$ | Data Hold on Read | 10 | 15 | 25 | ns |
| t_{DHW} | Data Hold on Write | 3 | — | — | ns |
| t_{DSW} | Data Setup on Write | 3 | — | — | ns |
| t_{RWH} | R/W Hold | 3 | — | — | ns |
| t_{RWS} | R/W Setup | 3 | — | — | ns |
| t_{SCSH} | CS Hold | 3 | — | — | ns |
| t_{SCSS} | CS Setup | 3 | — | — | ns |

NOTES:

1. $C_L = 30\text{pF}$
2. $R_L = 1\text{K}$
3. High-Impedance is measured by pulling to the appropriate rail with R_L , with timing corrected to cancel time taken to discharge C_L .
4. To achieve on clock cycle fast memory access, this setup time, t_{DSS} should be met. Otherwise, worst-case memory access operation is determined by t_{AKD} .

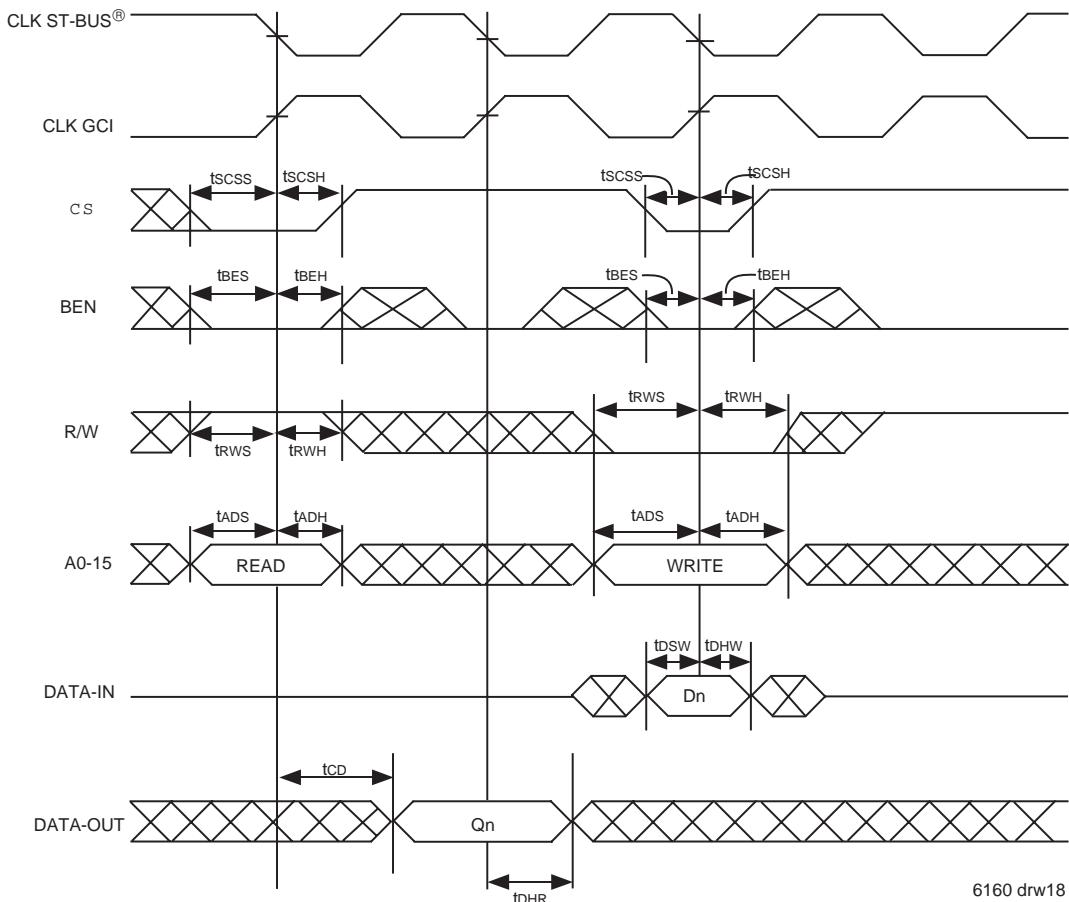


Figure 22. Synchronous Bus Timing

AC ELECTRICAL CHARACTERISTICS - BYTE ENABLE

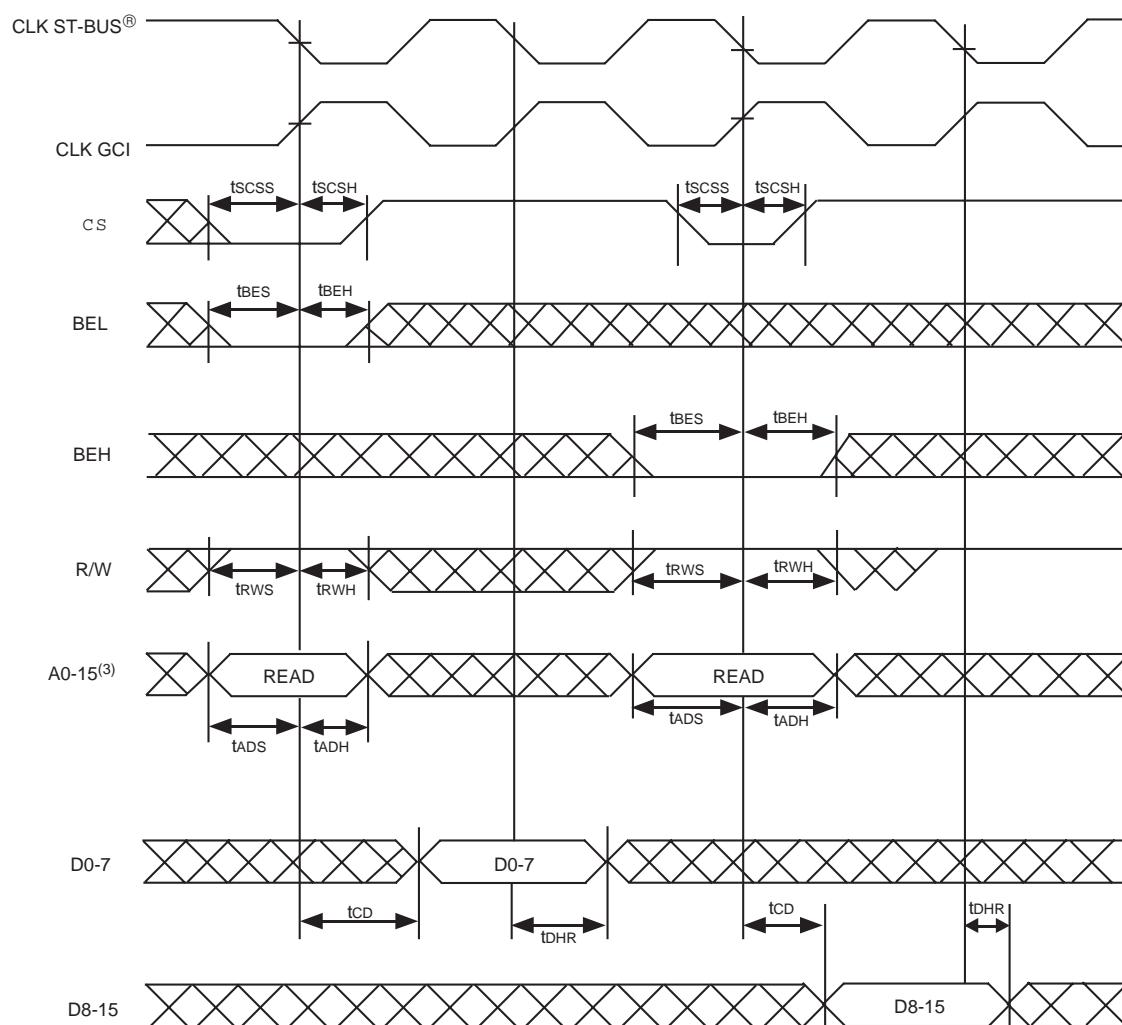
| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNITS |
|---------------------|-------------------|------|------|------|-------|
| tADH | Address Hold | 3 | — | — | ns |
| tADS | Address Setup | 3 | — | — | ns |
| tBEH | Byte Enable Hold | 3 | — | — | ns |
| tBES | Byte Enable Setup | 3 | — | — | ns |
| tCD | Clock to Data | — | — | 20 | ns |
| tDHR ⁽¹⁾ | Data Hold on Read | 10 | 15 | 25 | ns |
| tRWH | R/W Hold | 3 | — | — | ns |
| tRWS | R/W Setup | 3 | — | — | ns |
| tsCSH | CS Hold | 3 | — | — | ns |
| tsCSS | CS Setup | 3 | — | — | ns |

NOTES:

1. $C_L = 30\text{pF}$

2. $R_L = 1\text{K}$

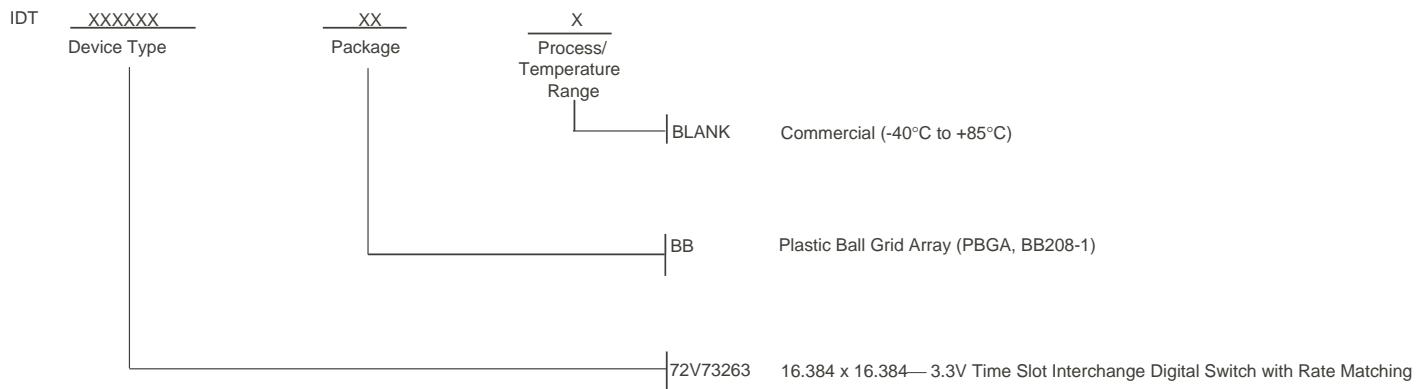
3. High-Impedance is measured by pulling to the appropriate rail with R_L , with timing corrected to cancel time taken to discharge C_L .



6160 drw19

Figure 23. Byte Enable

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