



## DUAL PROCESSOR SUPERVISORS

### FEATURES

- Dual Supervisory Circuits for DSP- and Processor-Based Systems
- Power-On Reset Generator with Fixed Delay Time of 200ms; no External Capacitor Needed
- Watchdog Timer Retriggeres the  $\overline{\text{RESET}}$  Output at  $\text{SENSEn} \geq V_{IT+}$
- Temperature-Compensated Voltage Reference
- Maximum Supply Current of 40 $\mu\text{A}$
- Supply Voltage Range: 2.7V to 6V
- Defined  $\overline{\text{RESET}}$  Output From  $V_{DD} \geq 1.1\text{V}$
- MSOP-8 and SO-8 Packages
- Temperature Range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

### APPLICATIONS

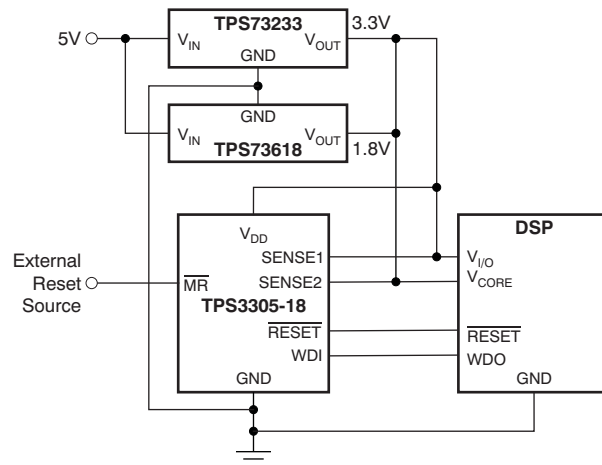
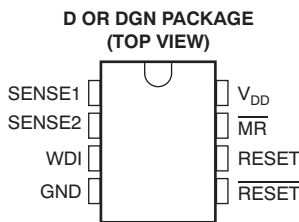
- Processor Supply Monitoring
- Industrial Equipment
- Automotive Systems
- Portable/Battery-Powered Equipment
- Wireless Communication Systems
- Notebook/Desktop Computers

### DESCRIPTION

The TPS3305 family is a series of micropower supply voltage supervisors designed for circuit initialization. Its dual monitor topology is well-suited to use in DSP and processor-based systems, which often require two supply voltages, core and I/O.

$\overline{\text{RESET}}$  is asserted when the voltage at either SENSEn pin falls below its threshold voltage,  $V_{IT}$ . When both SENSEn pins are again above their respective threshold voltages,  $\overline{\text{RESET}}$  is held low for the factory-programmed delay time (200ms typ).  $\overline{\text{RESET}}$  is also asserted if the watchdog input (WDI) is not toggled for more than 1.6s typ.

The TPS3305-xx devices are available in either 8-pin MSOP or SO packages, and are specified for operation over a temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**ORDERING INFORMATION<sup>(1)</sup>**

DEVICE	NOMINAL SUPERVISED VOLTAGE		THRESHOLD VOLTAGE (TYP)	
	SENSE1	SENSE2	SENSE1	SENSE2
TPS3305-18	3.3 V	1.8 V	2.93 V	1.68 V
TPS3305-25	3.3 V	2.5 V	2.93 V	2.25 V
TPS3305-33	5.0 V	3.3 V	4.55 V	2.93 V

(1) For the most current specifications and package information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

**ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>**

Over operating junction temperature range (unless otherwise noted).

	UNIT
Supply voltage range, $V_{DD}$	-0.3V to +7V
$V_{MR}$ , $V_{WDI}$	-0.3V to $V_{DD} + 0.3V$
Input voltage at SENSE1 and SENSE2, $V_I$	$(V_{DD} + 0.3)V_{IT} / 1.25V$
$V_{RESET}$ , $V_{\overline{RESET}}$	-0.3V to +7V
Maximum low output current, $I_{OL}$	5mA
Maximum high output current, $I_{OH}$	-5mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{DD}$ )	$\pm 20mA$
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{DD}$ )	$\pm 20mA$
Continuous total power dissipation	See <a href="#">Dissipation Ratings Table</a>
Operating junction temperature range, $T_J$	-40°C to +85°C
Storage temperature range, $T_{stg}$	-65°C to +150°C
Soldering temperature	+260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to GND.

**DISSIPATION RATINGS TABLE**

PACKAGE	$T_A \leq +25^\circ C$ POWER RATING	DERATING FACTOR ABOVE $T_A = +25^\circ C$	$T_A = +70^\circ C$ POWER RATING	$T_A = +85^\circ C$ POWER RATING
DGN	2.14W	17.1mW/°C	1.37W	1.11W
D	725mW	5.8mW/°C	464mW	377mW

## ELECTRICAL CHARACTERISTICS

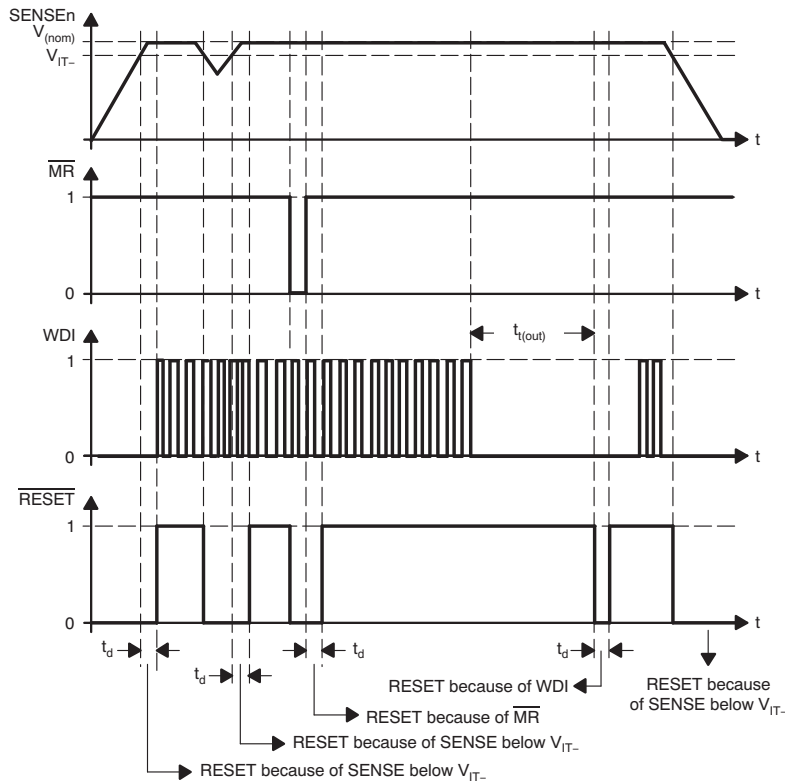
Over operating junction temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TPS3305-xx			UNIT		
			MIN	TYP	MAX			
V <sub>DD</sub>	Input supply range		2.7		6.0	V		
T <sub>J</sub>	Operating junction temperature range		-40		+85	°C		
V <sub>OH</sub>	High-level output voltage	V <sub>DD</sub> = 2.7V to 6V, I <sub>OH</sub> = -20μA	V <sub>DD</sub> - 0.2V			V		
		V <sub>DD</sub> = 3.3V, I <sub>OH</sub> = -2mA	V <sub>DD</sub> - 0.4V			V		
		V <sub>DD</sub> = 6V, I <sub>OH</sub> = -3mA	V <sub>DD</sub> - 0.4V			V		
V <sub>OL</sub>	Low-level output voltage	V <sub>DD</sub> = 2.7V to 6V, I <sub>OL</sub> = 20μA				0.2	V	
		V <sub>DD</sub> = 3.3V, I <sub>OL</sub> = 2mA				0.4	V	
		V <sub>DD</sub> = 6V, I <sub>OL</sub> = 3mA				0.4	V	
Power-up reset voltage <sup>(1)</sup>		V <sub>DD</sub> ≥ 1.1V, I <sub>OL</sub> = 20μA				0.4	V	
V <sub>IT-</sub>	Negative-going input threshold voltage <sup>(2)</sup>	V <sub>DD</sub> = 2.7V to 6V, T <sub>A</sub> = 0°C to +85°C	VSENSE1, VSENSE2	1.64	1.68	1.72	V	
				2.20	2.25	2.30	V	
				2.86	2.93	3.0	V	
				4.46	4.55	4.64	V	
		VSENSE1, VSENSE2	V <sub>DD</sub> = 2.7V to 6V, T <sub>A</sub> = -40°C to +85°C		1.64	1.68	1.73	V
					2.20	2.25	2.32	V
					2.86	2.93	3.02	V
					4.46	4.55	4.67	V
V <sub>hys</sub>	Hysteresis at VSENSEn input	V <sub>IT-</sub> = 1.68V				15	mV	
		V <sub>IT-</sub> = 2.25V				20	mV	
		V <sub>IT-</sub> = 2.93V				30	mV	
		V <sub>IT-</sub> = 4.55V				40	mV	
I <sub>H(AV)</sub>	Average high-level input current	WDI	WDI = V <sub>DD</sub> = 6V Time average (dc = 88%)		100	150	μA	
I <sub>L(AV)</sub>	Average low-level input current	WDI	WDI = 0V, V <sub>DD</sub> = 6V Time average (dc = 12%)		-15	-20	μA	
V <sub>IH</sub>	High-level input voltage at $\overline{MR}$ and WDI		0.7 x V <sub>DD</sub>			V		
V <sub>IL</sub>	Low-level input voltage at $\overline{MR}$ and WDI		0.3 x V <sub>DD</sub>			V		
Δt / ΔV	Input transition rise and fall rate at $\overline{MR}$					50	ns/V	
I <sub>H</sub>	High-level input current	WDI	WDI = V <sub>DD</sub> = 6V		120	170	μA	
		$\overline{MR}$	$\overline{MR} = 0.7 \times V_{DD}$ , V <sub>DD</sub> = 6V		-130	-180	μA	
		SENSE1	VSENSE1 = V <sub>DD</sub> = 6V		5	8	μA	
		SENSE2	VSENSE2 = V <sub>DD</sub> = 6V		6	9	μA	
I <sub>L</sub>	Low-level input current	WDI	WDI = 0V, V <sub>DD</sub> = 6V		-120	-170	μA	
		$\overline{MR}$	$\overline{MR} = 0V$ , V <sub>DD</sub> = 6V		-430	-600	μA	
		SENSEn	VSENSE1,2 = 0V		-1	1	μA	
I <sub>DD</sub>	Supply current					40	μA	
C <sub>I</sub>	Input capacitance	V <sub>I</sub> = 0V to V <sub>DD</sub>				10	pF	

(1) The lowest supply voltage at which **RESET** becomes active. t<sub>r</sub>, V<sub>DD</sub> ≥ 15 μs/V.

(2) To ensure best stability of the threshold voltage, a bypass capacitor (0.1 μF ceramic) should be placed close to the supply terminals.

**TIMING DIAGRAM**



**TIMING REQUIREMENTS**

At  $V_{DD} = 2.7V$  to  $6V$ ,  $R_L = 1M\Omega$ ,  $C_L = 50pF$ , and  $T_J = +25^\circ C$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_w$	Pulse width	$V_{SENSEnL} = V_{IT-} - 0.2V$ , $V_{SENSEnH} = V_{IT+} + 0.2V$	6			$\mu s$
		$V_{IH} = 0.7 \times V_{DD}$ , $V_{IL} = 0.3 \times V_{DD}$	100			ns
			100			ns

**SWITCHING CHARACTERISTICS**

At  $V_{DD} = 2.7V$  to  $6V$ ,  $R_L = 1M\Omega$ ,  $C_L = 50pF$ , and  $T_J = +25^\circ C$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{t(out)}$	Watchdog time-out	$V_{I(SENSEn)} \geq V_{IT+} + 0.2V$ , $\overline{MR} \geq 0.7 \times V_{DD}$ See <a href="#">Timing Diagram</a>	1.1	1.6	2.3	s
$t_d$	Delay time	$V_{I(SENSEn)} \geq V_{IT+} + 0.2V$ , $\overline{MR} \geq 0.7 \times V_{DD}$ See <a href="#">Timing Diagram</a>	140	200	280	ms
$t_{PHL}$	Propagation (delay) time, high-to-low level output	$\overline{MR}$ to $\overline{RESET}$ , $\overline{MR}$ to RESET $V_{I(SENSEn)} \geq V_{IT+} + 0.2V$ , $V_{IH} = 0.7 \times V_{DD}$ , $V_{IL} = 0.3 \times V_{DD}$		200	500	ns
$t_{PLH}$	Propagation (delay) time, low-to-high level output	$\overline{MR}$ to $\overline{RESET}$ , $\overline{MR}$ to RESET $V_{I(SENSEn)} \geq V_{IT+} + 0.2V$ , $V_{IH} = 0.7 \times V_{DD}$ , $V_{IL} = 0.3 \times V_{DD}$		200	500	ns
$t_{PHL}$	Propagation (delay) time, high-to-low level output	$\overline{SENSEn}$ to $\overline{RESET}$ , $\overline{SENSEn}$ to RESET $V_{IH} = V_{IT+} + 0.2V$ , $V_{IL} = V_{IT-} - 0.2V$ , $\overline{MR} \geq 0.7 \times V_{DD}$		1	5	$\mu s$
$t_{PLH}$	Propagation (delay) time, low-to-high level output	$\overline{SENSEn}$ to $\overline{RESET}$ , $\overline{SENSEn}$ to RESET $V_{IH} = V_{IT+} + 0.2V$ , $V_{IL} = V_{IT-} - 0.2V$ , $\overline{MR} \geq 0.7 \times V_{DD}$		1	5	$\mu s$

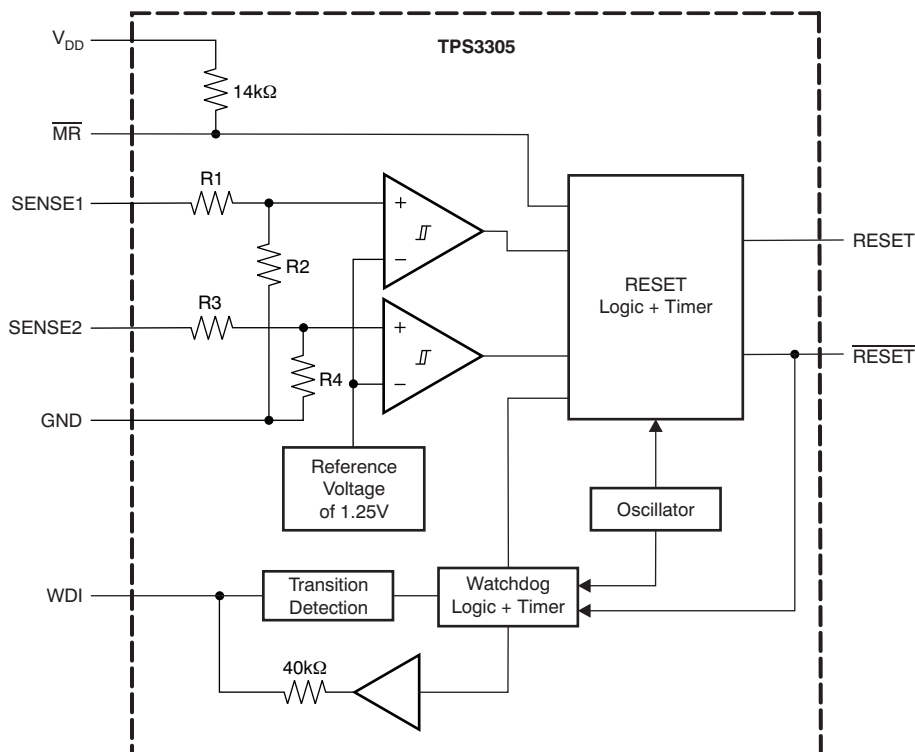
**DEVICE INFORMATION**

**FUNCTION/TRUTH TABLE<sup>(1)</sup>**

MR	SENSE1 > V <sub>IT1</sub>	SENSE2 > V <sub>IT2</sub>	RESET	RESET
L	X	X	L	H
H	0	0	L	H
H	0	1	L	H
H	1	0	L	H
H	1	1	H	L

(1) X = Don't care

**FUNCTIONAL BLOCK DIAGRAM**



**TERMINAL FUNCTIONS**

TERMINAL		DESCRIPTION
NAME	NO.	
GND	4	Ground
MR	7	Manual reset
RESET	5	Active-low reset output
RESET	6	Active-high reset output
SENSE1	1	Sense voltage input 1
SENSE2	2	Sense voltage input 2
WDI	3	Watchdog timer input
V <sub>DD</sub>	8	Supply voltage

TYPICAL CHARACTERISTICS

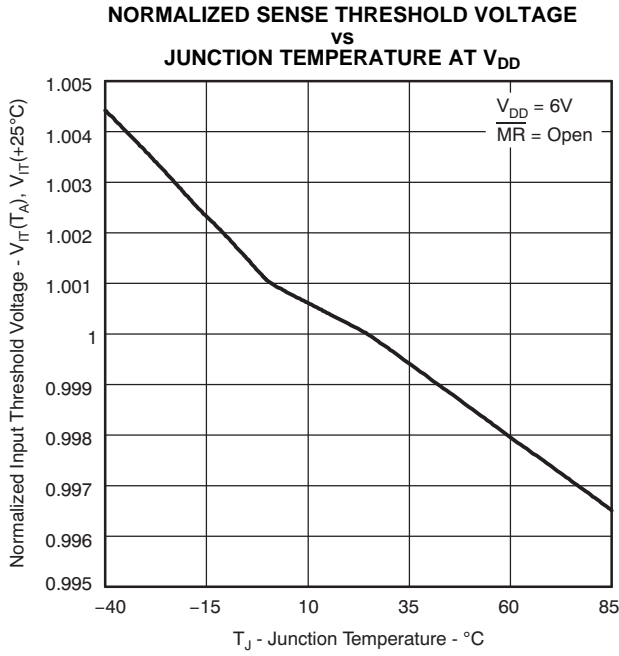


Figure 1.

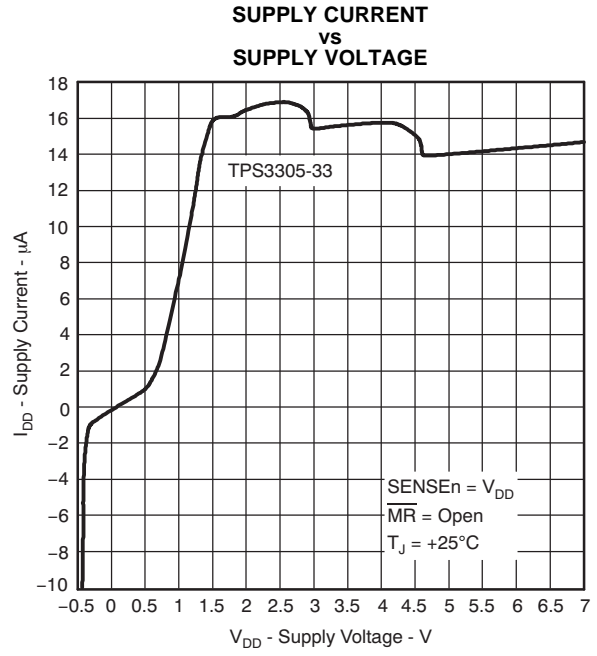


Figure 2.

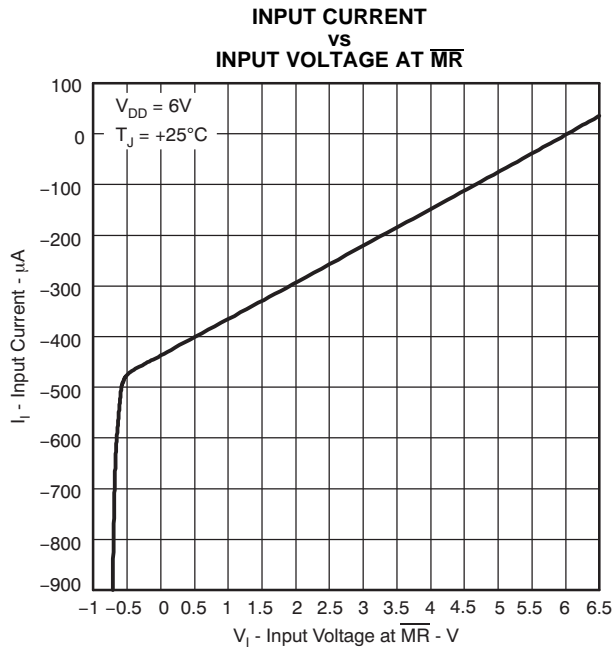


Figure 3.

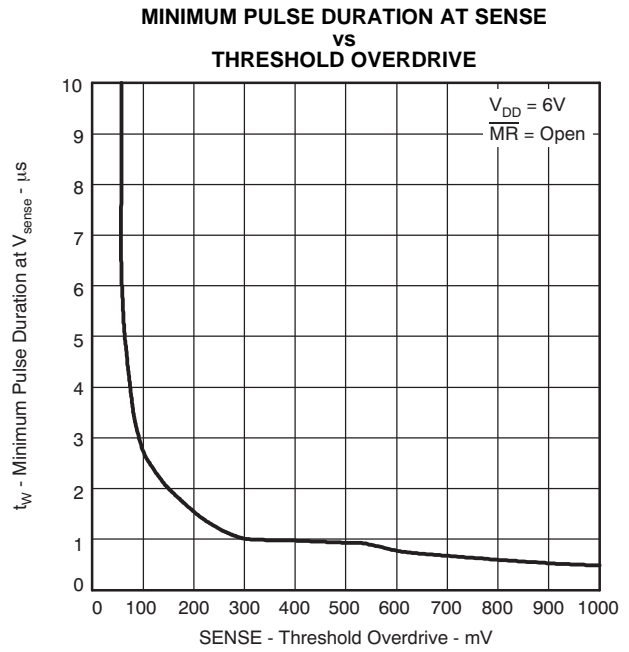
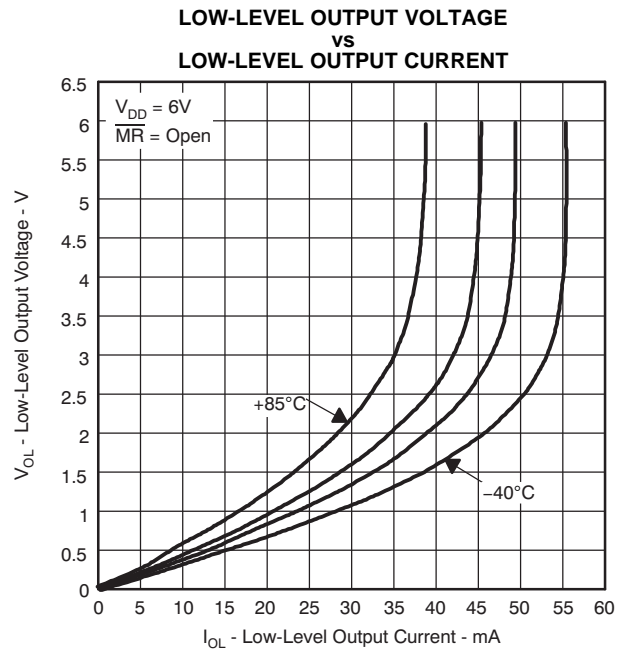
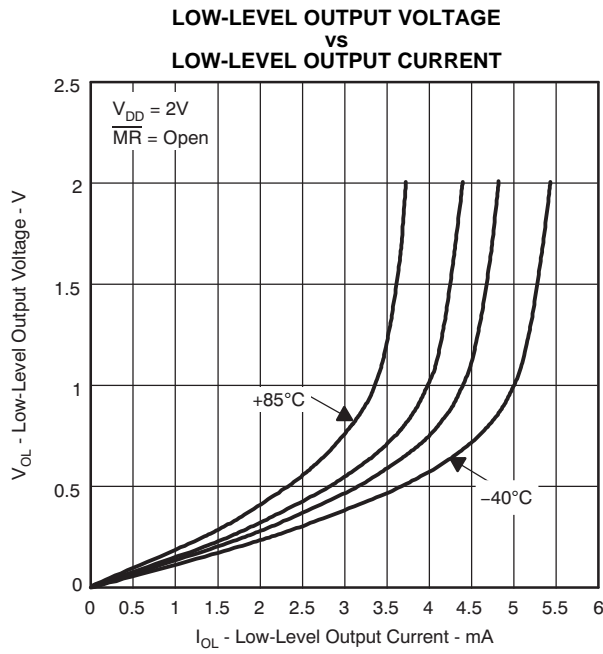
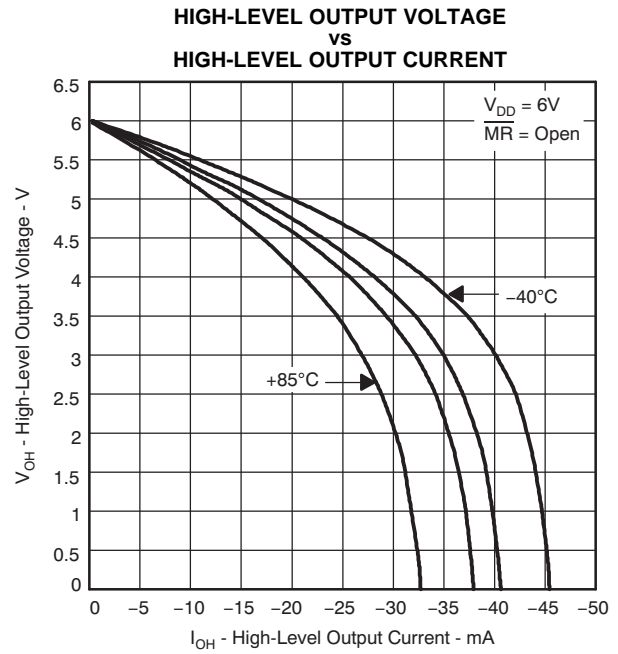
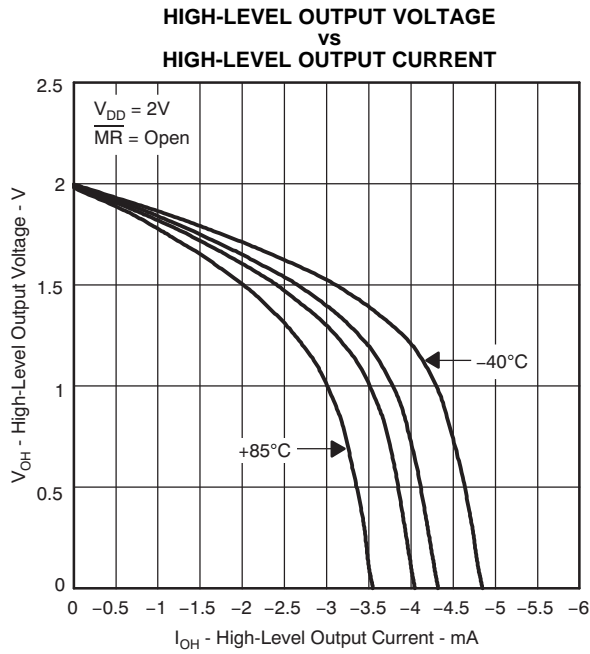


Figure 4.

**TYPICAL CHARACTERISTICS (continued)**



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3305-18D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30518	<a href="#">Samples</a>
TPS3305-18DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30518	<a href="#">Samples</a>
TPS3305-18DGN	ACTIVE	MSOP- PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAM	<a href="#">Samples</a>
TPS3305-18DGNG4	ACTIVE	MSOP- PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAM	<a href="#">Samples</a>
TPS3305-18DGNR	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAM	<a href="#">Samples</a>
TPS3305-18DGNRG4	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAM	<a href="#">Samples</a>
TPS3305-18DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30518	<a href="#">Samples</a>
TPS3305-18DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30518	<a href="#">Samples</a>
TPS3305-25D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30525	<a href="#">Samples</a>
TPS3305-25DGN	ACTIVE	MSOP- PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAN	<a href="#">Samples</a>
TPS3305-25DGNR	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAN	<a href="#">Samples</a>
TPS3305-25DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30525	<a href="#">Samples</a>
TPS3305-33D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30533	<a href="#">Samples</a>
TPS3305-33DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30533	<a href="#">Samples</a>
TPS3305-33DGN	ACTIVE	MSOP- PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAO	<a href="#">Samples</a>
TPS3305-33DGNG4	ACTIVE	MSOP- PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAO	<a href="#">Samples</a>
TPS3305-33DGNR	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAO	<a href="#">Samples</a>



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3305-33DGNRG4	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAO	<a href="#">Samples</a>
TPS3305-33DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30533	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3305-18DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3305-18DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3305-25DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3305-25DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3305-33DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3305-33DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3305-18DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
TPS3305-18DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS3305-25DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
TPS3305-25DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS3305-33DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
TPS3305-33DR	SOIC	D	8	2500	350.0	350.0	43.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

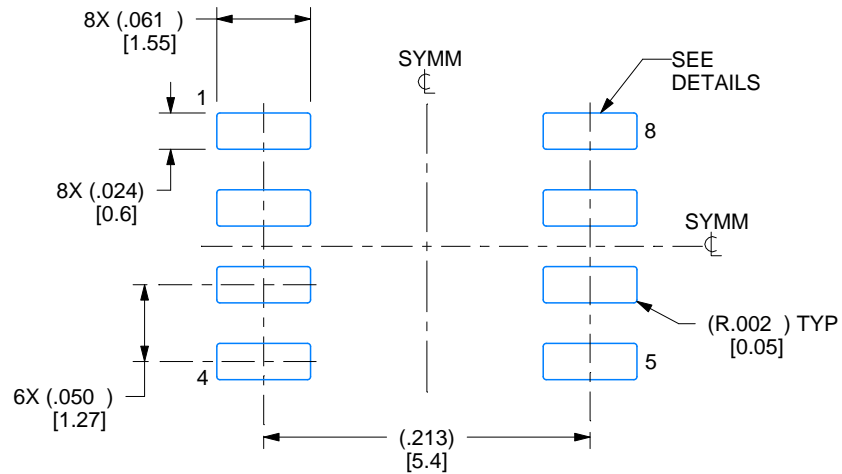
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-187 variation AA-T

PowerPAD is a trademark of Texas Instruments.

DGN (S-PDSO-G8)

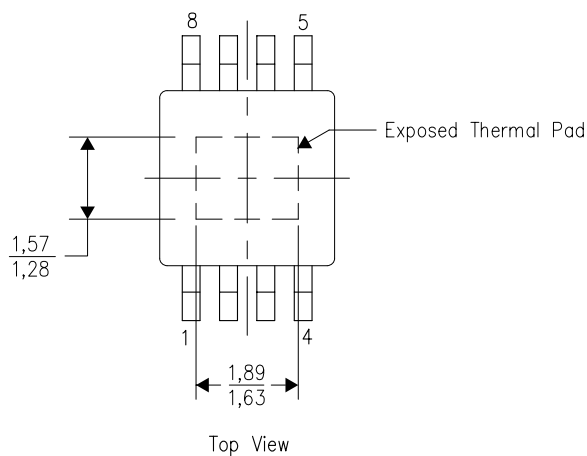
PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



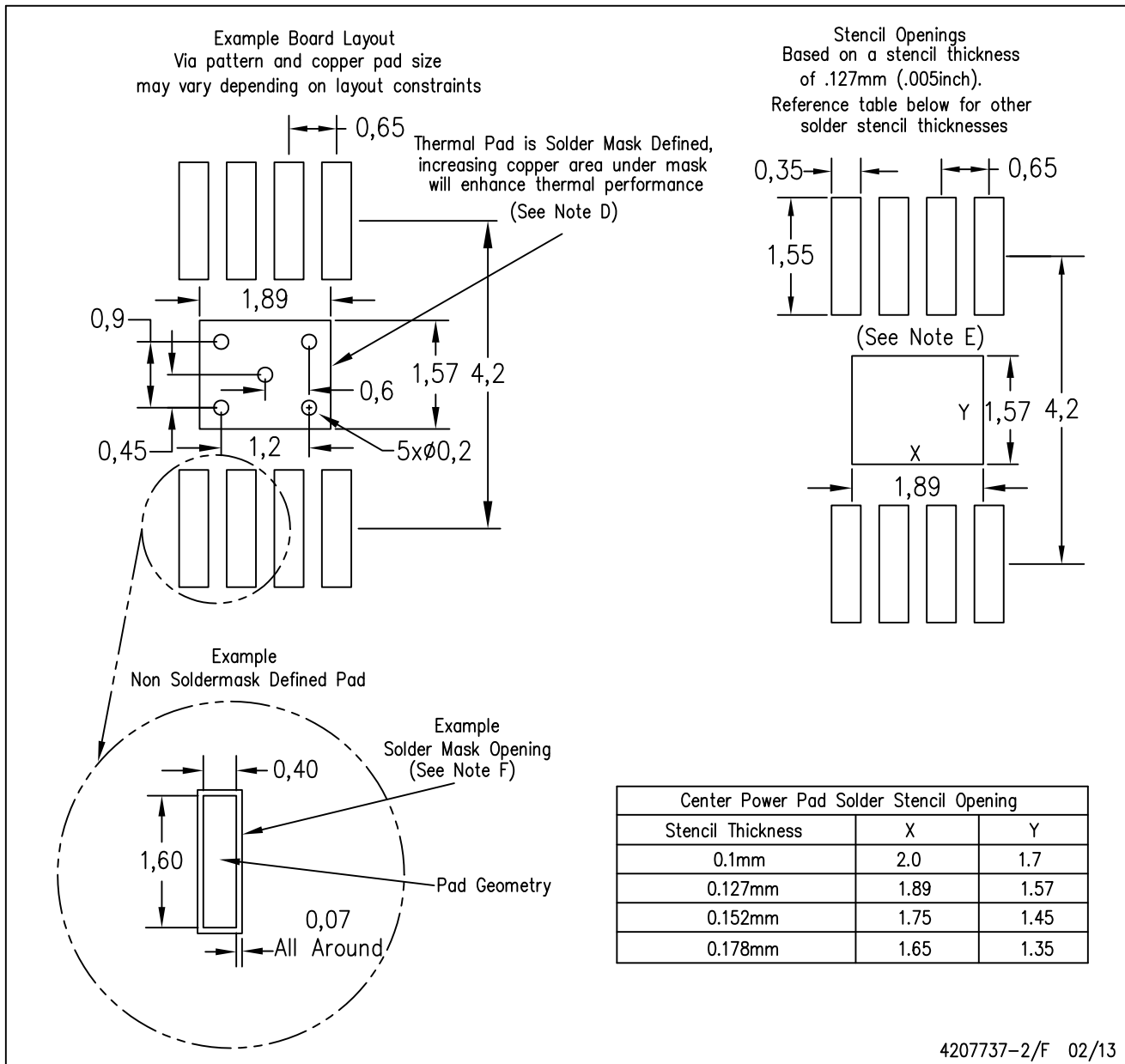
Exposed Thermal Pad Dimensions

4206323-2/1 12/11

NOTE: All linear dimensions are in millimeters

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- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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