Precision Sample and Hold Amplifier

FEATURES

- 4μs Typical Acquisition Time
- *Guaranteed* 0.01% Max. Gain Error
- 2mV Typ. Offset Voltage
- 2.5mV Max. Hold Step
- Very Low Feedthrough 80dB Min.
- High Input Impedance Under All Conditions
- Logic Inputs Compatible with All Logic Families

APPLICATIONS

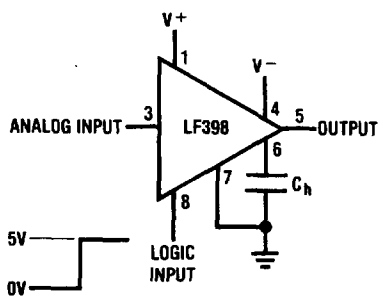
- 12-Bit Data Acquisition Systems
- Ramp Generators
- Analog Switches
- Staircase Generators
- Sample and Difference Circuits

DESCRIPTION

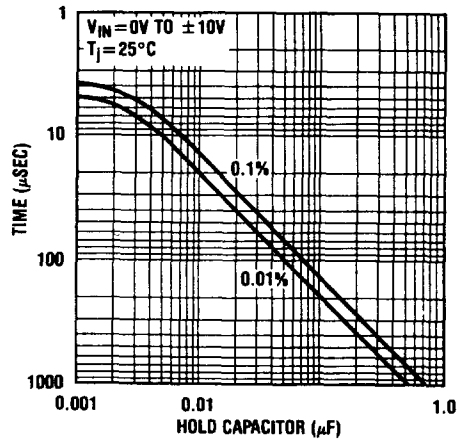
The LF398 is a precision sample and hold amplifier which uses a combination of bipolar and junction FET transistors to provide precision, high speed, and long hold times. A typical offset voltage of 2mV and gain error of 0.004% allow this sample and hold amplifier to be used in 12-bit systems. Dynamic performance can be optimized by proper selection of the external hold capacitor. Acquisition times can be as low as 4μs for small capacitors while hold step and droop errors can be held below 0.1mV and 30μV/sec respectively when using larger capacitors.

The LF398 is fixed at unity gain with $10^{10}\Omega$ input impedance independent of sample/hold mode. The logic inputs are high impedence differential to allow easy interfacing to any logic family without ground loop problems. A separate offset adjust pin can be used to zero the offset voltage in either the sample or hold mode. Additionally, the hold capacitor can be driven with an external signal to provide precision level shifting or "differencing" operation. The device will operate over a wide supply voltage range from ±5V to ±18V with very little change in performance, and key parameters are specified over this full supply range.

Basic Sample and Hold



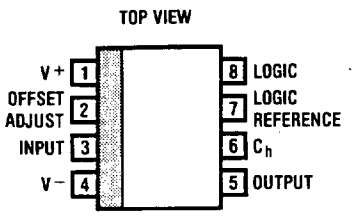
Acquisition Time



ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... Equal to Supply Voltage
Logic to Logic Reference Differential
Voltage (Note 2) ..... +30V, −30V
Output Short Circuit Duration ..... Indefinite
Hold Capacitor Short Circuit Duration ..... 10 sec
Lead Temperature (Soldering, 10 seconds) ..... 300°C
Supply Voltage ..... ±18V
Power Dissipation (Package Limitation)
(Note 1) 500mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
PLASTIC SO

ORDER PART NUMBER
LF398S8
PART MARKING
398

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LF398 MIN	LF398 TYP	LF398 MAX	UNITS
Input Offset Voltage (Note 6)				2	7	mV
		●			10	mV
Input Bias Current (Note 6)				10	50	nA
		●			100	nA
Input Impedance				10^{10}		Ω
Gain Error	$R_L = 10k$			0.004	0.01	%
		●			0.02	%
Feedthrough Attenuation Ratio at 1kHz	$C_h = 0.01\mu F$		80	96		dB
Output Impedance	"HOLD" Mode			0.5	4	Ω
		●			6	Ω
"HOLD" Step (Note 4)	$C_h = 0.01\mu F$, $V_{OUT} = 0$			0.5	2.5	mV
Supply Current (Note 6)	$T_j \geq 25°C$			4.5	6.5	mA
Logic and Logic Reference Input Current				2	10	μA
Leakage Current Into Hold Capacitor (Note 6)	"HOLD" Mode (Note 5)			30	200	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000pF$			4		μs
	$C_h = 0.01\mu F$			16		μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$		80	110		dB
Differential Logic Threshold			0.8	1.4	2.4	V

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: T_j max for the LF398S8 is 100°C.

Note 2: The logic inputs are protected to ±30V differential as long as the voltage on both pins does not exceed the supply voltage. For proper operation, however, both logic and logic reference pins must be at least 2V below the positive supply and one of these pins must be at least 3V above the negative supply.

Note 3: Unless otherwise noted, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, $R_L = 10k\Omega$ and unit is in "sample" mode. Logic reference = 0V and logic voltage = 2.5V.

Note 4: The hold step is sensitive to stray capacitance coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 5: Leakage current is measured at a *junction* temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

Note 6: These parameters are guaranteed over a supply voltage range of ±5V to ±18V.

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