

ZERO DELAY GLITCH-FREE CLOCK MULTIPLEXER

ICS581-01/02

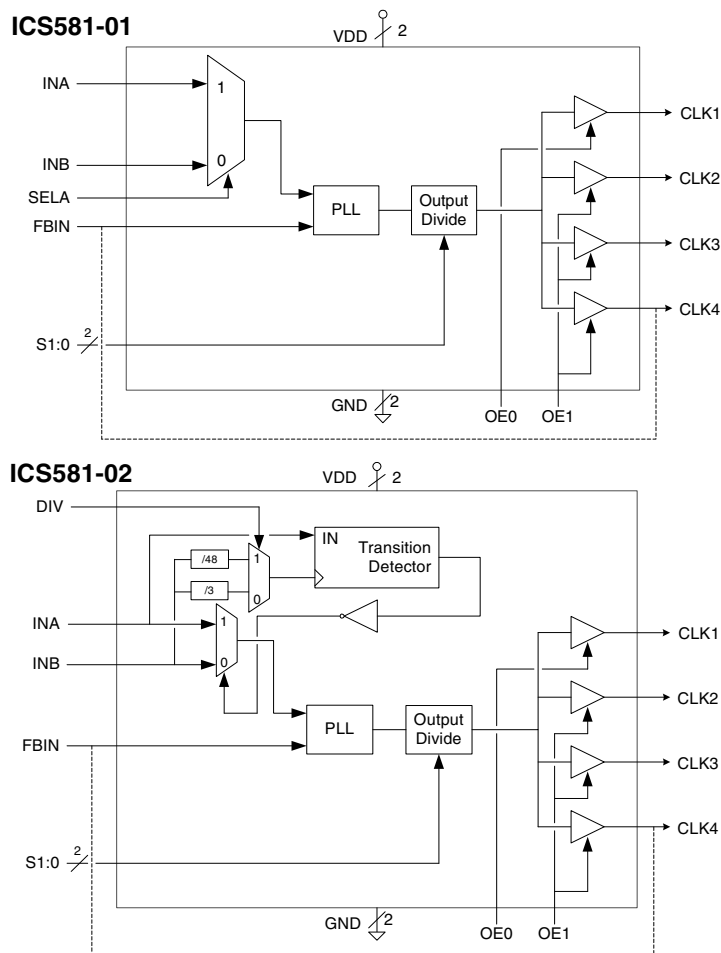
Description

The ICS581-01/02 are glitch free, Phase Locked Loop (PLL) based clock multiplexers (mux) with zero delay from input to output. They each have four low skew outputs which can be configured as a single output, three outputs, or four outputs. The ICS581-01 allows user control over the mux switching, while the ICS581-02 has automatic switching between the two clock inputs.

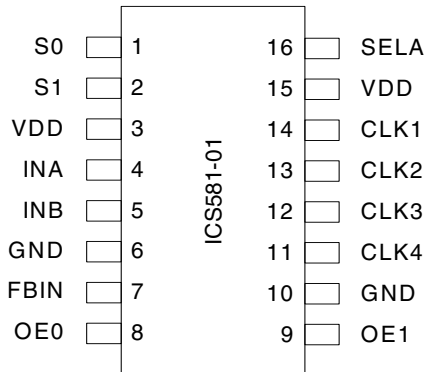
The ICS581-01 and -02 are members of IDT's ClockBlocks™ family of clock generation, synchronization, and distribution devices. For a non-PLL based clock mux, see the ICS580-01.

Features

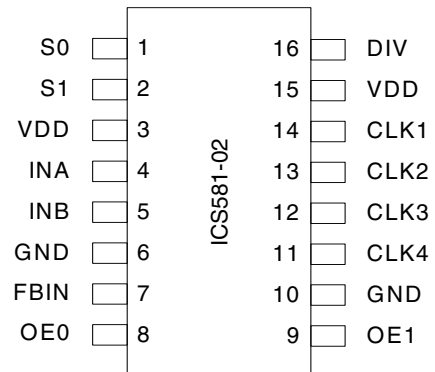
- 16-pin TSSOP package
- RoHS compliant packaging
- No short pulses or glitches on output
- Operates from 6 to 200 MHz
- Low skew outputs
- User controlled (-01) or automatic, timed mux switch (-02)
- Ideal for systems with back-up or redundant clocks
- Zero delay (input to output)
- 50% output duty cycle allows duty cycle correction
- SpreadSmart™ technology works with spread spectrum parts
- Industrial temperature of ICS581-02 available

Block Diagram


Pin Assignment



16 pin 4.40 mil body (0.65 mm pitch) TSSOP



16 pin 4.40 mil body (0.65 mm pitch) TSSOP

Clock Decoding

| SELA | CLK1-4 |
|------|--------|
| 0 | INB |
| 1 | INA |

ICS581-01 only

Timeout Selection

| DIV | Nominal Timeout |
|-----|-------------------|
| 0 | 3x period of INB |
| 1 | 48x period of INB |

ICS581-02 only

Tri-State and Power Down

| OE1 | OE0 | CLK1 | CLK2-4 | PLL |
|-----|-----|------|--------|-----|
| 0 | 0 | Z | Z | Off |
| 0 | 1 | On | Z | On |
| 1 | 0 | Z | On | On |
| 1 | 1 | On | On | On |

ICS581-01/02

Note: Z indicates that the output is in a high impedance state

Frequency Range Select

| S1 | S0 | Input Range (MHz) |
|----|----|-------------------|
| 0 | 0 | 50 - 150 |
| 0 | 1 | 19 - 75 |
| 1 | 0 | 6 - 19 |
| 1 | 1 | 150 - 200 |

ICS581-01/02

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|--|
| 1 | S0 | Input | Select 0 for frequency range. See table. Internal pull-up. |
| 2 | S1 | Input | Select 1 for frequency range. See table. Internal pull-up. |
| 3 | VDD | Power | Power Supply. Connect to +3.3 V or +5 V. |
| 4 | INA | Input | Input Clock A. |
| 5 | INB | Input | Input Clock B. |
| 6 | GND | Power | Connect to ground. |
| 7 | FBIN | Input | Feedback input. Connect to a clock output. |
| 8 | OE0 | Input | Output enable 0. See table. Internal pull-up. |
| 9 | OE1 | Input | Output enable 1. See table. Internal pull-up. |
| 10 | GND | Power | Connect to ground. |
| 11 | CLK4 | Output | Low skew clock output. |
| 12 | CLK3 | Output | Low skew clock output. |
| 13 | CLK2 | Output | Low skew clock output. |
| 14 | CLK1 | Output | Low skew clock output. |
| 15 | VDD | Power | Power Supply. Connect to +3.3 V or +5 V. |
| 16 (-01) | SELA | Input | Mux select. Selects INA when high. Internal pull-up. |
| 16 (-02) | DIV | Input | Timeout select. See table. Internal pull-up. |

Device Operation

The ICS581-01 and ICS581-02 are very similar. Following is a description of the operation of the ICS581-01 and the differences of the ICS581-02.

The ICS581-01 is a PLL-based, zero delay, clock multiplexer. The device consists of an input multiplexer controlled by SELA that selects between two clock inputs. The output of the mux drives the reference input of a phase locked loop. The other input to the PLL comes from a feedback input pin called FBIN. The output of the PLL drives four low skew outputs. These chip outputs are therefore buffered versions of the selected input clock with zero delay and 50/50 duty cycle.

For correct operation, one of the clock outputs must be connected to FBIN. In this datasheet, CLK4 is shown as the feedback, but any one of the four clock outputs can be used. If output termination resistors are used, the feedback should be connected before the resistor. It is a property of the PLL used on this chip that it will align rising edges on FBIN and

either INA or INB (depending on SELA). Since FBIN is connected to a clock output, this means that the outputs appear to align with the input with zero delay.

When the input select (SELA) is changed, the output clock will change frequency and/or phase until it lines up with the new input clock. This occurs in a smooth, gradual manner without any short pulses or glitches and will typically take a few tens of microseconds.

The part must be configured to operate in the correct frequency range. The table on page two gives the recommended range.

The four low skew outputs are controlled by two output enable pins that allow either one, three, or four simultaneous outputs. If both OE pins are low, the PLL is powered down.

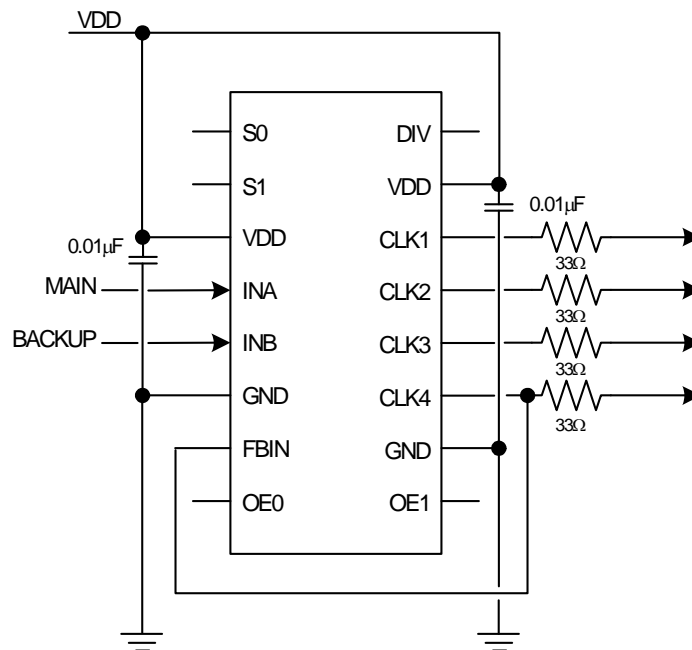
Note that the clock driving the FBIN pin must not be tri-stated unless the PLL is powered down. Otherwise the

PLL will run in an open loop.

The ICS581-02 is identical to the ICS581-01 except for the switching of the input mux. On the ICS581-02, the switching is automatically controlled by a transition detector. The transition detector monitors the clock on INA. If this clock stops, the output of the detector, NO_INA goes high, which then selects clock input INB to the mux. The definition of the clock stopping is determined by a timeout selected by input DIV. If DIV is low, NO_INA will go high after no transitions have occurred on INA for nominally three cycles of the clock on INB. If DIV is high, the timeout is nominally 48 cycles of INB. When INA restarts, the mux immediately switches back to the INA selection with no timeout.

Application Example

A typical application for the ICS581-02 is to provide a backup clock for a system. The backup reliable clock would be connected to INB while the main clock would be connected to INA. If the main clock failed, the ICS581-02 would automatically be switched to the backup clock. The following example shows the connection for this.



In this example, the clocks are 155 MHz and so the frequency range is address 11. Both S0 and S1 are left unconnected, causing the on-chip pull-ups to produce the required high inputs. The same is true for OE0, OE1, and DIV. In this example, CLK4 is used as the feedback. Note that the feedback path is before the series resistor.

Input Clock Frequency

The ICS581-01 and ICS581-02 are designed to switch between two clocks of the same frequency. They will also operate with different frequencies on each of the two input clocks. If the two input frequencies require different input ranges (see table on page two), then the highest range should be permanently selected. When the selected input clock is outside this range, jitter and input skew specifications may not be met. Consult IDT for more information.

External Components

The ICS581-01 and ICS581-02 require two 0.01 μ F capacitors between VDD and GND, one on each side of the chip. These must be close to the chip to minimize lead inductance. Series termination resistors of 33 Ω should be used on the outputs, should also be close to the chip, and the feedback path should be a direct connection from a clock output to a FBIN pin, routed directly under the chip to minimize trace length. This should be connected before the series termination resistor.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS581-01/02. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|--|---------------------|
| Supply Voltage, VDD | 7 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature (ICS581-01, ICS581-02) | 0 to +70°C |
| Ambient Operating Temperature (ICS581-01I, ICS581-02I) | -40 to +85°C |
| Storage Temperature | -65 to +150°C |
| Junction Temperature | 125°C |
| Soldering Temperature | 260°C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|--|------|------|------|-------|
| Ambient Operating Temperature (ICS581-01, ICS581-02) | 0 | | +70 | °C |
| Ambient Operating Temperature (ICS581-01I, ICS581-02I) | -40 | | +85 | °C |
| Power Supply Voltage (measured in respect to GND) | +3.0 | | +5.5 | V |

DC Electrical Characteristics

Unless stated otherwise, VDD = 3.3 V \pm 5%, Ambient Temperature -40 to +85°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--------------------|-----------------|------------------|-----------|-------|-----------|-------|
| Operating Voltage | VDD | | 3.0 | | 5.5 | V |
| Supply Current | IDD | 100 MHz, no load | | 26 | | mA |
| Input High Voltage | V _{IH} | Non-clock inputs | 2 | | | V |
| Input Low Voltage | V _{IL} | Non-clock inputs | | | 0.8 | V |
| Input High Voltage | V _{IH} | INA, INB, FBIN | (VDD/2)+1 | VDD/2 | | V |
| Input Low Voltage | V _{IL} | INA, INB, FBIN | | VDD/2 | (VDD/2)-1 | V |

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--------------------------|----------|---------------------------|---------------------------------------|----------|------|-----------|
| Input Capacitance | C_{IN} | | | 5 | | pF |
| Output High Voltage | V_{OH} | $I_{OH} = -12 \text{ mA}$ | $V_{DD}-0.5$ | | | V |
| Output Low Voltage | V_{OL} | $I_{OL} = 12 \text{ mA}$ | | | 0.5 | V |
| Short Circuit Current | I_{OS} | | | ± 70 | | mA |
| On-chip Pull-up Resistor | R_{PU} | | $S1=0, OE1=0, SELA, DIV \text{ pins}$ | 250 | | $k\Omega$ |

AC Electrical Characteristics

Unless stated otherwise, $V_{DD} = 3.3 \text{ V} \pm 5\%$, Ambient Temperature -40 to $+85^\circ \text{ C}$

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|------------|--|------|-----------|------|---------------|
| Input Frequency | f_{IN} | | 6 | | 200 | MHz |
| Input Clock Duty Cycle | | at $V_{DD}/2$ | 30 | | 70 | % |
| Skew | t_{SKEW} | selected input clock to FBIN, Note 1 | -250 | 0 | 250 | ps |
| | | between any output clocks, Note 2 | -250 | 0 | 250 | ps |
| Transition Detector Timeout ICS581-02 only | | $DIV = 0$ | 2 | 3 | 4 | INB periods |
| | | $DIV = 1$ | 32 | 48 | 64 | INB periods |
| Frequency Transition Time | t_{TRAN} | 50 to 150 MHz, Note 3, 4 | | 70 | 200 | μs |
| | | 100 to 100 MHz, Note 3, 5 | | 4 | 10 | μs |
| Output Clock Rise Time | t_{OR} | 0.8 V to 2.0 V | | 1 | 2 | ns |
| Output Clock Fall Time | t_{OF} | 2.0 V to 0.8 V | | 1 | 2 | ns |
| Output Clock Duty Cycle | | less than 133 MHz at $V_{DD}/2$, no load | 45 | | 55 | % |
| | | greater than 133 MHz at $V_{DD}/2$, no load | 40 | | 60 | % |
| | | with $S0=S1=1$ at $V_{DD}/2$, no load | 40 | | 60 | % |
| Absolute Output Clock Period Jitter | t_{JA} | Deviation from mean | | ± 150 | | ps |
| One Sigma Output Clock Period Jitter | t_{JA} | | | 40 | | ps |

Note 1: Assumes clocks with same rise times, measured at $V_{DD}/2$.

Note 2: Assumes identically loaded outputs with identical rise times, measured at $V_{DD}/2$. The maximum skew between any two clocks is 250 ps not 500 ps.

Note 3: Time taken for output to lock to new clock when mux selection changed from INA to INB.

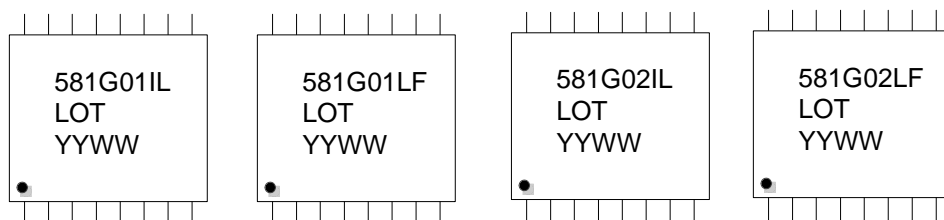
Note 4: With 50 MHz on INA and 150 MHz on INB.

Note 5: With 100 MHz on both INA and INB, 180° out of phase.

Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 78 | | °C/W |
| | θ_{JA} | 1 m/s air flow | | 70 | | °C/W |
| | θ_{JA} | 3 m/s air flow | | 68 | | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | | | 37 | | °C/W |

Marking Diagrams

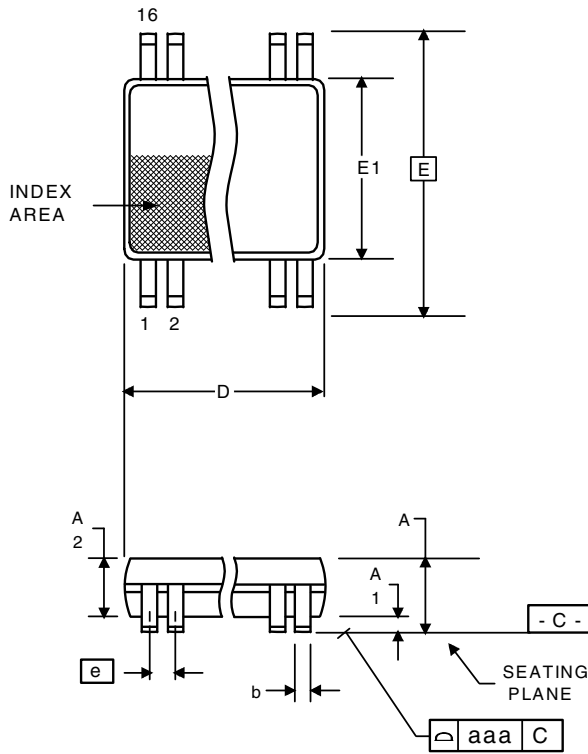


Notes:

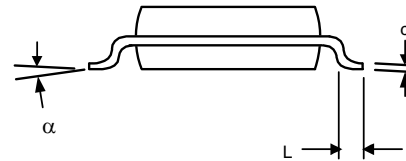
1. "LOT" is the lot number/sequence.
2. "YYWW" is the last two digits of the year and the week number that the part was assembled.
3. Bottom marking: country of origin if not USA.

Package Outline and Package Dimensions (16-pin TSSOP, 4.40 mm Body, 0.65 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153



| Symbol | Millimeters | | Inches | |
|----------|-------------|------|--------------|-------|
| | Min | Max | Min | Max |
| A | -- | 1.20 | -- | 0.047 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| A2 | 0.80 | 1.05 | 0.032 | 0.041 |
| b | 0.19 | 0.30 | 0.007 | 0.012 |
| C | 0.09 | 0.20 | 0.0035 | 0.008 |
| D | 4.90 | 5.1 | 0.193 | 0.201 |
| E | 6.40 BASIC | | 0.252 BASIC | |
| E1 | 4.30 | 4.50 | 0.169 | 0.177 |
| e | 0.65 Basic | | 0.0256 Basic | |
| L | 0.45 | 0.75 | 0.018 | 0.030 |
| α | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | 0.004 |



Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|------------|--------------------|--------------|---------------|
| 581G-01ILF | See page 7 | Tubes | 16-pin TSSOP | -40 to +85° C |
| 581G-01ILFT | | Tape and Reel | 16-pin TSSOP | -40 to +85° C |
| 581G-01LF | | Tubes | 16-pin TSSOP | 0 to +70° C |
| 581G-01LFT | | Tape and Reel | 16-pin TSSOP | 0 to +70° C |
| 581G-02ILF | | Tubes | 16-pin TSSOP | -40 to +85° C |
| 581G-02ILFT | | Tape and Reel | 16-pin TSSOP | -40 to +85° C |
| 581G-02LF | | Tubes | 16-pin TSSOP | 0 to +70° C |
| 581G-02LFT | | Tape and Reel | 16-pin TSSOP | 0 to +70° C |

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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