AN-2150 LM3450A Evaluation Board

1 Introduction

The LM3450A evaluation board is designed to provide an AC to LED solution for a 30W LED load. Specifically, it takes an AC mains input and converts it to a constant current output of 700mA for a series string of 1 to 13 LEDs (maximum LED stack voltage of 45V). There are two assembly versions designed to operate from two different nominal AC input voltages, $120V_{AC}$ or $230V_{AC}$. .

The board employs a two stage design with an LM3450A flyback primary stage and an LM3409HV secondary stage. The LM3450A provides an isolated 50V regulated output voltage and a power factor corrected input current. The LM3409HV uses the 50V flyback output as its input and provides a constant current of 700mA to the LED load. This two stage design provides excellent line and load regulation as well as isolation. The board is comprised of two copper layers with components on both sides and an FR4 dielelctric.

The two-stage design has several key advantages over a single stage design including:

- No 120Hz LED current ripple
- Better dimming performance at low dimming levels.
- Better line disturbance rejection
- Better efficiency using small LED stack voltages

2 Specifications

$120V_{AC}$ 30W Version

- Input Voltage Range: V_{IN} = $90V_{AC}$ – $135V_{AC}$
- Regulated Flyback Output Voltage: V_{OUT} = 50V
- Maximum LED Stack Voltage: V_{LED} < 45V
- Regulated LED Current: I_{LED} = 700mA

$230V_{AC}$ 30W Version

- Input Voltage Range: V_{IN} = $180V_{AC}$ – $265V_{AC}$
- Regulated Flyback Output Voltage: V_{OUT} = 50V
- Maximum LED Stack Voltage: V_{LED} < 45V
- Regulated LED Current: I_{LED} = 700mA

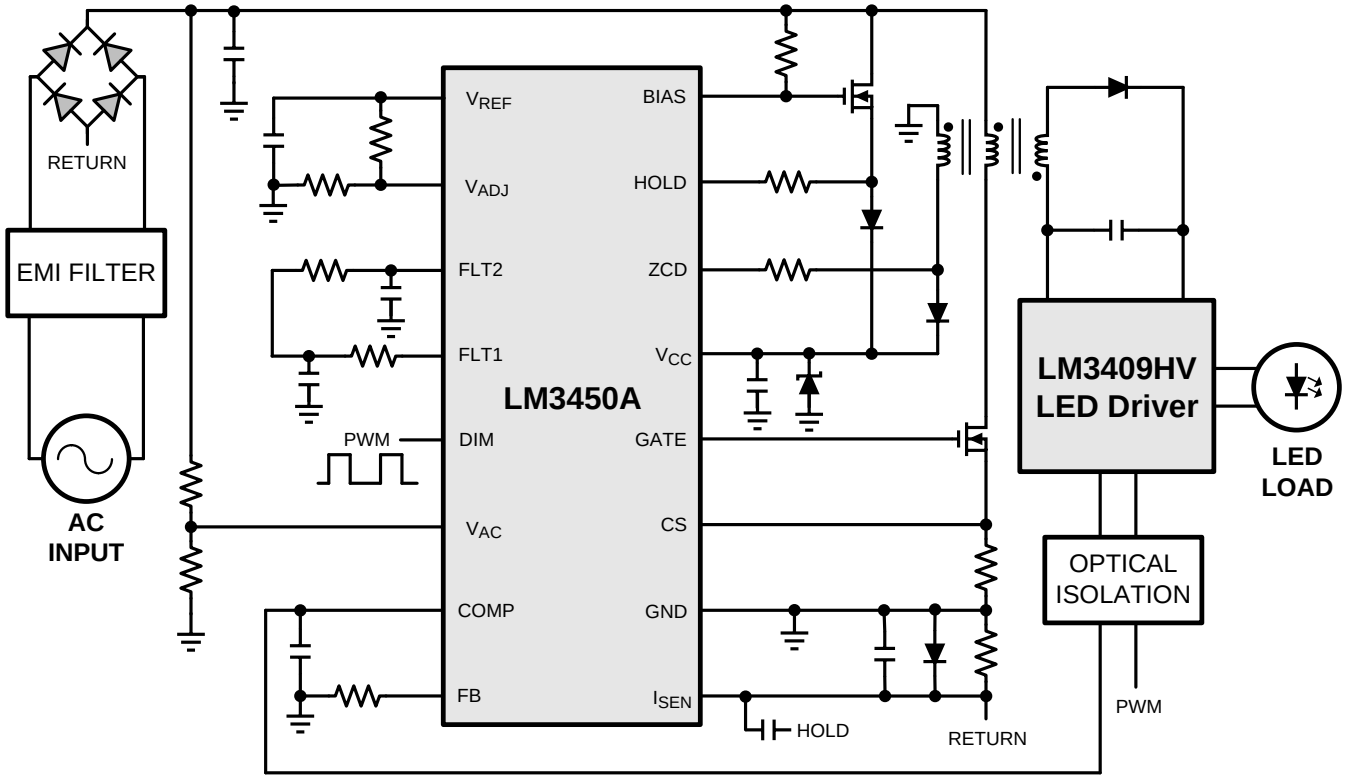


Figure 1. Schematic

3 Typical Performance

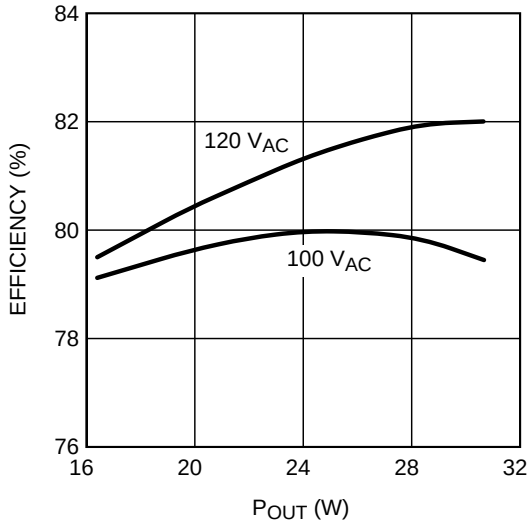


Figure 2. 120V, 30W Version Efficiency vs. Output Power

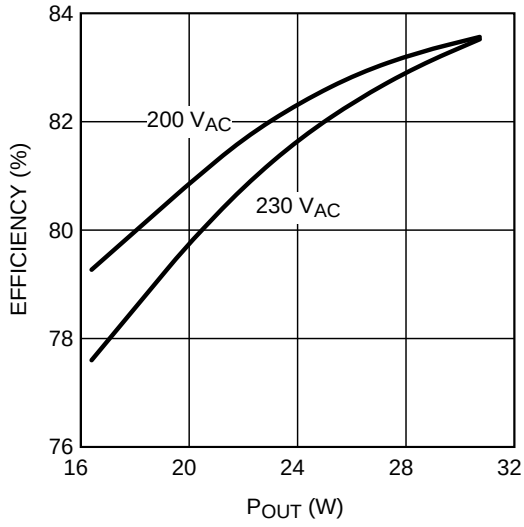


Figure 3. 230V, 30W Version Efficiency vs. Output Power

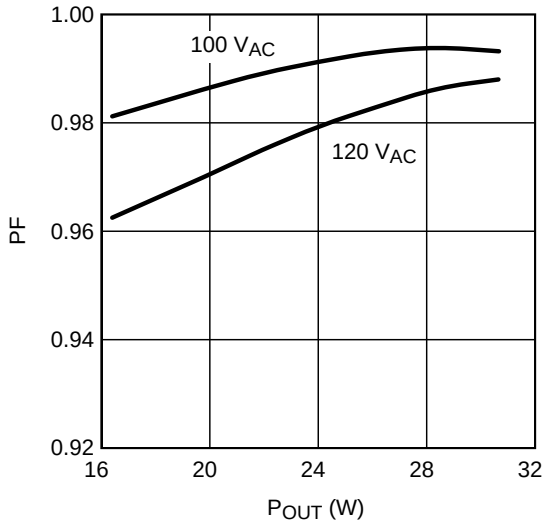


Figure 4. 120V, 30W Version Power Factor vs. Output Power

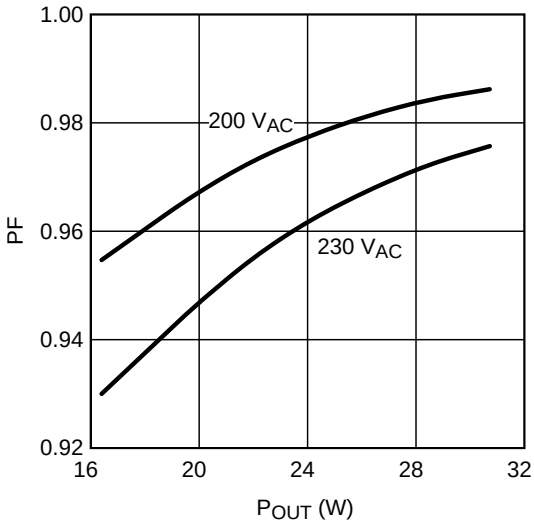


Figure 5. 230V, 30W Version Power Factor vs. Output Power

4 Conducted EMI Performance

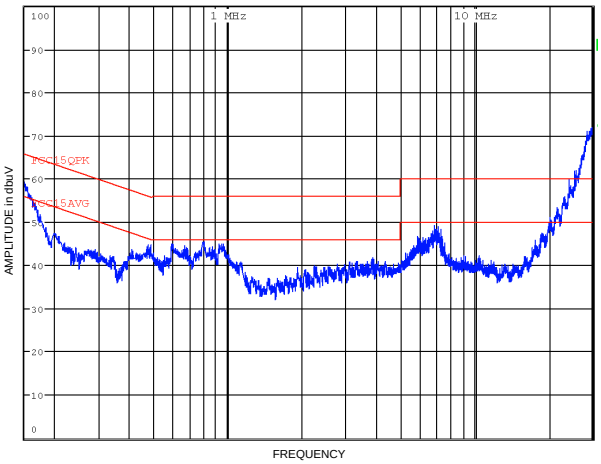


Figure 6. 120V, 30W Conducted EMI Peak Scan Line and Neutral - CISPR/FCC Class B Quasi Peak and Average Limits

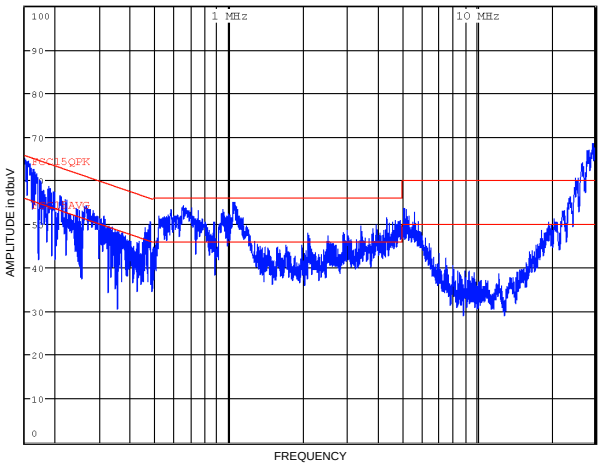


Figure 7. 230V, 30W Conducted EMI Peak Scan Line and Neutral - CISPR/FCC Class B Quasi Peak and Average Limits

5 THD / Harmonic Performance

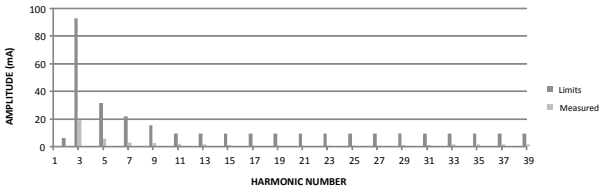


Figure 8. 120V, 30W THD Measurements EN 61000-3 Class C Limits THD = 6.27% ; Fundamental = 316mA

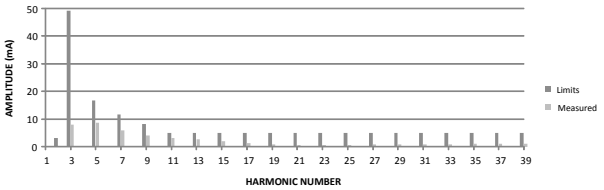
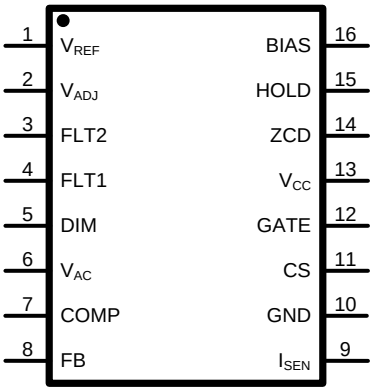


Figure 9. 230V, 30W THD Measurements EN 61000-3 Class C Limits THD = 8.96% ; Fundamental = 167mA

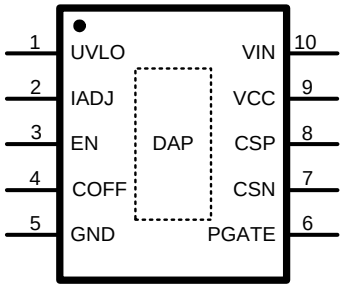
6 LM3450A Pin Descriptions



Pin	Name	Description	Application Information
1	V_{REF}	3V Reference	Reference Output: Connect directly to V_{ADJ} or to resistor divider feeding V_{ADJ} and to necessary external circuits.
2	V_{ADJ}	Analog Adjust	Analog Dim and Phase Dimming Range Input: Connect directly to V_{REF} to force standard 70% phase dimming range. Connect to resistor divider from V_{REF} to extend usable range of some phase dimmers or for analog dimming. Connect to GND for low power mode.
3	FLT2	Filter 2	Ramp Comparator Input: Connect a series resistor from FLT1 capacitor and a capacitor to GND to establish second filter pole.
4	FLT1	Filter 1	Angle Decoder Output: Connect a series resistor to a capacitor to ground to establish first filter pole.
5	DIM	500 Hz PWM Output	Open Drain PWM Dim Output: Connect to dimming input of output stage LED driver (directly or with isolation) to provide decoded dimming command.
6	V_{AC}	Sampled Rectified Line	Multiplier and Angle Decoder Input: Connect to resistor divider from rectified AC line.
7	COMP	Compensation	Error Amplifier Output and PWM Comparator Input: Connect a capacitor to GND to set the compensation.
8	FB	Feedback	Error Amplifier Inverting Input: Connect to output voltage via resistor divider to control PFC voltage loop for non-isolated designs. Connect to a 5.11kΩ resistor to GND for isolated designs (bypasses error amplifier). Also includes over-voltage protection and shutdown modes.
9	I_{SEN}	Input Current Sense	Input Current Sense Non-Inverting Input: Connect to diode bridge return and resistor to GND to sense input current for dynamic hold. Connect a 0.1µF capacitor and Schottky diode to GND, and a 0.22µF capacitor to HOLD.
10	GND	Power Ground	System Ground
11	CS	Current Sense	MosFET Current Sense Input: Connect to positive terminal of sense resistor in PFC MosFET source.
12	GATE	Gate Drive	Gate Drive Output: Connect to gate of main power MosFET for PFC.Gate Drive Output: Connect to gate of main power MosFET for PFC.
13	V_{CC}	Input Supply	Power Supply Input: Connect to primary bias supply. Connect a 0.1µF bypass capacitor to ground.
14	ZCD	Zero Crossing Detector	Demagnetization Sense Input: Connect a resistor to transformer/inductor winding to detect when all energy has been transferred.
15	HOLD	Dynamic Hold	Open Drain Dynamic Hold Input: Connect to holding resistor which is connected to source of passFET.

Pin	Name	Description	Application Information
16	BIAS	Pre-regulator Gate Bias	Pre-regulator Gate Bias Output: Connect to gate of passFET and to resistor to rectified AC (drain of passFET) to aid with startup.

7 LM3409HV Pin Descriptions



Pin	Name	Description	Application Information
1	UVLO	Input Under Voltage Lock-out	Connect to a resistor divider from V_{IN}. UVLO threshold is 1.24V and hysteresis is provided by a 22µA current source.
2	I_{ADJ}	Analog LED Current Adjust	Apply a voltage between 0 - 1.24V, or connect a resistor from this pin to GND, to set the current sense threshold voltage.
3	EN	Logic Level Enable	Apply a voltage >1.6V to enable device, a PWM signal to dim, or a voltage <0.6V for low power shutdown.
4	COFF	Off-time programming	Connect an external resistor from V_O to this pin, and a capacitor from this pin to GND to set the off-time.
5	GND	Power Ground	Connect to the system ground.
6	PGATE	Gate Drive	Connect to the gate of the external PFET.
7	CSN	Negative Current Sense	Connect to the negative side of the sense resistor.
8	CSP	Positive Current Sense	Connect to the positive side of the sense resistor (also connected to V_{IN}).
9	V_{CC}	V_{IN}-referenced Linear Regulator Output	Connect at least a 1 µF ceramic capacitor from this pin to CSN. The regulator provides power for P-FET drive.
10	V_{IN}	Input Voltage	Connect to the input voltage.
DAP	DAP	Thermal PAD on bottom of IC	Connect to pin 5 (GND). Place 4-6 vias from DAP to bottom layer GND plane.

8 Simplified Evaluation Board Schematic

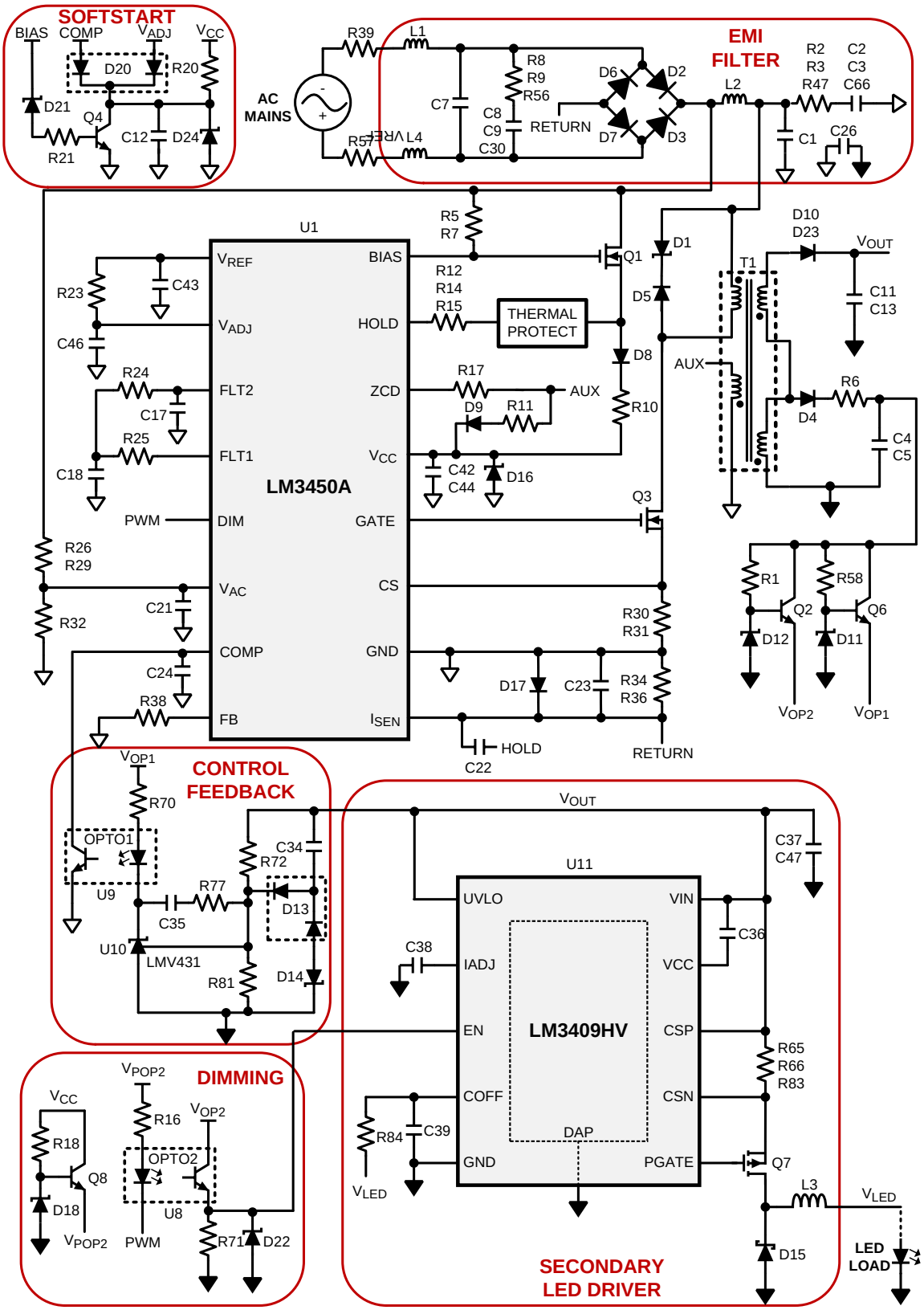


Figure 10. Simplified Evaluation Board Schematic

9 Design Information

The following section explains how to design using the LM3450A power factor controller and phase dimming decoder. Refer to *AN-1953 LM3409HV Evaluation Board* (SNVA390) for a detailed design procedure of the LM3409HV secondary stage and to the *LM3450/A LED Drivers with Active Power Factor Correction & Phase Dimming Decoder* (SNVAS681) data sheet for specific details regarding the function of the LM3450A device. All reference designators refer to the *Simplified Evaluation Board Schematic*. Note that parallel and series resistances are combined in one schematic symbol for simplification. To improve readability of this design document, each subsection is followed by a list of Definitions for new terms used in the calculations. Section 11, showing all components and connectors, is found at the end of this document as well as a Bill of Materials for each assembly version.

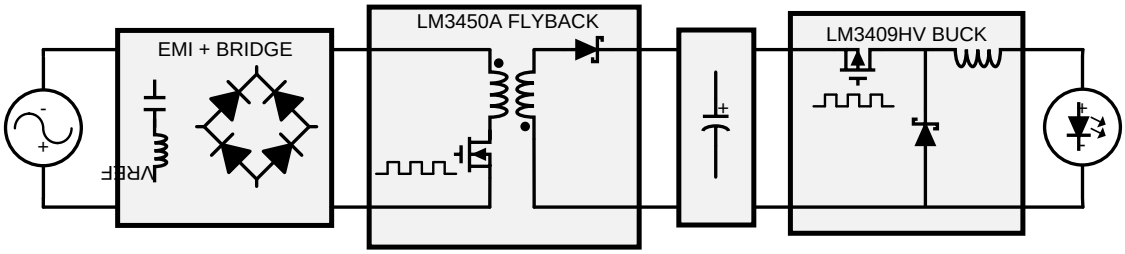


Figure 11. Two-Stage PFC LED Driver

9.1 1ST Stage - CRM Flyback

The first stage of the evaluation board shown in Figure 11 is a critical conduction mode (CRM) flyback converter controlled with the LM3450A. CRM converters operate at the boundary of continuous conduction mode (CCM) and discontinuous conduction mode (DCM). CRM is implemented by turning on the main switching FET (Q3) until the primary current rises to a peak threshold. Q3 is then turned off and the current falls until a zero crossing is detected. At this point, Q3 is turned on and the cycle repeats.

In the CRM flyback PFC application, the rectified AC input is fed forward to the control loop, yielding a sinusoidal peak current threshold. This peak threshold creates a sinusoidal primary peak current envelope $I_{P\text{-}pk}$ as shown in Figure 12. The secondary peak current envelope $I_{S\text{-}pk}$ will simply be a scaled version of the primary according to the turns ratio of the transformer. Assuming good attenuation of the switching ripple via the EMI filter, the average input current $I_{IN}(t)$, shown in red, can also be approximated as a sinusoid. Since the input current has the same shape and phase as the input voltage, high power factor (PF) can easily be achieved.

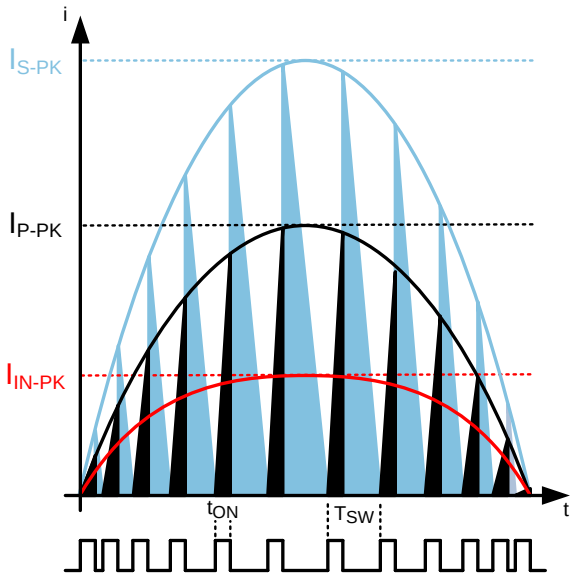


Figure 12. CRM Flyback Current Waveforms

The input current shaping happens instantly in CRM due to the feed-forward mechanism; however, the converter must also regulate the flyback output voltage with a traditional feedback loop. This is accomplished with a narrow bandwidth error amplifier coupled with energy storage capacitance at the output to limit the twice line frequency ripple. The output of the error amplifier is multiplied with the scaled rectified AC voltage to achieve both input current shaping and output voltage regulation. Refer to the datasheet for a more detailed explanation of the power factor controller.

The LM3450A also has a phase decoder that interprets the phase dimming angle and maps it to a 500Hz PWM open-drain output at the DIM pin. This signal is directly connected to an opto-isolator to send across the isolation boundary to the second stage LED driver. In addition, the LM3450A provides a dynamic hold circuit to ensure that the holding current requirement is satisfied in forward phase dimmers. Refer to the datasheet for a more detailed explanation of the phase dimmer decoder.

9.2 2ND Stage - Buck LED Driver

The second stage of the evaluation board is a buck LED driver controlled with the LM3409HV. The input to this stage is the flyback output voltage and the output is a regulated constant current of 700mA to a stack of <45V of LEDs. The LM3409HV is a hysteretic PFET controller using peak current detection and a constant off-timer to provide regulated LED current with a constant switching frequency ripple. Coupled with the flyback energy storage capacitance, the LM3409HV is able to remove all 120HZ ripple content from the LED output. The 500Hz PWM signal from the first stage is used as the dimming input to the LM3409HV. The output of the opto-isolator is connected directly to the EN pin of the LM3409HV to provide a PWM dimmed LED current according to the detected phase angle at the primary.

The LM3409HV design is not included in this document. Refer to AN-1953 for a detialed design procedure. The specifications for the second stage are:

- Nominal Input Voltage = 50V
- Regulated LED Current = 700mA
- Nominal LED Stack Voltage = 45V
- Switching Frequency at Nominal Input = 100kHz
- Inductor/LED Current Ripple = 115mA

9.3 CRM Flyback Converter

Operating Points

The AC mains voltage, at the line frequency f_L, is assumed to be perfectly sinusoidal and the diode bridge ideal. This yields a perfect rectified sinusoid at the input to the flyback. The input voltage $V_{in}(t)$ is defined in terms of the peak input voltage:

$$V_{in}(t) = V_{IN\text{-}PK} \times \left|\sin(2 \times \pi \times f_L \times t)\right|$$
$$V_{IN\text{-}PK} = V_{IN} \times \sqrt{2} \quad (1)$$

The controller and the transformer are also assumed to be ideal. These assumptions yield a sinusoidal peak primary current envelope $I_{P\text{-}pk}(t)$ and peak secondary current envelope $I_{S\text{-}pk}(t)$ as shown in Figure 12. Both are defined in terms of the peak primary current:

$$I_{P\text{-}pk}(t) = I_{P\text{-}pk} \times \left|\sin(2 \times \pi \times f_L \times t)\right|$$
$$I_{S\text{-}pk}(t) = n \times I_{P\text{-}pk}(t) \quad (2)$$

The output voltage reflected to the primary is defined:

$$V_R = n \times V_{OUT} \quad (3)$$

CRM control yields a variable duty cycle over a single line cycle with a minimum occurring at the peak input voltage:

$$D(t) = \frac{V_R}{V_R + V_{in}(t)}$$
$$D_{MIN} = \frac{V_R}{V_R + V_{IN\text{-}PK}} \quad (4)$$

The resulting sinusoidal average input current $I_{in}(t)$, shown in Figure 12, is approximated as the average of each triangular current pulse during a switching period. The peak input current occurs at the peak primary current:

$$I_{in}(t) = \frac{I_{P\text{-}PK} \times D(t)}{2}$$
$$I_{IN\text{-}PK} = \frac{I_{P\text{-}PK} \times D_{MIN}}{2} \quad (5)$$

Turns Ratio

The first thing to decide with an isolated design is the desired transformer turns ratio. This should be based on the specified output voltage and the maximum peak input voltage. Frequently the MosFET is already chosen for a design, given its cost and availability. With a desired MosFET voltage, the maximum reflected voltage at the primary is calculated:

$$V_{R\text{-}MAX} = \frac{2}{3} \times (V_{T\text{-}DES\text{-}MAX} - V_{IN\text{-}PK\text{-}MAX}) \quad (6)$$

Generally, an integer turns ratio is selected to achieve a reflected voltage at or below the defined maximum:

$$n < \frac{V_{R\text{-}MAX}}{V_{OUT}} \quad (7)$$

Switching MosFET

The main switching MosFET (Q3) can be sized as desired; to block the maximum drain-to-source voltage, operate at the maximum RMS current, and dissipate the maximum power:

$$V_{T\text{-}MAX} = V_{IN\text{-}PK\text{-}MAX} + (1.5 \times V_R)$$
$$I_{T\text{-}PK\text{-}MAX} = I_{P\text{-}PK\text{-}MAX}$$
$$I_{T\text{-}RMS\text{-}MAX} = I_{P\text{-}PK\text{-}MAX} \times \sqrt{\frac{D_{@IIN\text{-}PK\text{-}MAX}}{3}}$$
$$P_{T\text{-}MAX} = I_{T\text{-}RMS\text{-}MAX}^2 \times R_{DS\text{-}ON} \quad (8)$$

The peak current limit should be at least 25% higher than the maximum peak input current:

$$R30 \,||\, R31 = \frac{1.5V}{I_{LIM}} \tag{9}$$

The parallel sense resistor combination (R30||R31) has to dissipate the maximum power:

$$P_{R30||R31} = I_{T\text{-}RMS\text{-}MAX}^2 \times R30 \,||\, R31 \tag{10}$$

Switching Diode

The main switching diode (D10) should be sized to block the maximum reverse voltage , operate at the maximum average current, and dissipate the maximum power:

$$V_{RD\text{-}MAX} = V_{OUT} + \left(\frac{V_{IN\text{-}PK\text{-}MAX}}{n} \right)$$
$$I_{D\text{-}MAX} = I_{IN\text{-}PK\text{-}MAX} \times 2$$
$$I_{D\text{-}PK\text{-}MAX} = I_{P\text{-}PK\text{-}MAX} \times 2$$
$$P_{D\text{-}MAX} = I_{D\text{-}MAX} \times V_{FD} \tag{11}$$

Definitions

n – Primary to Secondary Turns Ratio

V_{OUT} – Regulated Output Voltage

V_{IN} – Nominal AC Input Voltage

$V_{IN\text{-}PK}$ – Peak Input Voltage

$V_{IN\text{-}PK\text{-}MAX}$ – Maximum Peak Input Voltage

$I_{P\text{-}PK}$ – Peak Primary Current

$I_{S\text{-}PK}$ – Peak Secondary Current

$I_{IN\text{-}PK}$ – Peak Input Current

I_{LIM} – Peak Current Limit

D_{MIN} – Minimum Duty Cycle over Line Cycle

V_R – Output Voltage Reflected to Primary

$V_{R\text{-}MAX}$ – Maximum Tolerable Reflected Voltage

$V_{T\text{-}DES\text{-}MAX}$ – Maximum Tolerable MosFET Voltage

$V_{T\text{-}MAX}$ – Maximum MosFET Blocking Voltage

$I_{T\text{-}RMS\text{-}MAX}$ – Maximum MosFET RMS Current

$I_{T\text{-}PK\text{-}MAX}$ – Maximum MosFET Peak Current

$P_{T\text{-}MAX}$ – Maximum MosFET Power Dissipation

$V_{RD\text{-}MAX}$ – Maximum Diode Blocking Voltage

$I_{D\text{-}MAX}$ – Maximum Diode Average Current

$I_{D\text{-}PK\text{-}MAX}$ – Maximum Diode Peak Current

$P_{D\text{-}MAX}$ – Maximum Diode Power Dissipation

9.4 Transformer

Primary Inductance

The maximum peak input current, occuring at the minimum AC voltage peak, determines the necessary flyback transformer energy storage. As a general rule of thumb, the desired duty cycle at this worst-case operating point should be specified near 0.5 to limit large conduction losses associated with high voltage diodes. The maximum input current can be approximated by the maximum output power, expected converter efficiency, and minimum input voltage. Note that there is also a 0.85 multiplier to account for the fact that maximum power with a triac dimmer in-line is demanded at approximately 85% of the full sinusoidal voltage waveform. Given the desired duty cycle, the maximum peak input current and corresponding maximum peak primary current can be approximated:

$$I_{IN-MAX} = \frac{P_{OUT-MAX}}{\eta \times 0.85 \times V_{IN-MIN}}$$
$$I_{IN-PK-MAX} = I_{IN-MAX} \times \sqrt{2}$$
$$I_{P-PK-MAX} = \frac{2 \times I_{IN-PK-MAX}}{D_{@IIN-MAX-PK}} \quad (12)$$

Using the calculated turns ratio and the desired minimum switching frequency, the minimum necessary primary inductance is calculated:

$$L_{P-MIN} > \frac{D_{MIN@IIN-PK-MAX}^2 \times V_{IN-MIN}}{2 \times f_{SW-MIN-DES} \times I_{IN-PK-MAX}} \quad (13)$$

Switching Frequency Range

Given a primary inductance that meets the above constraint, the variable switching frequency has the following limits:

$$f_{SW-MAX} = \frac{V_{IN-PK}}{L_P \times I_{P-PK}}$$
$$f_{SW-MIN} = \frac{V_{IN-PK} \times V_R}{L_P \times I_{P-PK} \times (V_R + V_{IN-PK})} \quad (14)$$

Transformer Geometries and Materials

The length of the gap necessary for energy storage in the flyback transformer can be determined numerically; however, this can lead to non-standard designs. Instead, an appropriate A_L core value (160nH/turns2 is a good standard value to start with) can be chosen that will imply the gap size. A_L is an industry standard used to define how much inductance, per turns squared, that a given core can provide. With the initial chosen A_L value, the number of turns on the primary and secondary are calculated:

$$N_P = \sqrt{\frac{L_P}{A_L}}$$
$$N_S = \frac{N_P}{n} \quad (15)$$

Given the switching frequency range and the maximum output power, a core size can be chosen using the vendor's specifications and recommendations. This choice can then be validated by calculating the maximum operating flux density given the core cross-sectional area of the chosen core.

$$B_{MAX} = \frac{L_P \times I_{P-PK-MAX}}{N_P \times A_{E-MAX}} \quad (16)$$

With most common core materials, the maximum operating flux density should be set between 300mT and 3400mT. If the calculation is below this range, then A_L should be increased to the next standard value and the turns and maximum flux density calculations iterated. If the calculation is above this range, then A_L should be decreased to the next standard value and the turns and maximum flux density calculations iterated.

With the flux density appropriately set, the core material for the chosen core size can be determined using the vendor's specifications and recommendations. Note that there are core materials that can tolerate higher flux densities; however, they are usually more expensive and not always practical for these designs.

The rest of the transformer design should be done with the aid of the manufacturer. There are calculated trade-offs between the different loss mechanisms and safety constraints that determine how well a transformer performs. This is an iterative process and can ultimately result in the choice of a new core or switching frequency range. The previous steps should reduce the number of iterations significantly but a good transformer manufacturer is invaluable for completion of the process.

Definitions

η – Expected converter efficiency

$P_{OUT-MAX}$ – Maximum Output Power

V_{IN-MIN} – Minimum RMS AC Line Voltage

$V_{IN-PK-MIN}$ – Minimum Peak Input Voltage

$I_{IN-PK-MAX}$ – Maximum Peak Input Current

$I_{P-PK-MAX}$ – Maximum Peak Primary Current

$D_{@IIN-PK-MAX}$ – Duty Cycle at Maximum Peak Input Current

L_{P-MIN} – Minimum Necessary Primary Inductance

L_P – Chosen Primary Inductance

$f_{SW-MIN-DES}$– Desired Minimum Switching Frequency

f_{SW-MIN} – Minimum Switching Frequency

f_{SW-MAX} – Maximum Switching Frequency

N_P – Number of Primary Turns

N_S – Number of Secondary Turns

A_{E-MAX} – Core Cross-Sectional Area

B_{MAX} – Maximum Operating Flux Density

A_L – Transformer Core Figure of Merit

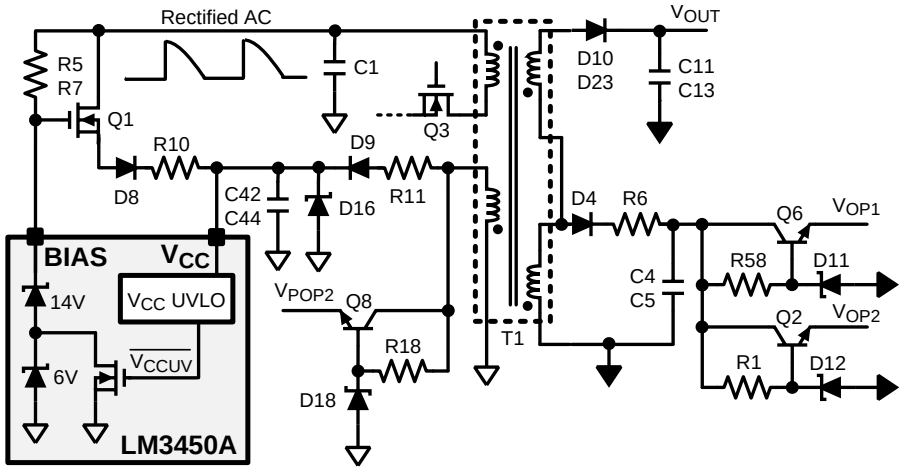


Figure 13. Bias Circuitry

9.5 Bias Supplies and Capacitances

Bias Supplies

The primary bias supply shown in Figure 13 enables instant turn-on through Q1 while providing an auxiliary winding for high efficiency steady state operation. The two bias paths are each connected to V_{CC} through a diode (D8, D9) to ensure the higher of the two is providing V_{CC} current. The LM3450A BIAS pin helps to ensure that the auxiliary winding is always providing V_{CC} during normal operation.

Since there is optical isolation, a secondary bias supply is also desirable. This is accomplished with another auxiliary winding, diode (D4), and capacitance (C4, C5) which creates another flyback output that scales with the regulated output (similar to the auxiliary primary bias winding). To ensure secondary bias regulation is closely coupled to the regulated flyback output, the output winding is tapped to provide the secondary bias output.

It is also advantageous to linear regulate down to approximately 9V, from the 12V bias supplies, for every opto-isolator supply rail (V_{POP1}, V_{OP1}, V_{OP2}) . This will stabilize the opto-isolator rail over the entire operating range, preventing noise coupling into COMP and the dimming input of the LM3409.

The primary and secondary bias outputs for both versions of the board are set to 12.5V at the nominal input voltage. The turns calculations (referred to the output) for the primary auxiliary winding and the tap point for the secondary winding are:

$$n_{AUX} = \frac{V_{OUT}}{V_{CC}}$$
$$N_A = \frac{N_S}{n_{AUX}} \quad (17)$$

The minimum primary bias supply capacitance is calculated, given a minimum V_{CC} ripple specification, to keep V_{CC} above UVLO at the worst-case current:

$$C44 = \frac{I_{CC}}{\Delta v_{CC} \times f_{2L}} \quad (18)$$

Input Capacitance

The input capacitor of the flyback (C1), also called the PFC capacitor, has to be able to provide energy during the worst-case switching period at the peak of the AC input. C1 should be a high frequency, high stability capacitor (usually a metallized film capacitor, either polypropylene or polyester) with an AC rating equal to the maximum input voltage. C1 should also have a DC voltage rating exceeding the maximum peak input voltage + half of the peak to peak input voltage ripple specification. The minimum required input capacitance is calculated given the same ripple specification:

$$C1 = \frac{L_P \times I_{P\text{-}PK\text{-}MAX}^2}{\left(V_{IN\text{-}PK\text{-}MIN} + \frac{\Delta v_{IN\text{-}PK}}{2}\right)^2 - \left(V_{IN\text{-}PK\text{-}MIN} - \frac{\Delta v_{IN\text{-}PK}}{2}\right)^2} \quad (19)$$

Output Capacitance

Since the LM3450A is a power factor controller, C1 is minimized and the output capacitor (C11) serves as the main energy storage device. C11 should be a high quality electrolytic capacitor that can tolerate the large current pulses associated with CRM operation. The voltage rating should be at least 25% greater than the regulated output voltage and, given the desired voltage ripple, the minimum output capacitance is calculated:

$$C11 = \frac{P_{OUT\text{-}MAX}}{2 \times \pi \times f_L \times V_{OUT} \times \Delta v_{OUT}} \quad (20)$$

Definitions

$\Delta v_{IN\text{-}PK}$ – Peak Input Voltage Switching Ripple

Δv_{OUT} – Nominal Output Voltage Ripple

Δv_{CC} – Nominal Primary Bias Ripple

V_{CC} – Primary Bias Capacitance

n_{AUX} – Output to Auxiliary Turns Ratio

N_A – Number of Auxiliary Turns

f_{2L} – Twice Line Frequency

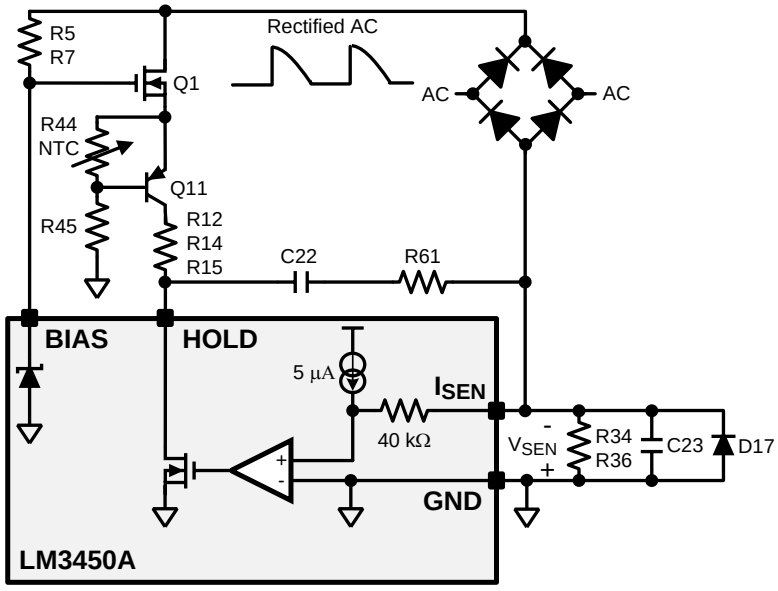


Figure 14. Dynamic Hold Circuit with Thermal Protection

9.6 Hold Current

Dynamic Hold

The LM3450A regulates the minimum input current with a dynamic hold circuit to ensure the triac holding current requirement is satisfied. The regulated minimum current is set by choosing the sense resistor (R34||R36):

$$I_{IN\text{-}MIN\text{-}REG} = \frac{200\ mV}{R34\ ||\ R36} \tag{21}$$

The maximum possible holding current (usually occurs during transients when triac fires) is set by choosing the hold resistor (R12||R14||R15) between the source of the Q1 and HOLD:

$$I_{HOLD\text{-}MAX} = \frac{V_{CC}}{R12\ ||\ R14\ ||\ R15 + 30\Omega} \tag{22}$$

PassFET

The passFET (Q1) is used in its linear region to stand-off the line voltage from the LM3450A controller. Both the V_{CC} startup current and the triac holding current are conducted through the device. Since the holding current is far larger than the startup current and is dynamically adjusted every cycle, it will dominate the calculations. Given this, Q1 is chosen to block the maximum peak input voltage and conduct the maximum holding current. The surge handling capability of Q1 is also important and is evaluated by looking at the safe operating area (SOA) of the device.

Finally, Q1 needs to be able to dissipate the maximum power. Looking at an absolute worst-case condition for the Q1 (during open load where the converter draws near-zero power), extremely large power dissipation is required (many Watts). Designing for this case is unrealistic and costly. Instead, Figure 15 can be used to find the maximum $I_{IN\text{-}MIN\text{-}REG}$ for the desired minimum output power level. The minimum output power is defined as the output power that causes the dynamic hold to force approximately 1W of power dissipation in Q1 (causing approximately 100°C rise in a DPAK). Below the minimum output power level, Q1 can reach temperatures exceeding 125°C, depending on the conduction angle, causing potential catastrophic failure. Figure 15 is only a general guideline based on experimental testing of this evaluation board. Each application will have a different passFET thermal characteristic, which suggests thermal protection of the passFET is usually necessary.

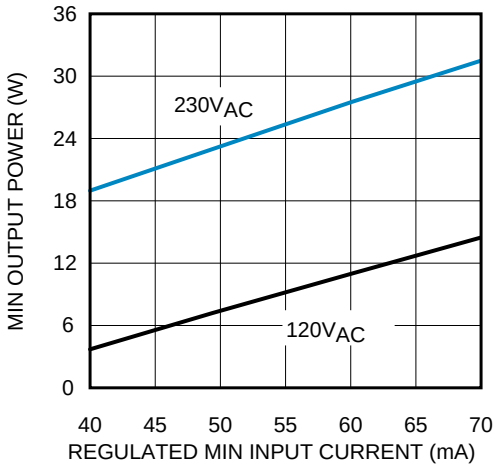


Figure 15. Output Power Restrictions (without thermal protection)

Thermal Protection

Using the previously mentioned design methodology, thermal protection is indeed necessary for the open load condition and for power levels below the specified operating range shown in Figure 15. The thermal protection circuit shown in Figure 14 will reduce the maximum holding current when the temperature rises too high, thus preventing catastrophic failure of Q1. Keep in mind that the thermal foldback does not prevent the circuit from operating, it simply reduces the amplitude of the dynamic hold. The only negative effect of the thermal protection is a possible reduction in contrast ratio, meaning the minimum attainable output current potentially increases as the dynamic hold level decreases.

The thermal protection is accomplished using a PNP transistor (Q11) and a resistor divider comprised of a fixed resistor (R45) and an NTC thermistor (R44). As Q1 heats up, R44 decreases causing the collector voltage of Q11 to decrease, effectively reducing the maximum attainable holding current. Placement of R44 is critical to ensure the best possible thermal coupling to Q1. The drain of Q1 will have the highest temperature rise but it is at a much higher voltage than the source where R44 is electrically connected. Because of this, the best placement for R44 is on the other side of the PCB, directly under the drain of Q1. The dielectric of the PCB provides adequate electrical insulation while yielding the best thermal coupling. Obviously, R44 placement in potted solutions is much more forgiving. A 10kΩ NTC is suggested for R44 and Q11 can be a basic PNP (i.e. MMBT3906). R45 has to be sized experimentally since the thermal coupling will vary with each PCB layout. A good starting point for R45 is 15kΩ.

Definitions

$I_{IN\text{-}MIN\text{-}REG}$ – Regulated Minimum Input Current

$I_{HOLD\text{-}MAX}$ – Maximum Hold Current

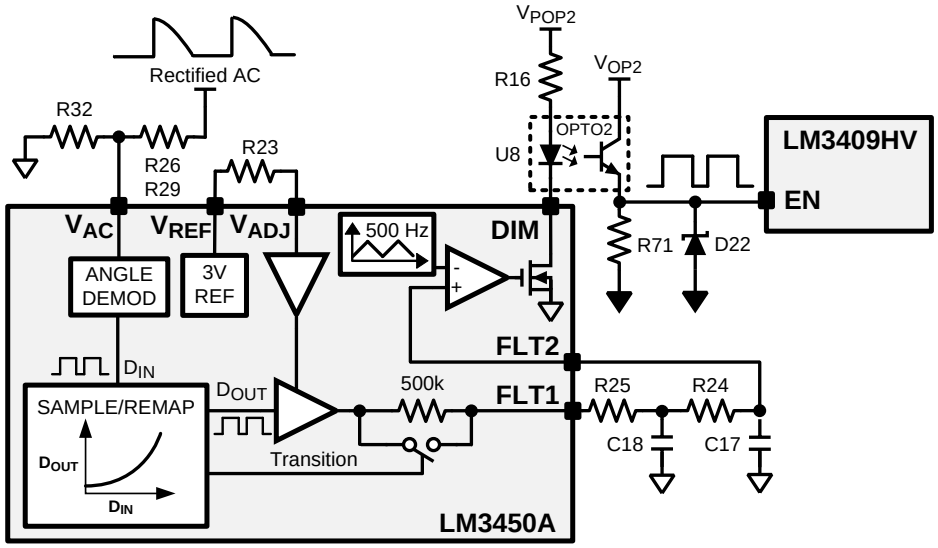


Figure 16. Dimming Decoder Circuit

9.7 Dimming Decoder

Angle Sense

V_{AC} is a dual input for both the PFC multiplier and the angle decoder. The resistor divider (R26+R29, R32) should be sized according to the desired angle detect voltage V_{DET}. A general rule of thumb is to set $V_{DET} = V_{IN\text{-}PK}/x$ where x is a value between 4 and 7. R26+R29 should be chosen to be between 1MΩ and 2MΩ to limit power dissipation.

$$R32 = \frac{356\ mV \times (R26 + R29)}{V_{DET} - 356\ mV} \quad (23)$$

Decoder Mapping

The mapping from the demodulated input (VAC pin of the LM3450A) to output (EN pin of the LM3409HV) is shown in Figure 17. Varying V_{ADJ} will adjust the mapping as desired for the target dimmers. Keep in mind that the demodulated input angle is a function of the resistor divider at the V_{AC} pin. This means that the input duty cycle can be shifted by changing V_{DET} within the previously suggested range.

Filters

The filters (FLT1, FLT2) are chosen to provide the desired dimming transition response (how the light changes during dimmer movement). The filter frequency should be set between 2Hz and 10Hz for best operation (2Hz has a fade feeling, 10Hz is very snappy). The capacitors (C17, C18) can both be set to 1µF for all designs and given the filter frequencies, the resistors (R24, R25) are calculated:

$$R24 = \frac{1}{2 \times \pi \times f_{FLT2} \times C17}$$
$$R25 = \frac{1}{2 \times \pi \times f_{FLT1} \times C18} \quad (24)$$

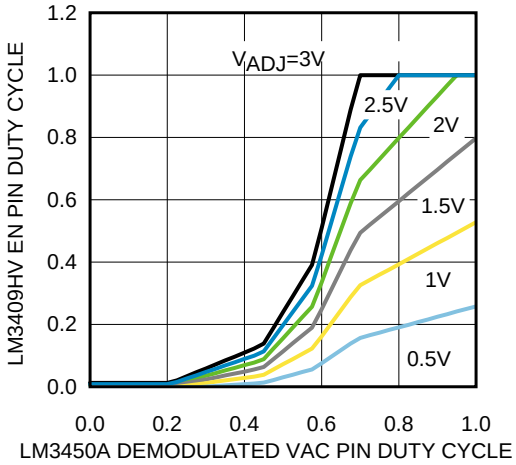


Figure 17. Dimming Decoder Mapping

Opto-Isolator

A standard low cost opto-isolator (same type used for feedback of the output) is used to transfer the dimming command from DIM to the secondary. It needs to be driven with at least 1-2mA of current to obtain full 70:1 contrast ratio (more current creates faster edges). With V_{POP2} = 9V and R16 = 6.04kΩ, there is > 1mA of drive current. The output of the opto-isolator should be clamped to just above the dimming input threshold of the secondary driver. This is accomplished with a 1.8V Zener clamp (D22) at the EN pin of the LM3409HV on the evaluation boards. R71 needs to be large enough that the Zener clamp is activated whenever the LM3409HV EN pin should be high.

Definitions

V_{DET} – Rectified AC Angle Detect Voltage

f_{FLT1} – FLT1 frequency

f_{FLT2} – FLT2 frequency

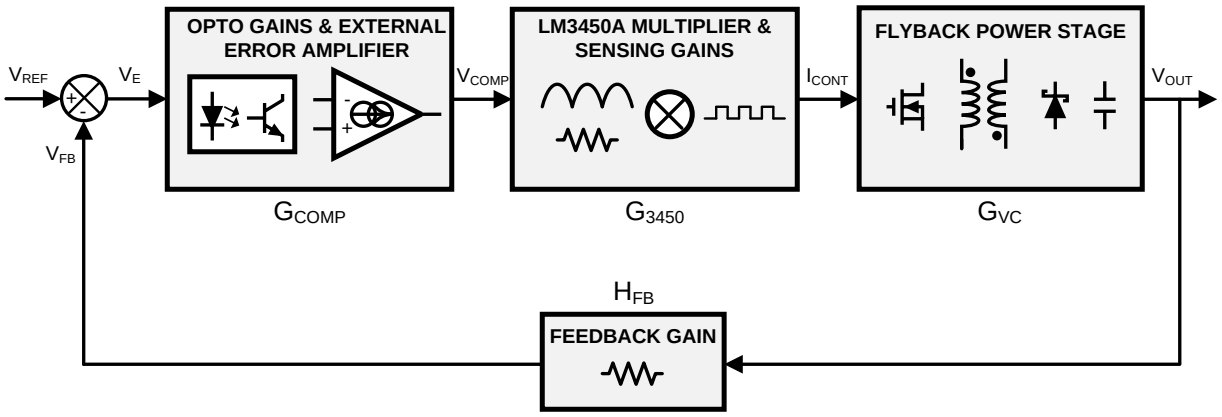


Figure 18. Control Loop Block Diagram

9.8 Voltage Control Loop

The CRM topology requires a narrow bandwidth voltage control loop to regulate the output voltage. This loop needs to be compensated to maintain stability over the desired operating range. The flyback topology is isolated, therefore the LM3450A internal error amplifier is bypassed and an external secondary side error amplifier is used instead. The control loop shown in Figure 18 is comprised of the converter control-to-output transfer function, the compensator transfer function, and all of the other gains in the loop.

The output voltage is sensed with a resistor divider (R81, R72) and regulated to 1.24V using an LMV431:

$$R81 = \frac{1.24V \times R72}{V_{OUT} - 1.24V} \tag{25}$$

The converter control-to-output transfer function can be approximated as a single pole system:

$$G_{VC}(s) = G_{C0} \times \frac{1}{\left(1 + \frac{s}{\omega_{P1}}\right)}$$

$$\omega_{P1} = \frac{P_{OUT\text{-}MAX}}{V_{OUT}^2 \times C11}$$

$$G_{C0} = \frac{V_{OUT}}{I_{P\text{-}PK}} \tag{26}$$

The feedback gain (H_{FB}) is unity due to the control implementation and the LM3450A device and external gains are defined:

$$G_{3450} = \frac{5k\Omega \times CTR \times K_V \times 0.55\frac{1}{V} \times V_{IN\text{-}PK}}{(R30 \,||\, R31) \times R70}$$

$$K_V = \frac{R32}{R32 + (R26 + R29)} \tag{27}$$

A standard PI compensator is used on the secondary to stabilize the system. The error amplifier is implemented with an LMV431 and a series resistor (R77) and capacitor (C35) in the feedback path as shown in Figure 19. The output of the LMV431 is tied to the cathode of the opto photo-diode. A resistor (R70 = 2kΩ) from the anode of the photodiode to the bias rail provides the current path and ultimately the output voltage swing of the secondary error amplifier. The primary side of the opto is connected directly to COMP. With the 5kΩ internal pull-up resistor, the maximum current through the primary side of the opto will be 1mA. A higher frequency roll-off pole is placed on the primary in the form of a capacitor (C24) from COMP to GND. The resistor divided flyback output voltage is regulated to the 1.24V LMV431 internal reference. Note the additional soft-start circuit using C34, D13, and D14.

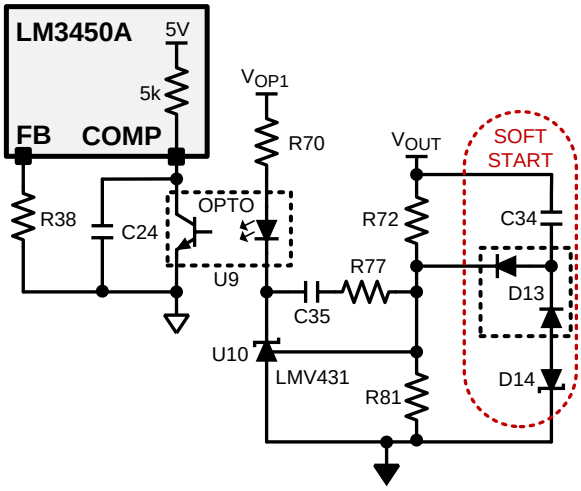


Figure 19. Secondary Error Amplifier Circuit

The compensator transfer function is defined:

$$G_{COMP}(s) = \frac{\left(1 + \frac{s}{\omega_{Z1}}\right)}{\left(\frac{s}{\omega_{P2}}\right) x \left(1 + \frac{s}{\omega_{P3}}\right)} \quad (28)$$

Where the secondary compensator pole is defined:

$$\omega_{P2} = \frac{1}{R72 \, x \, C35} \quad (29)$$

And the compensator zero is defined:

$$\omega_{Z1} = \frac{1}{R77 \, x \, C35} \quad (30)$$

And the primary roll-off pole is defined:

$$\omega_{P3} = \frac{1}{5 \, k\Omega \, x \, C24} \quad (31)$$

The resulting control loop gain is

$$T(s) = G_{COMP}(s) \, x \, G_{3450} \, x \, G_{VC}(s) \, x \, H_{FB} \quad (32)$$

The compensator design for this system can be complicated; however with some useful assumptions, it can be simplified. Looking at the total DC gain ($G_{3450}xG_{C0}xH_{FB}$), the following can be made relatively constant over all designs:

- R70 = 2kΩ, the 5kΩ internal pull-up, and the 0.55 multiplier gain.
- The opto CTR, though variable over temperature, given a fixed supply rail and a fixed R70 value.

In several cases, the product of two DC gain terms can also be identified as relatively constant over all designs if all of the previous LM3450A design methodology is observed:

- V_{INPK} and K_V are almost exactly inversely proportional (given x remains constant when solving $V_{DET} = V_{IN}/x$).
- I_{P-PK} and R30||R31 are closely inversely proportional (given current limit is a constant percentage above I_{P-PK}).

Given these relationships and following the complete LM3450A design method, the DC gain should only vary largely with change in output voltage (directly proportional).

The output pole of the converter on the other hand follows these basic relationships:

- $P_{OUT-MAX}$ and C11 are exactly directly proportional given a constant output ripple specification, therefore there is no relative change to ω_{P1}.
- V_{OUT} is exactly inversely proportional to ω_{P1} given a constant output ripple specification.

With the opposing conditions of the output pole moving inversely proportional to V_{OUT} and the DC gain moving proportional to V_{OUT}, the net result gives a very consistent uncompensated loop gain. Because of this, the exact compensator on this evaluation board can be a starting point for any LM3450A design.

During prototyping, If stability becomes a concern, the R77 value can be changed to improve stability. In general the compensator calculated in the Design Calculations section is sized to be stable and have a bandwidth of around 50-60Hz. This is a fairly high bandwidth for a PFC converter which will cause there to be some 120Hz ripple on COMP. This will decrease PF but improve transient response which is very helpful in phase dimmable applications.

Since it is usually desirable to maximize bandwidth (within the PFC limitation), there is a simple method to adjust the R77 value. Measure the twice-line frequency ripple on COMP. If the ripple is less than 200-300mV, increase R77 until it is within that range. If the ripple is larger, then decrease R77 until it is within that range. This will result in a very small PFC degradation, while maximizing bandwidth of the control loop.

9.9 STARTUP

When using the LM3450A with a phase dimmer, startup can be very disruptive. Any time the dimmer is turned on (via a separate switch or some state where the dimmer has been previously disconnected from its load), the LM3450A will attempt to bring the system to regulation. Because phase dimmers can be turned on and off quickly, the system capacitances may or may not be fully discharged, this can lead to a large variance in startup conditions. The best way to control startup transients is to softstart the dimming command and the PFC control simultaneously. This can be accomplished with the circuit shown in Figure 20. D20 is a dual common cathode schottky with very low forward voltage to allow COMP and VADJ to be pulled as close to zero as possible. The softstart time constant is set by C12 and R20. Q4, R21, and D21 form a reset circuit for C12. Since BIAS transitions to 20V whenever VCC hits the falling UVLO threshold and D21 is an 18V Zener, the base of Q4 will go high turning on Q4 and immediately resetting the capacitor to 0V. Then when VCC reaches the UVLO rising threshold and BIAS transitions to 14V, Q4 turns off and softstart is active again.

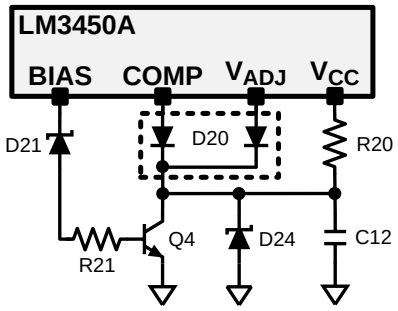


Figure 20. Primary Soft-start Circuit

Relevant Definitions

$G_{VC}(s)$ – Converter Control-to-Output Transfer Function

G_{C0} – Converter Control-to-Output DC Gain

G_{3450} – LM3450A and External Gains

$G_{COMP}(s)$ – Compensator Transfer Function

H_{FB} – Feedback Gain

ω_{P1} – Converter Output Pole

ω_{P2} – Compensator Secondary Integrator Pole

ω_{Z1} – Compensator Secondary Zero

ω_{P3} – Compensator Primary HF Pole

T(s) – Total Loop Gain

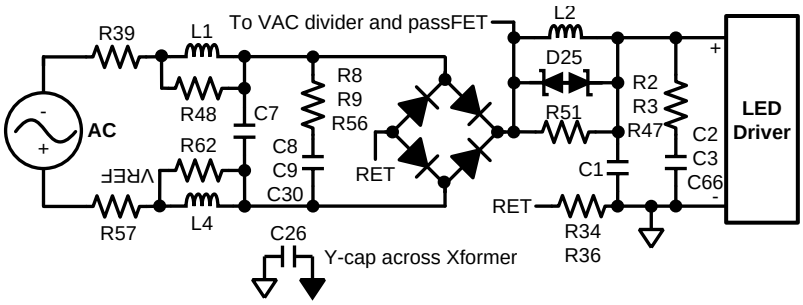


Figure 21. Input EMI Filter

9.10 Input Filter

Background

Since the LM3450A is used for AC to DC systems, electromagnetic interference (EMI) filtering is critical to pass the necessary standards for both conducted and radiated EMI. This filter will vary depending on the output power, the switching frequencies, and the layout of the PCB. There are two major components to EMI: differential noise and common-mode noise. Differential noise is typically represented in the EMI spectrum below approximately 500kHz while common-mode noise shows up at higher frequencies.

Conducted

Figure 21 shows a typical filter used with an LM3450A design. To conform to conducted standards, a fourth order filter (two second order stages) is implemented using shielded inductors (L1, L2, L4), an EMI suppression X1/X2 film capacitor (C7), and a pulse-rated film capacitor (C1) which is also the primary PFC capacitor sized previously. In addition to the basic filter components, damping is used to prevent excitation of the resonant frequencies of the filter itself. The best practice for damping an EMI filter is to use an RC damper network across each filter capacitor. The C of the damper should be set to be 3 times the filter capacitor value. This EMI filter, if sized properly, can provide ample attenuation of the switching frequency and lower order harmonics contributing to differential noise. The filter can be described as follows:

- Stage 1 pole: L1+L4 and C7 gives 40db/decade roll-off
  - Stage 1 damping: C8||C9||C30 and R8||R9||R56
- Stage 2 pole: L2 and C1 gives 40db/decade roll-off
  - Stage 2 damping: C2||C3||C66 and R2||R3||R47

Since L1 and L4 are symmetrically placed in both the line and neutral legs of the AC line, they help to reduce common-mode noise also. It is sometimes necessary to place a high value resistance (R48, R51, R62) across each inductor to prevent excitation of the SRF of the inductor which is usually at higher frequencies. A Y1/Y2 film capacitor (C26) from the primary ground to the secondary ground is also commonly used for reduction of common mode noise.

Radiated

Conforming to radiated EMI standards is much more difficult and is dependent on the entire system including the enclosure. C26 will greatly help reduce radiated EMI; however, reduction of dV/dt on switching edges and PCB layout iterations are frequently necessary as well. Consult available literature and/or an EMI specialist for help with this. It can be a daunting task.

Interaction with Dimmers

In general, input filters and forward phase dimmers do not work well together. The triac needs a minimum amount of holding current to function. The converter itself is demanding a certain amount of current from the input to provide to its output. With no filter, the difference of the necessary hold current and the converter current is provided by the LM3450A dynamic hold circuit. Unfortunately, the actual dimmer current is not being monitored; instead a filtered version is being measured. In reality, the input filter is providing or taking current depending upon the dV/dt of the capacitors. The discrepancy between the measured input current at ISEN and the actual input current through the triac is the worst at the highest dV/dt of the input filter capacitors. The best way to deal with this problem is to minimize filter capacitance and increase the regulated hold current until there is enough current to satisfy the dimmer and filter simultaneously.

Figure 21 shows one effective way to improve the dynamic hold functionality when using an EMI filter. The hold current path through the passFET is derived between the two filter stages. In this configuration, the measured input current has only one stage of filtering capacitance to contribute to the descrepancy between measured and actual input current. In addition, the damping network for the C7 capacitor is directly connected to the dynamic hold point of the rectified AC (passFET drain). This, combined with the filter stage between the passFET and the transformer, help attenuate any unwanted switching frequency coupling into the dynamic hold circuit.

This configuration also provides some extra filtering of the feedforward VAC signal, which is now derived at the same point as the dynamic hold. One important addition to this EMI filter is a back-to-back TVS clamp across L2. During transient conditions, if the L2 filter rings too much, the current will try to change directions. There is no continuous path for current at the passFET drain, therefore the voltage can rise uncontrolled and damage the passFET. A 20V back-to-back TVS is sufficient to provide this protection.

9.11 Inrush Limiting, Damping and Clamping

Clamp

In any flyback converter there exists large ringing (V_{RING}) on the Q3 drain, as shown in Figure 22. This is due to the rising edge of the Q3 drain after turn-off, which excites the resonance created by the leakage inductance of the transformer and output capacitance of Q3. A clamp circuit is necessary to prevent damage to Q3 from excessive voltage. The evaluation boards use a transil (TVS) clamp, shown in Figure 23

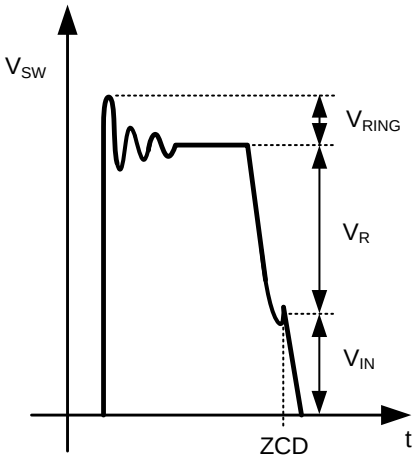


Figure 22. Switch Node Ringing

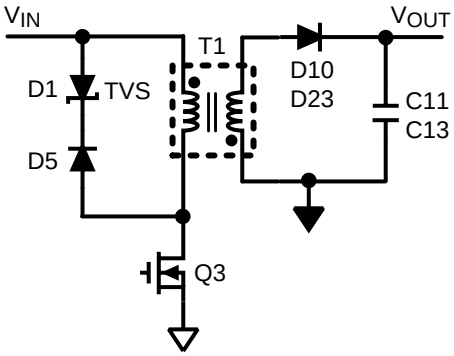


Figure 23. Transil Clamp

When Q3 is on and the drain voltage is low, the blocking diode (D5) is reverse biased and the clamp is inactive. When the MosFET is turned off, the drain voltage rises past the nominal voltage (reflected voltage plus the input voltage). If it reaches the TVS clamp voltage + the input voltage, the clamp prevents any further rise. The TVS diode (D1) voltage is set to prevent the MosFET from exceeding its maximum rating:

$$V_{TVS\text{-}D1} \leq \frac{3}{2} \times V_R \quad (33)$$

This clamp method is fairly efficient and very simple compared to other commonly used methods. Note that if the ringing is large enough that the clamp activates, the ringing energy is radiated at higher frequencies. Depending on PCB layout, EMI filtering method, and other application specific items, the transil clamp can present problems conforming to radiated EMI standards.

If the transil clamp becomes problematic at higher frequencies, an RCD clamp can be used to dampen the ringing. Looking at the *EMI Performance* section, it is obvious that the evaluation board fails near 30MHz. This would indicate an RCD clamp is indeed necessary for this design. C29 and R49, shown on the *Complete Evaluation Board Schematic* can be populated as desired to improve the EMI signature. This will degrade efficiency some.

Inrush

With a forward phase dimmer, a very steep rising edge causes a large inrush current every cycle as shown in Figure 24. Series resistance (R39, R57) can be placed between the filter and the triac to limit the effect of this current on the converter. This will, of course, degrade efficiency but some inrush protection is also necessary in any AC system due to startup. The size of R39 and R57 are best found experimentally as they provide attenuation for the whole system.

The inrush spike excites resonance(s) of the input filter, which can cause the current to ring negative, as shown in Figure 24, thereby shutting off the triac. The RC damper of the first stage of the input filter should be increased to dampen the worst-case ringing energy due to this edge. This can require a significant increase in capacitance depending upon the dimmer tested (more than 10x the filter capacitance). The resistance is then experimentally changed to create a ringing waveform that is most contained. The objective is to prevent the input current ringing from crossing the minimum regulated holding current thereby preventing misfires.

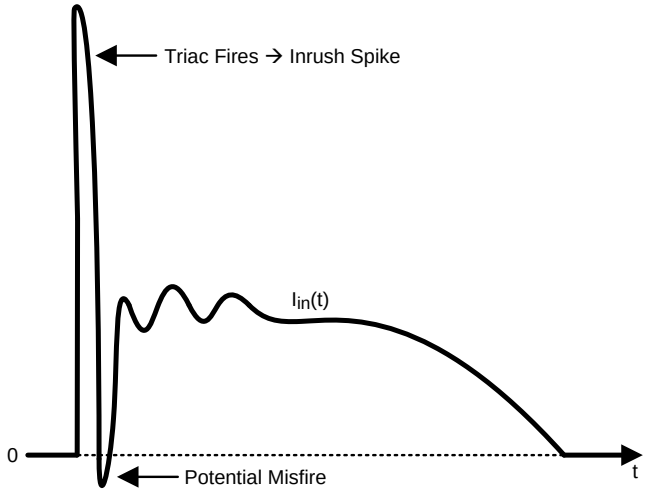


Figure 24. Inrush Current Spike

10 Design Calculations - 120V, 30W

The following is a step-by-step procedure with calculations for the 120V 30W Evaluation Board. The 230V calculations can be done in the same manner. Many components are identical between both boards for simplicity, therefore some components on the 120V board are over-sized.

10.1 Specifications

f_L – 60Hz

f_{SW-MIN}– 45kHz

V_{IN} – 120V_{AC}

V_{IN-MIN} – 90V_{AC}

V_{IN-MAX} – 135V_{AC}

I_{LED} – 700mA

Δv_{OUT} = 2V

Δv_{IN-PK} = 60V

$I_{P-PK-LIM}$ = 3A

$V_{T-DES-MAX}$ = 400V

$P_{OUT-MAX}$ = 30W

$D_{@IIN-MAX-PK}$ = 0.5

V_{OUT} = 50V

η=0.9

10.2 Preliminary Calculations

Maximum peak input voltage:

$$V_{IN-PK-MAX}=135V\times\sqrt{2}=191V \quad (34)$$

Minimum peak input voltage:

$$V_{IN-PK-MIN}=90V\times\sqrt{2}=127V \quad (35)$$

Maximum average input current:

$$I_{IN-MAX}=\frac{30W}{0.9\times0.85\times90V}=436mA \quad (36)$$

Maximum peak input current:

$$I_{IN-PK-MAX}=436mA\times\sqrt{2}=617mA \quad (37)$$

Maximum peak primary current:

$$I_{P-PK-MAX}=\frac{2\times617mA}{0.5}=2.47A \quad (38)$$

10.3 Main Switching MOSFET

Maximum drain-to-source voltage:

$$V_{T-MAX}=191V+(1.5\times100V)=341V \quad (39)$$

Maximum peak MosFET current:

$$I_{T-PK-MAX}=2.47A \quad (40)$$

Maximum RMS MosFET current:

$$I_{T-RMS-MAX}=2.47A\times\sqrt{\frac{0.5}{3}}=1A \quad (41)$$

Maximum power dissipation:

$$P_{T-MAX}=1A^2\times1\Omega=1W \quad (42)$$

Resulting component choice:

$$V_{RD\text{-}MAX}=50V+\left(\frac{191V}{2}\right)=145V \quad (43)$$

10.4 Re-Circulating DIODE

Maximum reverse blocking voltage:

$$V_{RD\text{-}MAX}=50V+\left(\frac{191V}{2}\right)=145V \quad (44)$$

Maximum peak diode current:

$$I_{D\text{-}PK\text{-}MAX}=2.47A\times 2=4.94A \quad (45)$$

Maximum average diode current:

$$I_{D\text{-}MAX}=617mA\times 2=1.23A \quad (46)$$

Maximum power dissipation:

$$P_{D\text{-}MAX}=1.23A\times 1V=1.23W \quad (47)$$

Resulting component choice:

$$\boxed{D10\rightarrow 200V,2A,SMB\ x\ 2} \quad (48)$$

10.5 Current Sense

Sense resistor:

$$R30||R31=\frac{1.5V}{3A}=0.5\,\Omega \quad (49)$$

Power dissipation:

$$P_{R30||R31}=1A^2\times 0.5\,\Omega=500mW \quad (50)$$

Resulting component choice:

$$\boxed{R30||R31\rightarrow 1\Omega, 0.25W\ ||\ 1\Omega, 0.25W} \quad (51)$$

10.6 Input Capacitance

Minimum capacitance:

$$C1=\frac{430\,\mu H\times 2.47A^2}{\left(127V+\frac{60V}{2}\right)^2-\left(127V-\frac{60V}{2}\right)^2}=172nF \quad (52)$$

Voltage rating:

$$V_{C1}=191V\times 2=382V \quad (53)$$

Resulting component choice:

$$\boxed{C1\rightarrow 220\,nF,\ 400V} \quad (54)$$

10.7 Output Capacitance

Minimum capacitance:

$$C11=\frac{30W}{2\times\pi\times 60Hz\times 50V\times 2V}=796nF \quad (55)$$

Voltage rating:

$$V_{C11}=50V\times 1.25=62.5V \quad (56)$$

Resulting component choice:

$$\boxed{C11 \rightarrow 1\,mF, 63V} \tag{57}$$

10.8 Transformer

Maximum acceptable reflected voltage:

$$V_{R\text{-}MAX} = \frac{2}{3} \times (400V - 191V) = 140V \tag{58}$$

Primary to secondary turns ratio:

$$n < \frac{140V}{50V} = 2.8, \text{ choose } 2 \tag{59}$$

Actual reflected voltage:

$$V_R = 2 \times 50V = 100V \tag{60}$$

Primary to auxiliary turns ratio:

$$n_A < \frac{50V}{12.5V} = 4 \tag{61}$$

Transformer primary inductance:

$$L_{P\text{-}MIN} = \frac{0.5^2 \times 90V}{2 \times 45kHz \times 617mA} = 405\,\mu H$$
$$L_P = 430\,\mu H \tag{62}$$

Number of primary turns:

$$N_P = \sqrt{\frac{430\,\mu H}{160\frac{nH}{turns^2}}} = 52 \text{ turns} \tag{63}$$

Number of secondary turns:

$$N_S = \frac{52 \text{ turns}}{2} = 26 \text{ turns} \tag{64}$$

Number of auxiliary turns:

$$N_A = \frac{26 \text{ turns}}{4} = 6.5 \text{ turns, choose } 7 \tag{65}$$

Maximum flux density:

$$B_{MAX} = \frac{430\,\mu H \times 2.47A}{52 \times 52mm^2} = 392mT \tag{66}$$

Resulting component choice:

$$\boxed{\begin{array}{l} N_P \rightarrow 52 \text{ turns} \\ N_S \rightarrow 26 \text{ turns} \\ N_A \rightarrow 7 \text{ turns} \end{array}} \tag{67}$$

10.9 Transil Clamp

TVS clamp voltage:

$$V_{TVS\text{-}D1} = \frac{3}{2} \times 100V = 150V \tag{68}$$

Resulting component choice:

$$\boxed{D1 \rightarrow 150V \text{ TVS}} \tag{69}$$

10.10 Dynamic Hold

ISEN sense resistance:

$$R34||R36=\frac{200mV}{70mA}=2.86\,\Omega \tag{70}$$

HOLD resistance:

$$R12||R14||R15=\frac{12V-30\,\Omega\times 90mA}{90mA}=103\,\Omega \tag{71}$$

Resulting component choice:

$$\boxed{\begin{array}{l} R12||R14||R15=300\Omega||300\Omega||300\Omega \\ R34||R36=5.62\Omega||5.62\Omega \end{array}} \tag{72}$$

10.11 Decoder Input

Resistor divider:

$$R32=\frac{356mV\times 1M\,\Omega}{35V-356mV}=10.3k\,\Omega \tag{73}$$

Resulting component choice:

$$\boxed{\begin{array}{l} R26+R29\rightarrow 1M\Omega \\ R32\rightarrow 10\,k\Omega \end{array}} \tag{74}$$

10.12 Output Voltage Sense

Resistance:

$$R81=\frac{1.24V\times 105k\,\Omega}{50V-1.24V}=2.67k\,\Omega \tag{75}$$

Resulting component choice:

$$\boxed{\begin{array}{l} R81\rightarrow 2.67\,k\Omega \\ R72\rightarrow 105\,k\Omega \end{array}} \tag{76}$$

10.13 Loop Compensation

Converter output pole:

$$\omega_{P1}=\frac{30W}{50V^2\times 1mF}=12\frac{rad}{sec} \tag{77}$$

Converter DC gain:

$$G_{C0}=\frac{50V}{2.47A}=20.2\,\Omega \tag{78}$$

LM3450A and external sensing DC gain:

$$G_{3450}=\frac{5k\,\Omega\times 1\times 0.01\times 0.55\frac{1}{V}\times 191V}{0.5\,\Omega\times 2k\,\Omega}=5.25S \tag{79}$$

Secondary compensator dominant pole:

$$\omega_{P2}=\frac{1}{105k\,\Omega\times 10\,\mu F}=0.952\frac{rad}{sec} \tag{80}$$

Secondary compensator zero:

$$\omega_{Z2}=\frac{1}{30.1k\,\Omega\times 10\,\mu F}=3.32\frac{rad}{sec} \tag{81}$$

Primary roll-off pole:

$$\omega_{P3} = \frac{1}{5k\Omega \times 1\mu F} = 200\frac{rad}{sec} \quad (82)$$

Resulting component choice:

$$\boxed{\begin{array}{l} C35 \rightarrow 10\,\mu F \\ C24 \rightarrow 1\,\mu F \\ R77 \rightarrow 30.1\,k\Omega \end{array}} \quad (83)$$

11 Complete Evaluation Board Schematic

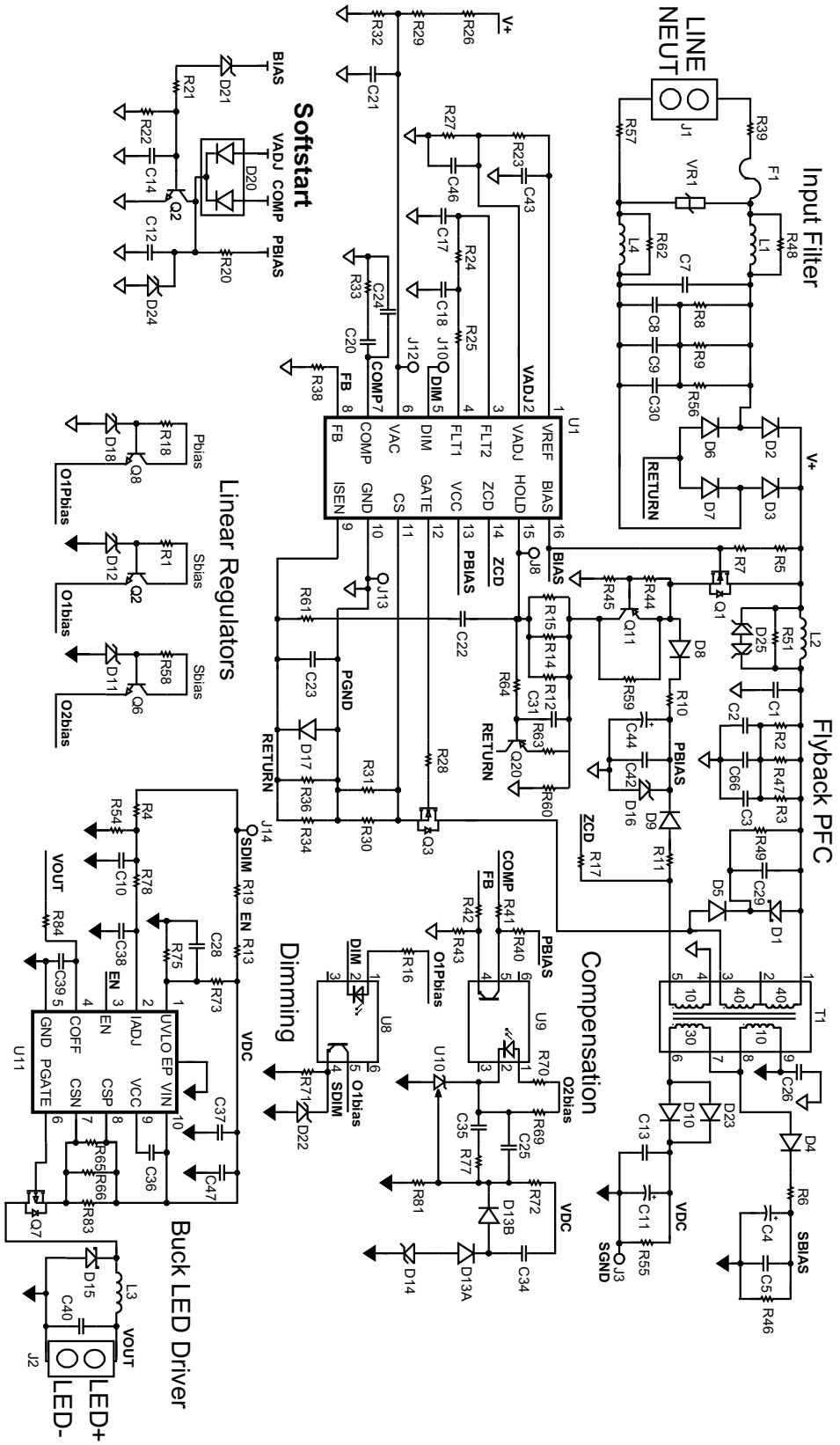


Figure 25. Complete Evaluation Board Schematic

12 120V Bill of Materials

Table 1. 120V Bill of Materials

Reference Designator	Part Value	Manufacturer	Part Number
C1	CAP MPY 0.22µF 400V RAD	WIMA	MKP10-.22/400/20
C2, C3, C8, C9, C30, C66	CAP CER 0.22µF 250V RAD	TDK	FK20X7R2E224K
C4, C44	CAP ELEC 220µF 35V RAD	NICHICON	UHE1V221MPD
C5, C23, C42, C46	CAP CER 0.10µF 25V 0603	MURATA	GRM188R71E104KA01D
C7	CAP MPY 33nF 330VAC X1 RAD	EPCOS	B32912A3333M
C11	CAP ELEC 1000µF 63V RAD	NICHICON	UPW1J102MHD6
C12	CAP CER 47µF 6.3V 1206	MURATA	GRM31CR60J476ME19L
C13, C34, C47	CAP CER 1µF 100V 1206	TDK	C3216X7R2A105M
C17, C18, C24, C36	CAP CER 1µF 16V 0603	MURATA	GRM188R71C105KA12D
C21, C43	CAP CER 10nF 25V 0603	MURATA	GRM188R71E103KA01D
C22	CAP CER 0.22µF 16V 0603	TDK	C1608X7R1C224K
C26	CAP CER 4.7nF 500VAC Y1 RAD	EPCOS	VY1472M63Y5UQ63V0
C35	CAP CER 10µF 16V 1206	MURATA	GRM31CR71C106KAC7L
C37	CAP CER 0.10µF 50V 0603	MURATA	GRM188R71H104KA93D
C38	CAP CER 2.2µF 6.3V 0603	TDK	C1608X5R0J225M
C39	CAP CER 470pF 100V 0603	TDK	C1608C0G2A471J
D1	DIODE TVS 150V 600W UNI SMB	LITTLEFUSE	SMBJ150A
D2, D3, D6, D7	DIODE GEN PURPOSE 1000V 1A SMA	COMCHIP	CGRA4007-G
D4, D9	DIODE ULTRAFAST 100V 0.2A SOT-23	FAIRCHILD	MMBD914
D5	DIODE ULTRAFAST 600V 1A SMA	FAIRCHILD	ES1J
D8, D10, D23	DIODE ULTRAFAST 200V 1A SMA	FAIRCHILD	ES1D
D11, D12, D18	DIODE ZENER 10V 500mW SOD-123	FAIRCHILD	MMSZ5240B
D13	DIODE ULTRAFAST 70V 0.2A SOT-23	FAIRCHILD	BAV99
D14	DIODE ZENER 3.3V 500mW SOD-123	ON-SEMI	MMSZ3V3T1G
D15	DIODE SCHOTTKY 60V 2A SMB	ON-SEMI	SS26T3G
D16	DIODE ZENER 24V 1.5W SMA	MICRO-SEMI	SMAJ5934B-TP
D17	DIODE SCHOTTKY 50V 3A SMA	FAIRCHILD	ES2AA-13-F
D20	DIODE SCHOTTKY (DUAL) 30V 0.5A SOT-23	DIODES INC	PMEG3005CT,215
D21	DIODE ZENER 18V 500MW SOD-123	FAIRCHILD	MMSZ5248B
D22	DIODE ZENER 1.8V 500MW SOD-123	ON-SEMI	MMSZ4678T1G
D24	DIODE ZENER 3.9V 500MW SOD-123	ON-SEMI	MMSZ4686T1G
D25	DIODE TVS 20V 400W BIDIR SMA	LITTLEFUSE	SMAJ20CA
F1	FUSE 500mA T-LAG RST	BEL FUSE	RST 500
J1, J2	CONN HEADER 2x1 VERT	AMP	1-1318301-2
L1, L2, L4	IND SHIELD 1mH 1.14A SMT	COILCRAFT	MSS1278-105KL
L3	IND SHIELD 270µH 2.18A SMT	COILCRAFT	MSS1278-274KL
Q1	MOSFET N-CH 800V 3A DPAK	ST MICRO	STD4NK80ZT4
Q2, Q6, Q8	TRANS NPN 40V 0.6A SOT-23	FAIRCHILD	MMBT4401
Q3	MOSFET N-CH 500V 9A DPAK	ST MICRO	STD11NM50N
Q4	TRANS NPN 40V 0.2A SOT-23	FAIRCHILD	MMBT3904
Q7	MOSFET P-CH 70V 5.7A DPAK	ZETEX	ZXMP7A17K
Q11	TRANS PNP 40V 0.2A SOT-23	FAIRCHILD	MMBT3906
R1, R18, R32, R58	RES 10kΩ 1% 0.1W 0603	VISHAY	CRCW060310K0FKEA
R2, R3, R8, R9, R47, R56	RES 820Ω 5% 1W 2512	VISHAY	CRCW2512820RJNEG
R5, R7	RES 200kΩ 1% 0.25W 1206	VISHAY	CRCW1206200KFKEA
R6, R11	RES 10Ω 1% 0.25W 1206	VISHAY	CRCW120610R0FKEA

Table 1. 120V Bill of Materials (continued)

R10	RES 40.2Ω 1% 0.25W 1206	VISHAY	CRCW120640R2FKEA
R12, R14, R15	RES 301Ω 1% 0.25W 1206	VISHAY	CRCW1206301RFKEA
R16	RES 6.04kΩ 1% 0.125W 0805	VISHAY	CRCW08056K04FKEA
R17	RES 100kΩ 1% 0.1W 0603	VISHAY	CRCW0603100KFKEA
R19, R41, R43, R61, R73	RES 0Ω 5% 0.1W 0603	VISHAY	CRCW06030000Z0EA
R20	RES 499kΩ 1% 0.1W 0603	VISHAY	CRCW0603499KFKEA
R21, R69	RES 20.0kΩ 1% 0.1W 0603	VISHAY	CRCW060320K0FKEA
R23	RES 6.04kΩ 1% 0.1W 0603	VISHAY	CRCW06036K04FKEA
R24, R25	RES 75.0kΩ 1% 0.1W 0603	VISHAY	CRCW060375K0FKEA
R26, R29	RES 499kΩ 1% 0.25W 1206	VISHAY	CRCW1206499KFKEA
R28	RES 10Ω 1% 0.125W 0805	VISHAY	CRCW080510R0FKEA
R30, R31, R65, R66, R83	RES 1.00Ω 1% 0.25W 1206	VISHAY	CRCW12061R00FKEA
R34, R36	RES 5.62Ω 1% 0.25W 1206	VISHAY	CRCW12065R62FKEA
R38	RES 5.11kΩ 1% 0.1W 0603	VISHAY	CRCW06035K11FKEA
R39, R57	RES 5Ω 1% 3W WIREWOUND	VISHAY	PAC300005008FAC000
R44	THERM 10kΩ NTC 0603	MURATA	NTCG163JF103F
R45	RES 15.0kΩ 1% 0.1W 0603	VISHAY	CRCW060315K0FKEA
R46	RES 5.11kΩ 1% 0.125W 0805	VISHAY	CRCW08055K11FKEA
R48, R51, R62	RES 20.0kΩ 1% 0.25W 1206	VISHAY	CRCW120620K0FKEA
R55	RES 51.1kΩ 1% 0.25W 1206	VISHAY	CRCW120651K1FKEA
R70	RES 2.00kΩ 1% 0.125W 0805	VISHAY	CRCW08052K00FKEA
R71	RES 10.0kΩ 1% 0.125W 0805	VISHAY	CRCW080510K0FKEA
R72	RES 105kΩ 1% 0.125W 0805	VISHAY	CRCW0805105KFKEA
R77	RES 30.1kΩ 1% 0.1W 0603	VISHAY	CRCW060330K1FKEA
R81	RES 2.67kΩ 1% 0.1W 0603	VISHAY	CRCW06032K67FKEA
R84	RES 49.9kΩ 1% 0.1W 0603	VISHAY	CRCW060349K9FKEA
T1	XFORMER 120V 30W OUTPUT 50V	WURTH	750813651
U1	IC PFC CONT 16-TSSOP	TI	LM3450
U8, U9	OPTO-ISOLATOR SMD	LITE ON	CNY17F-3S
U10	IC SHUNT REG SOT-23	NSC	LMV431AIM5
U11	IC LED DRIVR 10-eMSOP	NSC	LM3409HVMY
C10, C14, C20, C25, C28, C29, C31, C40, Q20, R4, R13, R22, R27, R33, R40, R42, R49, R54, R59, R60, R63, R64, R75, R78, VR1	Did not populate		

13 230V Bill of Materials

Table 2. 230V Bill of Materials

Reference Designator	Part Value	Manufacturer	Part Number
C1	CAP MPY 0.062µF 1000V RAD	VISHAY	BFC238330623
C2, C3, C8, C9, C30, C66	CAP CER 0.1µF 630V RAD	TDK	FK22X7R2J104K
C4, C44	CAP ELEC 220µF 35V RAD	NICHICON	UHE1V221MPD
C5, C23, C42, C46	CAP CER 0.10µF 25V 0603	MURATA	GRM188R71E104KA01D
C7	CAP MPY 68nF 275VAC X1 RAD	PANASONIC	ECQU2A683ML
C11	CAP ELEC 1000µF 63V RAD	NICHICON	UPW1J102MHD6
C12	CAP CER 47µF 6.3V 1206	MURATA	GRM31CR60J476ME19L
C13, C34, C47	CAP CER 1µF 100V 1206	TDK	C3216X7R2A105M
C17, C18, C24, C36	CAP CER 1µF 16V 0603	MURATA	GRM188R71C105KA12D
C21, C43	CAP CER 10nF 25V 0603	MURATA	GRM188R71E103KA01D
C22	CAP CER 0.22µF 16V 0603	TDK	C1608X7R1C224K
C26	CAP CER 4.7nF 500VAC Y1 RAD	EPCOS	VY1472M63Y5UQ63V0
C35	CAP CER 10µF 16V 1206	MURATA	GRM31CR71C106KAC7L
C37	CAP CER 0.10µF 50V 0603	MURATA	GRM188R71H104KA93D
C38	CAP CER 2.2µF 6.3V 0603	TDK	C1608X5R0J225M
C39	CAP CER 470pF 100V 0603	TDK	C1608C0G2A471J
D1	DIODE TVS 220V 600W UNI SMB	LITTLEFUSE	SMBJ220A
D2, D3, D6, D7	DIODE GEN PURPOSE 1000V 1A SMA	COMCHIP	CGRA4007-G
D4, D9	DIODE ULTRAFAST 100V 0.2A SOT-23	FAIRCHILD	MMBD914
D5	DIODE ULTRAFAST 600V 1A SMA	FAIRCHILD	ES1J
D8	DIODE ULTRAFAST 200V 1A SMA	FAIRCHILD	ES1D
D10, D23	DIODE ULTRAFAST 400V 1A SMA	FAIRCHILD	ES1G
D11, D12, D18	DIODE ZENER 10V 500mW SOD-123	FAIRCHILD	MMSZ5240B
D13	DIODE ULTRAFAST 70V 0.2A SOT-23	FAIRCHILD	BAV99
D14	DIODE ZENER 3.3V 500mW SOD-123	ON-SEMI	MMSZ3V3T1G
D15	DIODE SCHOTTKY 60V 2A SMB	ON-SEMI	SS26T3G
D16	DIODE ZENER 24V 1.5W SMA	MICRO-SEMI	SMAJ5934B-TP
D17	DIODE SCHOTTKY 50V 3A SMA	FAIRCHILD	ES2AA-13-F
D20	DIODE SCHOTTKY (DUAL) 30V 0.5A SOT-23	DIODES INC	PMEG3005CT,215
D21	DIODE ZENER 18V 500MW SOD-123	FAIRCHILD	MMSZ5248B
D22	DIODE ZENER 1.8V 500MW SOD-123	ON-SEMI	MMSZ4678T1G
D24	DIODE ZENER 3.9V 500MW SOD-123	ON-SEMI	MMSZ4686T1G
D25	DIODE TVS 20V 400W BIDIR SMA	LITTLEFUSE	SMAJ20CA
F1	FUSE 500mA T-LAG RST	BEL FUSE	RST 500
J1, J2	CONN HEADER 2x1 VERT	AMP	1-1318301-2
L1, L2, L4	IND SHIELD 1mH 1.14A SMT	COILCRAFT	MSS1278-105KL
L3	IND SHIELD 270µH 2.18A SMT	COILCRAFT	MSS1278-274KL
Q1	MOSFET N-CH 800V 3A DPAK	ST MICRO	STD4NK80ZT4
Q2, Q6, Q8	TRANS NPN 40V 0.6A SOT-23	FAIRCHILD	MMBT4401
Q3	MOSFET N-CH 800V 6A DPAK	INFINEON	SPD06N80C3
Q4	TRANS NPN 40V 0.2A SOT-23	FAIRCHILD	MMBT3904
Q7	MOSFET P-CH 70V 5.7A DPAK	ZETEX	ZXMP7A17K
Q11	TRANS PNP 40V 0.2A SOT-23	FAIRCHILD	MMBT3906
R1, R18, R58	RES 10kΩ 1% 0.1W 0603	VISHAY	CRCW060310K0FKEA
R2, R3, R47	RES 820Ω 5% 1W 2512	VISHAY	CRCW2512820RJNEG
R5, R7	RES 475kΩ 1% 0.25W 1206	VISHAY	CRCW1206475KFKEA

Table 2. 230V Bill of Materials (continued)

R6, R11	RES 10Ω 1% 0.25W 1206	VISHAY	CRCW120610R0FKEA
R8, R9, R56	RES 2.4kΩ 5% 1W 2512	VISHAY	CRCW25122K40JNEG
R10	RES 40.2Ω 1% 0.25W 1206	VISHAY	CRCW120640R2FKEA
R12, R14, R15	RES 301Ω 1% 0.25W 1206	VISHAY	CRCW1206301RFKEA
R16	RES 6.04kΩ 1% 0.125W 0805	VISHAY	CRCW08056K04FKEA
R17	RES 100kΩ 1% 0.1W 0603	VISHAY	CRCW0603100KFKEA
R19, R41, R43, R61, R73	RES 0Ω 5% 0.1W 0603	VISHAY	CRCW06030000Z0EA
R20	RES 499kΩ 1% 0.1W 0603	VISHAY	CRCW0603499KFKEA
R21, R69	RES 20.0kΩ 1% 0.1W 0603	VISHAY	CRCW060320K0FKEA
R23	RES 6.04kΩ 1% 0.1W 0603	VISHAY	CRCW06036K04FKEA
R24, R25	RES 75.0kΩ 1% 0.1W 0603	VISHAY	CRCW060375K0FKEA
R26, R29	RES 1MΩ 1% 0.25W 1206	VISHAY	CRCW12061M00FKEA
R28	RES 10Ω 1% 0.125W 0805	VISHAY	CRCW080510R0FKEA
R30, R31, R65, R66, R83	RES 1.00Ω 1% 0.25W 1206	VISHAY	CRCW12061R00FKEA
R32, R45, R77	RES 15.0kΩ 1% 0.1W 0603	VISHAY	CRCW060315K0FKEA
R34, R36	RES 5.62Ω 1% 0.25W 1206	VISHAY	CRCW12065R62FKEA
R38	RES 5.11kΩ 1% 0.1W 0603	VISHAY	CRCW06035K11FKEA
R39, R57	RES 10Ω 1% 3W WIREWOUND	VISHAY	PAC300001009FAC000
R44	THERM 10kΩ NTC 0603	MURATA	NTCG163JF103F
R46	RES 5.11kΩ 1% 0.125W 0805	VISHAY	CRCW08055K11FKEA
R48, R51, R62	RES 20.0kΩ 1% 0.25W 1206	VISHAY	CRCW120620K0FKEA
R55	RES 51.1kΩ 1% 0.25W 1206	VISHAY	CRCW120651K1FKEA
R70	RES 2.00kΩ 1% 0.125W 0805	VISHAY	CRCW08052K00FKEA
R71	RES 10.0kΩ 1% 0.125W 0805	VISHAY	CRCW080510K0FKEA
R72	RES 105kΩ 1% 0.125W 0805	VISHAY	CRCW0805105KFKEA
R81	RES 2.67kΩ 1% 0.1W 0603	VISHAY	CRCW06032K67FKEA
R84	RES 49.9kΩ 1% 0.1W 0603	VISHAY	CRCW060349K9FKEA
T1	XFORMER 230V 30W OUTPUT 50V	WURTH	750817651
U1	IC PFC CONT 16-TSSOP	NSC	LM3450AMT
U8, U9	OPTO-ISOLATOR SMD	LITE ON	CNY17F-3S
U10	IC SHUNT REG SOT-23	NSC	LMV431AIM5
U11	IC LED DRIVR 10-eMSOP	NSC	LM3409HVMY
C10, C14, C20, C25, C28, C29, C31, C40, Q20, R4, R13, R22, R27, R33, R40, R42, R49, R54, R59, R60, R63, R64, R75, R78, VR1	Did not populate		

14 PCB Layout

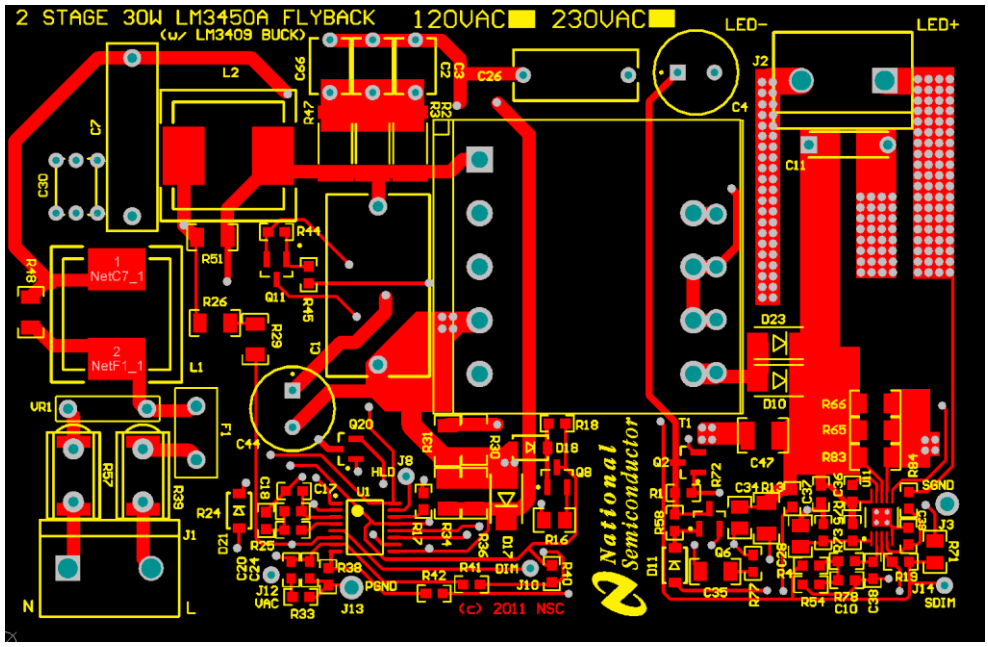


Figure 26. Top Copper and Silkscreen

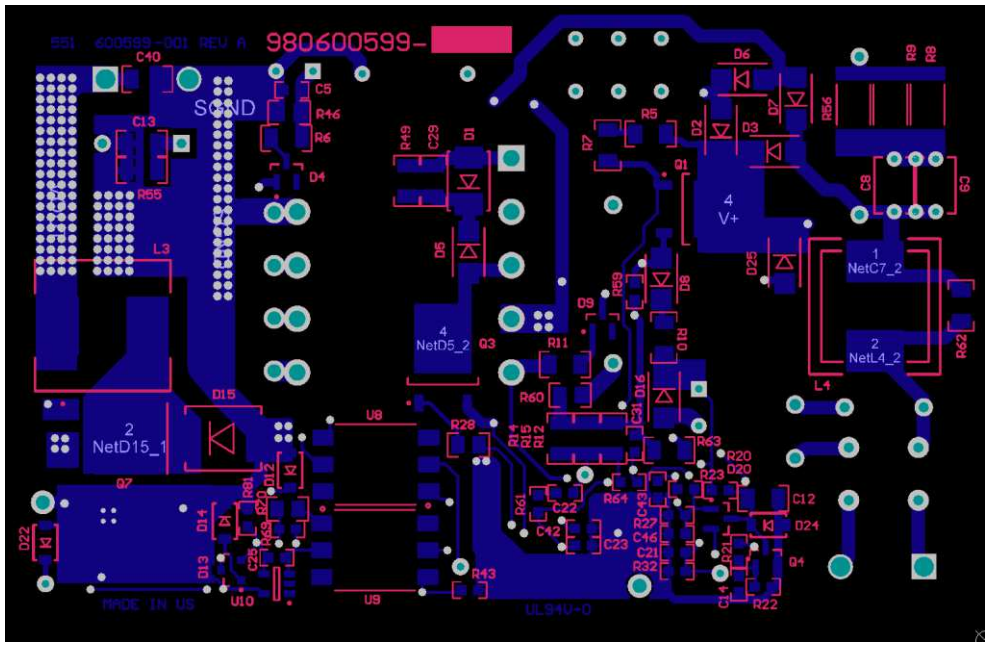


Figure 27. Bottom Copper and Silkscreen

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