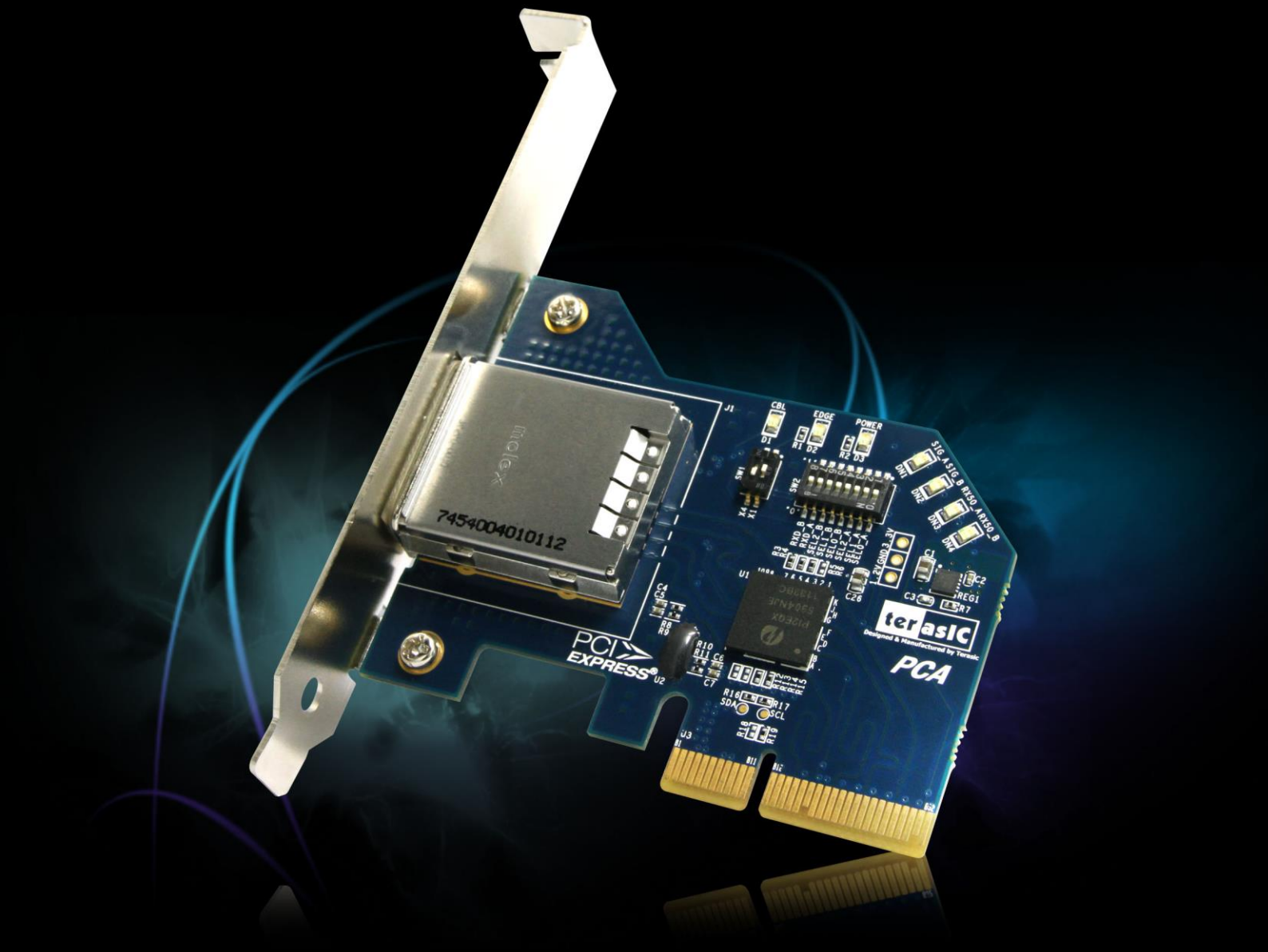
PCA

User Manual

Terasic PCIe Cable Adapter Daughter Card



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Chapter 1
Introduction

The Terasic PCIe x4 Cable Adapter (PCA) is used to connect a PCIe upstream slot with downstream target board via PCIe x4 cable, supporting PCIe x4 & x1 lanes. The PCA can provide programmable equalization, amplification, and de-emphasis for PCIe transceiver signal by using 8 select bits. It is also available to optimize performance over a variety of physical mediums by reducing Inter-symbol interference.

1.1 Features

Figure 1-1 shows a photograph of the PCA.

Figure 1-1 Exterior View

The key features of the card are listed below:

- Up to 5.0Gbps PCIe 2.0 Serial Re-Driver
- PCIe x4 Gen 2
- Adjustable receiver equalization
- Adjustable transmitter amplitude and de-emphasis

1.2 Getting Help

Here is information of how to get help if you encounter any problem:

Terasic Technologies

- Tel: +886-3-550-8800
- Email: support@terasic.com

Chapter 2
Architecture

This chapter provides information about architecture and block diagram of the PCA board.

2.1 Layout and Components

The picture of the Terasic PCIe x4 Cable Adapter (PCA) is shown in Figure 2-1 and Figure 2-2. It depicts the layout of the board and indicates the locations of the connectors and key components.

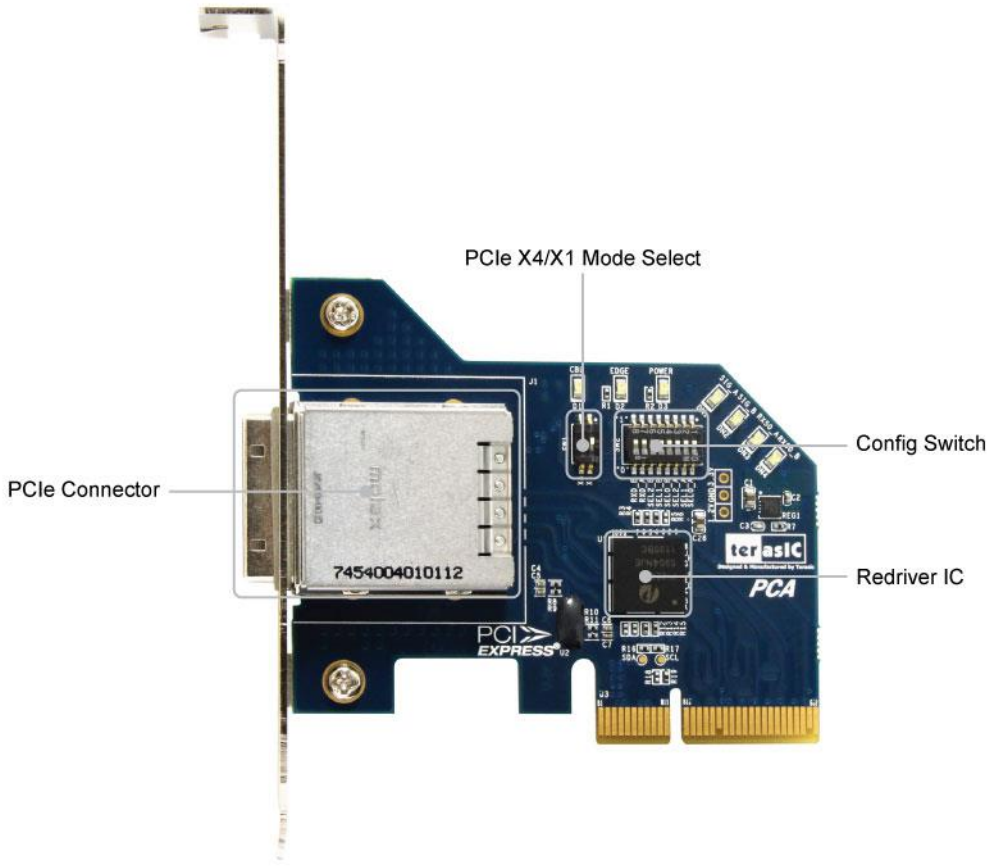

Figure 2-1 The PCA Card PCB and Component Diagram (top view)

Figure 2-2 The PCA Card PCB and Component Diagram (bottom view)

2.2 Block Diagram of the PCA Board

Figure 2-3 shows the block diagram of the PCA card.

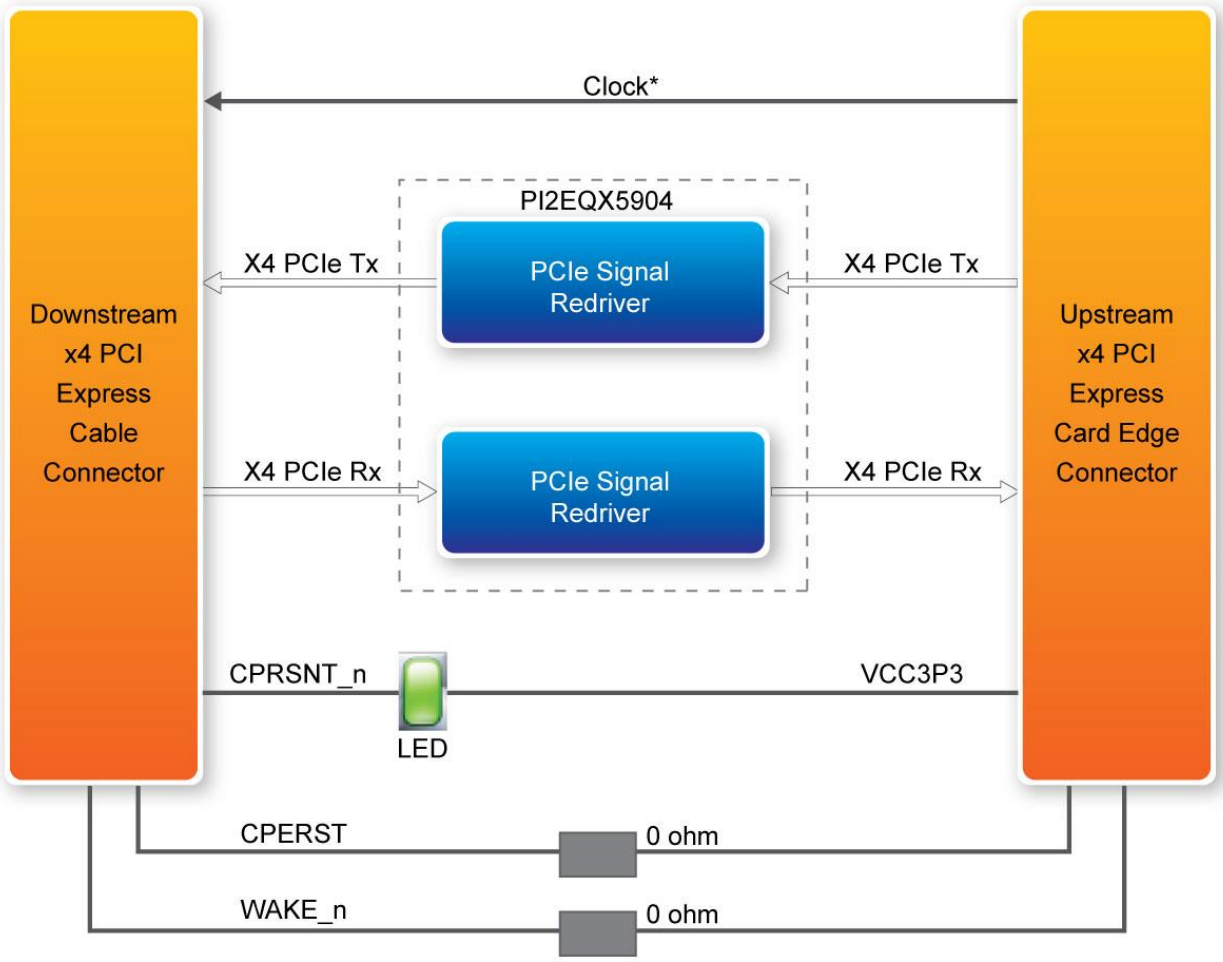

Figure 2-3 Block Diagram of PCA

Chapter 3
Board Components

This chapter describes the specifications of the on board components.

3.1 PCIe Edge Connector

This PCIe edge connector is used to connect the PCA with PC motherboard PCIe slot, as show **Figure 3-1** and **Figure 3-2**.

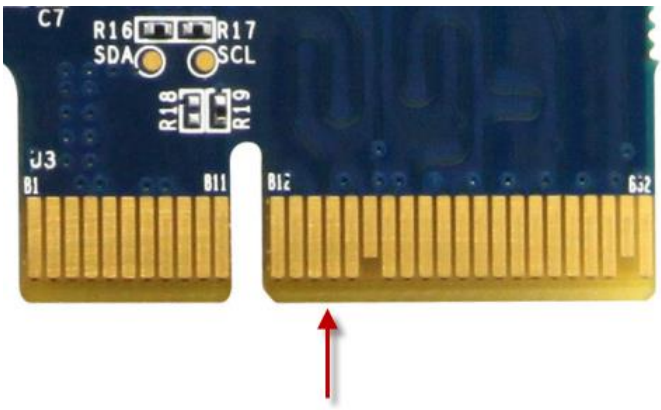

Figure 3-1 PCA Edge Connector

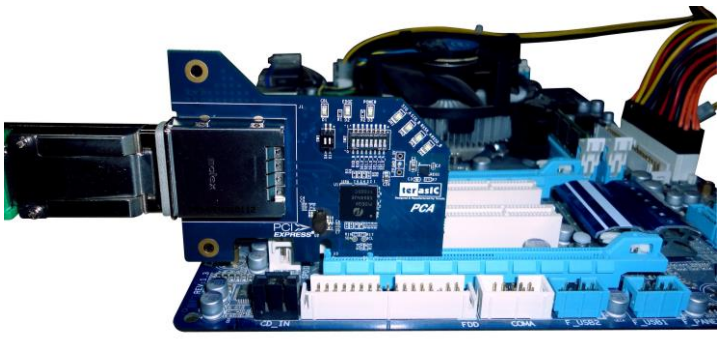

Figure 3-2 Plug the PCA into the PCIe slot of the Motherboard

The pins are numbered as shown in Table 3-1 with side A on the top of the center-line on the solder side of the board and side B on the bottom of the centerline on the component side of the board.

The PCIe interface pins PETpx, PETnx, PERpx, and PERnx are named with the following convention: “PE” stands for PCIe high speed, “T” for Transmitter, “R” for Receiver, “p” for positive (+), and “n” for negative (-).

Note that adjacent differential pairs are separated by two ground pins to manage the connector crosstalk.

Table 3-1 gives the wiring information of the PCIe Edge connector.

Table 3-1 Pin assignments and descriptions on PCIe Edge connector

Pin Numbers	*Side B*		*Side A*	
	Name	*Description*	*Name*	*Description*
1	NC	NC	PRSNT1n	Hot-Plug presence detect
2	NC	NC	NC	NC
3	NC	NC	NC	NC
4	GND	Ground	GND	Ground
5	NC	NC	NC	NC
6	NC	NC	NC	NC
7	GND	Ground	NC	NC
8	VCC3P3	3.3V Power	NC	NC
9	NC	NC	VCC3P3	3.3V Power
10	3.3VAUX	3.3 V Auxiliary Power	VCC3P3	3.3V Power
11	WAKE	NC	PERSTn	Fundamental Reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference clock (differential pair)
14	PETp0	Transmitter differential pair, Lane 0	REFCLK-	
15	PETn0		GND	Ground
16	GND	Ground	PERp0	Receiver differential pair, Lane 0
17	PRSNT2n	Hot-Plug presence detect	PERn0	
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential pair, Lane 1		
20	PETn1		GND	Ground
21	GND	Ground	PERp1	Receiver differential pair, Lane 1
22	GND	Ground	PERn1	
23	PETp2	Transmitter differential pair,	GND	Ground
24	PETn2		GND	Ground

		Lane 2		
25	GND	Ground	PERp2	Receiver differential pair, Lane 2
26	GND	Ground	PERn2	
27	PETp3	Transmitter differential pair, Lane 3	GND	Ground
28	PETn3		GND	Ground
29	GND	Ground	PERp3	Receiver differential pair, Lane 3
30	RSVD	Reserved	PERn3	
31	PRSNT2n	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved

3.2 PCIe Cable Connector

A PCIe cable connector is used to connect the PCIe x4 Cable and PCA cable connector, Connect the adapter by using a PCIe x4 Cable, as show **Figure 3-3.**

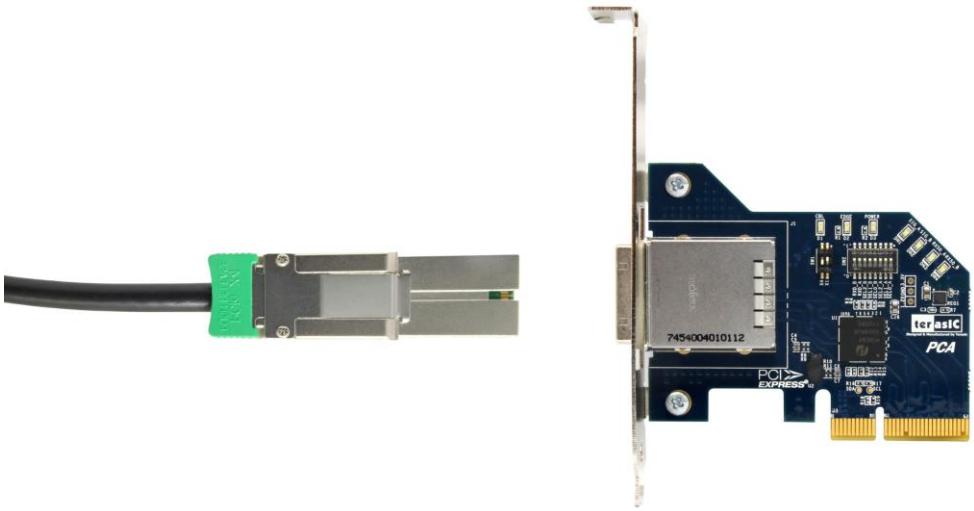

Figure 3-3 PCIe x4 Cable and PCA

To purchase the PCIe x4 Cable, please refer the url: ***PCIe_Cable.terasic.com***.

Figure 3-4 as show the PCIe Cable connects PCA connector

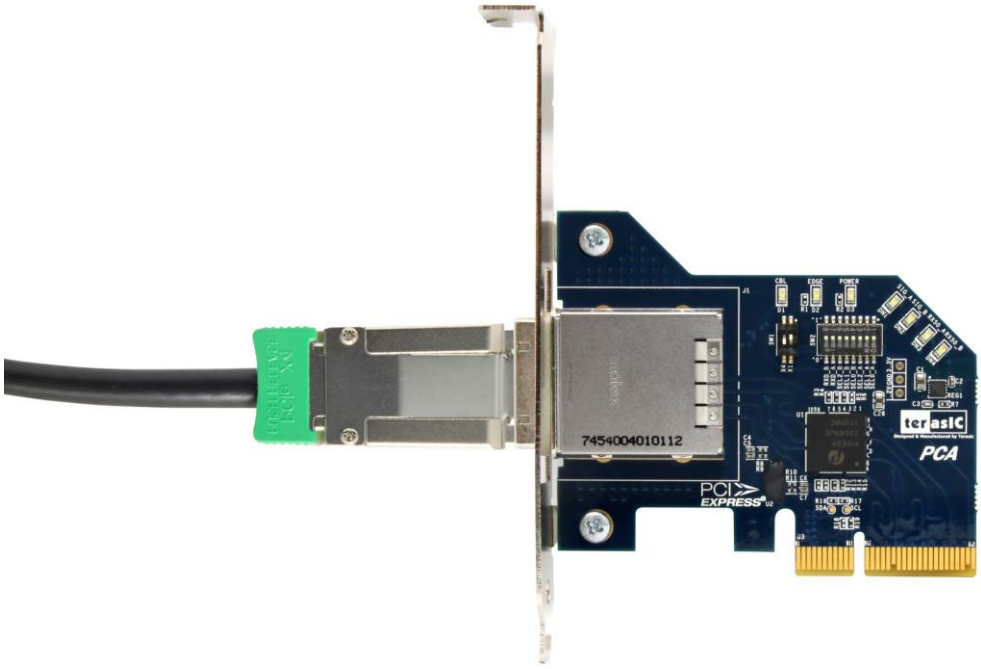

Figure 3-4 PCIe Cable and PCA connector Connected

Table 3-2 gives the wiring information of the PCIe Cable connector.

Pin Numbers	*Name*	*Description*
A1	GND	Ground reference for PCI Express transmitter Lanes
A2	PETp0	Differential PCI Express transmitter Lane 0
A3	PETn0	Differential PCI Express transmitter Lane 0
A4	GND	Ground reference for PCI Express transmitter Lanes
A5	PETp1	Differential PCI Express transmitter Lane 1
A6	PETn1	Differential PCI Express transmitter Lane 1
A7	GND	Ground reference for PCI Express transmitter Lanes
A8	PETp2	Differential PCI Express transmitter Lane 2
A9	PETn2	Differential PCI Express transmitter Lane 2
A10	GND	Ground reference for PCI Express transmitter Lanes

A11	PETp3	Differential PCI Express transmitter Lane 3
A12	PETn3	Differential PCI Express transmitter Lane 3
A13	GND	Ground reference for PCI Express transmitter Lanes
A14	CREFCLK+	Differential 100MHz cable reference clock
A15	CREFCLK-	Differential 100MHz cable reference clock
A16	GND	Ground reference for PCI Express transmitter Lanes
A17	SB_RTN	Signal return for single ended sideband signals
A18	CPRSNTn	Used for detection of whether a cable is installed and the downstream subsystem is powered
A19	CPWRON	Turns power on / off to slavetype downstream subsystems
B1	GND	Ground reference for PCI Express transmitter Lanes
B2	PERp0	Differential PCI Express receiver Lane 0
B3	PERn0	Differential PCI Express receiver Lane 0
B4	GND	Ground reference for PCI Express transmitter Lanes
B5	PERp1	Differential PCI Express receiver Lane 1
B6	PERn1	Differential PCI Express receiver Lane 1
B7	GND	Ground reference for PCI Express transmitter Lanes
B8	PERp2	Differential PCI Express receiver Lane 2
B9	PERn2	Differential PCI Express receiver Lane 2
B10	GND	Ground reference for PCI Express transmitter Lanes
B11	PERp3	Differential PCI Express receiver Lane 3
B12	PERn3	Differential PCI Express receiver Lane 3
B13	GND	Ground reference for PCI Express transmitter Lanes

B14	PWR	+3.3VCable power
B15	PWR	+3.3VCable power
B16	PWR RTN	Cable power return
B17	PWR RTN	Cable power return
B18	CWAKEn	Power management signal for wakeup events (optional)
B19	CPERSTn	Cable PERSTn

3.3 Switches

The PCA contains x2 and x8 switches that allow configuration of the PCA PCIe mode (SW1), equalization and de-emphasis (SW2). The two switches, SW1 and SW2, are located on top of the front side of the PCA card. Figure 3-5 show the location of the board.

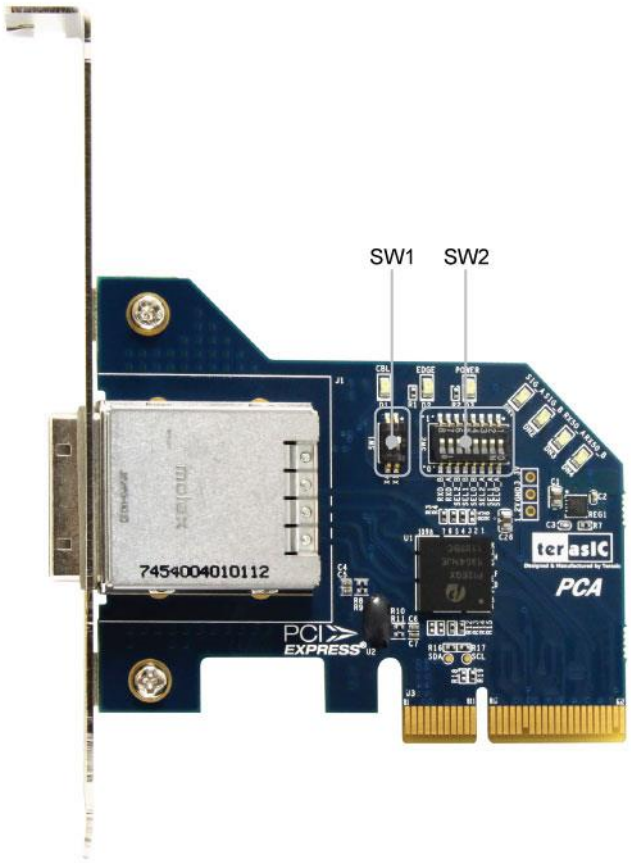

Figure 3-5 Switches

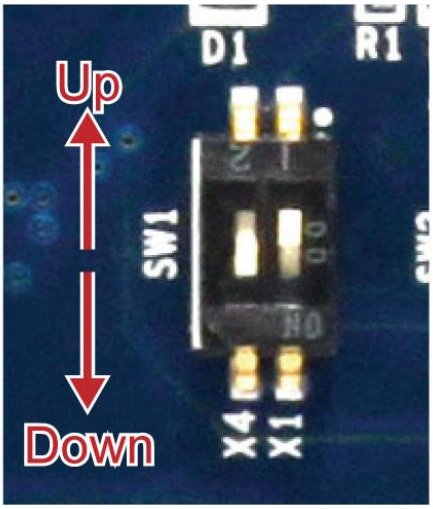

Figure 3-6 show the SW1 settings

Table 3-3 SW1 Settings

Pin 2	*Pin 1*	*PCIe Mode (x1/x4)*
UP	UP	NULL
UP	Down	x1
Down	UP	x4(Default mode)
Down	Down	NULL

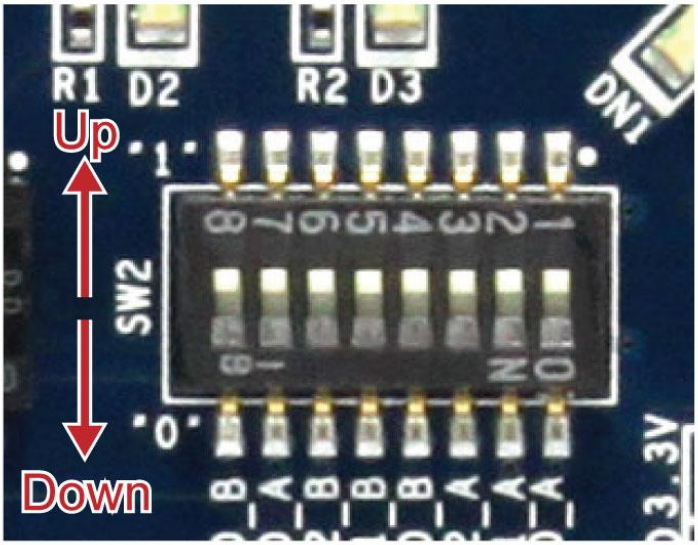

Figure 3-7 Show the SW2 Settings

The PI2EQX5904 chip located on the PCA has two channels, A and B, which are separately equalization controlled. **Figure 3-8** shows the block diagram of the channel A and B. Table 3-4 & Table 3-5 list the SW2 pins settings on Equalizer Configuration for channel A or channel B.

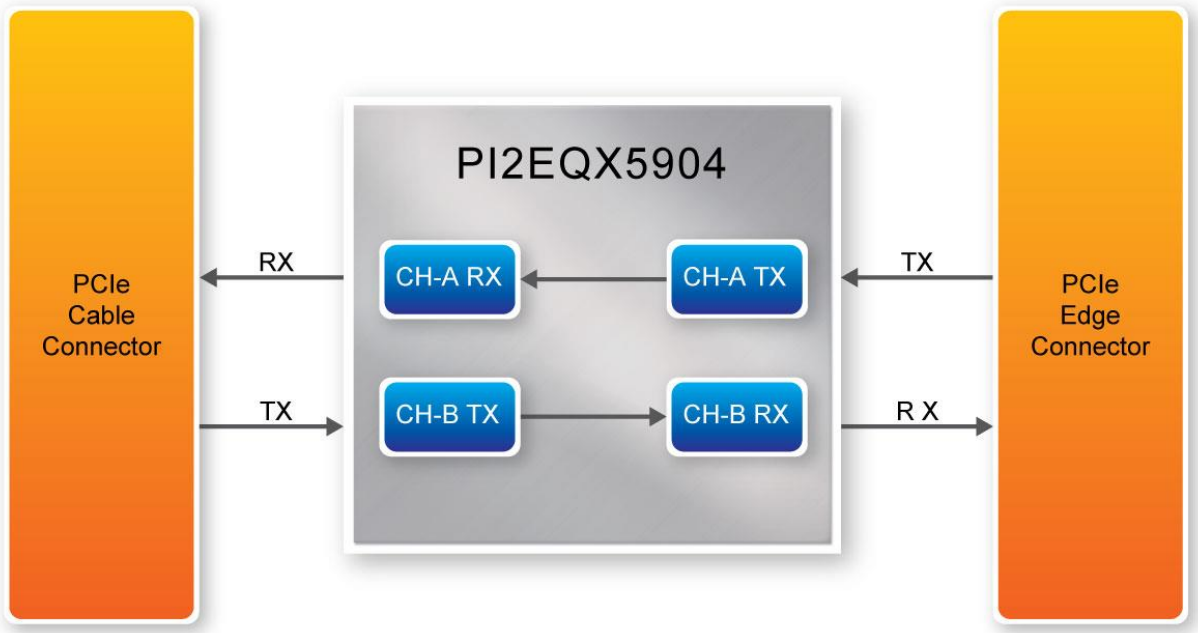

Figure 3-8 CH_A and CH_B of PI2EQX5904

Table 3-4 SW2 Settings (Input Equalizer Configuration for Channel A)

Pin 1 SEL0_A	*Pin 2 SEL1_A*	*Pin 3 SEL2_A*	*@1.25GHz*	*@2.5GHz*
0	0	0	0.5dB	1.2 dB
0	0	1	0.6dB	1.5 dB
0	1	0	1.0 dB	2.6 dB
0	1	1	1.9 dB	4.3 dB
1	0	0	2.8 dB	5.8 dB
1	0	1	3.6 dB	7.1 dB
1	1	0	5.0 dB	9.0 dB
1	1	1	7.7 dB(Default Setting)	12.3 dB(Default Setting)

Table 3-5 SW2 Settings (Input Equalizer Configuration for Channel B)

Pin 4 SEL0_B	*Pin 5 SEL1_B*	*Pin 6 SEL2_B*	*@1.25GHz*	*@2.5GHz*
0	0	0	0.5dB	1.2 dB
0	0	1	0.6dB	1.5 dB
0	1	0	1.0 dB	2.6 dB
0	1	1	1.9 dB	4.3 dB
1	0	0	2.8 dB	5.8 dB
1	0	1	3.6 dB	7.1 dB
1	1	0	5.0 dB	9.0 dB
1	1	1	7.7 dB(Default Setting)	12.3 dB(Default Setting)

The SW2 pin 7 connects to the PI2EQX5904 RXD_A pin, while SW2 pin 8 connects to PI2EQX5904 RXD_B pin. These 2 pins are used to control channel A & B Receiver Detect Enable function. Automatic Receiver Detection is a feature that can set the number of active channels. By sensing the presence of a load device on the output, the channel can be automatically enabled to operate.
When setting the RXD_A or RXD_B to a high level, Automatic Receiver Detection will be enabled. Please refer the datasheet of PI2EQX5904 for more settings.

Table 3-6 SW2 Settings (Receiver Detect Function Enable for CH_A & CH_B)

Pin 7 RXD_A	*Pin 8 RXD_B*	*Receiver Detect Function Enable*
1	1	CH_A & CH_B Receiver Detect Enable (Default Setting)
1	0	CH_A Receiver Detect Enable CH_B Receiver Detect Disable
0	1	CH_A Receiver Detect Disable CH_B Receiver Detect Enable
0	0	CH_A & CH_B Receiver Detect Disable

3.4 LEDs

The PCA includes status LEDs, Please refer **Table 3-7** for the status of the LED indicator.

Board Reference	*LED name*	*Description*
D1	CBL	Cable PRSNT1n

D2	**EDGE**	**Edge PRSNT1n**
D3	**POWER**	**Power LED**
DN1	**SIG_A**	**Signal detect output for CH_A**
DN2	**SIG_B**	**Signal detect output for CH_B**
DN3	**RX50_A**	**Receiver Detect Output for CH_A0**
DN4	**RX50_B**	**Receiver Detect Output for CH_B0**

Chapter 4 *Appendix*

4.1 Revision History

Version	*Change Log*
V1.0	Initial Version (Preliminary)
V1.1	Delete the chapter of TR4 demo

4.2 Copyright Statement

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