

# 8-Mbit (512K × 16) Static RAM

## Features

- Very high speed: 45 ns
- Wide voltage range: 2.2 V to 3.6 V and 4.5 V to 5.5 V
- Ultra low standby power
  - Typical Standby current: 2 μA
  - Maximum Standby current: 8 μA
- Ultra low active power
  - Typical active current: 1.8 mA at f = 1 MHz
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 44-pin thin small outline package (TSOP) II package

## Functional Description

The CY62157ESL is a high performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications. The device also has an automatic power down feature that significantly reduces power consumption when

addresses are not toggling. Place the device into standby mode when deselected ( $\overline{CE}$  HIGH or both  $\overline{BHE}$  and  $\overline{BLE}$  are HIGH). The input or output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), both the Byte High Enable and the Byte Low Enable are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during an active write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

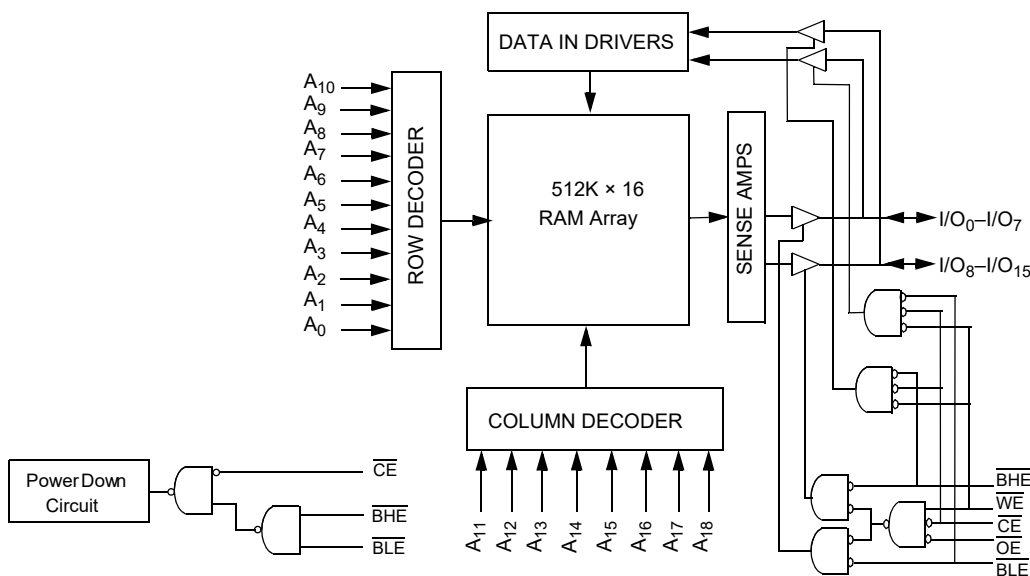
To write to the device, take Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from  $I/O$  pins ( $I/O_0$  through  $I/O_7$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from  $I/O$  pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ).

To read from the device, take Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on  $I/O_8$  to  $I/O_{15}$ . See the Truth Table on page 11 for a complete description of read and write modes.

The CY62157ESL device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see Electrical Characteristics on page 4 for more details and suggested alternatives.

For a complete list of related documentation, click [here](#).

## Logic Block Diagram



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## Pin Configurations

Figure 1. 44-pin TSOP II pinout (Top View)

A <sub>4</sub>	□ 1	44	□ A <sub>5</sub>
A <sub>3</sub>	□ 2	43	□ A <sub>6</sub>
A <sub>2</sub>	□ 3	42	□ A <sub>7</sub>
A <sub>1</sub>	□ 4	41	□ OE
A <sub>0</sub>	□ 5	40	□ BHE
$\overline{CE}$	□ 6	39	□ BLE
I/O <sub>0</sub>	□ 7	38	□ I/O <sub>15</sub>
I/O <sub>1</sub>	□ 8	37	□ I/O <sub>14</sub>
I/O <sub>2</sub>	□ 9	36	□ I/O <sub>13</sub>
I/O <sub>3</sub>	□ 10	35	□ I/O <sub>12</sub>
V <sub>CC</sub>	□ 11	34	□ V <sub>SS</sub>
V <sub>SS</sub>	□ 12	33	□ V <sub>CC</sub>
I/O <sub>4</sub>	□ 13	32	□ I/O <sub>11</sub>
I/O <sub>5</sub>	□ 14	31	□ I/O <sub>10</sub>
I/O <sub>6</sub>	□ 15	30	□ I/O <sub>9</sub>
I/O <sub>7</sub>	□ 16	29	□ I/O <sub>8</sub>
$\overline{WE}$	□ 17	28	□ A <sub>8</sub>
A <sub>18</sub>	□ 18	27	□ A <sub>9</sub>
A <sub>17</sub>	□ 19	26	□ A <sub>10</sub>
A <sub>16</sub>	□ 20	25	□ A <sub>11</sub>
A <sub>15</sub>	□ 21	24	□ A <sub>12</sub>
A <sub>14</sub>	□ 22	23	□ A <sub>13</sub>

## Product Portfolio

Product	Range	V <sub>CC</sub> Range (V) <sup>[1]</sup>	Speed (ns)	Power Dissipation					
				Operating I <sub>CC</sub> , (mA)				Standby, I <sub>SB2</sub> (μA)	
				f = 1MHz		f = f <sub>max</sub>			
				Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max
CY62157ESL	Industrial	2.2 V–3.6 V and 4.5 V–5.5 V	45	1.8	3	18	25	2	8

### Notes

- Datasheet specifications are not guaranteed for V<sub>CC</sub> in the range of 3.6 V to 4.5 V.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 3 V, and V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .....	-65 °C to +150 °C
Ambient Temperature with Power Applied .....	-55 °C to +125 °C
Supply Voltage to Ground Potential .....	-0.5 V to 6.0 V
DC Voltage Applied to Outputs in High Z State <sup>[3, 4]</sup> .....	-0.5 V to 6.0 V
DC Input Voltage <sup>[3, 4]</sup> .....	-0.5 V to 6.0 V

Output Current into Outputs (LOW) .....	20 mA
Static Discharge Voltage (MIL-STD-883, Method 3015) .....	>2001 V
Latch up Current .....	>200 mA

## Operating Range

Device	Range	Ambient Temperature	V <sub>CC</sub> <sup>[5]</sup>
CY62157ESL	Industrial	-40 °C to +85 °C	2.2 V–3.6 V, and 4.5 V–5.5 V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns			Unit	
			Min	Typ <sup>[6]</sup>	Max		
V <sub>OH</sub>	Output high voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7	I <sub>OH</sub> = -0.1 mA	2.0	-	-	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6	I <sub>OH</sub> = -1.0 mA	2.4	-	-	
		4.5 ≤ V <sub>CC</sub> ≤ 5.5	I <sub>OH</sub> = -1.0 mA	2.4	-	-	
		4.5 ≤ V <sub>CC</sub> ≤ 5.5	I <sub>OH</sub> = -0.1 mA	-	-	3.4 <sup>[7]</sup>	
V <sub>OL</sub>	Output low voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7	I <sub>OL</sub> = 0.1 mA	-	-	0.4	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6	I <sub>OL</sub> = 2.1 mA	-	-	0.4	
		4.5 ≤ V <sub>CC</sub> ≤ 5.5	I <sub>OL</sub> = 2.1 mA	-	-	0.4	
V <sub>IH</sub>	Input high voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7		1.8	-	V <sub>CC</sub> + 0.3	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6		2.2	-	V <sub>CC</sub> + 0.3	
		4.5 ≤ V <sub>CC</sub> ≤ 5.5		2.2	-	V <sub>CC</sub> + 0.5	
V <sub>IL</sub>	Input low voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7		-0.3	-	0.6	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6		-0.3	-	0.8	
		4.5 ≤ V <sub>CC</sub> ≤ 5.5		-0.5	-	0.8	
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1	-	+1	μA
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1	-	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	f = f <sub>max</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = V <sub>CCmax</sub>	-	18	25	mA
		f = 1 MHz	I <sub>OUT</sub> = 0 mA, CMOS levels	-	1.8	3	
I <sub>SB1</sub> <sup>[8]</sup>	Automatic CE power down current – CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2 V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> ≤ 0.2 V, f = f <sub>max</sub> (address and data only), f = 0 ( $\overline{OE}$ , $\overline{BHE}$ , $\overline{BLE}$ and $\overline{WE}$ ), V <sub>CC</sub> = V <sub>CC(max)</sub>		-	2	8	μA
I <sub>SB2</sub> <sup>[8]</sup>	Automatic CE power down current – CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2 V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> ≤ 0.2 V, f = 0, V <sub>CC</sub> = V <sub>CC(max)</sub>		-	2	8	μA

### Notes

- V<sub>IL</sub> (min) = -2.0 V for pulse durations less than 20 ns.
- V<sub>IH</sub> (max) = V<sub>CC</sub> + 0.75 V for pulse durations less than 20 ns.
- Full device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC</sub> (min) and 200 μs wait time after V<sub>CC</sub> stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 3 V, and V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25 °C.
- Please note that the maximum V<sub>OH</sub> limit does not exceed minimum CMOS V<sub>IH</sub> of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V<sub>IH</sub> of 3.5 V, please refer to Application Note AN6081 for technical details and options you may consider.
- Chip enable (CE) needs to be tied to CMOS levels to meet the I<sub>SB1</sub>/I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.

### Capacitance

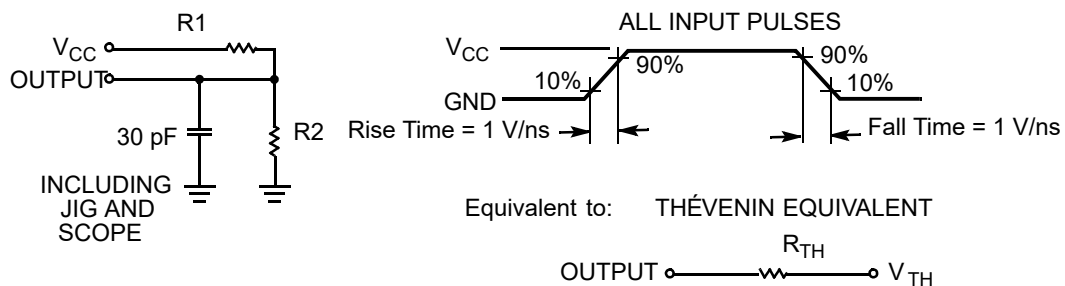
Parameter <sup>[9]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	10	pF
C <sub>OUT</sub>	Output capacitance		10	pF

### Thermal Resistance

Parameter <sup>[9]</sup>	Description	Test Conditions	TSOP II	Unit
θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	57.92	°C/W
θ <sub>JC</sub>	Thermal resistance (junction to case)		17.44	°C/W

### AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	2.5 V	3.0 V	5.0 V	Unit
R1	16667	1103	1800	Ω
R2	15385	1554	990	Ω
R <sub>TH</sub>	8000	645	639	Ω
V <sub>TH</sub>	1.20	1.75	1.77	V

**Note**

9. Tested initially and after any design or process changes that may affect these parameters.

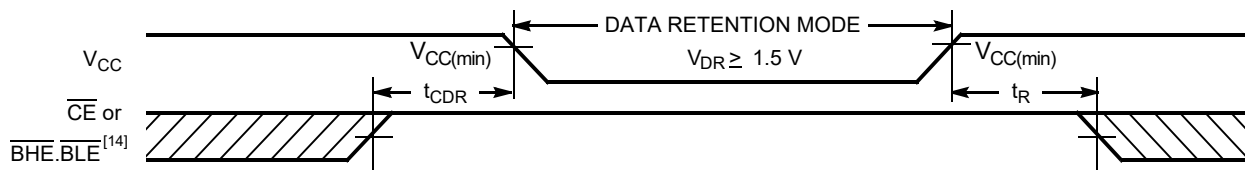
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[10]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1.5	–	–	V
$I_{CCDR}$ <sup>[10]</sup>	Data retention current	$\overline{CE} \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$				$\mu\text{A}$
		$V_{CC} = 1.5\text{ V}$	–	2	5	
		$V_{CC} = 2.0\text{ V}$	–	2	8	
$t_{CDR}$ <sup>[12]</sup>	Chip deselect to data retention time		0	–	–	ns
$t_R$ <sup>[13]</sup>	Operation recovery time		45	–	–	ns

## Data Retention Waveform

Figure 3. Data Retention Waveform



### Notes

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 3\text{ V}$ , and  $V_{CC} = 5\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ .
11. Chip enable ( $\overline{CE}$ ) needs to be tied to CMOS levels to meet the  $I_{SB1}/I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating.
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ .
14.  $\overline{BHE.BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Deselect the chip by either disabling chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

## Switching Characteristics

Over the Operating Range

Parameter <sup>[15, 16]</sup>	Description	45 ns		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{RC}$	Read cycle time	45	–	ns
$t_{AA}$	Address to data valid	–	45	ns
$t_{OHA}$	Data hold from address change	10	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid	–	45	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	22	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[17]</sup>	5	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[17, 18]</sup>	–	18	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[17]</sup>	10	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[17, 18]</sup>	–	18	ns
$t_{PU}$	$\overline{CE}$ LOW to power up	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to power down	–	45	ns
$t_{DBE}$	$\overline{BLE}/\overline{BHE}$ LOW to data valid	–	45	ns
$t_{LZBE}$	$\overline{BLE}/\overline{BHE}$ LOW to Low Z <sup>[17, 19]</sup>	5	–	ns
$t_{HZBE}$	$\overline{BLE}/\overline{BHE}$ HIGH to High Z <sup>[17, 18]</sup>	–	18	ns
<b>Write Cycle <sup>[20, 21]</sup></b>				
$t_{WC}$	Write cycle time	45	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	35	–	ns
$t_{AW}$	Address setup to write end	35	–	ns
$t_{HA}$	Address hold from write end	0	–	ns
$t_{SA}$	Address setup to write start	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	35	–	ns
$t_{BW}$	$\overline{BLE}/\overline{BHE}$ LOW to write end	35	–	ns
$t_{SD}$	Data setup to write end	25	–	ns
$t_{HD}$	Data hold from write end	0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[17, 18]</sup>	–	18	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[17]</sup>	10	–	ns

### Notes

15. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Note is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
16. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified IOL/IOH as shown in the Figure 2 on page 5.
17. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
18.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high-impedance state.
19. If both byte enables are toggled together, this value is 10 ns.
20. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IL}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
21. The minimum write cycle pulse width for Write Cycle No. 4 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be equal to the sum of  $t_{SD}$  and  $t_{HZWE}$ .

## Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [22, 23]

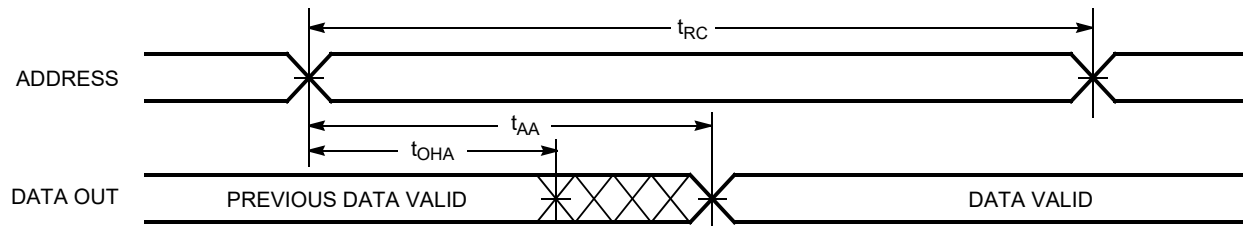
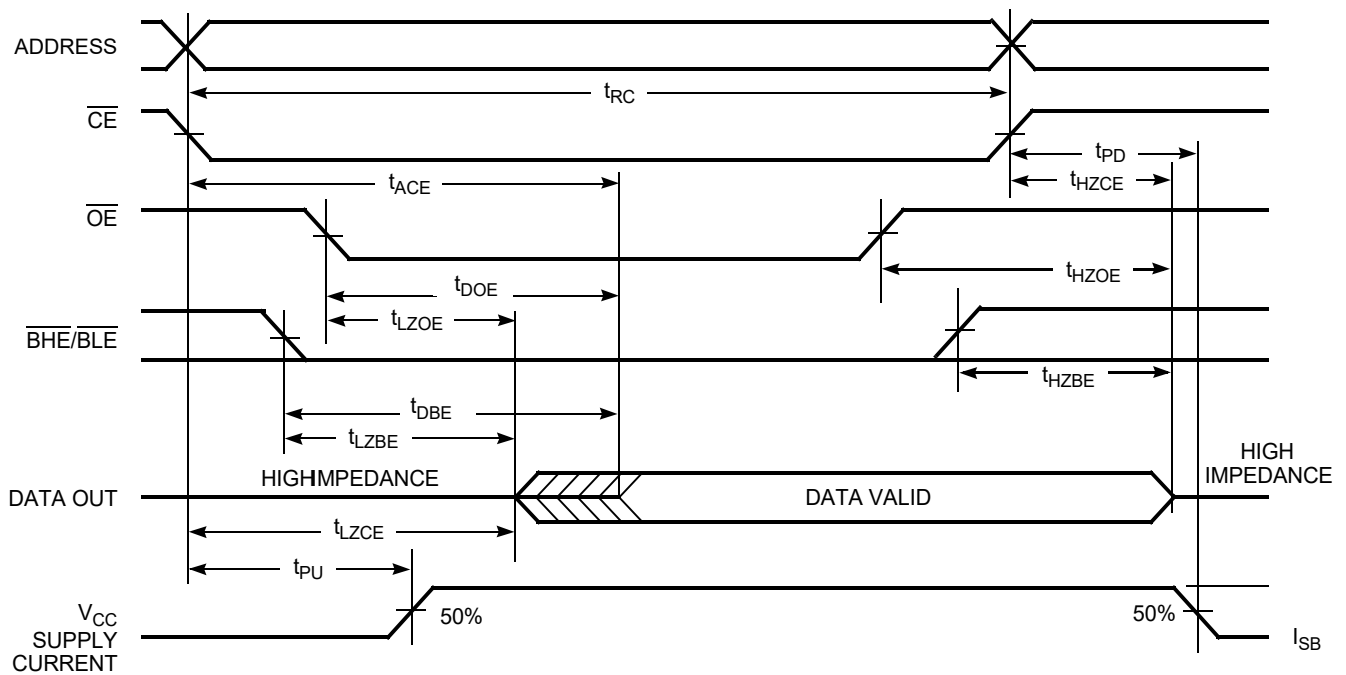


Figure 5. Read Cycle No. 2 ( $\overline{\text{OE}}$  Controlled) [23, 24]



### Notes

- 22. The device is continuously selected.  $\overline{\text{OE}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$ , or both =  $V_{\text{IL}}$ .
- 23.  $\overline{\text{WE}}$  is HIGH for read cycle.
- 24. Address valid before or similar to  $\overline{\text{CE}}$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  transition LOW.



Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ( $\overline{WE}$  Controlled) [25, 26]

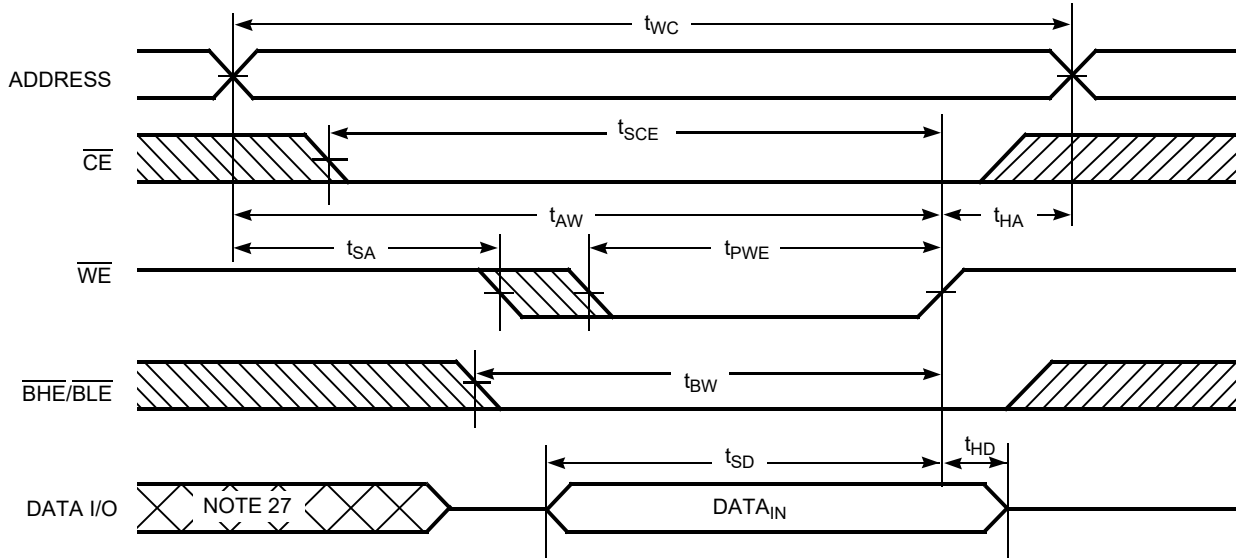
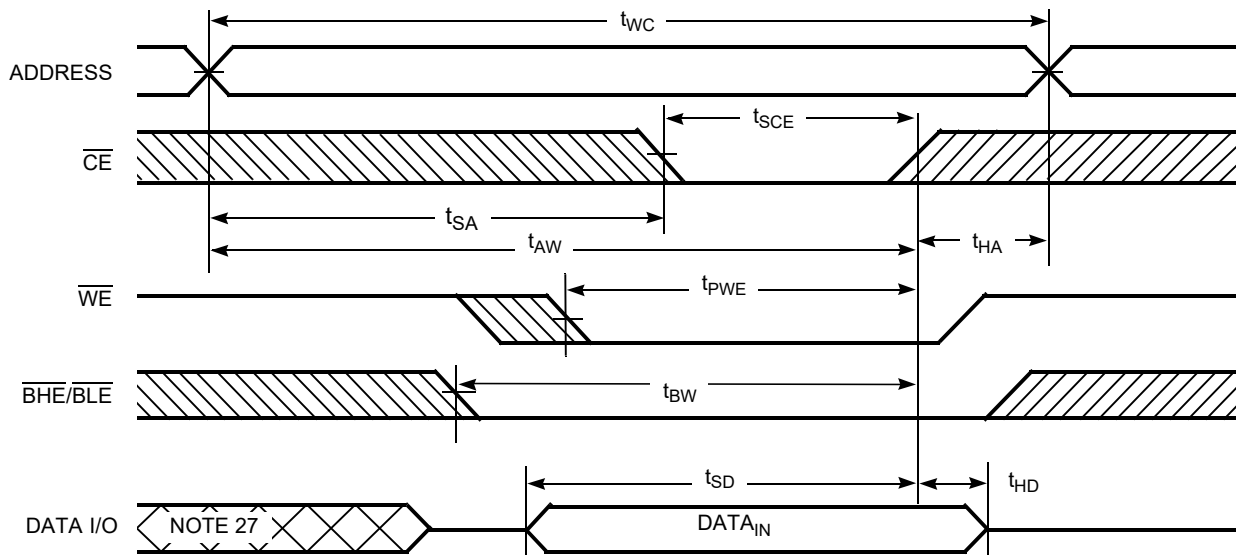


Figure 7. Write Cycle No. 2 ( $\overline{CE}$  Controlled) [25, 26]



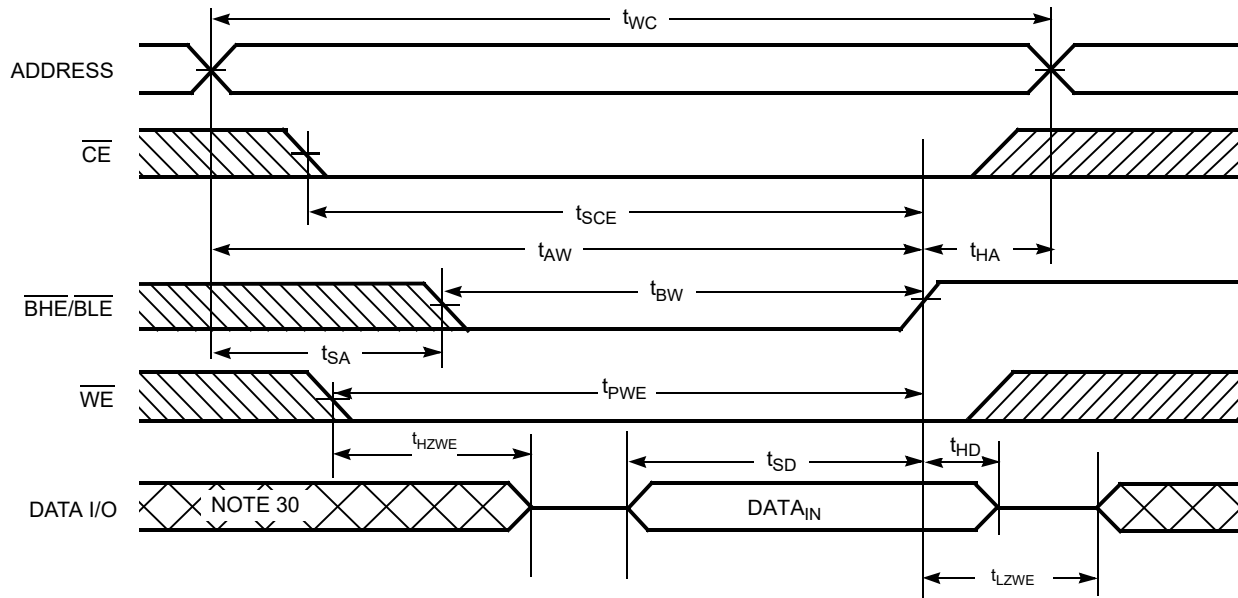
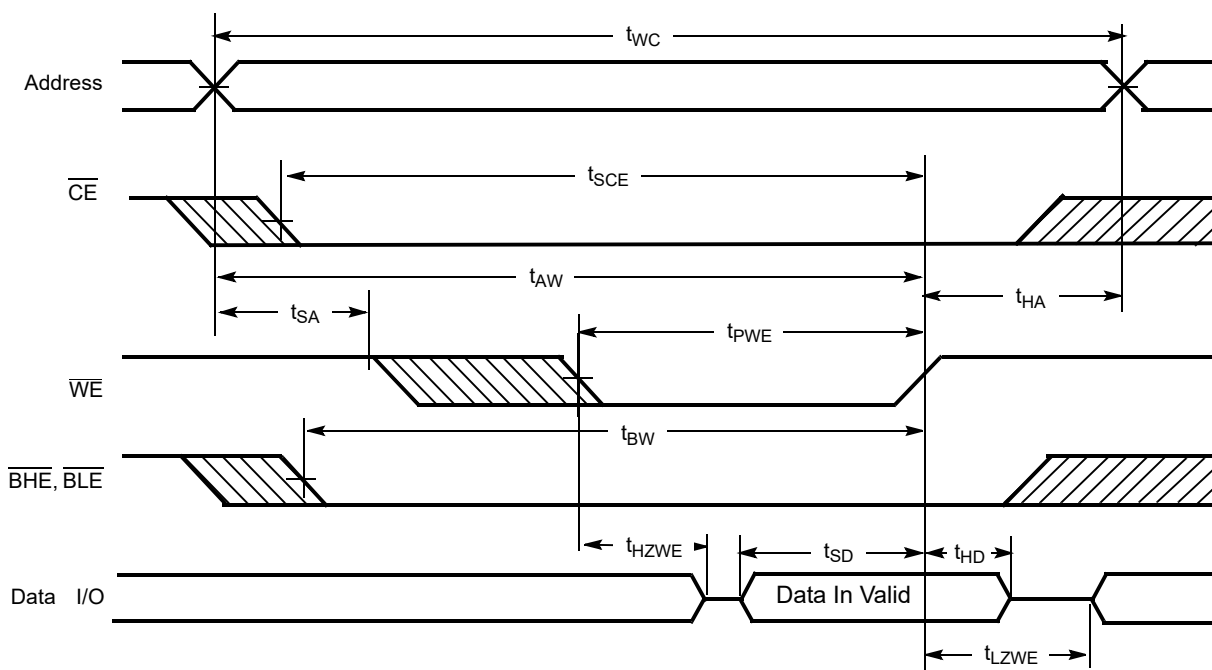
Notes

25. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IL}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

26. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.

27. During this period, the I/Os are in output state. Do not apply input signals.

**Switching Waveforms** (continued)

**Figure 8. Write Cycle No. 3 ( $\overline{\text{BHE}}/\overline{\text{BLE}}$  Controlled)** [28, 29]

**Figure 9. Write Cycle No. 4 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)** [28, 29, 31]

**Notes**

28. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  or both =  $V_{\text{IL}}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

29. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}} = V_{\text{IH}}$ , the output remains in a high impedance state.

30. During this period, the I/Os are in output state. Do not apply input signals.

31. The minimum write cycle pulse width should be equal to the sum of  $t_{\text{SD}}$  and  $t_{\text{HZWE}}$ .

**Truth Table**

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/power down	Standby ( $I_{SB}$ )
X <sup>[32]</sup>	X	X	H	H	High Z	Deselect/power down	Standby ( $I_{SB}$ )
L	H	L	L	L	Data Out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	L	H	L	Data Out ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Read	Active ( $I_{CC}$ )
L	H	H	L	L	High-Z	Output disabled	Active ( $I_{CC}$ )
L	H	H	H	L	High-Z	Output disabled	Active ( $I_{CC}$ )
L	H	H	L	H	High-Z	Output disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	L	X	H	L	Data In ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Write	Active ( $I_{CC}$ )

**Note**

32. The 'X' (Don't care) state for the Chip enable in the truth table refers to the logic state (either HIGH or LOW). Intermediate voltage levels on this pin is not permitted.

## Ordering Information

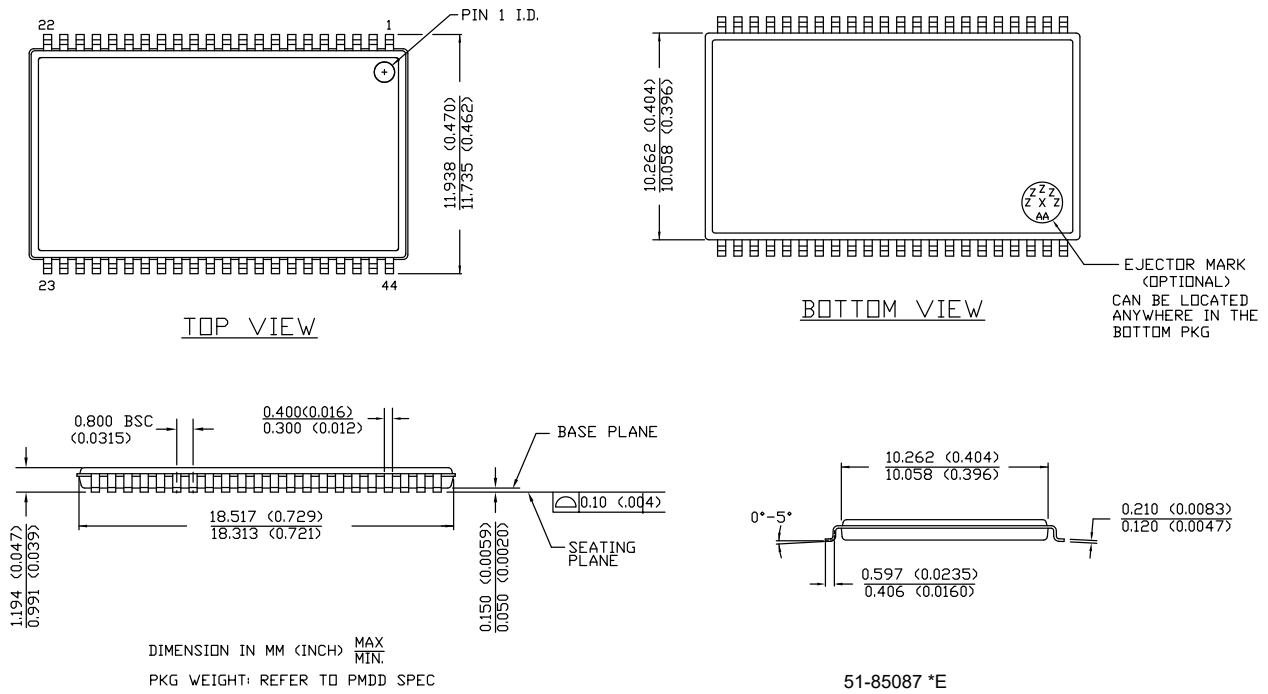
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62157ESL-45ZSXI	51-85087	44-pin TSOP Type II (Pb-free)	Industrial

## Ordering Code Definitions

CY	621	5	7	E	SL	-	45	ZS	X	I	
											Temperature Range: I = Industrial
											Pb-free
											Package Type: ZS = 44-pin TSOP II
											Speed Grade: 45 ns
											Voltage Range: SL = 3 V typical; 5 V typical
											Process Technology: E = 90 nm
											Bus Width: 7 = × 16
											Density: 5 = 8-Mbit
											Family Code: MoBL SRAM family
											Company ID: CY = Cypress

Package Diagram

Figure 10. 44-pin TSOP II Package Outline, 51-85087



## Acronyms

Acronym	Description
BHE	Byte High Enable
BLE	Byte Low Enable
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
OE	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
WE	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
MHz	megahertz
μA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

**Document History Page**

Document Title: CY62157ESL MoBL <sup>®</sup> , 8-Mbit (512K × 16) Static RAM Document Number: 001-43141				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	1875228	VKN / AESA	01/02/2008	New data sheet.
*A	2943752	VKN	06/03/2010	Added <a href="#">Contents</a> . Updated <a href="#">Electrical Characteristics</a> : Added Note 8 and referred the same note in I <sub>SB2</sub> parameter. Updated <a href="#">Truth Table</a> : Added Note 32 and referred the same note in $\overline{CE}$ column. Updated <a href="#">Package Diagram</a> : spec 51-85087 – Changed revision from *A to *C. Added <a href="#">Acronyms</a> . Updated to new template.
*B	3109266	PRAS	12/13/2010	Changed Table Footnotes to Footnotes. Updated <a href="#">Ordering Information</a> : No change in part numbers. Added <a href="#">Ordering Code Definitions</a> . Completing Sunset Review.
*C	3295175	RAME	06/29/2011	Updated <a href="#">Functional Description</a> : Updated description (Removed “For best practice recommendations, refer to the Cypress application note <a href="#">AN1064, SRAM System Guidelines</a> .”). Updated <a href="#">Electrical Characteristics</a> : Updated Note 8 (Added I <sub>SB1</sub> ) and referred the same note in I <sub>SB1</sub> parameter. Updated <a href="#">Capacitance</a> : Added Note 9 and referred the same note in parameter column. Updated <a href="#">Thermal Resistance</a> : Added Note 9 and referred the same note in parameter column. Updated <a href="#">Data Retention Characteristics</a> : Added Note 11 and referred the same note in I <sub>CCDR</sub> parameter. Updated <a href="#">Ordering Information</a> : No change in part numbers. Updated <a href="#">Ordering Code Definitions</a> . Added <a href="#">Units of Measure</a> .
*D	3904207	MEMJ	02/14/2013	Updated <a href="#">Switching Waveforms</a> : Updated <a href="#">Figure 6</a> (Removed $\overline{OE}$ signal). Updated <a href="#">Figure 7</a> (Removed $\overline{OE}$ signal). Removed the Note “Data I/O is high impedance if $\overline{OE} = V_{IH}$ .” and its reference in <a href="#">Figure 6</a> , <a href="#">Figure 7</a> . Removed the figure “Write Cycle 3: $\overline{WE}$ controlled, $\overline{OE}$ LOW”. Updated <a href="#">Figure 8</a> (Removed “ $\overline{OE}$ LOW” in caption only). Removed the Note “Data I/O is high impedance if $\overline{OE} = V_{IH}$ .” and its reference in <a href="#">Figure 8</a> . Updated <a href="#">Package Diagram</a> : spec 51-85087 – Changed revision from *C to *E. Completing Sunset Review.
*E	4019657	MEMJ	06/04/2013	Updated <a href="#">Functional Description</a> : Updated description. Updated <a href="#">Electrical Characteristics</a> : Added one more Test Condition “ $4.5 \leq V_{CC} \leq 5.5$ , I <sub>OH</sub> = -0.1 mA” for V <sub>OH</sub> parameter and added maximum value corresponding to that Test Condition. Added Note 7 and referred the same note in maximum value for V <sub>OH</sub> parameter corresponding to Test Condition “ $4.5 \leq V_{CC} \leq 5.5$ , I <sub>OH</sub> = -0.1 mA”.
*F	4100920	VINI	08/21/2013	Updated <a href="#">Switching Characteristics</a> : Added Note 15 and referred the same note in “Parameter” column. Updated to new template.

**Document History Page** (continued)

Document Title: CY62157ESL MoBL <sup>®</sup> , 8-Mbit (512K × 16) Static RAM				
Document Number: 001-43141				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*G	4576406	VINI	01/16/2015	Updated <a href="#">Functional Description</a> : Added "For a complete list of related documentation, click <a href="#">here</a> ." at the end. Updated <a href="#">Switching Characteristics</a> : Added Note 21 and referred the same note in "Write Cycle". Updated <a href="#">Switching Waveforms</a> : Added <a href="#">Figure 9</a> . Added Note 31 and referred the same note in <a href="#">Figure 9</a> .
*H	5169392	VINI	03/10/2016	Updated <a href="#">Thermal Resistance</a> : Replaced "two-layer" with "four-layer" in "Test Conditions" column. Changed value of $\theta_{JA}$ parameter from 77 °C/W to 57.92 °C/W. Changed value of $\theta_{JC}$ parameter from 13 °C/W to 17.44 °C/W. Updated to new template. Completing Sunset Review.
*I	5963507	AESATMP8	11/10/2017	Updated Cypress Logo and Copyright.
*J	6529321	VINI	04/01/2019	Updated to new template. Completing Sunset Review.



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