Freescale Semiconductor
Technical Data

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DSP56362

24-Bit Audio Digital Signal Processor

1 Overview

Freescale Semiconductor, Inc. designed the DSP56362 to support digital audio applications requiring digital audio compression and decompression, sound field processing, acoustic equalization, and other digital audio algorithms. The DSP56362 uses the high performance, single-clock-per-cycle DSP56300 core family of programmable CMOS digital signal processors (DSPs) combined with the audio signal processing capability of the Freescale Symphony™ DSP family, as shown in Figure 1-1. This design provides a two-fold performance increase over Freescale's popular Symphony family of DSPs while retaining code compatibility. Significant architectural enhancements include a barrel shifter, 24-bit addressing, instruction cache, and direct memory access (DMA). The DSP56362 offers 100 million instructions per second (MIPS) using an internal 100 MHz clock at 3.3 V.

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Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
"asserted"	Means that a high true (active high) signal is high or that a low true (active low) signal is low
"deasserted"	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:	**Signal/Symbol**	**Logic State**	**Signal State**	**Voltage***
	$\overline{\text{PIN}}$	True	Asserted	V_{IL} / V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH} / V_{OH}
	PIN	True	Asserted	V_{IH} / V_{OH}
	PIN	False	Deasserted	V_{IL} / V_{OL}

Note: *Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

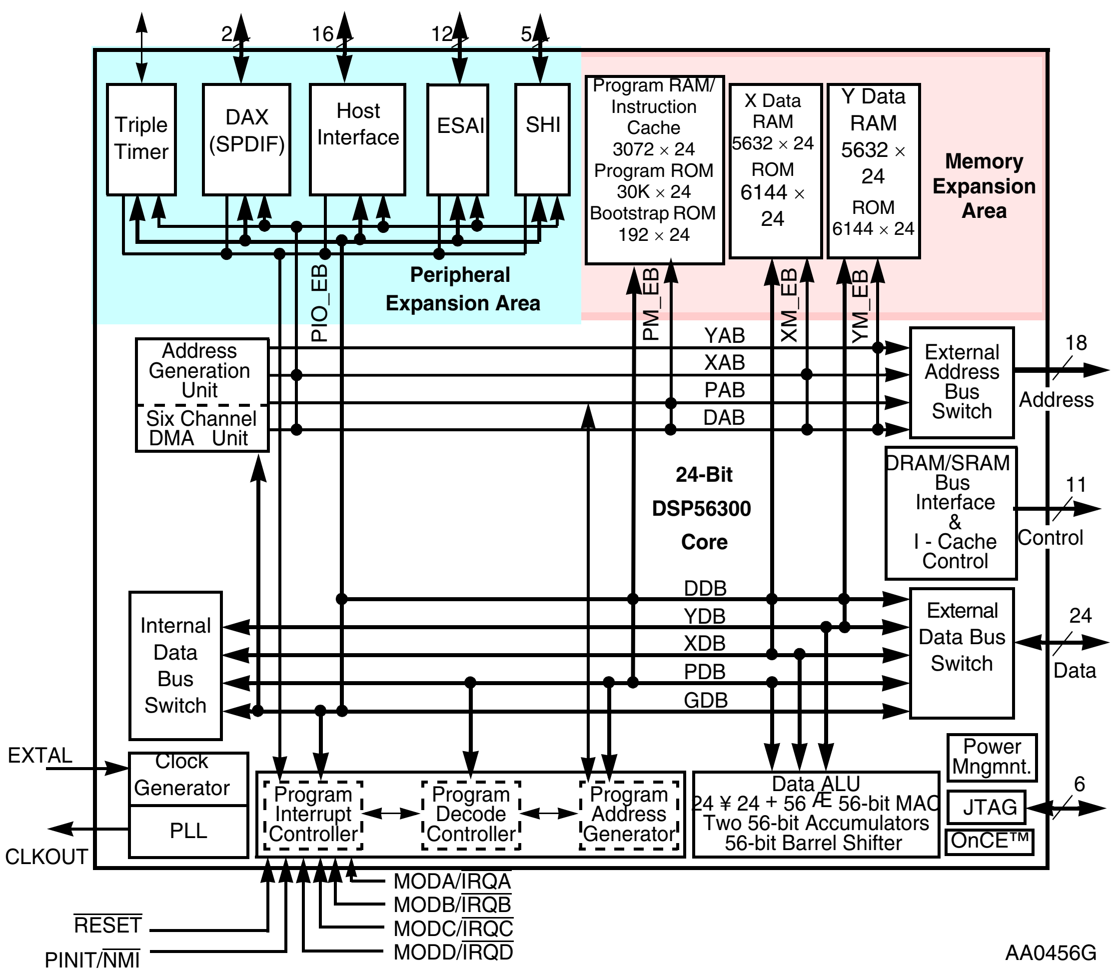


Figure 1-1 DSP56362 Block Diagram

1.1 Features

- Multimode, multichannel decoder software functionality
  - Dolby Digital and Pro Logic
  - MPEG2 5.1
  - DTS
  - Bass management
- Digital audio post-processing capabilities
  - 3D Virtual surround sound
  - Lucasfilm THX5.1
  - Soundfield processing
  - Equalization
- Digital Signal Processing Core
  - 100 MIPS with a 100 MHz clock at 3.3 V +/- 5%
  - Object code compatible with the DSP56000 core
  - Highly parallel instruction set
  - Data arithmetic logic unit (ALU)
    - Fully pipelined 24 x 24-bit parallel multiplier-accumulator (MAC)
    - 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing)
    - Conditional ALU instructions
    - 24-bit or 16-bit arithmetic support under software control
  - Program control unit (PCU)
    - Position independent code (PIC) support
    - Addressing modes optimized for DSP applications (including immediate offsets)
    - On-chip instruction cache controller
    - On-chip memory-expandable hardware stack
    - Nested hardware DO loops
    - Fast auto-return interrupts
  - Direct memory access (DMA)
    - Six DMA channels supporting internal and external accesses
    - One-, two-, and three- dimensional transfers (including circular buffering)
    - End-of-block-transfer interrupts
    - Triggering from interrupt lines and all peripherals
  - Phase-locked loop (PLL)
    - Software programmable PLL-based frequency synthesizer for the core clock
    - Allows change of low-power divide factor (DF) without loss of lock
    - Output clock with skew elimination
  - Hardware debugging support

- On-Chip Emulation (OnCE‘) module
- Joint Action Test Group (JTAG) test access port (TAP)
- Address trace mode reflects internal program RAM accesses at the external port

- On-Chip Memories
  - Modified Harvard architecture allows simultaneous access to program and data memories
  - 30720 x 24-bit on-chip program ROM[1] (disabled in 16-bit compatibility mode)
  - 6144 x 24-bit on-chip X-data ROM[1]
  - 6144 x 24-bit on-chip Y-data ROM[1]
  - Program RAM, instruction cache, X data RAM, and Y data RAM sizes are programmable

Instruction Cache	Switch Mode	Program RAM Size	Instruction Cache Size	X Data RAM Size	Y Data RAM Size
Disabled	Disabled	3072 × 24-bit	0	5632 × 24-bit	5632 × 24-bit
Enabled	Disabled	2048 × 24-bit	1024 × 24-bit	5632 × 24-bit	5632 × 24-bit
Disabled	Enabled	5120 × 24-bit	0	5632 × 24-bit	3584 × 24-bit
Enabled	Enabled	4096 × 24-bit	1024 × 24-bit	5632 × 24-bit	3584 × 24-bit

  - 192 x 24-bit bootstrap ROM (disabled in sixteen-bit compatibility mode)
- Off-Chip Memory Expansion
  - Data memory expansion to 256K x 24-bit word memory for P, X, and Y memory using SRAM.
  - Data memory expansion to 16M x 24-bit word memory for P, X, and Y memory using DRAM.
  - External memory expansion port(twenty-four data pins for high speed external memory access allowing for a large number of external accesses per sample)
  - Chip select logic for glueless interface to SRAMs
  - On-chip DRAM controller for glueless interface to DRAMs
- Peripheral and Support Circuits
  - Enhanced serial audio interface (ESAI) includes:
    - Six serial data lines, 4 selectable as receive or transmit and 2 transmit only.
    - Master or slave capability
    - I^2S, Sony, AC97, and other audio protocol implementations
  - Serial host interface (SHI) features:
    - SPI protocol with multi-master capability
    - I^2C protocol with single-master capability
    - Ten-word receive FIFO
    - Support for 8-, 16-, and 24-bit words.
  - Byte-wide parallel host interface (HDI08) with DMA support
  - DAX features one serial transmitter capable of supporting S/PDIF, IEC958, IEC1937, CP-340, and AES/EBU digital audio formats; alternate configuration supports up to two GPIO lines

1. These ROMs may be factory programmed with data or programs provided by the application developer.

- — Triple timer module with single external interface or GPIO line
- — On-chip peripheral registers are memory mapped in data memory space
- Reduced Power Dissipation
  - — Very low-power (3.3 V) CMOS design
  - — Wait and stop low-power standby modes
  - — Fully-static logic, operation frequency down to 0 Hz (dc)
  - — Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)

1.2 Package

- 144-pin plastic thin quad flat pack (LQFP) surface-mount package

1.3 Documentation

Table 1-1 lists the documents that provide a complete description of the DSP56362 and are required to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, a Freescale Literature Distribution Center, or through the Freescale DSP home page on the Internet (the source for the latest information).

Table 1-1 DSP56362 Documentation

Document Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the 56000-family architecture and the 24-bit core processor and instruction set	DSP56300FM
DSP56362 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56362UM
DSP56362 Product Brief	Brief description of the chip	DSP56362P
DSP56362 Data Sheet (this document)	Electrical and timing specifications; pin and package descriptions	DSP56362

NOTES

2 Signal/Connection Descriptions

2.1 Signal Groupings

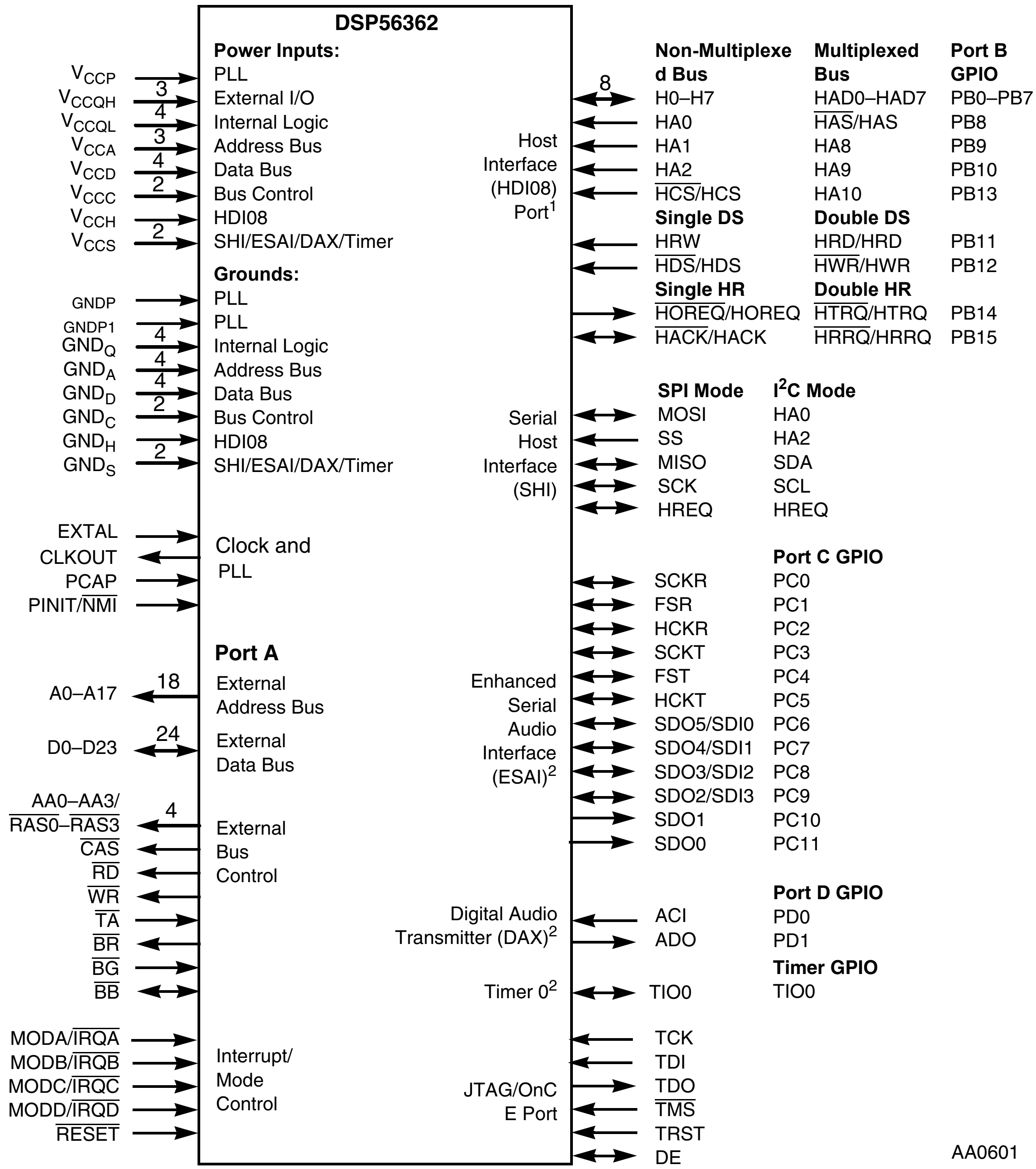
The input and output signals of the DSP56362 are organized into functional groups, which are listed in Table 2-1 and illustrated in Figure 2-1.

The DSP56362 is operated from a 3.3 V supply; however, some of the inputs can tolerate 5 V. A special notice for this feature is added to the signal descriptions of those inputs.

Table 2-1 DSP56362 Functional Signal Groupings

Functional Group		Number of Signals	Detailed Description
Power (V_{CC})		20	Table 2-2
Ground (GND)		19	Table 2-3
Clock and PLL		4	Table 2-4
Address bus	Port A[1]	18	Table 2-5
Data bus		24	Table 2-6
Bus control		11	Table 2-7
Interrupt and mode control		5	Table 2-8
HDI08	Port B[2]	16	Table 2-9
SHI		5	Table 2-10
ESAI	Port C[3]	12	Table 2-11
Digital audio transmitter (DAX)	Port D[4]	2	Table 2-12
Timer		1	Table 2-13
JTAG/OnCE Port		6	Table 2-14

1 Port A is the external memory interface port, including the external address bus, data bus, and control signals.
2 Port B signals are the GPIO port signals which are multiplexed with the HDI08 signals.
3 Port C signals are the GPIO port signals which are multiplexed with the ESAI signals.
4 Port D signals are the GPIO port signals which are multiplexed with the DAX signals.



Notes: 1. The HDI08 port supports a nonmultiplexed or a multiplexed bus, single or double data strobe (DS), and single or double host request (HR) configurations. Since each of these modes is configured independently, any combination of these modes is possible. These HDI08 signals can also be configured alternately as GPIO signals (PB0–PB15). Signals with dual designations (e.g., HAS/HAS) have configurable polarity.

2. The ESAI signals are multiplexed with the port C GPIO signals (PC0–PC11). The DAX signals are multiplexed with the Port D GPIO signals (PD0–PD1). The timer 0 signal can be configured alternately as the timer GPIO signal (TIO0).

Figure 2-1 Signals Identified by Functional Group

2.2 Power

Table 2-2 Power Inputs

Power Name	Description
V_{CCP}	**PLL Power**—V_{CCP} is V_{CC} dedicated for PLL use. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail. There is one V_{CCP} input.
V_{CCQL} (4)	**Quiet Core (Low) Power—**V_{CCQL} is an isolated power for the core processing logic. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are four V_{CCQ} inputs.
V_{CCQH} (3)	**Quiet External (High) Power**—V_{CCQH} is a quiet power source for I/O lines. This input must be tied externally to all other chip power inputs. The user must provide adequate decoupling capacitors. There are three V_{CCQH} inputs.
V_{CCA} (3)	**Address Bus Power**—V_{CCA} is an isolated power for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are three V_{CCA} inputs.
V_{CCD} (4)	**Data Bus Power**—V_{CCD} is an isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are four V_{CCD} inputs.
V_{CCC} (2)	**Bus Control Power**—V_{CCC} is an isolated power for the bus control I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are two V_{CCC} inputs.
V_{CCH}	**Host Power**—V_{CCH} is an isolated power for the HDI08 I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There is one V_{CCH} input.
V_{CCS} (2)	**SHI, ESAI, DAX, and Timer Power**—V_{CCS} is an isolated power for the SHI, ESAI, DAX, and Timer I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are two V_{CCS} inputs.

2.3 Ground

Table 2-3 Grounds

Ground Name	Description
GND_P	**PLL Ground**—GND_P is a ground dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. V_{CCP} should be bypassed to GND_P by a 0.47 μF capacitor located as close as possible to the chip package. There is one GND_P connection.
GND_{P1}	**PLL Ground 1**—GND_{P1} is a ground dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. There is one GND_{P1} connection.
GND_Q (4)	**Quiet Ground**—GND_Q is an isolated ground for the internal processing logic. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND_Q connections.
$GND_{A\ (4)}$	**Address Bus Ground**—GND_A is an isolated ground for sections of the address bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND_A connections.
GND_D (4)	**Data Bus Ground**—GND_D is an isolated ground for sections of the data bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND_D connections.
GND_C (2)	**Bus Control Ground**—GND_C is an isolated ground for the bus control I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are two GND_C connections.
GND_H	**Host Ground**—GND_H is an isolated ground for the HDI08 I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There is one GND_H connection.
GND_S (2)	**SHI, ESAI, DAX, and Timer Ground**—GND_S is an isolated ground for the SHI, ESAI, DAX, and Timer I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are two GND_S connections.

2.4 Clock and PLL

Table 2-4 Clock and PLL Signals

Signal Name	Type	State during Reset	Signal Description
EXTAL	Input	Input	**External Clock** Input—An external clock source must be connected to EXTAL in order to supply the clock to the internal clock generator and PLL. *This input **cannot** tolerate 5V.*
CLKOUT	Output	Chip-Driven	**Clock Output**—CLKOUT provides an output clock synchronized to the internal core clock phase. If the PLL is enabled and both the multiplication and division factors equal one, then CLKOUT is also synchronized to EXTAL. If the PLL is disabled, the CLKOUT frequency is half the frequency of EXTAL. CLKOUT is not functional at frequencies of 100 MHz and above.

Table 2-4 Clock and PLL Signals (continued)

Signal Name	Type	State during Reset	Signal Description
PCAP	Input	Input	**PLL Capacitor**—PCAP is an input connecting an off-chip capacitor to the PLL filter. Connect one capacitor terminal to PCAP and the other terminal to V_{CCP}. If the PLL is not used, PCAP may be tied to V_{CC}, GND, or left floating.
PINIT/$\overline{NMI}$	Input	Input	**PLL Initial/Non maskable Interrupt**—During assertion of $\overline{RESET}$, the value of PINIT/$\overline{NMI}$ is written into the PLL Enable (PEN) bit of the PLL control register, determining whether the PLL is enabled or disabled. After $\overline{RESET}$ deassertion and during normal instruction processing, the PINIT/$\overline{NMI}$ Schmitt-trigger input is a negative-edge-triggered non maskable interrupt (NMI) request internally synchronized to CLKOUT. *PINIT/$\overline{NMI}$ **cannot** tolerate 5 V.*

2.5 External Memory Expansion Port (Port A)

When the DSP56362 enters a low-power standby mode (stop or wait), it releases bus mastership and tri-states the relevant port A signals: A0–A17, D0–D23, AA0/$\overline{RAS0}$–AA3/$\overline{RAS3}$, $\overline{RD}$, $\overline{WR}$, $\overline{BB}$, $\overline{CAS}$.

2.5.1 External Address Bus

Table 2-5 External Address Bus Signals

Signal Name	Type	State during Reset	Signal Description
A0–A17	Output	Tri-Stated	**Address Bus**—When the DSP is the bus master, A0–A17 are active-high outputs that specify the address for external program and data memory accesses. Otherwise, the signals are tri-stated. To minimize power dissipation, A0–A17 do not change state when external memory spaces are not being accessed.

2.5.2 External Data Bus

Table 2-6 External Data Bus Signals

Signal Name	Type	State during Reset	Signal Description
D0–D23	Input/Output	Tri-Stated	**Data Bus**—When the DSP is the bus master, D0–D23 are active-high, bidirectional input/outputs that provide the bidirectional data bus for external program and data memory accesses. Otherwise, D0–D23 are tri-stated.

2.5.3 External Bus Control

Table 2-7 External Bus Control Signals

Signal Name	Type	State during Reset	Signal Description
AA0–AA3/RAS0–RAS3	Output	Tri-Stated	**Address Attribute or Row Address Strobe**—When defined as AA, these signals can be used as chip selects or additional address lines. When defined as RAS, these signals can be used as RAS for DRAM interface. These signals are can be tri-stated outputs with programmable polarity.
CAS	Output	Tri-Stated	**Column Address Strobe**—When the DSP is the bus master, CAS is an active-low output used by DRAM to strobe the column address. Otherwise, if the bus mastership enable (BME) bit in the DRAM control register is cleared, the signal is tri-stated.
RD	Output	Tri-Stated	**Read Enable**—When the DSP is the bus master, RD is an active-low output that is asserted to read external memory on the data bus (D0–D23). Otherwise, RD is tri-stated.
WR	Output	Tri-Stated	**Write Enable**—When the DSP is the bus master, WR is an active-low output that is asserted to write external memory on the data bus (D0–D23). Otherwise, the signals are tri-stated.
TA	Input	Ignored Input	**Transfer Acknowledge**—If the DSP56362 is the bus master and there is no external bus activity, or the DSP56362 is not the bus master, the TA input is ignored. The TA input is a data transfer acknowledge (DTACK) function that can extend an external bus cycle indefinitely. Any number of wait states (1, 2. . .infinity) may be added to the wait states inserted by the BCR by keeping TA deasserted. In typical operation, TA is deasserted at the start of a bus cycle, is asserted to enable completion of the bus cycle, and is deasserted before the next bus cycle. The current bus cycle completes one clock period after TA is asserted synchronous to CLKOUT. The number of wait states is determined by the TA input or by the bus control register (BCR), whichever is longer. The BCR can be used to set the minimum number of wait states in external bus cycles. In order to use the TA functionality, the BCR must be programmed to at least one wait state. A zero wait state access cannot be extended by TA deassertion, otherwise improper operation may result. TA can operate synchronously or asynchronously, depending on the setting of the TAS bit in the operating mode register (OMR). TA functionality may not be used while performing DRAM type accesses, otherwise improper operation may result.

Table 2-7 External Bus Control Signals (continued)

Signal Name	Type	State during Reset	Signal Description
$\overline{BR}$	Output	Output (deasserted)	**Bus Request**—$\overline{BR}$ is an active-low output, never tri-stated. $\overline{BR}$ is asserted when the DSP requests bus mastership. $\overline{BR}$ is deasserted when the DSP no longer needs the bus. $\overline{BR}$ may be asserted or deasserted independent of whether the DSP56362 is a bus master or a bus slave. Bus “parking” allows $\overline{BR}$ to be deasserted even though the DSP56362 is the bus master. (See the description of bus “parking” in the $\overline{BB}$ signal description.) The bus request hold (BRH) bit in the BCR allows $\overline{BR}$ to be asserted under software control even though the DSP does not need the bus. $\overline{BR}$ is typically sent to an external bus arbitrator that controls the priority, parking, and tenure of each master on the same external bus. $\overline{BR}$ is only affected by DSP requests for the external bus, never for the internal bus. During hardware reset, $\overline{BR}$ is deasserted and the arbitration is reset to the bus slave state.
$\overline{BG}$	Input	Ignored Input	**Bus Grant**—$\overline{BG}$ is an active-low input. $\overline{BG}$ is asserted by an external bus arbitration circuit when the DSP56362 becomes the next bus master. When $\overline{BG}$ is asserted, the DSP56362 must wait until $\overline{BB}$ is deasserted before taking bus mastership. When $\overline{BG}$ is deasserted, bus mastership is typically given up at the end of the current bus cycle. This may occur in the middle of an instruction that requires more than one external bus cycle for execution. The default mode of operation of this signal requires a setup and hold time referred to CLKOUT. But CLKOUT operation is not guaranteed from 100MHz and up, so the asynchronous bus arbitration must be used for clock frequencies 100MHz and above. The asynchronous bus arbitration is enabled by setting the ABE bit in the OMR register.
$\overline{BB}$	Input/ Output	Input	**Bus Busy**—$\overline{BB}$ is a bidirectional active-low input/output. $\overline{BB}$ indicates that the bus is active. Only after $\overline{BB}$ is deasserted can the pending bus master become the bus master (and then assert the signal again). The bus master may keep $\overline{BB}$ asserted after ceasing bus activity regardless of whether $\overline{BR}$ is asserted or deasserted. This is called “bus parking” and allows the current bus master to reuse the bus without rearbitration until another device requires the bus. The deassertion of $\overline{BB}$ is done by an “active pull-up” method (i.e., $\overline{BB}$ is driven high and then released and held high by an external pull-up resistor). The default mode of operation of this signal requires a setup and hold time referred to CLKOUT. But CLKOUT operation is not guaranteed from 100MHz and up, so the asynchronous bus arbitration must be used for clock frequencies 100MHz and above. The asynchronous bus arbitration is enabled by setting the ABE bit in the OMR register. $\overline{BB}$ requires an external pull-up resistor.

2.6 Interrupt and Mode Control

The interrupt and mode control signals select the chip's operating mode as it comes out of hardware reset. After $\overline{\text{RESET}}$ is deasserted, these inputs are hardware interrupt request lines.

Table 2-8 Interrupt and Mode Control

Signal Name	Type	State during Reset	Signal Description
MODA/$\overline{\text{IRQA}}$	Input	Input	**Mode Select A/External Interrupt Request A—**MODA/$\overline{\text{IRQA}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODA/$\overline{\text{IRQA}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the OMR when the $\overline{\text{RESET}}$ signal is deasserted. If $\overline{\text{IRQA}}$ is asserted synchronous to CLKOUT, multiple processors can be resynchronized using the WAIT instruction and asserting $\overline{\text{IRQA}}$ to exit the wait state. If the processor is in the stop standby state and the MODA/$\overline{\text{IRQA}}$ pin is pulled to GND, the processor will exit the stop state. This input is 5 V tolerant.
MODB/$\overline{\text{IRQB}}$	Input	Input	**Mode Select B/External Interrupt Request B—**MODB/$\overline{\text{IRQB}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODB/$\overline{\text{IRQB}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is deasserted. If $\overline{\text{IRQB}}$ is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting $\overline{\text{IRQB}}$ to exit the wait state. This input is 5 V tolerant.
MODC/$\overline{\text{IRQC}}$	Input	Input	**Mode Select C/External Interrupt Request C—**MODC/$\overline{\text{IRQC}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODC/$\overline{\text{IRQC}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is deasserted. If $\overline{\text{IRQC}}$ is asserted synchronous to CLKOUT, multiple processors can be resynchronized using the WAIT instruction and asserting $\overline{\text{IRQC}}$ to exit the wait state. This input is 5 V tolerant.

Table 2-8 Interrupt and Mode Control (continued)

Signal Name	Type	State during Reset	Signal Description
MODD/$\overline{\text{IRQD}}$	Input	Input	**Mode Select D/External Interrupt Request D**—MODD/$\overline{\text{IRQD}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODD/$\overline{\text{IRQD}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is deasserted. If $\overline{\text{IRQD}}$ is asserted synchronous to CLKOUT, multiple processors can be resynchronized using the WAIT instruction and asserting $\overline{\text{IRQD}}$ to exit the wait state. This input is 5 V tolerant.
$\overline{\text{RESET}}$	Input	Input	**Reset—**$\overline{\text{RESET}}$ is an active-low, Schmitt-trigger input. When asserted, the chip is placed in the reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. If $\overline{\text{RESET}}$ is deasserted synchronous to CLKOUT, exact start-up timing is guaranteed, allowing multiple processors to start synchronously and operate together in “lock-step.” When the $\overline{\text{RESET}}$ signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. The $\overline{\text{RESET}}$ signal must be asserted during power up. A stable EXTAL signal must be supplied while $\overline{\text{RESET}}$ is being asserted. This input is 5 V tolerant.

2.7 Host Interface (HDI08)

The HDI08 provides a fast, 8-bit, parallel data port that may be connected directly to the host bus. The HDI08 supports a variety of standard buses and can be directly connected to a number of industry standard microcomputers, microprocessors, DSPs, and DMA hardware.

2.7.1 Host Port Configuration

Signal functions associated with the HDI08 vary according to the interface operating mode as determined by the HDI08 port control register (HPCR). See **6.5.6 Host Port Control Register (HPCR)** on page Section 6-13 for detailed descriptions of this register and (See **Host Interface (HDI08)** on page Section 6-1.) for descriptions of the other HDI08 configuration registers.

Table 2-9 Host Interface

Signal Name	Type	State during Reset	Signal Description
H0–H7	Input/Output	GPIO Disconnected	**Host Data—**When the HDI08 is programmed to interface a nonmultiplexed host bus and the HI function is selected, these signals are lines 0–7 of the bidirectional, tri-state data bus.
HAD0–HAD7	Input/Output		**Host Address—**When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the address/data bidirectional, multiplexed, tri-state bus.
PB0–PB7	Input, Output, or Disconnected		**Port B 0–7—**When the HDI08 is configured as GPIO, these signals are individually programmable as input, output, or internally disconnected. The default state after reset for these signals is GPIO disconnected. This input is 5 V tolerant.
HA0	Input	GPIO Disconnected	**Host Address Input 0**—When the HDI08 is programmed to interface a nonmultiplexed host bus and the HI function is selected, this signal is line 0 of the host address input bus.
$\overline{HAS}$/HAS	Input		**Host Address Strobe—**When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is the host address strobe (HAS) Schmitt-trigger input. The polarity of the address strobe is programmable, but is configured active-low ($\overline{HAS}$) following reset.
PB8	Input, output, or disconnected		**Port B 8**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 5 V tolerant.
HA1	Input	GPIO Disconnected	**Host Address Input 1**—When the HDI08 is programmed to interface a nonmultiplexed host bus and the HI function is selected, this signal is line 1 of the host address (HA1) input bus.
HA8	Input		**Host Address 8**—When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line 8 of the host address (HA8) input bus.
PB9	Input, Output, or Disconnected		**Port B 9**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 5 V tolerant.

Table 2-9 Host Interface (continued)

Signal Name	Type	State during Reset	Signal Description
HA2 HA9 PB10	Input Input Input, Output, or Disconnected	GPIO Disconnected	**Host Address Input 2**—When the HDI08 is programmed to interface a non-multiplexed host bus and the HI function is selected, this signal is line 2 of the host address (HA2) input bus. **Host Address 9**—When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line 9 of the host address (HA9) input bus. **Port B 10**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 5 V tolerant.
HRW $\overline{\text{HRD}}$/HRD PB11	Input Input Input, Output, or Disconnected	GPIO Disconnected	**Host Read/Write**—When HDI08 is programmed to interface a single-data-strobe host bus and the HI function is selected, this signal is the Host Read/$\overline{\text{Write}}$ (HRW) input. **Host Read Data**—When HDI08 is programmed to interface a double-data-strobe host bus and the HI function is selected, this signal is the host read data strobe (HRD) Schmitt-trigger input. The polarity of the data strobe is programmable, but is configured as active-low ($\overline{\text{HRD}}$) after reset. **Port B 11**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 5 V tolerant.
$\overline{\text{HDS}}$/HDS $\overline{\text{HWR}}$/HWR PB12	Input Input Input, Output, or Disconnected	GPIO Disconnected	**Host Data Strobe—**When HDI08 is programmed to interface a single-data-strobe host bus and the HI function is selected, this signal is the host data strobe (HDS) Schmitt-trigger input. The polarity of the data strobe is programmable, but is configured as active-low ($\overline{\text{HDS}}$) following reset. **Host Write Data**—When HDI08 is programmed to interface a double-data-strobe host bus and the HI function is selected, this signal is the host write data strobe (HWR) Schmitt-trigger input. The polarity of the data strobe is programmable, but is configured as active-low ($\overline{\text{HWR}}$) following reset. **Port B 12**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 5 V tolerant.

Table 2-9 Host Interface (continued)

Signal Name	Type	State during Reset	Signal Description
HCS HA10 PB13	Input Input Input, Output, or Disconnected	GPIO Disconnected	**Host Chip Select—**When HDI08 is programmed to interface a nonmultiplexed host bus and the HI function is selected, this signal is the host chip select (HCS) input. The polarity of the chip select is programmable, but is configured active-low ($\overline{HCS}$) after reset. **Host Address 10**—When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line 10 of the host address (HA10) input bus. **Port B 13**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 5 V tolerant.

Table 2-9 Host Interface (continued)

Signal Name	Type	State during Reset	Signal Description
$\overline{\text{HOREQ}}$/HORE	Output	GPIO Disconnected	**Host Request**—When HDI08 is programmed to interface a single host request host bus and the HI function is selected, this signal is the host request (HOREQ) output. The polarity of the host request is programmable, but is configured as active-low ($\overline{\text{HOREQ}}$) following reset. The host request may be programmed as a driven or open-drain output.
$\overline{\text{HTRQ}}$/HTRQ	Output		**Transmit Host Request—**When HDI08 is programmed to interface a double host request host bus and the HI function is selected, this signal is the transmit host request (HTRQ) output. The polarity of the host request is programmable, but is configured as active-low ($\overline{\text{HTRQ}}$) following reset. The host request may be programmed as a driven or open-drain output.
PB14	Input, Output, or Disconnected		**Port B 14**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 5 V tolerant.
$\overline{\text{HACK}}$/HACK	Input	GPIO Disconnected	**Host Acknowledge**—When HDI08 is programmed to interface a single host request host bus and the HI function is selected, this signal is the host acknowledge (HACK) Schmitt-trigger input. The polarity of the host acknowledge is programmable, but is configured as active-low ($\overline{\text{HACK}}$) after reset.
$\overline{\text{HRRQ}}$/HRRQ	Output		**Receive Host Request**—When HDI08 is programmed to interface a double host request host bus and the HI function is selected, this signal is the receive host request (HRRQ) output. The polarity of the host request is programmable, but is configured as active-low ($\overline{\text{HRRQ}}$) after reset. The host request may be programmed as a driven or open-drain output.
PB15	Input, Output, or Disconnected		**Port B 15**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 5 V tolerant.

2.8 Serial Host Interface

The SHI has five I/O signals that can be configured to allow the SHI to operate in either SPI or I^2C mode.

Table 2-10 Serial Host Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
SCK SCL	Input or Output Input or Output	Tri-Stated	**SPI Serial Clock**—The SCK signal is an output when the SPI is configured as a master and a Schmitt-trigger input when the SPI is configured as a slave. When the SPI is configured as a master, the SCK signal is derived from the internal SHI clock generator. When the SPI is configured as a slave, the SCK signal is an input, and the clock signal from the external master synchronizes the data transfer. The SCK signal is ignored by the SPI if it is defined as a slave and the slave select ($\overline{SS}$) signal is not asserted. In both the master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI transfer protocol. **I^2C Serial Clock**—SCL carries the clock for I^2C bus transactions in the I^2C mode. SCL is a Schmitt-trigger input when configured as a slave and an open-drain output when configured as a master. SCL should be connected to V_{CC} through a pull-up resistor. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This input is 5 V tolerant.
MISO SDA	Input or Output Input or Open-Drain Output	Tri-Stated	**SPI Master-In-Slave-Out**—When the SPI is configured as a master, MISO is the master data input line. The MISO signal is used in conjunction with the MOSI signal for transmitting and receiving serial data. This signal is a Schmitt-trigger input when configured for the SPI Master mode, an output when configured for the SPI Slave mode, and tri-stated if configured for the SPI Slave mode when $\overline{SS}$ is deasserted. An external pull-up resistor is not required for SPI operation. **I^2C Data and Acknowledge**—In I^2C mode, SDA is a Schmitt-trigger input when receiving and an open-drain output when transmitting. SDA should be connected to V_{CC} through a pull-up resistor. SDA carries the data for I^2C transactions. The data in SDA must be stable during the high period of SCL. The data in SDA is only allowed to change when SCL is low. When the bus is free, SDA is high. The SDA line is only allowed to change during the time SCL is high in the case of start and stop events. A high-to-low transition of the SDA line while SCL is high is a unique situation, and is defined as the start event. A low-to-high transition of SDA while SCL is high is a unique situation defined as the stop event. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This input is 5 V tolerant.

Table 2-10 Serial Host Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
MOSI	Input or Output	Tri-Stated	**SPI Master-Out-Slave-In**—When the SPI is configured as a master, MOSI is the master data output line. The MOSI signal is used in conjunction with the MISO signal for transmitting and receiving serial data. MOSI is the slave data input line when the SPI is configured as a slave. This signal is a Schmitt-trigger input when configured for the SPI Slave mode.
HA0	Input		**I^{2}C Slave Address 0**—This signal uses a Schmitt-trigger input when configured for the I^{2}C mode. When configured for I^{2}C slave mode, the HA0 signal is used to form the slave device address. HA0 is ignored when configured for the I^{2}C master mode. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This input is 5 V tolerant.
$\overline{SS}$	Input	Tri-Stated	**SPI Slave Select**—This signal is an active low Schmitt-trigger input when configured for the SPI mode. When configured for the SPI Slave mode, this signal is used to enable the SPI slave for transfer. When configured for the SPI master mode, this signal should be kept deasserted (pulled high). If it is asserted while configured as SPI master, a bus error condition is flagged. If $\overline{SS}$ is deasserted, the SHI ignores SCK clocks and keeps the MISO output signal in the high-impedance state.
HA2	Input		**I^{2}C Slave Address 2**—This signal uses a Schmitt-trigger input when configured for the I^{2}C mode. When configured for the I^{2}C Slave mode, the HA2 signal is used to form the slave device address. HA2 is ignored in the I^{2}C master mode. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This input is 5 V tolerant.
$\overline{HREQ}$	Input or Output	Tri-Stated	**Host Request**—This signal is an active low Schmitt-trigger input when configured for the master mode but an active low output when configured for the slave mode. When configured for the slave mode, $\overline{HREQ}$ is asserted to indicate that the SHI is ready for the next data word transfer and deasserted at the first clock pulse of the new data word transfer. When configured for the master mode, $\overline{HREQ}$ is an input. When asserted by the external slave device, it will trigger the start of the data word transfer by the master. After finishing the data word transfer, the master will await the next assertion of $\overline{HREQ}$ to proceed to the next transfer. This signal is tri-stated during hardware, software, personal reset, or when the HREQ1–HREQ0 bits in the HCSR are cleared. There is no need for external pull-up in this state. This input is 5 V tolerant.

2.9 Enhanced Serial Audio Interface

Table 2-11 Enhanced Serial Audio Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
HCKR PC2	Input or Output Input, Output, or Disconnected	GPIO Disconnected	**High Frequency Clock for Receiver**—When programmed as an input, this signal provides a high frequency clock source for the ESAI receiver as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high-frequency sample clock (e.g., for external digital to analog converters [DACs]) or as an additional system clock. **Port C 2**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
HCKT PC5	Input or Output Input, Output, or Disconnected	GPIO Disconnected	**High Frequency Clock for Transmitter**—When programmed as an input, this signal provides a high frequency clock source for the ESAI transmitter as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high frequency sample clock (e.g., for external DACs) or as an additional system clock. **Port C 5**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
FSR PC1	Input or Output Input, Output, or Disconnected	GPIO Disconnected	**Frame Sync for Receiver**—This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1). When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode. **Port C 1**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.

Table 2-11 Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
FST PC4	Input or Output Input, Output, or Disconnected	GPIO Disconnected	**Frame Sync for Transmitter**—This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI transmit clock control register (TCCR). **Port C 4**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SCKR PC0	Input or Output Input, Output, or Disconnected	GPIO Disconnected	**Receiver Serial Clock**—SCKR provides the receiver serial bit clock for the ESAI. The SCKR operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1). When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode. **Port C 0**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SCKT PC3	Input or Output Input, Output, or Disconnected	GPIO Disconnected	**Transmitter Serial Clock**—This signal provides the serial bit rate clock for the ESAI. SCKT is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode. **Port C 3**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SDO5 SDI0 PC6	Output Input Input, Output, or Disconnected	GPIO Disconnected	**Serial Data Output 5**—When programmed as a transmitter, SDO5 is used to transmit data from the TX5 serial transmit shift register. **Serial Data Input 0**—When programmed as a receiver, SDI0 is used to receive serial data into the RX0 serial receive shift register. **Port C 6**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.

Table 2-11 Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO4 SDI1 PC7	Output Input Input, Output, or Disconnected	GPIO Disconnected	**Serial Data Output 4**—When programmed as a transmitter, SDO4 is used to transmit data from the TX4 serial transmit shift register. **Serial Data Input 1**—When programmed as a receiver, SDI1 is used to receive serial data into the RX1 serial receive shift register. **Port C 7**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SDO3 SDI2 PC8	Output Input Input, Output, or Disconnected	GPIO Disconnected	**Serial Data Output 3**—When programmed as a transmitter, SDO3 is used to transmit data from the TX3 serial transmit shift register. **Serial Data Input 2**—When programmed as a receiver, SDI2 is used to receive serial data into the RX2 serial receive shift register. **Port C 8**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SDO2 SDI3 PC9	Output Input Input, Output, or Disconnected	GPIO Disconnected	**Serial Data Output 2**—When programmed as a transmitter, SDO2 is used to transmit data from the TX2 serial transmit shift register. **Serial Data Input 3**—When programmed as a receiver, SDI3 is used to receive serial data into the RX3 serial receive shift register. **Port C 9**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SDO1 PC10	Output Input, Output, or Disconnected	GPIO Disconnected	**Serial Data Output 1**—SDO1 is used to transmit data from the TX1 serial transmit shift register. **Port C 10**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SDO0 PC11	Output Input, Output, or Disconnected	GPIO Disconnected	**Serial Data Output 0**—SDO0 is used to transmit data from the TX0 serial transmit shift register. **Port C 11**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.

2.10 Digital Audio Interface (DAX)

Table 2-12 Digital Audio Interface (DAX) Signals

Signal Name	Type	State During Reset	Signal Description
ACI PD0	Input Input, Output, or Disconnected	Disconnected	**Audio Clock Input**—This is the DAX clock input. When programmed to use an external clock, this input supplies the DAX clock. The external clock frequency must be 256, 384, or 512 times the audio sampling frequency (256 × Fs, 384 × Fs or 512 × Fs, respectively). **Port D 0**—When the DAX is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
ADO PD1	Output Input, Output, or Disconnected	Disconnected	**Digital Audio Data Output**—This signal is an audio and non-audio output in the form of AES/EBU, CP340 and IEC958 data in a biphase mark format. **Port D 1**—When the DAX is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.

2.11 Timer

Table 2-13 Timer Signal

Signal Name	Type	State During Reset	Signal Description
TIO0	Input or Output	Input	**Timer 0 Schmitt-Trigger Input/Output**—When timer 0 functions as an external event counter or in measurement mode, TIO0 is used as input. When timer 0 functions in watchdog, timer, or pulse modulation mode, TIO0 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer 0 control/status register (TCSR0). If TIO0 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input but connected it to Vcc through a pull-up resistor in order to ensure a stable logic level at the input. This input is 5 V tolerant.

2.12 JTAG/OnCE Interface

Table 2-14 JTAG/OnCE™ Interface

Signal Name	Type	State During Reset	Signal Description
TCK	Input	Input	**Test Clock**—TCK is a test clock input signal used to synchronize the JTAG test logic. It has an internal pull-up resistor. This input is 5 V tolerant.
TDI	Input	Input	**Test Data Input**—TDI is a test data serial input signal used for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor. This input is 5 V tolerant.
TDO	Output	Tri-Stated	**Test Data Output**—TDO is a test data serial output signal used for test instructions and data. TDO can be tri-stated and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.
TMS	Input	Input	**Test Mode Select**—TMS is an input signal used to sequence the test controller's state machine. TMS is sampled on the rising edge of TCK and has an internal pull-up resistor. This input is 5 V tolerant.
$\overline{\text{TRST}}$	Input	Input	**Test Reset**—$\overline{\text{TRST}}$ is an active-low Schmitt-trigger input signal used to asynchronously initialize the test controller. $\overline{\text{TRST}}$ has an internal pull-up resistor. The use of $\overline{\text{TRST}}$ is not recommended for new designs. It is recommended to leave $\overline{\text{TRST}}$ disconnected. This input is 5 V tolerant.
$\overline{\text{DE}}$	Input/Output	Input	**Debug Event**—$\overline{\text{DE}}$ is an open-drain, bidirectional, active-low signal providing, as an input, a means of entering the debug mode of operation from an external command controller, and, as an output, a means of acknowledging that the chip has entered the debug mode. This signal, when asserted as an input, causes the DSP56300 core to finish the current instruction being executed, save the instruction pipeline information, enter the debug mode, and wait for commands to be entered from the debug serial input line. This signal is asserted as an output for three clock cycles when the chip enters the debug mode as a result of a debug request or as a result of meeting a breakpoint condition. The $\overline{\text{DE}}$ has an internal pull-up resistor. This is not a standard part of the JTAG TAP controller. The signal connects directly to the OnCE module to initiate debug mode directly or to provide a direct external indication that the chip has entered the debug mode. All other interface with the OnCE module must occur through the JTAG port. The use of $\overline{\text{DE}}$ is not recommended for new designs. It is recommended to leave $\overline{\text{DE}}$ disconnected. This input is **not** 5 V tolerant.

3 Specifications

3.1 Introduction

The DSP56362 is fabricated in high density CMOS with Transistor-Transistor Logic (TTL) compatible inputs and outputs. The DSP56362 specifications are preliminary and are from design simulations, and may not be fully tested or guaranteed. Finalized specifications will be published after full characterization and device qualifications are complete.

3.2 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are pulled to an appropriate logic voltage level (e.g., either GND or V_{CC}). The suggested value for a pullup or pulldown resistor is 10 kΩ.

NOTE

In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification will never occur in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 3-1 Maximum Ratings

Rating[1]	Symbol	Value[1, 2]	Unit
Supply Voltage	V_{CC}	−0.3 to +4.0	V
All input voltages excluding “5 V tolerant” inputs[3]	V_{IN}	GND −0.3 to V_{CC} + 0.3	V
All “5 V tolerant” input voltages[3]	V_{IN5}	GND −0.3 to V_{CC} + 3.95	V
Current drain per pin excluding V_{CC} and GND	I	10	mA

Table 3-1 Maximum Ratings (continued)

Rating[1]	Symbol	Value[1, 2]	Unit
Operating temperature range	T_J	–40 to +105	°C
Storage temperature	T_{STG}	–55 to +125	°C

1 GND = 0 V, V_{CC} = 3.3 V ± .16 V, T_J = 0°C to +100°C, C_L = 50 pF

2 Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.

3 **CAUTION**: All “5 V Tolerant” input voltages must not be more than 3.95 V greater than the supply voltage; this restriction applies to “power on”, as well as during normal operation. In any case, the input voltages cannot be more than 5.75 V. “5 V Tolerant” inputs are inputs that tolerate 5 V.

3.3 Thermal Characteristics

Table 3-2 Thermal Characteristics

Characteristic	Symbol	LQFP Value	Unit
Junction-to-ambient thermal resistance[1]	$R_{\theta JA}$ or θ_{JA}	45.3	°C/W
Junction-to-case thermal resistance[2]	$R_{\theta JC}$ or θ_{JC}	10.1	°C/W
Thermal characterization parameter	Ψ_{JT}	5.5	°C/W

1 Junction-to-ambient thermal resistance is based on measurements on a horizontal single-sided printed circuit board per SEMI G38-87 in natural convection.(SEMI is Semiconductor Equipment and Materials International, 805 East Middlefield Rd., Mountain View, CA 94043, (415) 964-5111.
Measurements were done with parts mounted on thermal test boards conforming to specification EIA/JESD51-3.

2 Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88, with the exception that the cold plate temperature is used for the case temperature.

3.4 DC Electrical Characteristics

Table 3-3 DC Electrical Characteristics[1]

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.14	3.3	3.46	V
Input high voltage • D(0:23), $\overline{BG}$, $\overline{BB}$, $\overline{TA}$, $\overline{DE}$, and PINIT/$\overline{NMI}$ • MOD[2]/$\overline{IRQ}$[2], $\overline{RESET}$, and TCK/TDI/TMS/$\overline{TRST}$/ESAI/Timer/HDI08/ SHI($_{SPI\ mode}$) pins • SHI($_{I2C\ mode}$) pins • EXTAL[3]	 V_{IH} V_{IHP} V_{IHX}	 2.0 2.0 1.5 0.8 × V_{CC}	 — — —	 V_{CC} V_{CC} + 3.95 V_{CC} + 3.95 V_{CC}	V
Input low voltage • D(0:23), $\overline{BG}$, $\overline{BB}$, $\overline{TA}$, MOD[2]/$\overline{IRQ}$[2], $\overline{RESET}$, PINIT/$\overline{NMI}$ • All JTAG/ESAI/Timer/HDI08/ SHI($_{SPI\ mode}$) pins • SHI($_{I2C\ mode}$) pins • EXTAL[3]	 V_{IL} V_{ILP} V_{ILX}	 –0.3 –0.3 –0.3 –0.3	 — — —	 0.8 0.8 0.3 × V_{CC} 0.2 × V_{CC}	V

Table 3-3 DC Electrical Characteristics[1] (continued)

Characteristics	Symbol	Min	Typ	Max	Unit
Input leakage current	I_{IN}	–10	—	10	μA
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I_{TSI}	–10	—	10	μA
Output high voltage • TTL (I_{OH} = –0.4 μA)[4, 5] • CMOS (I_{OH} = –10 μA)[4]	V_{OH}	 2.4 V_{CC} – 0.01	 — —	 —	V
Output low voltage • TTL (I_{OL} = 3.0 μA, open-drain pins I_{OL} = 6.7 μA)[4, 5] • CMOS (I_{OL} = 10 μA)[4]	V_{OL}	—	—	 0.4 0.01	V
Internal supply current[6] (Operating frequency 100MHz for current measurements) • In Normal mode • In Wait mode • In Stop mode[7]	 I_{CCI} I_{CCW} I_{CCS}	 — — —	 127 7. 5 100	 181 11 150	μA
PLL supply current		—	1	2.5	μA
Input capacitance[4]	C_{IN}	—	—	10	pF

1 V_{CC} = 3.3 V ± 5% V; T_J = 0°C to +100°C, C_L = 50 pF
2 Refers to MODA/$\overline{IRQA}$, MODB/$\overline{IRQB}$, MODC/$\overline{IRQC}$, and MODD/$\overline{IRQD}$ pins.
3 Driving EXTAL to the low V_{IHX} or the high V_{ILX} value may cause additional power consumption (DC current). To minimize power consumption, the minimum V_{IHX} should be no lower than 0.9 V_{CC} and the maximum V_{ILX} should be no higher than 0.1 V_{CC}.
4 Periodically sampled and not 100% tested.
5 This characteristic does not apply to PCAP.
6 Section 5.3, "Power Consumption Considerations" provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). Measurements are based on synthetic intensive DSP benchmarks. The power consumption numbers in this specification are 90% of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CC} = 3.3 V at T_J = 100°C. Maximum internal supply current is measured with V_{CC} = 3.46 V at T_J = 100°C.
7 In order to obtain these results, all inputs, which are not disconnected at Stop mode, must be terminated (i.e., not allowed to float).

3.5 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.3 V and a V_{IH} minimum of 2.4 V for all pins except EXTAL, which is tested using the input levels shown in Note 6 of the previous table. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. DSP56362 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.4 V and 2.4 V, respectively.

NOTE

Although the minimum value for the frequency of EXTAL is 0 MHz, the device AC test conditions are 15 MHz and rated speed.

3.6 Internal Clocks

Table 3-4 Internal Clocks, CLKOUT

Characteristics	Symbol	Expression[1, 2]		
		Min	Typ	Max
Internal operation frequency and CLKOUT with PLL enabled	f	—	$(Ef \times MF)/(PDF \times DF)$	—
Internal operation frequency and CLKOUT with PLL disabled	f	—	Ef/2	—
Internal clock and CLKOUT high period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_H	— $0.49 \times ET_C \times PDF \times DF/MF$ $0.47 \times ET_C \times PDF \times DF/MF$	ET_C — —	— $0.51 \times ET_C \times PDF \times DF/MF$ $0.53 \times ET_C \times PDF \times DF/MF$
Internal clock and CLKOUT low period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_L	— $0.49 \times ET_C \times PDF \times DF/MF$ $0.47 \times ET_C \times PDF \times DF/MF$	ET_C — —	— $0.51 \times ET_C \times PDF \times DF/MF$ $0.53 \times ET_C \times PDF \times DF/MF$
Internal clock and CLKOUT cycle time with PLL enabled	T_C	—	$ET_C \times PDF \times DF/MF$	—
Internal clock and CLKOUT cycle time with PLL disabled	T_C	—	$2 \times ET_C$	—
Instruction cycle time	I_{CYC}	—	T_C	—

[1] DF = Division Factor
Ef = External frequency
ET_C = External clock cycle
MF = Multiplication Factor
PDF = Predivision Factor
T_C = internal clock cycle

[2] See the PLL and Clock Generation section in the *DSP56300 Family Manual* for a detailed discussion of the PLL.

3.7 EXTERNAL CLOCK OPERATION

The DSP56362 system clock is an externally supplied square wave voltage source connected to EXTAL (Figure 3-1).

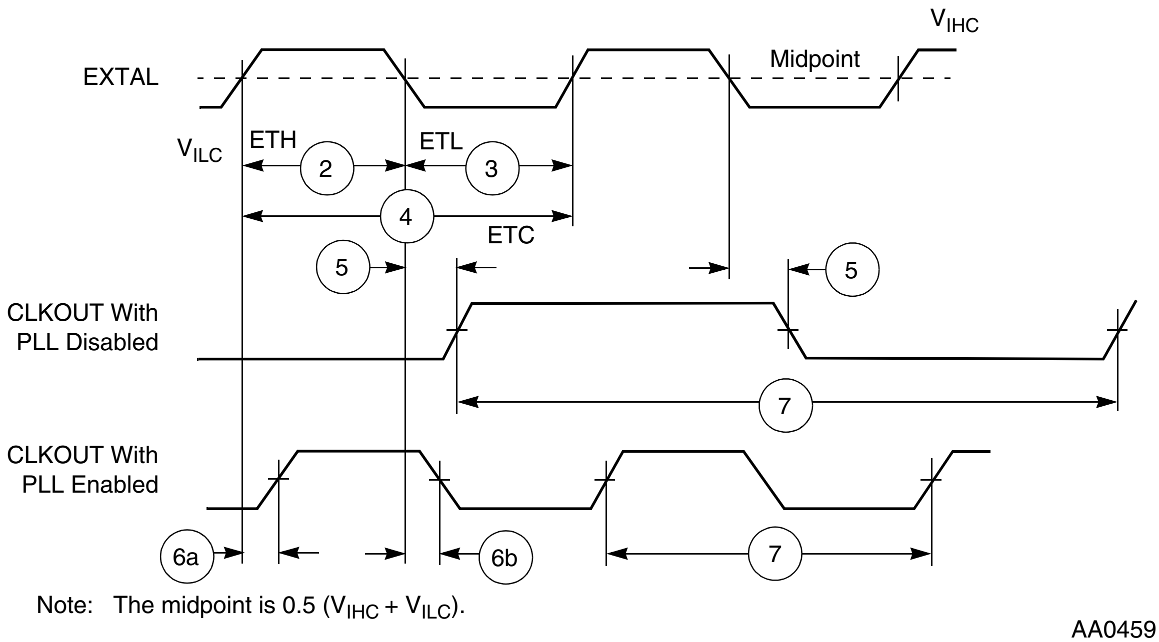


Figure 3-1 External Clock Timing

Table 3-5 Clock Operation 100 and 120 MHz Values

No.	Characteristics	Symbol	100 MHz		120 MHz	
			Min	Max	Min	Max
1	Frequency of EXTAL (EXTAL Pin Frequency) The rise and fall time of this external clock should be 3 ns maximum.	Ef	0	100.0	0	120.0
2	EXTAL input high[1, 2] • With PLL disabled (46.7%–53.3% duty cycle)[3] • With PLL enabled (42.5%–57.5% duty cycle)[3]	ET_H	 4.67 ns 4.25 ns	 ∞ 157.0 µs	 0.00 ns 0.00 ns	 ∞ 157.0 µs
3	EXTAL input low[1, 2] • With PLL disabled (46.7%–53.3% duty cycle)[3] • With PLL enabled (42.5%–57.5% duty cycle)[3]	ET_L	 4.67 ns 4.25 ns	 ∞ 157.0 µs	 4.67 ns 4.25 ns	 — 1570.00
4	EXTAL cycle time[2] • With PLL disabled • With PLL enabled	ET_C	 10.00 ns 10.00 ns	 ∞ 273.1 µs	 8.33 ns 8.33 ns	 — 273.1 µs
5	CLKOUT change from EXTAL fall with PLL disabled		4.3 ns	11.0 ns		

Table 3-5 Clock Operation (continued) 100 and 120 MHz Values

No.	Characteristics	Symbol	100 MHz		120 MHz	
			Min	Max	Min	Max
6	CLKOUT rising edge from EXTAL rising edge with PLL enabled (MF = 1, PDF = 1, Ef > 15 MHz)[4, 5]		0.0 ns	1.8 ns		
	CLKOUT falling edge from EXTAL rising edge with PLL enabled (MF = 2 or 4, PDF = 1, Ef > 15 MHz)[4, 5]		0.0 ns	1.8 ns		
	CLKOUT falling edge from EXTAL falling edge with PLL enabled (MF ≤ 4, PDF ≠ 1, Ef / PDF > 15 MHz)[4, 5]		0.0 ns	1.8 ns		
7	Instruction cycle time = I_{CYC} = T_C[6] See Table 3-5 (46.7%–53.3% duty cycle)	I_{CYC}				
	• With PLL disabled		0.00 ns	∞		
	• With PLL enabled		0.00 ns	8.53 µs		8.53 µs

1 Measured at 50% of the input transition.
2 The maximum value for PLL enabled is given for minimum V_{CO} and maximum MF.
3 The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correction operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.
4 Periodically sampled and not 100% tested.
5 The skew is not guaranteed for any other MF value.
6 The maximum value for PLL enabled is given for minimum V_{CO} and maximum DF.

3.8 Phase Lock Loop (PLL) Characteristics

Table 3-6 PLL Characteristics

Characteristics	100 MHz		Unit
	Min	Max	
V_{CO} frequency when PLL enabled (MF × E_f × 2/PDF)	30	200	MHz
PLL external capacitor (PCAP pin to V_{CCP}) (C_{PCAP})[1]			
• @ MF ≤ 4	(MF × 580) – 100	(MF × 780) – 140	pF
• @ MF > 4	MF × 830	MF × 1470	pF
Note:			

1 C_{PCAP} is the value of the PLL capacitor (connected between the PCAP pin and V_{CCP}). The recommended value in pF for C_{PCAP} can be computed from one of the following equations:
(680 × MF) – 120, for MF ≤ 4, or
1100 × MF, for MF > 4

3.9 Reset, Stop, Mode Select, and Interrupt Timing

Table 3-7 Reset, Stop, Mode Select, and Interrupt Timing 100 and 120 MHz Values[1]

No	Characteristics	Expression[2]	100 MHz		120 MHz		Unit
			Min	Max	Min	Max	
8	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[3]	—	—	26.0		26.0	ns
9	Required $\overline{\text{RESET}}$ duration[4]						
	• Power on, external clock generator, PLL disabled	$50 \times ET_C$	500.0	—	416.7	—	ns
	• Power on, external clock generator, PLL enabled	$1000 \times ET_C$	10.0	—	8.3	—	µs
	• Power on, internal oscillator	$75000 \times ET_C$	750	—	625	—	µs
	• During STOP, XTAL disabled (PCTL Bit 16 = 0)	$75000 \times ET_C$	750	—	625	—	µs
	• During STOP, XTAL enabled (PCTL Bit 16 = 1)	$2.5 \times T_C$	25.0	—	20.8	—	ns
	• During normal operation	$2.5 \times T_C$	25.0	—	20.8	—	ns
10	Delay from asynchronous $\overline{\text{RESET}}$ deassertion to first external address output (internal reset deassertion)[5]						
	• Minimum	$3.25 \times T_C + 2.0$	34.5	—	29.1		ns
	• Maximum	$20.25\ T_C + 7.50$	—	211.5		176.2	ns
11	Synchronous reset setup time from $\overline{\text{RESET}}$ deassertion to CLKOUT Transition 1						
	• Minimum	T_C	5.9	—			ns
	• Maximum		—	10.0			ns
12	Synchronous reset deasserted, delay time from the CLKOUT Transition 1 to the first external address output						
	• Minimum	$3.25 \times T_C + 2.0$	33.5	—			ns
	• Maximum	$20.25\ T_C + 7.5$	—	207.5			ns
13	Mode select setup time		30.0	—	30.0		ns
14	Mode select hold time		0.0	—	0.0		ns
15	Minimum edge-triggered interrupt request assertion width		6.6	—	5.5		ns
16	Minimum edge-triggered interrupt request deassertion width		6.6	—	5.5		ns
17	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory access address out valid						
	• Caused by first interrupt instruction fetch	$4.25 \times T_C + 2.0$	44.5	—	37.4		ns
	• Caused by first interrupt instruction execution	$7.25 \times T_C + 2.0$	74.5	—	62.4		ns
18	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution	$10 \times T_C + 5.0$	105.0	—	88.3		ns

Table 3-7 Reset, Stop, Mode Select, and Interrupt Timing 100 and 120 MHz Values[1] (continued)

No	Characteristics	Expression[2]	100 MHz		120 MHz		Unit
			Min	Max	Min	Max	
19	Delay from address output valid caused by first interrupt instruction execute to interrupt request deassertion for level sensitive fast interrupts[6]	$(3.75 + WS) \times T_C - 10.94$	—	Note[7]	—	Note 7	ns
20	Delay from $\overline{RD}$ assertion to interrupt request deassertion for level sensitive fast interrupts[6]	$(3.25 + WS) \times T_C - 10.94$	—	Note 7	—	Note 7	
21	Delay from $\overline{WR}$ assertion to interrupt request deassertion for level sensitive fast interrupts[6 8]						
	• DRAM for all WS	$(WS + 3.5) \times T_C - 10.94$	—	Note 7	—	Note 7	ns
	• SRAM WS =1	$(WS + 3.5) \times T_C - 10.94$	—	Note 7	—	Note 7	ns
	• SRAM WS=2, 3	$1.75 \times T_C - 4.0$	—	Note 7	—	Note 7	ns
	• SRAM WS ≥ 4	$2.75 \times T_C - 4.0$	—	Note 7	—	Note 7	ns
22	Synchronous interrupt setup time from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{NMI}$ assertion to the CLKOUT Transition 2	$0.6 \times T_C - 0.1$	5.9		4.9	—	ns
23	Synchronous interrupt delay time from the CLKOUT Transition 2 to the first external address output valid caused by the first instruction fetch after coming out of Wait Processing state						
	• Minimum	$9.25 \times T_C + 1.0$	93.5	—	78.1	—	ns
	• Maximum	$24.75 \times T_C + 5.0$	—	252.5	—	211.2	ns
24	Duration for $\overline{IRQA}$ assertion to recover from Stop state	$0.6 \times T_C - 0.1$	5.9	—	4.9	—	ns
25	Delay from $\overline{IRQA}$ assertion to fetch of first instruction (when exiting Stop)[9, 3]						
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (OMR Bit 6 = 0)	$PLC \times ET_C \times PDF + (128\ K - PLC/2) \times T_C$	1.3	13.6	—	—	ms
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (OMR Bit 6 = 1)	$PLC \times ET_C \times PDF + (23.75 \pm 0.5) \times T_C$	232.5 ns	12.3 ms	—	—	
	• PLL is active during Stop (PCTL Bit 17 = 1) (Implies No Stop Delay)	$(8.25 \pm 0.5) \times T_C$	77.5	87.5	64.6	72.9	ns
26	Duration of level sensitive $\overline{IRQA}$ assertion to ensure interrupt service (when exiting Stop)[9, 3]						
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (OMR Bit 6 = 0)	$PLC \times ET_C \times PDF + (128K - PLC/2) \times T_C$	13.6	—			ms
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (OMR Bit 6 = 1)	$PLC \times ET_C \times PDF + (20.5 \pm 0.5) \times T_C$	12.3	—			ms
	• PLL is active during Stop (PCTL Bit 17 = 1) (implies no Stop delay)	$5.5 \times T_C$	55.0	—	45.8	—	ns

Table 3-7 Reset, Stop, Mode Select, and Interrupt Timing 100 and 120 MHz Values[1] (continued)

No	Characteristics	Expression[2]	100 MHz		120 MHz		Unit
			Min	Max	Min	Max	
27	Interrupt Requests Rate						
	• HI08, ESAI, SHI, Timer	$12T_C$	—	120.0	—	100.0	ns
	• DMA	$8T_C$	—	80.0	—	66.7	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	$8T_C$	—	80.0	—	66.7	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (level trigger)	$12T_C$	—	120.0	—	100.0	ns
28	DMA Requests Rate						
	• Data read from HI08, ESAI, SHI	$6T_C$	—	60.0	—	50.0	ns
	• Data write to HI08, ESAI, SHI	$7T_C$	—	70.0	—	58.0	ns
	• Timer	$2T_C$	—	20.0	—	16.7	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	$3T_C$	—	30.0	—	25.0	ns
29	Delay from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{NMI}$ assertion to external memory (DMA source) access address out valid	$4.25 \times T_C + 2.0$	44.0	—	37.4	—	ns

1 $V_{CC} = 3.3\ V \pm 0.16\ V$; $T_J = 0°C$ to $+100°C$, $C_L = 50\ pF$
2 Use expression to compute maximum value.
3 Periodically sampled and not 100% tested.
4 For an external clock generator, $\overline{RESET}$ duration is measured during the time in which $\overline{RESET}$ is asserted, V_{CC} is valid, and the EXTAL input is active and valid. For internal oscillator, $\overline{RESET}$ duration is measured during the time in which $\overline{RESET}$ is asserted and V_{CC} is valid. The specified timing reflects the crystal oscillator stabilization time after power-up. This number is affected both by the specifications of the crystal and other components connected to the oscillator and reflects worst case conditions. When the V_{CC} is valid, but the other “required $\overline{RESET}$ duration” conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.
5 If PLL does not lose lock.
6 When using fast interrupts and $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, and $\overline{IRQD}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.
7 These values depend on the number of wait states (WS) selected.
8 WS = number of wait states (measured in clock cycles, number of T_C.
9 This timing depends on several settings: For PLL disable, using internal oscillator (PLL Control Register (PCTL) Bit 16 = 0) and oscillator disabled during Stop (PCTL Bit 17 = 0), a stabilization delay is required to assure the oscillator is stable before executing programs. In that case, resetting the Stop delay (OMR Bit 6 = 0) will provide the proper delay. While it is possible to set OMR Bit 6 = 1, it is not recommended and these specifications do not guarantee timings for that case.

For PLL disable, using internal oscillator (PCTL Bit 16 = 0) and oscillator enabled during Stop (PCTL Bit 17=1), no stabilization delay is required and recovery time will be minimal (OMR Bit 6 setting is ignored).

For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time will be defined by the PCTL Bit 17 and OMR Bit 6 settings.

For PLL enable, if PCTL Bit 17 is 0, the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0 to 1000 cycles. This procedure occurs in parallel with the stop delay counter, and stop recovery will end when the last of these two events occurs. The stop delay counter completes count or PLL lock procedure completion. PLC value for PLL disable is 0.

The maximum value for ET_C is 4096 (maximum MF) divided by the desired internal frequency (i.e., for 100 MHz it is 4096/100 MHz = 40.96μs). During the stabilization period, T_C, T_H, and T_L will not be constant, and their width may vary, so timing may vary as well.

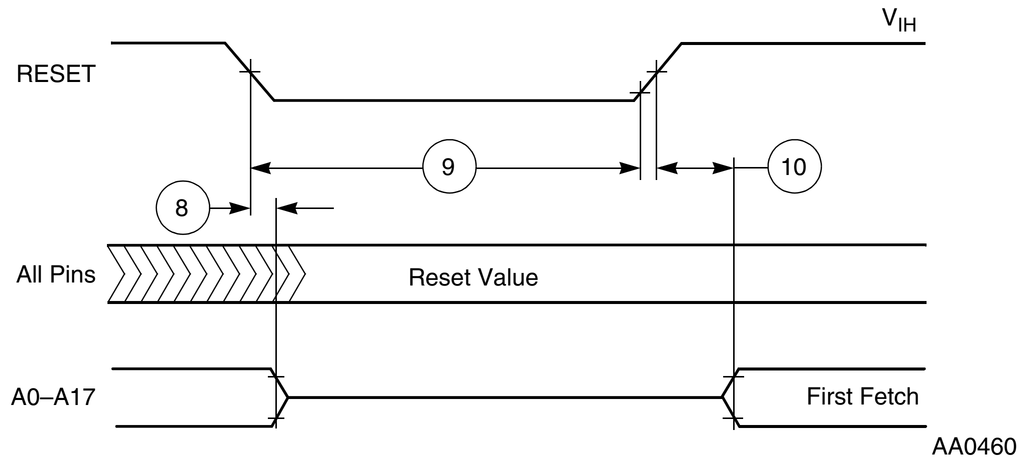


Figure 3-2 Reset Timing

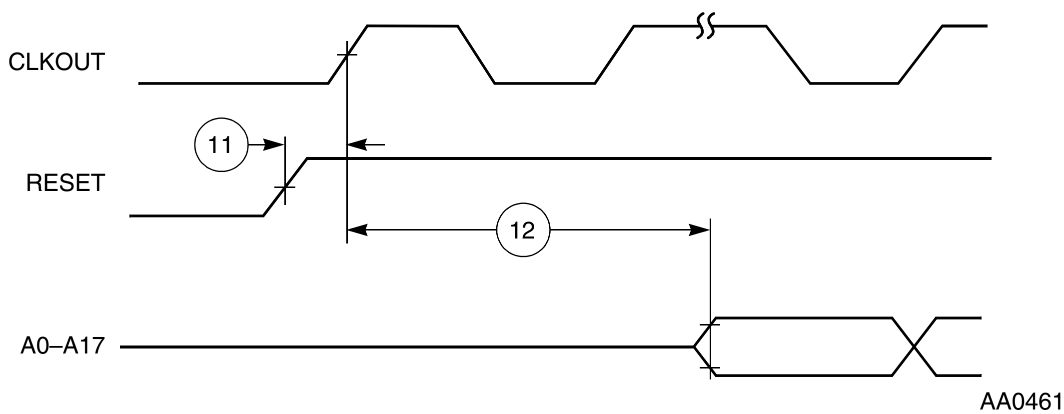


Figure 3-3 Synchronous Reset Timing

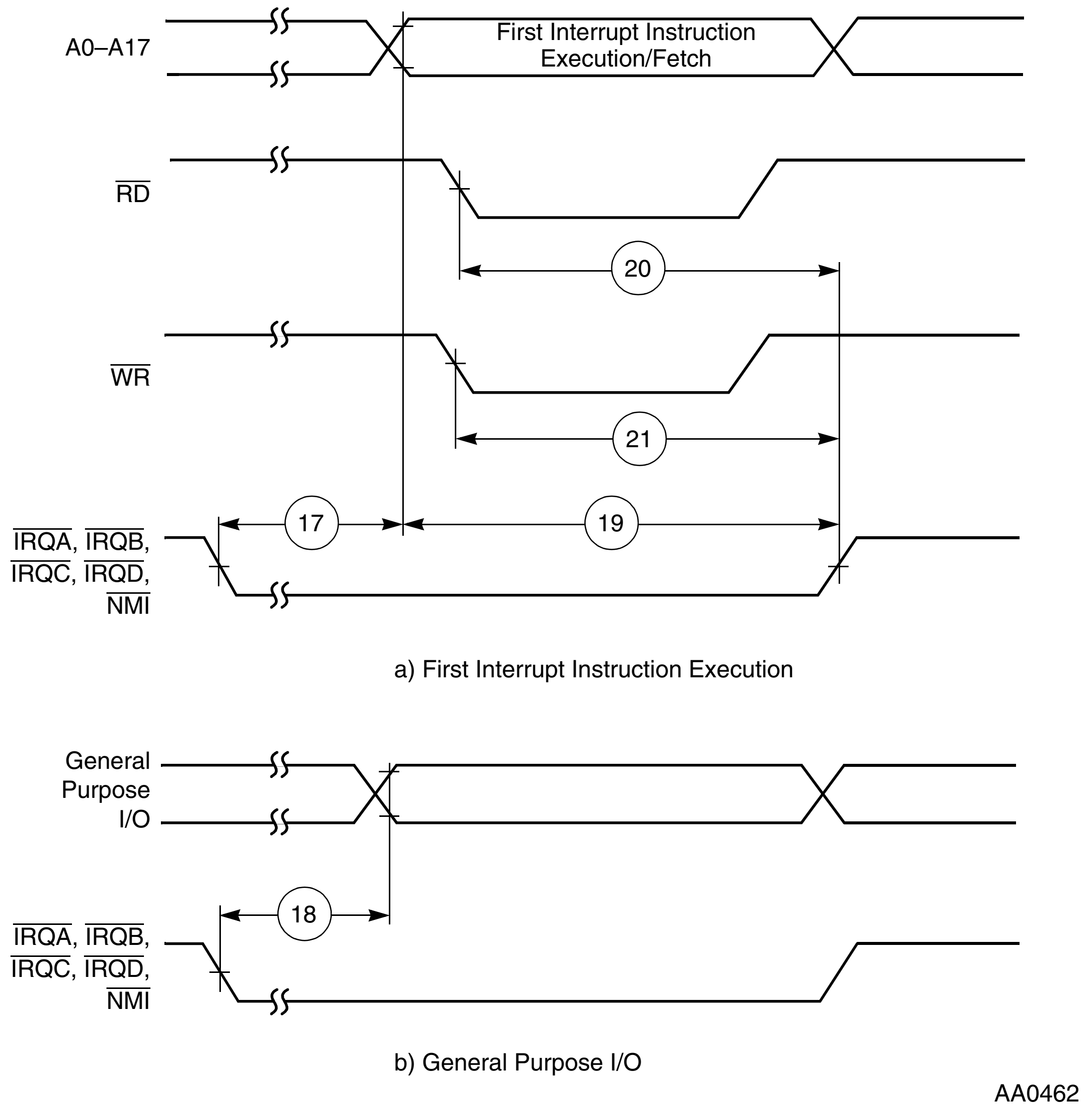


Figure 3-4 External Fast Interrupt Timing

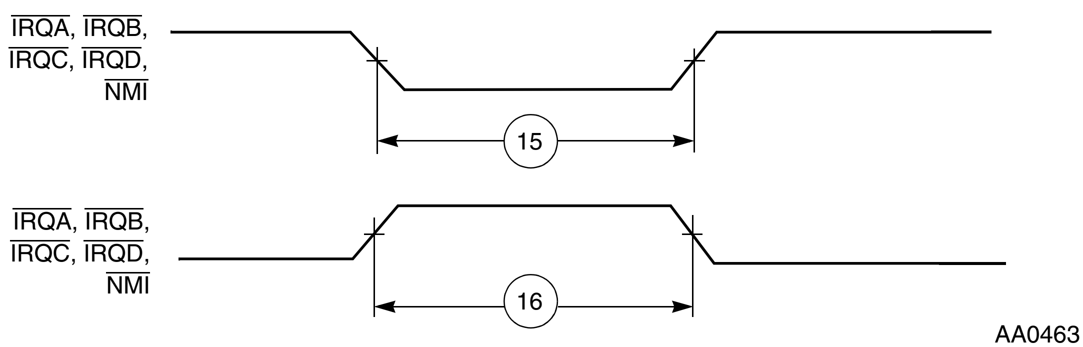


Figure 3-5 External Interrupt Timing (Negative Edge-Triggered)

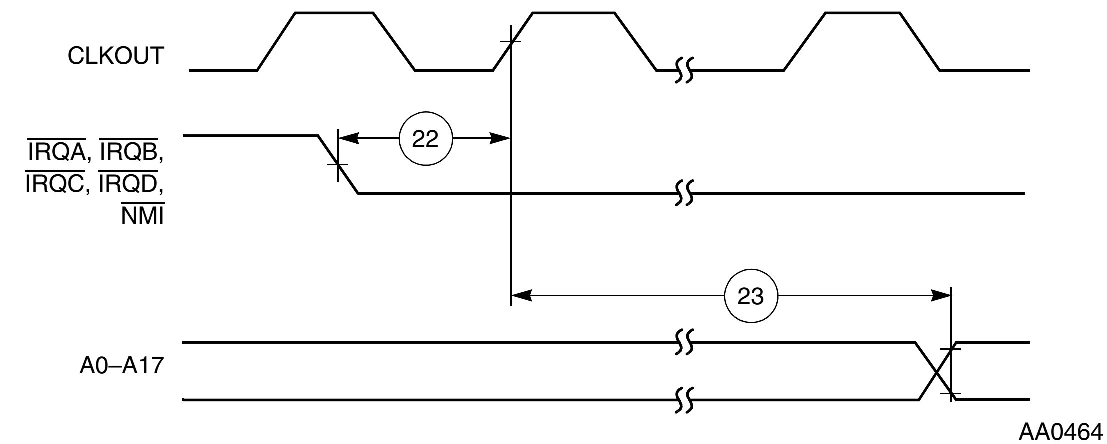


Figure 3-6 Synchronous Interrupt from Wait State Timing

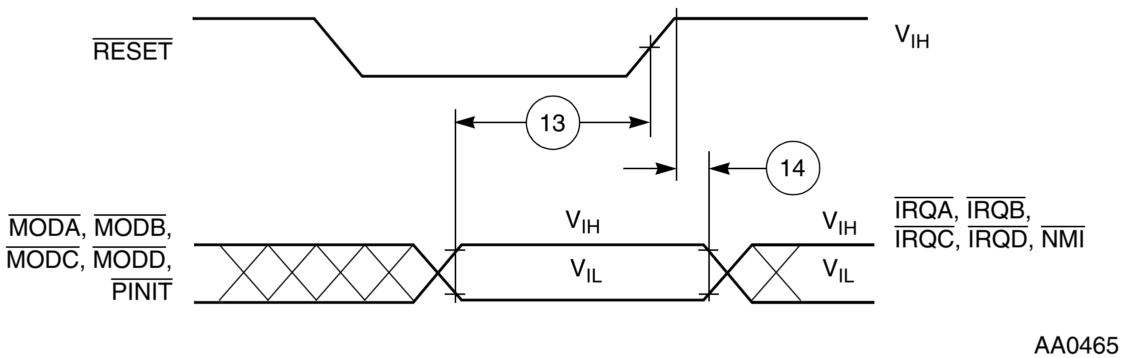


Figure 3-7 Operating Mode Select Timing

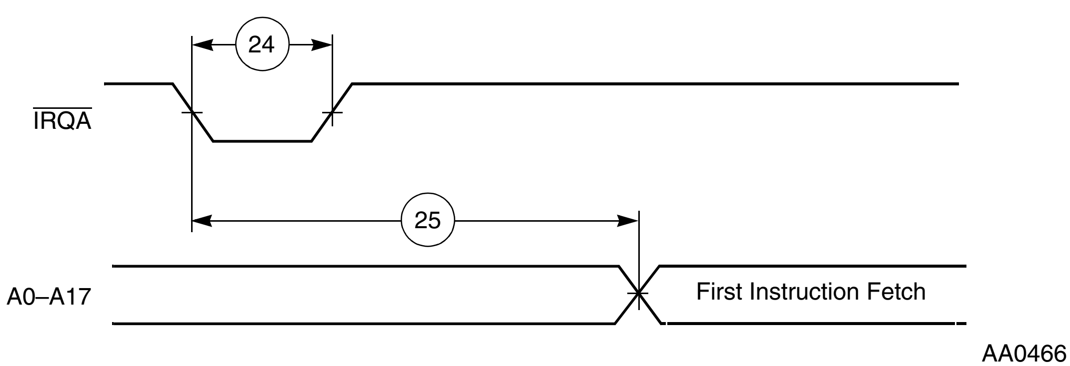


Figure 3-8 Recovery from Stop State Using IRQA

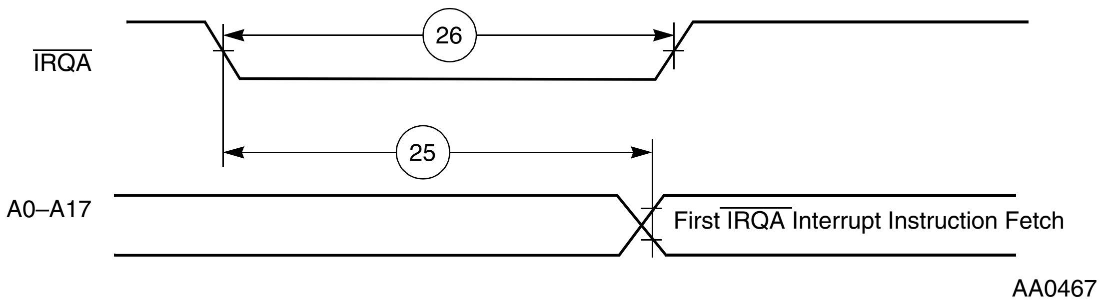


Figure 3-9 Recovery from Stop State Using IRQA Interrupt Service

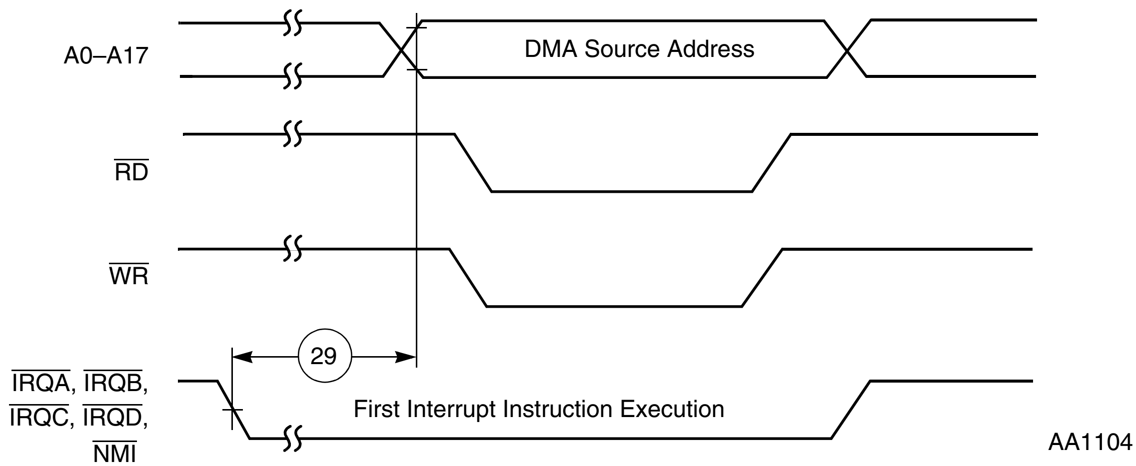


Figure 3-10 External Memory Access (DMA Source) Timing

3.10 External Memory Expansion Port (Port A)

3.10.1 SRAM Timing

Table 3-8 SRAM Read and Write Accesses 100 and 120 MHz[1]

No.	Characteristics	Symbol	Expression[2]	100 MHz		120 MHz		Unit
				Min	Max	Min	Max	
100	Address valid and AA assertion pulse width[3]	t_{RC}, t_{WC}	$(WS + 1) \times T_C - 4.0$ $[1 \leq WS \leq 3]$	16.0	—	12.0	—	ns
			$(WS + 2) \times T_C - 4.0$ $[4 \leq WS \leq 7]$	56.0	—	46.0	—	ns
			$(WS + 3) \times T_C - 4.0$ $[WS \geq 8]$	106.0	—	87.0	—	ns
101	Address and AA valid to $\overline{WR}$ assertion	t_{AS}	**100 MHz:** $0.25 \times T_C - 2.0$ $[WS = 1]$	0.5	—	0.1	—	ns
			$1.25 \times T_C - 2.0$ $[WS \geq 4]$	10.5	—	8.4	—	ns
102	$\overline{WR}$ assertion pulse width	t_{WP}	**100 MHz:** $1.5 \times T_C - 4.0$ $[WS = 1]$	11.0	—	8.5	—	ns
			All frequencies: $WS \times T_C - 4.0$ $[2 \leq WS \leq 3]$	16.0	—	12.7	—	ns
			$(WS - 0.5) \times T_C - 4.0$ $[WS \geq 4]$	31.0	---	25.2	—	
103	$\overline{WR}$ deassertion to address not valid	t_{WR}	**100 MHz:** $0.25 \times T_C - 2.0$ $[1 \leq WS \leq 3]$	0.5	—	0.1	—	ns
			$1.25 \times T_C - 2.0$ $[4 \leq WS \leq 7]$	10.5	—	8.4	—	
			$2.25 \times T_C - 2.0$ $[WS \geq 8]$	20.5	—	16.7	—	
			All frequencies: $1.25 \times T_C - 4.0$ $[4 \leq WS \leq 7]$	8.5	—	6.4	—	
			$2.25 \times T_C - 4.0$ $[WS \geq 8]$	18.5	—	14.7	—	

Table 3-8 SRAM Read and Write Accesses 100 and 120 MHz[1] (continued)

No.	Characteristics	Symbol	Expression[2]	100 MHz		120 MHz		Unit
				Min	Max	Min	Max	
104	Address and AA valid to input data valid	t_{AA}, t_{AC}	**100 MHz:** $(WS + 0.75) \times T_C - 7.0$ $[WS \geq 1]$	—	10.5		7.6	ns
105	$\overline{RD}$ assertion to input data valid	t_{OE}	**100 MHz:** $(WS + 0.25) \times T_C - 7.0$ $[WS \geq 1]$	—	5.5	—	3.4	ns
106	$\overline{RD}$ deassertion to data not valid (data hold time)	t_{OHZ}		0.0	—	0.0	—	ns
107	Address valid to $\overline{WR}$ deassertion[3]	t_{AW}	$(WS + 0.75) \times T_C - 4.0$ $[WS \geq 1]$	13.5	—	10.6	—	ns
108	Data valid to $\overline{WR}$ deassertion (data setup time)	t_{DS} (t_{DW})	**100 MHz:** $(WS - 0.25) \times T_C - 3.0$ $[WS \geq 1]$	4.5	—	3.2	—	ns
109	Data hold time from $\overline{WR}$ deassertion	t_{DH}	**100 MHz:** $0.25 \times T_C - 2.0$ $[1 \leq WS \leq 3]$	0.5	—	0.1	—	ns
			$1.25 \times T_C - 2.0$ $[4 \leq WS \leq 7]$	10.5	—	8.4	—	
			$2.25 \times T_C - 2.0$ $[WS \geq 8]$	20.5	—	16.7	—	
110	$\overline{WR}$ assertion to data active[4]		$0.75 \times T_C - 3.7$ $[WS = 1]$	—	—	2.5	—	ns
			$0.25 \times T_C - 3.7$ $[2 \leq WS \leq 3]$	—	—	0.0	—	
			$-0.25 \times T_C - 3.7$ $[WS \geq 4]$	—	—	0.0	—	
111	$\overline{WR}$ deassertion to data high impedance[4]		$0.25 \times T_C + 0.2$ $[1 \leq WS \leq 3]$	—	—	—	2.3	ns
			$1.25 \times T_C + 0.2$ $[4 \leq WS \leq 7]$	—	—	—	10.6	
			$2.25 \times T_C + 0.2$ $[WS \geq 8]$	—	—	—	18.9	

Table 3-8 SRAM Read and Write Accesses 100 and 120 MHz[1] (continued)

No.	Characteristics	Symbol	Expression[2]	100 MHz		120 MHz		Unit
				Min	Max	Min	Max	
112	Previous $\overline{RD}$ deassertion to data active (write)[4]		$1.25 \times T_C - 4.0$ [$1 \le WS \le 3$]	—	—	6.4	—	ns
			$2.25 \times T_C - 4.0$ [$4 \le WS \le 7$]	—	—	14.7	—	
			$3.25 \times T_C - 4.0$ [$WS \ge 8$]	—	—	23.1	—	
113	$\overline{RD}$ deassertion time		**100 MHz:** $0.75 \times T_C - 4.0$ [$1 \le WS \le 3$]	3.5	—	2.2	—	ns
			$1.75 \times T_C - 4.0$ [$4 \le WS \le 7$]	13.5	—	10.6	—	
			$2.75 \times T_C - 4.0$ [$WS \ge 8$]	23.5	—	18.9	—	
114	$\overline{WR}$ deassertion time		**100 MHz:** $0.5 \times T_C - 4.0$ [$WS = 1$]	1.0	—	0.2	—	ns
			$T_C - 2.0$ [$2 \le WS \le 3$]	6.0	—	6.3	—	
			$2.5 \times T_C - 4.0$ [$4 \le WS \le 7$]	21.0	—	16.8	—	
			$3.5 \times T_C - 4.0$ [$WS \ge 8$]	31.0	—	25.2	—	
115	Address valid to $\overline{RD}$ assertion		**100 MHz:** $0.5 \times T_C - 4.0$	1.0	—	0.2	—	ns
116	$\overline{RD}$ assertion pulse width		**100 MHz:** $(WS + 0.25) \times T_C - 4.0$	8.5	—	6.4	—	ns
117	$\overline{RD}$ deassertion to address not valid		**100 MHz:** $0.25 \times T_C - 2.0$ [$1 \le WS \le 3$]	0.5	—	0.1	—	ns
			$1.25 \times T_C - 2.0$ [$4 \le WS \le 7$]	10.5	—	8.4	—	
			$2.25 \times T_C - 2.0$ [$WS \ge 8$]	20.5	—	16.7	—	

Table 3-8 SRAM Read and Write Accesses 100 and 120 MHz[1] (continued)

No.	Characteristics	Symbol	Expression[2]	100 MHz		120 MHz		Unit
				Min	Max	Min	Max	
118	$\overline{TA}$ setup before $\overline{RD}$ or $\overline{WR}$ deassertion[5]		$0.25 \times T_C + 2.0$	4.5	—	4.1	—	ns
119	$\overline{TA}$ hold after $\overline{RD}$ or $\overline{WR}$ deassertion			0	—	0.0	—	ns

1 All timings for 100 MHz are measured from 0.5 Vcc to .05 Vcc
2 WS is the number of wait states specified in the BCR.
3 Timings 100, 107 are guaranteed by design, not tested.
4 Timing 110, 111, and 112, are not specified for 100 MHz.
5 In the case of $\overline{TA}$ negation: timing 118 is relative to the deassertion edge of $\overline{RD}$ or WR were $\overline{TA}$ to remain active.

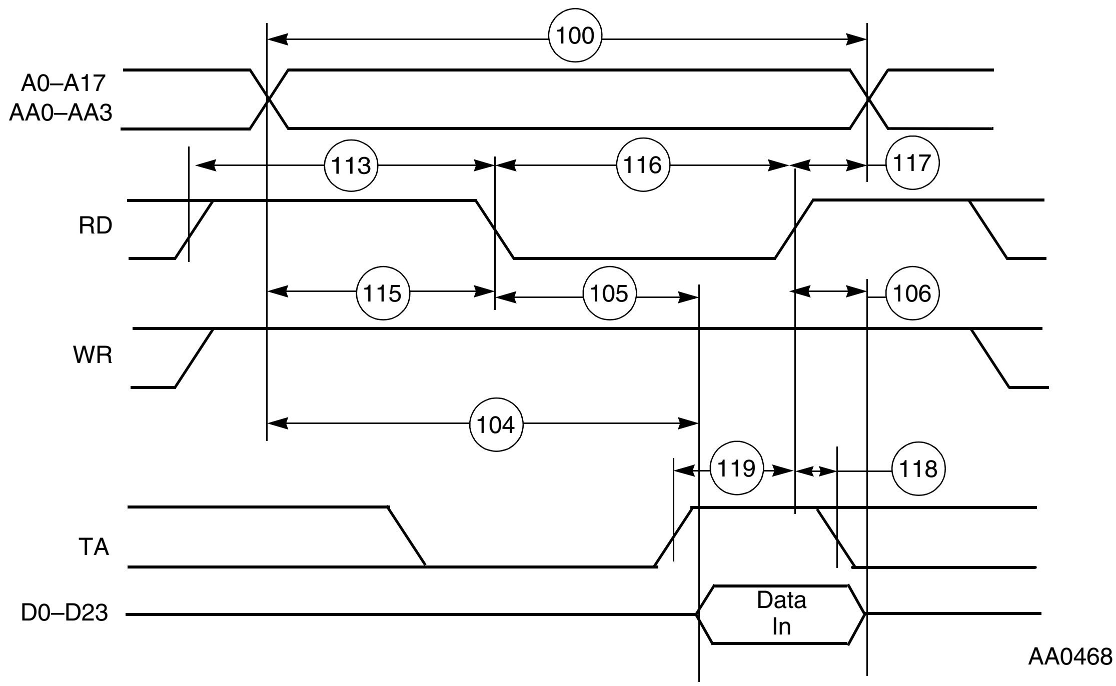


Figure 3-11 SRAM Read Access

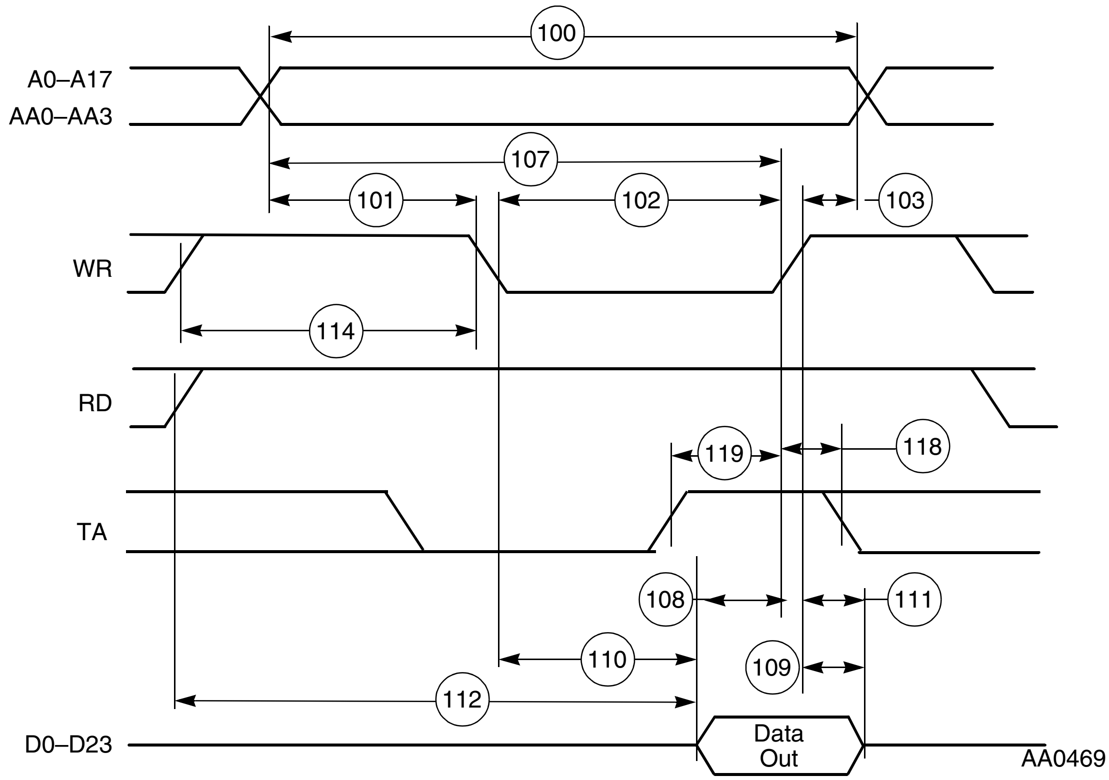


Figure 3-12 SRAM Write Access

3.10.2 DRAM Timing

The selection guides provided in Figure 3-13 and Figure 3-16 should be used for primary selection only. Final selection should be based on the timing provided in the following tables. As an example, the selection guide suggests that 4 wait states must be used for 100 MHz operation when using Page Mode DRAM. However, by using the information in the appropriate table, a designer may choose to evaluate whether fewer wait states might be used by determining which timing prevents operation at 100 MHz, running the chip at a slightly lower frequency (e.g., 95 MHz), using faster DRAM (if it becomes available), and control factors such as capacitive and resistive load to improve overall system performance.

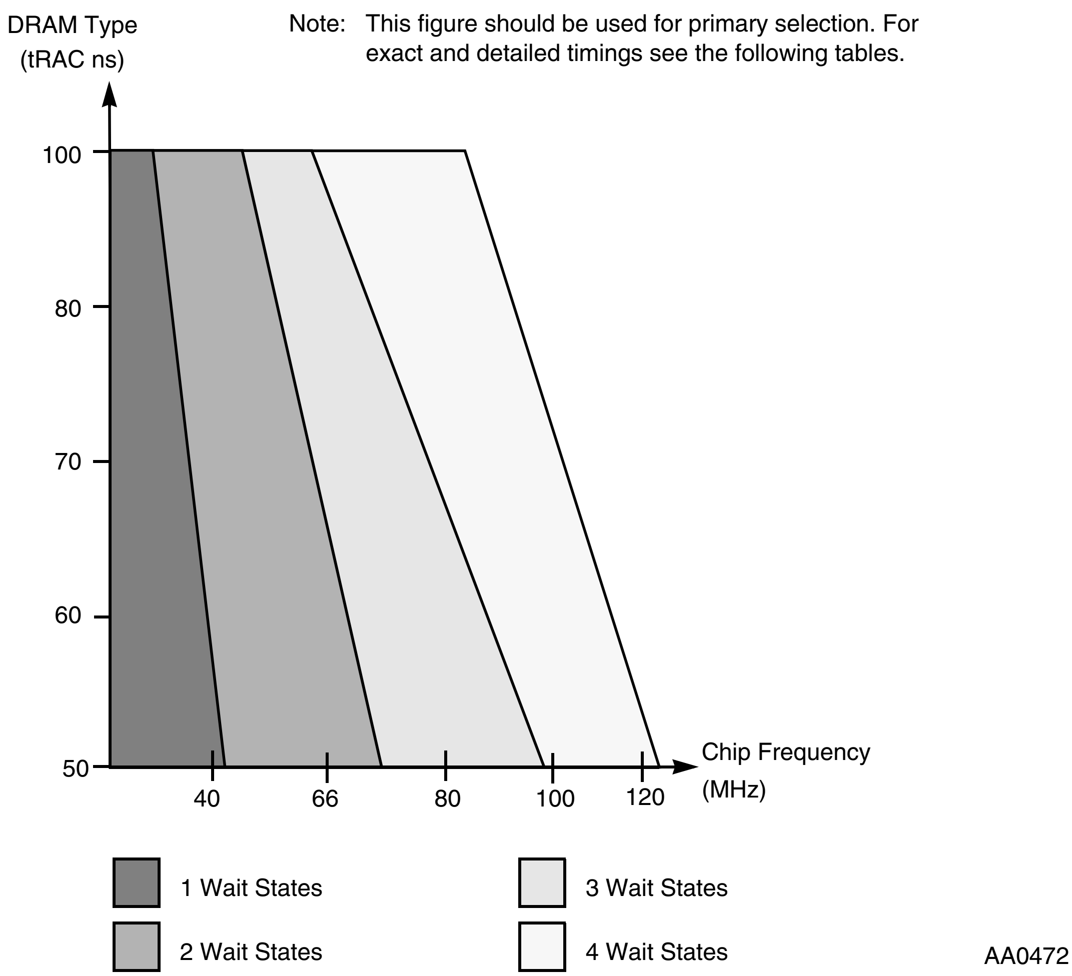


Figure 3-13 DRAM Page Mode Wait States Selection Guide

Table 3-9 DRAM Page Mode Timings, One Wait State (Low-Power Applications)[1, 2, 3]

No.	Characteristics	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
131	Page mode cycle time for two consecutive accesses of the same direction Page mode cycle time for mixed (read and write) accesses.	t_{PC}	$2 \times T_C$ 1.25 x Tc	100.0 62.5	— —	66.7 41.7	— —	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$T_C - 7.5$	—	42.5	—	25.8	ns
133	Column address valid to data valid (read)	t_{AA}	$1.5 \times T_C - 7.5$	—	67.5	—	42.5	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$2 \times T_C - 4.0$	96.0	—	62.7	—	ns

Table 3-9 DRAM Page Mode Timings, One Wait State (Low-Power Applications)[1, 2, 3] (continued)

No.	Characteristics	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion[5]	t_{CRP}						ns
	• BRW[1:0] = 00		$1.75 \times T_C - 6.0$	81.5	—	52.3	—	
	• BRW[1:0] = 01		$3.25 \times T_C - 6.0$	156.5	—	102.2	—	
	• BRW[1:0] = 10		$4.25 \times T_C - 6.0$	206.5	—	135.5	—	
	• BRW[1:0] = 11		$6.25 \times T_C - 6.0$	306.5	—	202.1	—	
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$0.5 \times T_C - 4.0$	21.0	—	12.7	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.5 \times T_C - 4.0$	21.0	—	12.7	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$2 \times T_C - 4.0$	96.0	—	62.7	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$0.75 \times T_C - 3.8$	33.7	—	21.2	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.25 \times T_C - 3.7$	8.8	—	4.6	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$0.5 \times T_C - 4.2$	20.8	—	12.5	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$1.5 \times T_C - 4.5$	70.5	—	45.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$1.75 \times T_C - 4.3$	83.2	—	54.0	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$1.75 \times T_C - 4.3$	83.2	—	54.0	—	ns
149	Data valid to $\overline{CAS}$ assertion (Write)	t_{DS}	$0.25 \times T_C - 4.0$	8.5	—	4.3	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$T_C - 4.3$	45.7	—	29.0	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$1.5 \times T_C - 4.0$	71.0	—	46.0	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$T_C - 7.5$	—	42.5	—	25.8	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	37.2	—	24.7	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	12.5	—	8.3	ns

[1] The number of wait states for Page mode access is specified in the DCR.
[2] The refresh period is specified in the DCR.
[3] All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $2 \times T_C$ for read-after-read or write-after-write sequences).
[4] Reduced DSP clock speed allows use of Page Mode DRAM with one Wait state. See Figure 3-13.
[5] BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
[6] $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

Table 3-10 DRAM Page Mode Timings, Two Wait States[1, 2, 3, 4]

No.	Characteristics	Symbol	Expression	80 MHz		Unit
				Min	Max	
131	Page mode cycle time for two consecutive accesses of the same direction[5] Page mode cycle time for mixed (read and write) accesses.[5]	t_{PC}	$3 \times T_C$ 2.75 x Tc	37.5 34.4	— —	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$1.5 \times T_C - 6.5$	—	12.3	ns
133	Column address valid to data valid (read)	t_{AA}	$2.5 \times T_C - 6.5$	—	24.8	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$1.75 \times T_C - 4.0$	17.9	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$3.25 \times T_C - 4.0$	36.6	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$1.5 \times T_C - 4.0$	14.8	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion[6] • BRW[1:0] = 00 • BRW[1:0] = 01 • BRW[1:0] = 10 • BRW[1:0] = 11	t_{CRP}	 $2.0 \times T_C - 6.0$ $3.5 \times T_C - 6.0$ $4.5 \times T_C - 6.0$ $6.5 \times T_C - 6.0$	 19.0 37.8 50.3 75.3	 — — — —	ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.25 \times T_C - 4.0$	11.6	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	8.5	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$1.75 \times T_C - 4.0$	17.9	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$3 \times T_C - 4.0$	33.5	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 3.8$	11.8	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.5 \times T_C - 3.7$	2.6	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$1.5 \times T_C - 4.2$	14.6	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$2.5 \times T_C - 4.5$	26.8	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$2.75 \times T_C - 4.3$	30.1	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$2.5 \times T_C - 4.3$	27.0	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.25 \times T_C - 3.0$	0.1	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$1.75 \times T_C - 4.0$	17.9	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$T_C - 4.3$	8.2	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$2.5 \times T_C - 4.0$	27.3	—	ns

Table 3-10 DRAM Page Mode Timings, Two Wait States[1, 2, 3, 4] (continued)

No.	Characteristics	Symbol	Expression	80 MHz		Unit
				Min	Max	
153	$\overline{\text{RD}}$ assertion to data valid	t_{GA}	$1.75 \times T_C - 6.5$	—	15.4	ns
154	$\overline{\text{RD}}$ deassertion to data not valid[7]	t_{GZ}		0.0	—	ns
155	$\overline{\text{WR}}$ assertion to data active		$0.75 \times T_C - 0.3$	9.1	—	ns
156	$\overline{\text{WR}}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.1	ns

1 The number of wait states for Page mode access is specified in the DCR.
2 The refresh period is specified in the DCR.
3 The asynchronous delays specified in the expressions are valid for DSP56362.
4 All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $3 \times T_C$ for read-after-read or write-after-write sequences).
5 There are not any fast enough DRAMs to fit to two wait states Page mode @ 100MHz. See Figure 3-13.
6 BRW[1:0] (DRAM Control Register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
7 $\overline{\text{RD}}$ deassertion will always occur after $\overline{\text{CAS}}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

Table 3-11 DRAM Page Mode Timings, Three Wait States[1, 2, 3, 4]

No.	Characteristics	Symbol	Expression	100 MHz		Unit
				Min	Max	
131	Page mode cycle time for two consecutive accesses of the same direction Page mode cycle time for mixed (read and write) accesses.	t_{PC}	$4 \times T_C$ 3.5 x Tc	40.0 35.0	— —	ns
132	$\overline{\text{CAS}}$ assertion to data valid (read)	t_{CAC}	**100 MHz**: $2 \times T_C - 7.0$	—	13.0	ns
133	Column address valid to data valid (read)	t_{AA}	**100 MHz**: $3 \times T_C - 7.0$	—	23.0	ns
134	$\overline{\text{CAS}}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
135	Last $\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RSH}	$2.5 \times T_C - 4.0$	21.0	—	ns
136	Previous $\overline{\text{CAS}}$ deassertion to $\overline{\text{RAS}}$ deassertion	t_{RHCP}	$4.5 \times T_C - 4.0$	41.0	—	ns
137	$\overline{\text{CAS}}$ assertion pulse width	t_{CAS}	$2 \times T_C - 4.0$	16.0	—	ns
138	Last $\overline{\text{CAS}}$ deassertion to $\overline{\text{RAS}}$ assertion[5] • BRW[1:0] = 00 • BRW[1:0] = 01 • BRW[1:0] = 10 • BRW[1:0] = 11	t_{CRP}	 $2.25 \times T_C - 6.0$ $3.75 \times T_C - 6.0$ $4.75 \times T_C - 6.0$ $6.75 \times T_C - 6.0$	 — — 41.5 61.5	 — — — —	ns

Table 3-11 DRAM Page Mode Timings, Three Wait States[1, 2, 3, 4] (continued)

No.	Characteristics	Symbol	Expression	100 MHz		Unit
				Min	Max	
139	$\overline{\text{CAS}}$ deassertion pulse width	t_{CP}	$1.5 \times T_C - 4.0$	11.0	—	ns
140	Column address valid to $\overline{\text{CAS}}$ assertion	t_{ASC}	$T_C - 4.0$	6.0	—	ns
141	$\overline{\text{CAS}}$ assertion to column address not valid	t_{CAH}	$2.5 \times T_C - 4.0$	21.0	—	ns
142	Last column address valid to $\overline{\text{RAS}}$ deassertion	t_{RAL}	$4 \times T_C - 4.0$	36.0	—	ns
143	$\overline{\text{WR}}$ deassertion to $\overline{\text{CAS}}$ assertion	t_{RCS}	**100 MHz**: $1.25 \times T_C - 4.0$	8.5		ns
144	$\overline{\text{CAS}}$ deassertion to $\overline{\text{WR}}$ assertion	t_{RCH}	**100 MHz**: $0.75 \times T_C - 4.0$	3.5		ns
145	$\overline{\text{CAS}}$ assertion to $\overline{\text{WR}}$ deassertion	t_{WCH}	$2.25 \times T_C - 4.2$	18.3	—	ns
146	$\overline{\text{WR}}$ assertion pulse width	t_{WP}	$3.5 \times T_C - 4.5$	30.5	—	ns
147	Last $\overline{\text{WR}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RWL}	$3.75 \times T_C - 4.3$	33.2	—	ns
148	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ deassertion	t_{CWL}	$3.25 \times T_C - 4.3$	28.2	—	ns
149	Data valid to $\overline{\text{CAS}}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.0$	1.0	—	ns
150	$\overline{\text{CAS}}$ assertion to data not valid (write)	t_{DH}	$2.5 \times T_C - 4.0$	21.0	—	ns
151	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ assertion	t_{WCS}	$1.25 \times T_C - 4.3$	8.2	—	ns
152	Last $\overline{\text{RD}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{ROH}	$3.5 \times T_C - 4.0$	31.0	—	ns
153	$\overline{\text{RD}}$ assertion to data valid	t_{GA}	**100 MHz**: $2.5 \times T_C - 7.0$	—	18.0	ns
154	$\overline{\text{RD}}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	ns
155	$\overline{\text{WR}}$ assertion to data active		$0.75 \times T_C - 0.3$	7.2	—	ns
156	$\overline{\text{WR}}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	ns

1 The number of wait states for Page mode access is specified in the DCR.

2 The refresh period is specified in the DCR.

3 The asynchronous delays specified in the expressions are valid for DSP56362.

4 All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $4 \times T_C$ for read-after-read or write-after-write sequences).

5 BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of page-access.

6 $\overline{\text{RD}}$ deassertion will always occur after $\overline{\text{CAS}}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

Table 3-12 DRAM Page Mode Timings, Four Wait States 100 and 120MHz[1, 2, 3, 4]

No.	Characteristics	Symbol	Expression	100 MHz		120 MHz		Unit
				Min	Max	Min	Max	
131	Page mode cycle time for two consecutive accesses of the same direction Page mode cycle time for mixed (read and write) accesses.	t_{PC}	$5 \times T_C$ $4.5 \times T_C$	50.0 45.0	— —	41.7 37.5		ns
132	$\overline{\text{CAS}}$ assertion to data valid (read)	t_{CAC}	**100 MHz**: $2.75 \times T_C - 7.0$	—	20.5	—	15.9	ns
133	Column address valid to data valid (read)	t_{AA}	**100 MHz**: $3.75 \times T_C - 7.0$	—	30.5	—	24.2	ns
134	$\overline{\text{CAS}}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	ns
135	Last $\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RSH}	$3.5 \times T_C - 4.0$	31.0	—	25.2	—	ns
136	Previous $\overline{\text{CAS}}$ deassertion to $\overline{\text{RAS}}$ deassertion	t_{RHCP}	$6 \times T_C - 4.0$	56.0	—	46.0	—	ns
137	$\overline{\text{CAS}}$ assertion pulse width	t_{CAS}	$2.5 \times T_C - 4.0$	21.0	—	16.8	—	ns
138	Last $\overline{\text{CAS}}$ deassertion to $\overline{\text{RAS}}$ assertion[5] BRW[1:0] = 00 BRW[1:0] = 01 BRW[1:0] = 10 BRW[1:0] = 11	t_{CRP}	 $2.75 \times T_C - 6.0$ $4.25 \times T_C - 6.0$ $5.25 \times T_C - 6.0$ $7.25 \times T_C - 6.0$	 — — 46.5 66.5	 — — — —	 — — 37.7 54.4	 — — — —	ns
139	$\overline{\text{CAS}}$ deassertion pulse width	t_{CP}	$2 \times T_C - 4.0$	16.0	—	12.7	—	ns
140	Column address valid to $\overline{\text{CAS}}$ assertion	t_{ASC}	$T_C - 4.0$	6.0	—	4.3	—	ns
141	$\overline{\text{CAS}}$ assertion to column address not valid	t_{CAH}	$3.5 \times T_C - 4.0$	31.0	—	25.2	—	ns
142	Last column address valid to $\overline{\text{RAS}}$ deassertion	t_{RAL}	$5 \times T_C - 4.0$	46.0	—	37.7	—	ns
143	$\overline{\text{WR}}$ deassertion to $\overline{\text{CAS}}$ assertion	t_{RCS}	**100 MHz**: $1.25 \times T_C - 4.0$	8.5	—	6.4	—	ns
144	$\overline{\text{CAS}}$ deassertion to $\overline{\text{WR}}$ assertion	t_{RCH}	**100 MHz**: $1.25 \times T_C - 4.0$	8.5	—	6.4	—	ns
145	$\overline{\text{CAS}}$ assertion to $\overline{\text{WR}}$ deassertion	t_{WCH}	$3.25 \times T_C - 4.2$	28.3	—	22.9	—	ns
146	$\overline{\text{WR}}$ assertion pulse width	t_{WP}	$4.5 \times T_C - 4.5$	40.5	—	33.0	—	ns
147	Last $\overline{\text{WR}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RWL}	$4.75 \times T_C - 4.3$	43.2	—	35.3	—	ns
148	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ deassertion	t_{CWL}	$3.75 \times T_C - 4.3$	33.2	—	26.9	—	ns

Table 3-12 DRAM Page Mode Timings, Four Wait States 100 and 120MHz[1, 2, 3, 4] (continued)

No.	Characteristics	Symbol	Expression	100 MHz		120 MHz		Unit
				Min	Max	Min	Max	
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.0$	1.0	—	0.2	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$3.5 \times T_C - 4.0$	31.0	—	25.2	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$1.25 \times T_C - 4.3$	8.2	—	6.1	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$4.5 \times T_C - 4.0$	41.0	—	33.5	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	**100 MHz**: $3.25 \times T_C - 7.0$	—	25.5	—	20.1	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	7.2	—	5.9		ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	—	2.1	ns

1 The number of wait states for Page mode access is specified in the DCR.

2 The refresh period is specified in the DCR.

3 The asynchronous delays specified in the expressions are valid for DSP56362.

4 All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $3 \times T_C$ for read-after-read or write-after-write sequences).

5 BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.

6 $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

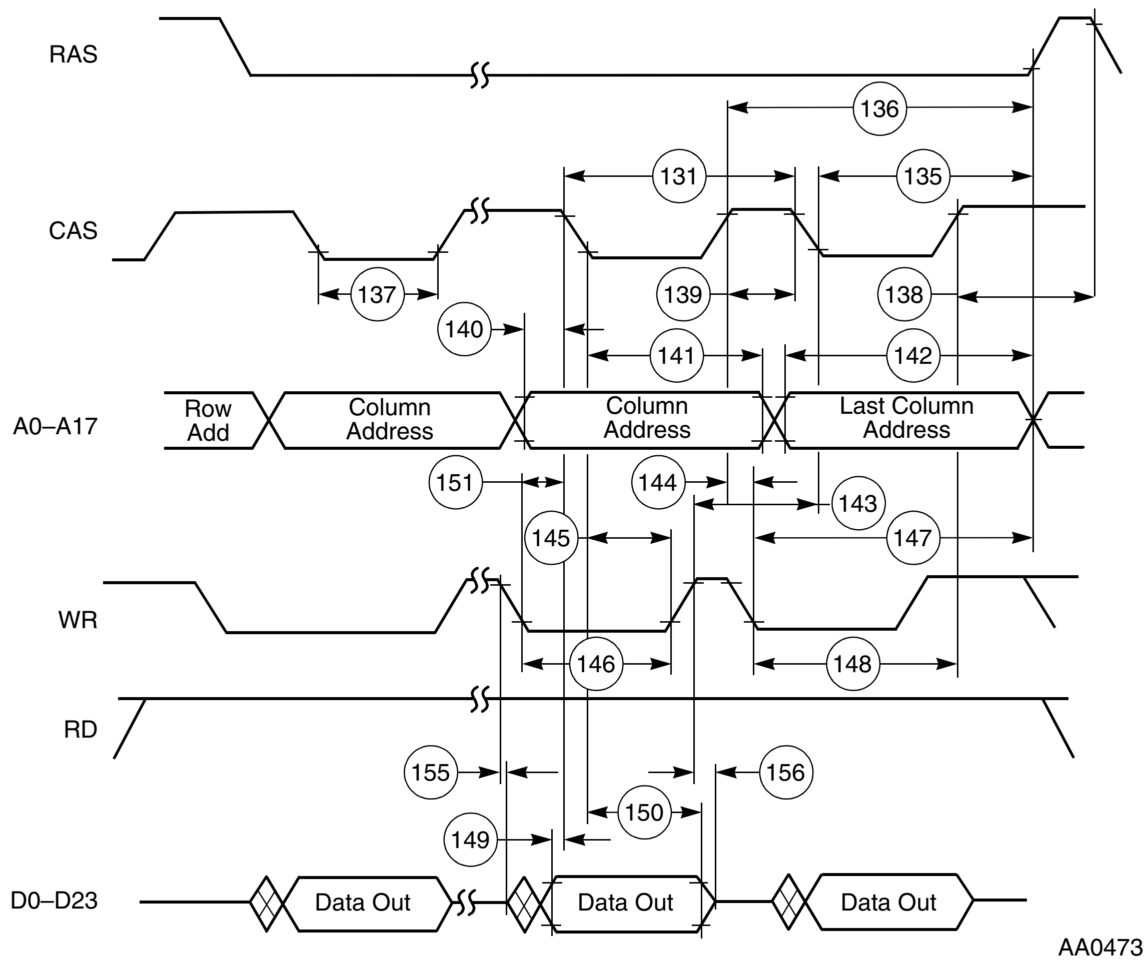


Figure 3-14 DRAM Page Mode Write Accesses

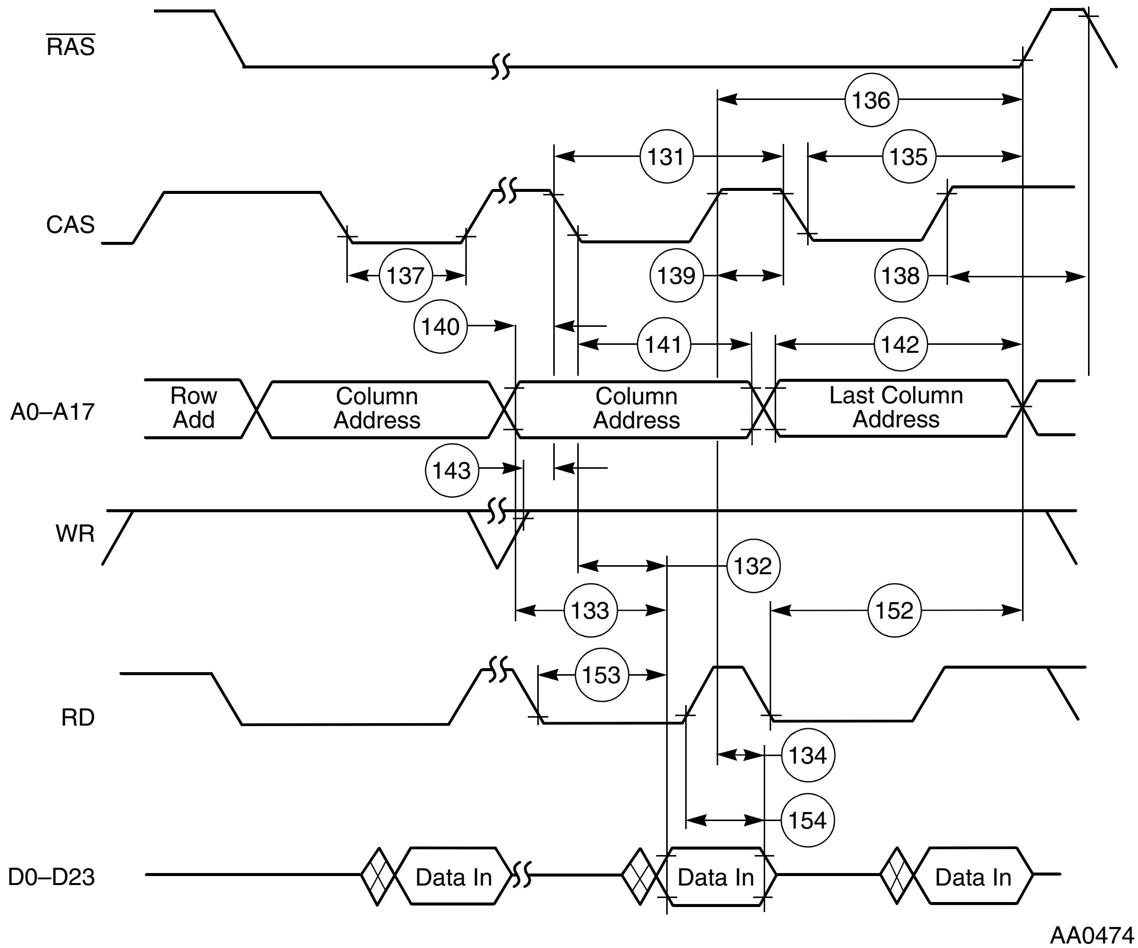


Figure 3-15 DRAM Page Mode Read Accesses

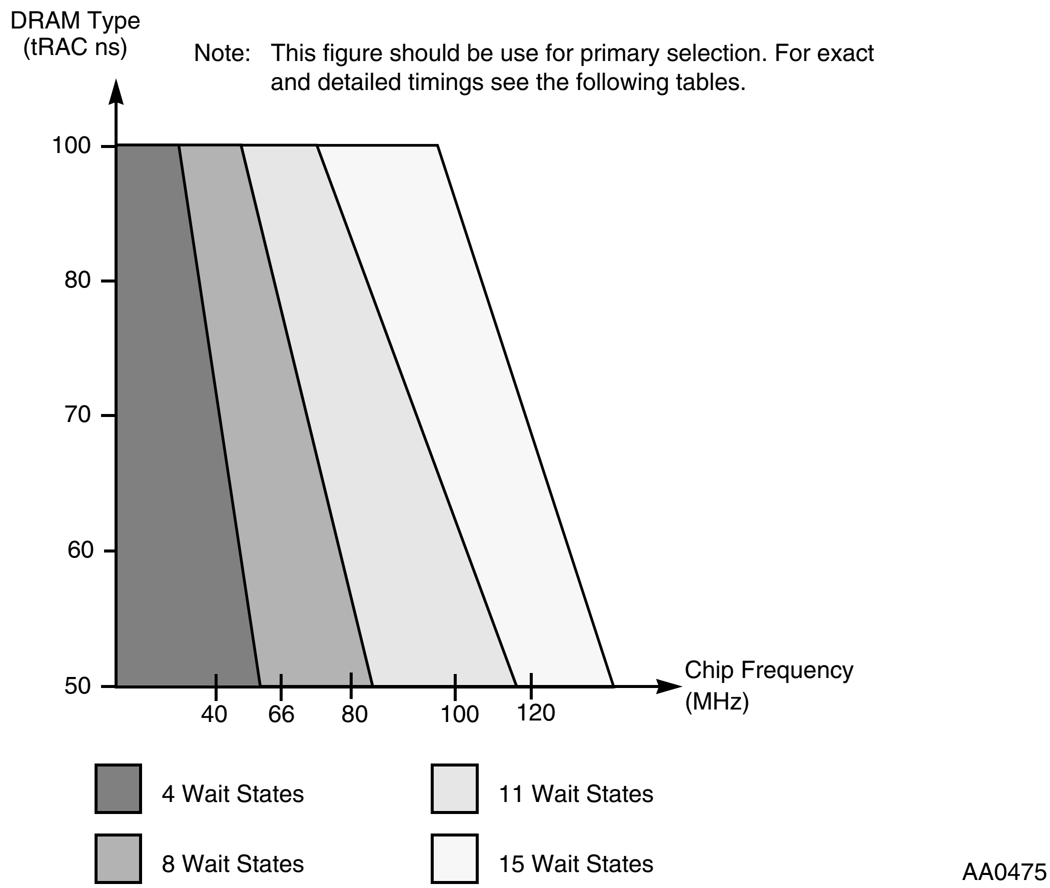


Figure 3-16 DRAM Out-of-Page Wait States Selection Guide

Table 3-13 DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2]

No.	Characteristics[3]	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
157	Random read or write cycle time	t_{RC}	$5 \times T_C$	250.0	—	166.7	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	$2.75 \times T_C - 7.5$	—	130.0	—	84.2	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$1.25 \times T_C - 7.5$	—	55.0	—	34.2	ns
160	Column address valid to data valid (read)	t_{AA}	$1.5 \times T_C - 7.5$	—	67.5	—	42.5	ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns

Table 3-13 DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2] (continued)

No.	Characteristics[3]	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
165	$\overline{\text{RAS}}$ assertion to $\overline{\text{CAS}}$ deassertion	t_{CSH}	$2.75 \times T_C - 4.0$	133.5	—	87.7	—	ns
166	$\overline{\text{CAS}}$ assertion pulse width	t_{CAS}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns
167	$\overline{\text{RAS}}$ assertion to $\overline{\text{CAS}}$ assertion	t_{RCD}	$1.5 \times T_C \pm 2$	73.0	77.0	48.0	52.0	ns
168	$\overline{\text{RAS}}$ assertion to column address valid	t_{RAD}	$1.25 \times T_C \pm 2$	60.5	64.5	39.7	43.7	ns
169	$\overline{\text{CAS}}$ deassertion to $\overline{\text{RAS}}$ assertion	t_{CRP}	$2.25 \times T_C - 4.0$	108.5	—	71.0	—	ns
170	$\overline{\text{CAS}}$ deassertion pulse width	t_{CP}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
171	Row address valid to $\overline{\text{RAS}}$ assertion	t_{ASR}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
172	$\overline{\text{RAS}}$ assertion to row address not valid	t_{RAH}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns
173	Column address valid to $\overline{\text{CAS}}$ assertion	t_{ASC}	$0.25 \times T_C - 4.0$	8.5	—	4.3	—	ns
174	$\overline{\text{CAS}}$ assertion to column address not valid	t_{CAH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
175	$\overline{\text{RAS}}$ assertion to column address not valid	t_{AR}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
176	Column address valid to $\overline{\text{RAS}}$ deassertion	t_{RAL}	$2 \times T_C - 4.0$	96.0	—	62.7	—	ns
177	$\overline{\text{WR}}$ deassertion to $\overline{\text{CAS}}$ assertion	t_{RCS}	$1.5 \times T_C - 3.8$	71.2	—	46.2	—	ns
178	$\overline{\text{CAS}}$ deassertion to $\overline{\text{WR}}$ assertion	t_{RCH}	$0.75 \times T_C - 3.7$	33.8	—	21.3	—	ns
179	$\overline{\text{RAS}}$ deassertion to $\overline{\text{WR}}$ assertion	t_{RRH}	$0.25 \times T_C - 3.7$	8.8	—	4.6	—	ns
180	$\overline{\text{CAS}}$ assertion to $\overline{\text{WR}}$ deassertion	t_{WCH}	$1.5 \times T_C - 4.2$	70.8	—	45.8	—	ns
181	$\overline{\text{RAS}}$ assertion to $\overline{\text{WR}}$ deassertion	t_{WCR}	$3 \times T_C - 4.2$	145.8	—	95.8	—	ns
182	$\overline{\text{WR}}$ assertion pulse width	t_{WP}	$4.5 \times T_C - 4.5$	220.5	—	145.5	—	ns
183	$\overline{\text{WR}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RWL}	$4.75 \times T_C - 4.3$	233.2	—	154.0	—	ns
184	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ deassertion	t_{CWL}	$4.25 \times T_C - 4.3$	208.2	—	137.4	—	ns
185	Data valid to $\overline{\text{CAS}}$ assertion (write)	t_{DS}	$2.25 \times T_C - 4.0$	108.5	—	71.0	—	ns
186	$\overline{\text{CAS}}$ assertion to data not valid (write)	t_{DH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
187	$\overline{\text{RAS}}$ assertion to data not valid (write)	t_{DHR}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
188	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ assertion	t_{WCS}	$3 \times T_C - 4.3$	145.7	—	95.7	—	ns
189	$\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ assertion (refresh)	t_{CSR}	$0.5 \times T_C - 4.0$	21.0	—	12.7	—	ns
190	$\overline{\text{RAS}}$ deassertion to $\overline{\text{CAS}}$ assertion (refresh)	t_{RPC}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns

Table 3-13 DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2] (continued)

No.	Characteristics[3]	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
191	$\overline{\text{RD}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{ROH}	$4.5 \times T_C - 4.0$	221.0	—	146.0	—	ns
192	$\overline{\text{RD}}$ assertion to data valid	t_{GA}	$4 \times T_C - 7.5$	—	192.5	—	125.8	ns
193	$\overline{\text{RD}}$ deassertion to data not valid[3]	t_{GZ}		0.0	—	0.0	—	ns
194	$\overline{\text{WR}}$ assertion to data active		$0.75 \times T_C - 0.3$	37.2	—	24.7	—	ns
195	$\overline{\text{WR}}$ deassertion to data high impedance		$0.25 \times T_C$	—	12.5	—	8.3	ns

1 The number of wait states for out of page access is specified in the DCR.
2 The refresh period is specified in the DCR.
3 $\overline{\text{RD}}$ deassertion will always occur after $\overline{\text{CAS}}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
4 Reduced DSP clock speed allows use of DRAM out-of-page access with four Wait states. See Figure 3-16.

Table 3-14 DRAM Out-of-Page and Refresh Timings, Eight Wait States[1, 2]

No.	Characteristics[3]	Symbol	Expression[4]	80 MHz		Unit
				Min	Max	
157	Random read or write cycle time	t_{RC}	$9 \times T_C$	112.5	—	ns
158	$\overline{\text{RAS}}$ assertion to data valid (read)	t_{RAC}	$4.75 \times T_C - 6.5$		52.9	ns
159	$\overline{\text{CAS}}$ assertion to data valid (read)	t_{CAC}	$2.25 \times T_C - 6.5$	—	21.6	ns
160	Column address valid to data valid (read)	t_{AA}	$3 \times T_C - 6.5$	—	31.0	ns
161	$\overline{\text{CAS}}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
162	$\overline{\text{RAS}}$ deassertion to $\overline{\text{RAS}}$ assertion	t_{RP}	$3.25 \times T_C - 4.0$	36.6	—	ns
163	$\overline{\text{RAS}}$ assertion pulse width	t_{RAS}	$5.75 \times T_C - 4.0$	67.9	—	ns
164	$\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RSH}	$3.25 \times T_C - 4.0$	36.6	—	ns
165	$\overline{\text{RAS}}$ assertion to $\overline{\text{CAS}}$ deassertion	t_{CSH}	$4.75 \times T_C - 4.0$	55.4	—	ns
166	$\overline{\text{CAS}}$ assertion pulse width	t_{CAS}	$2.25 \times T_C - 4.0$	24.1	—	ns
167	$\overline{\text{RAS}}$ assertion to $\overline{\text{CAS}}$ assertion	t_{RCD}	$2.5 \times T_C \pm 2$	29.3	33.3	ns
168	$\overline{\text{RAS}}$ assertion to column address valid	t_{RAD}	$1.75 \times T_C \pm 2$	19.9	23.9	ns
169	$\overline{\text{CAS}}$ deassertion to $\overline{\text{RAS}}$ assertion	t_{CRP}	$4.25 \times T_C - 4.0$	49.1	—	ns
170	$\overline{\text{CAS}}$ deassertion pulse width	t_{CP}	$2.75 \times T_C - 4.0$	30.4	—	ns
171	Row address valid to $\overline{\text{RAS}}$ assertion	t_{ASR}	$3.25 \times T_C - 4.0$	36.6	—	ns

Table 3-14 DRAM Out-of-Page and Refresh Timings, Eight Wait States[1, 2] (continued)

No.	Characteristics[3]	Symbol	Expression[4]	80 MHz		Unit
				Min	Max	
172	$\overline{\text{RAS}}$ assertion to row address not valid	t_{RAH}	$1.75 \times T_C - 4.0$	17.9	—	ns
173	Column address valid to $\overline{\text{CAS}}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	5.4	—	ns
174	$\overline{\text{CAS}}$ assertion to column address not valid	t_{CAH}	$3.25 \times T_C - 4.0$	36.6	—	ns
175	$\overline{\text{RAS}}$ assertion to column address not valid	t_{AR}	$5.75 \times T_C - 4.0$	67.9	—	ns
176	Column address valid to $\overline{\text{RAS}}$ deassertion	t_{RAL}	$4 \times T_C - 4.0$	46.0	—	ns
177	$\overline{\text{WR}}$ deassertion to $\overline{\text{CAS}}$ assertion	t_{RCS}	$2 \times T_C - 3.8$	21.2	—	ns
178	$\overline{\text{CAS}}$ deassertion to $\overline{\text{WR}}$[5] assertion	t_{RCH}	$1.25 \times T_C - 3.7$	11.9	—	ns
179	$\overline{\text{RAS}}$ deassertion to $\overline{\text{WR}}$[5] assertion	t_{RRH}	$0.25 \times T_C - 3.0$	0.1	—	ns
180	$\overline{\text{CAS}}$ assertion to $\overline{\text{WR}}$ deassertion	t_{WCH}	$3 \times T_C - 4.2$	33.3	—	ns
181	$\overline{\text{RAS}}$ assertion to $\overline{\text{WR}}$ deassertion	t_{WCR}	$5.5 \times T_C - 4.2$	64.6	—	ns
182	$\overline{\text{WR}}$ assertion pulse width	t_{WP}	$8.5 \times T_C - 4.5$	101.8	—	ns
183	$\overline{\text{WR}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RWL}	$8.75 \times T_C - 4.3$	105.1	—	ns
184	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ deassertion	t_{CWL}	$7.75 \times T_C - 4.3$	92.6	—	ns
185	Data valid to $\overline{\text{CAS}}$ assertion (write)	t_{DS}	$4.75 \times T_C - 4.0$	55.4	—	ns
186	$\overline{\text{CAS}}$ assertion to data not valid (write)	t_{DH}	$3.25 \times T_C - 4.0$	36.6	—	ns
187	$\overline{\text{RAS}}$ assertion to data not valid (write)	t_{DHR}	$5.75 \times T_C - 4.0$	67.9	—	ns
188	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ assertion	t_{WCS}	$5.5 \times T_C - 4.3$	64.5	—	ns
189	$\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	14.8	—	ns
190	$\overline{\text{RAS}}$ deassertion to $\overline{\text{CAS}}$ assertion (refresh)	t_{RPC}	$1.75 \times T_C - 4.0$	17.9	—	ns
191	$\overline{\text{RD}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{ROH}	$8.5 \times T_C - 4.0$	102.3	—	ns
192	$\overline{\text{RD}}$ assertion to data valid	t_{GA}	$7.5 \times T_C - 6.5$	—	87.3	ns
193	$\overline{\text{RD}}$ deassertion to data not valid[3]	t_{GZ}	0.0	0.0	—	ns
194	$\overline{\text{WR}}$ assertion to data active		$0.75 \times T_C - 0.3$	9.1	—	ns
195	$\overline{\text{WR}}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.1	ns

1 The number of wait states for out-of-page access is specified in the DCR.
2 The refresh period is specified in the DCR.
3 $\overline{\text{RD}}$ deassertion will always occur after $\overline{\text{CAS}}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
4 The asynchronous delays specified in the expressions are valid for DSP56362.
5 Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

Table 3-15 DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2]

No.	Characteristics[3]	Symbol	Expression[4]	100 MHz		Unit
				Min	Max	
157	Random read or write cycle time	t_{RC}	$12 \times T_C$	120.0	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	$6.25 \times T_C - 7.0$	—	55.5	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$3.75 \times T_C - 7.0$	—	30.5	ns
160	Column address valid to data valid (read)	t_{AA}	$4.5 \times T_C - 7.0$	—	38.0	ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$4.25 \times T_C - 4.0$	38.5	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$7.75 \times T_C - 4.0$	73.5	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$5.25 \times T_C - 4.0$	48.5	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$6.25 \times T_C - 4.0$	58.5	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$3.75 \times T_C - 4.0$	33.5	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$2.5 \times T_C \pm 4.0$	21.0	29.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$1.75 \times T_C \pm 4.0$	13.5	21.5	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$5.75 \times T_C - 4.0$	53.5	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$4.25 \times T_C - 4.0$	38.5	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$4.25 \times T_C - 4.0$	38.5	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$1.75 \times T_C - 4.0$	13.5	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	3.5	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$5.25 \times T_C - 4.0$	48.5	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$7.75 \times T_C - 4.0$	73.5	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$6 \times T_C - 4.0$	56.0	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$3.0 \times T_C - 4.0$	26.0	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RCH}	$1.75 \times T_C - 4.0$	13.5	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RRH}	$0.25 \times T_C - 3.0$	—	—	ns
			$0.25 \times T_C - 2.0$	0.5	—	
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$5 \times T_C - 4.2$	45.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$7.5 \times T_C - 4.2$	70.8	—	ns

Table 3-15 DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2] (continued)

No.	Characteristics[3]	Symbol	Expression[4]	100 MHz		Unit
				Min	Max	
182	$\overline{WR}$ assertion pulse width	t_{WP}	$11.5 \times T_C - 4.5$	110.5	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$11.75 \times T_C - 4.3$	113.2	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$10.25 \times T_C - 4.3$	103.2	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$5.75 \times T_C - 4.0$	53.5	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$5.25 \times T_C - 4.0$	48.5	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$7.75 \times T_C - 4.0$	73.5	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$6.5 \times T_C - 4.3$	60.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	11.0	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$2.75 \times T_C - 4.0$	23.5	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$11.5 \times T_C - 4.0$	111.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	$10 \times T_C - 7.0$		93.0	ns
193	$\overline{RD}$ deassertion to data not valid[3]	t_{GZ}		0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	7.2	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	ns

1 The number of wait states for out-of-page access is specified in the DCR.
2 The refresh period is specified in the DCR.
3 $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
4 The asynchronous delays specified in the expressions are valid for DSP56362.
5 Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

Table 3-16 DRAM Out-of-Page and Refresh Timings, Fifteen Wait States 100 and 120MHz[1, 2]

No.	Characteristics[3]	Symbol	Expression	100 MHz		120 MHz		Unit
				Min	Max	Min	Max	
157	Random read or write cycle time	t_{RC}	$16 \times T_C$	160.0	—	133.3	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	$8.25 \times T_C - 5.7$	—	76.8	—	63.0	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$4.75 \times T_C - 5.7$	—	41.8	—	33.9	ns
160	Column address valid to data valid (read)	t_{AA}	$5.5 \times T_C - 5.7$	—	49.3		40.1	ns

Table 3-16 DRAM Out-of-Page and Refresh Timings, Fifteen Wait States 100 and 120MHz[1, 2] (continued)

No.	Characteristics[3]	Symbol	Expression	100 MHz		120 MHz		Unit
				Min	Max	Min	Max	
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}	0.0	0.0	—	0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$6.25 \times T_C - 4.0$	58.5	—	48.1	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$9.75 \times T_C - 4.0$	93.5	—	77.2	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$6.25 \times T_C - 4.0$	58.5	—	48.1	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$8.25 \times T_C - 4.0$	78.5	—	64.7	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$4.75 \times T_C - 4.0$	43.5	—	35.6	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$3.5 \times T_C \pm 2$	33.0	37.0	27.2	31.2	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$2.75 \times T_C \pm 2$	25.5	29.5	20.9	24.9	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$7.75 \times T_C - 4.0$	73.5	—	60.6	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$6.25 \times T_C - 4.0$	58.5	—	48.1	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$6.25 \times T_C - 4.0$	58.5	—	48.1	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$2.75 \times T_C - 4.0$	23.5	—	18.9	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	3.5	—	2.2	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$6.25 \times T_C - 4.0$	58.5	—	48.1	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$9.75 \times T_C - 4.0$	93.5	—	77.2	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$7 \times T_C - 4.0$	66.0	—	54.3	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$5 \times T_C - 3.8$	46.2	—	37.9	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$[4] assertion	t_{RCH}	$1.75 \times T_C - 3.7$	13.8	—	10.9	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[4] assertion	t_{RRH}	$0.25 \times T_C - 2.0$	0.5	—	0.1	—	ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$6 \times T_C - 4.2$	55.8	—	45.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$9.5 \times T_C - 4.2$	90.8	—	75.0	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$15.5 \times T_C - 4.5$	150.5	—	124.7	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$15.75 \times T_C - 4.3$	153.2	—	126.9	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$14.25 \times T_C - 4.3$	138.2	—	114.4	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$8.75 \times T_C - 4.0$	83.5	—	68.9	—	ns

Table 3-16 DRAM Out-of-Page and Refresh Timings, Fifteen Wait States 100 and 120MHz[1, 2] (continued)

No.	Characteristics[3]	Symbol	Expression	100 MHz		120 MHz		Unit
				Min	Max	Min	Max	
186	$\overline{\text{CAS}}$ assertion to data not valid (write)	t_{DH}	$6.25 \times T_C - 4.0$	58.5	—	48.1	—	ns
187	$\overline{\text{RAS}}$ assertion to data not valid (write)	t_{DHR}	$9.75 \times T_C - 4.0$	93.5	—	77.2	—	ns
188	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ assertion	t_{WCS}	$9.5 \times T_C - 4.3$	90.7	—	74.9	—	ns
189	$\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	11.0	—	8.5	—	ns
190	$\overline{\text{RAS}}$ deassertion to $\overline{\text{CAS}}$ assertion (refresh)	t_{RPC}	$4.75 \times T_C - 4.0$	43.5	—	35.6	—	ns
191	$\overline{\text{RD}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{ROH}	$15.5 \times T_C - 4.0$	151.0	—	125.2	—	ns
192	$\overline{\text{RD}}$ assertion to data valid	t_{GA}	$14 \times T_C - 5.7$	—	134.3	—	111.0	ns
193	$\overline{\text{RD}}$ deassertion to data not valid[3]	t_{GZ}		0.0	—	0.0	—	ns
194	$\overline{\text{WR}}$ assertion to data active		$0.75 \times T_C - 0.3$	7.2	—	5.9	—	ns
195	$\overline{\text{WR}}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	—	2.1	ns

1 The number of wait states for out-of-page access is specified in the DCR.
2 The refresh period is specified in the DCR.
3 $\overline{\text{RD}}$ deassertion will always occur after $\overline{\text{CAS}}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
4 Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

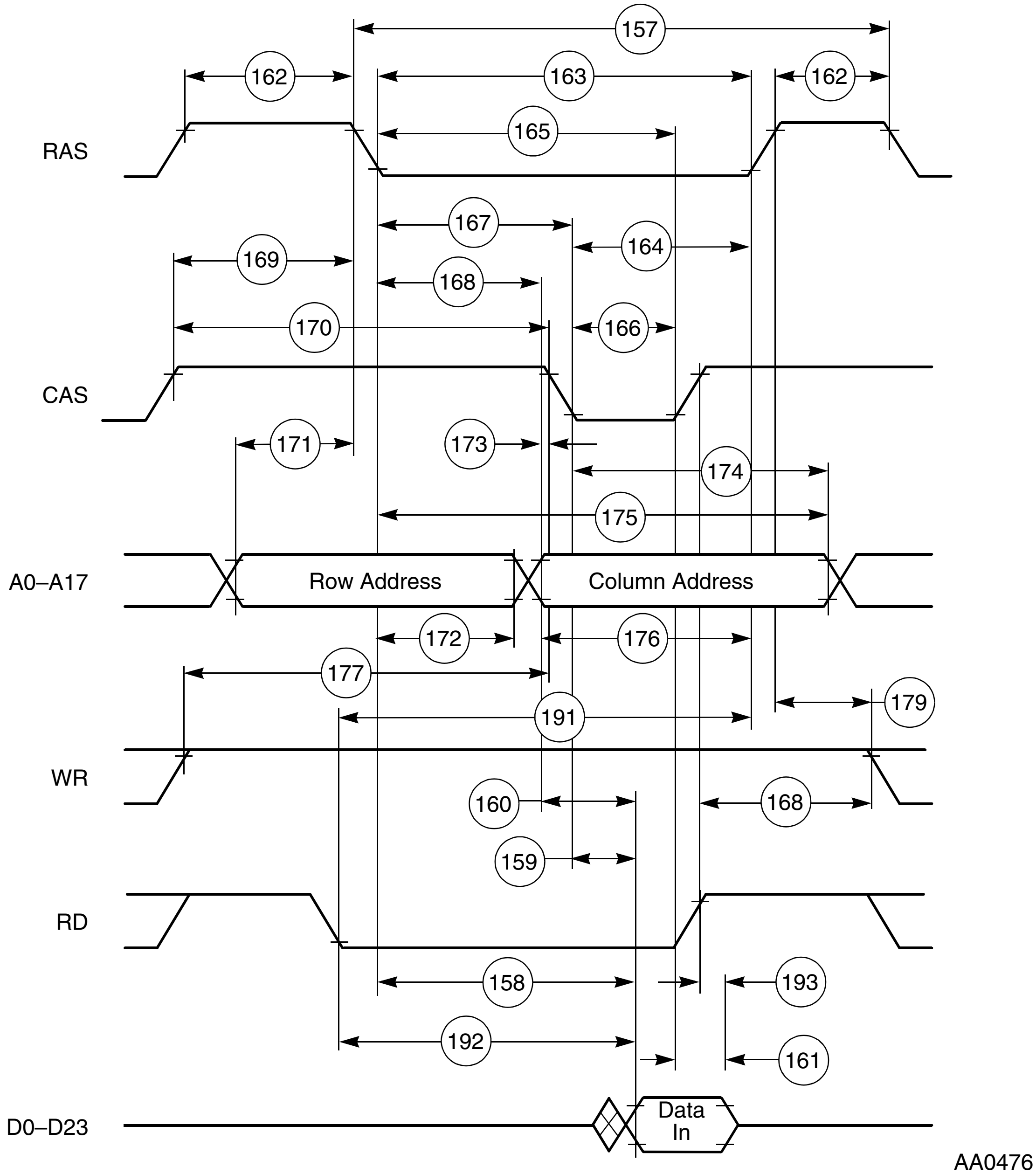


Figure 3-17 DRAM Out-of-Page Read Access

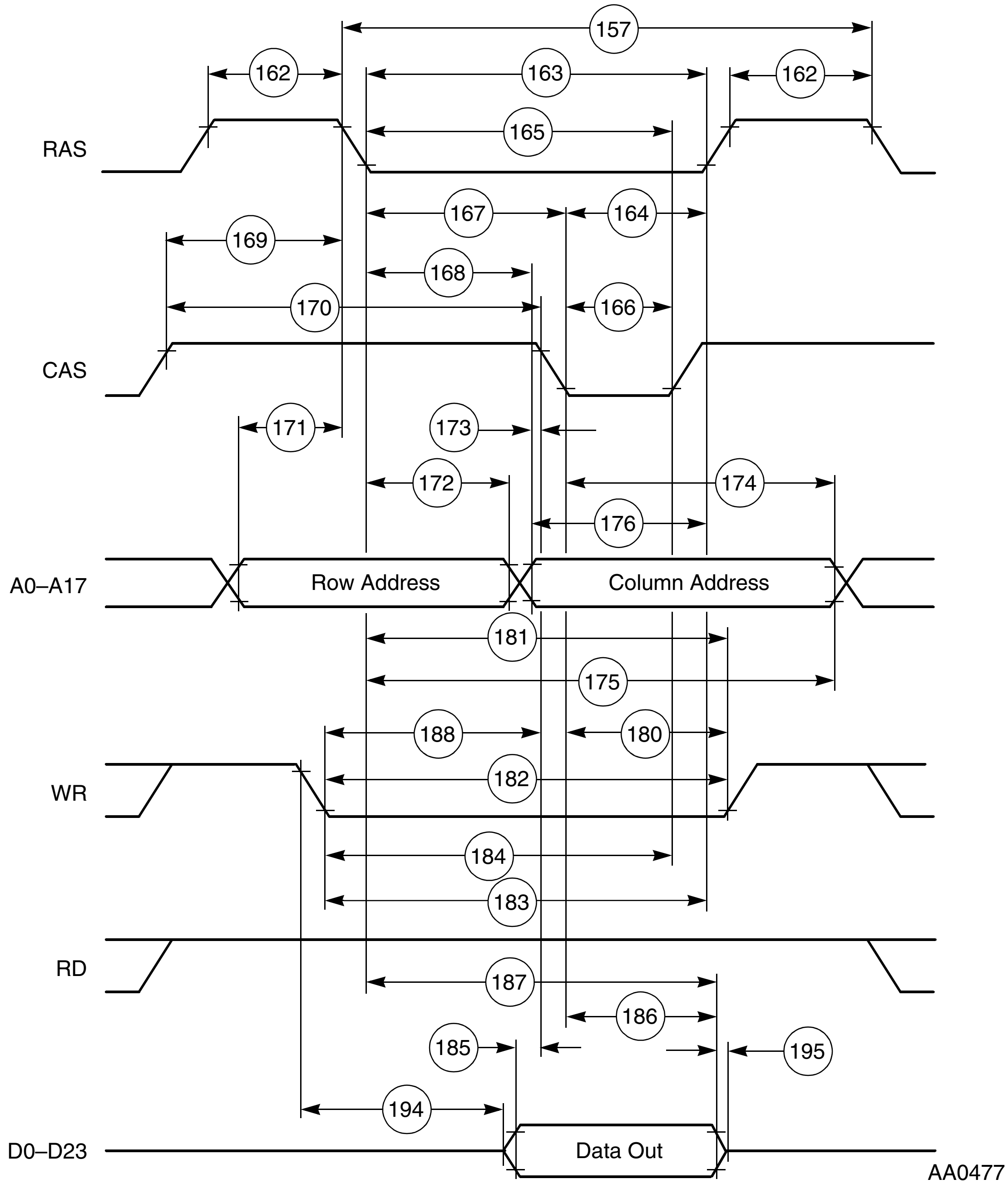


Figure 3-18 DRAM Out-of-Page Write Access

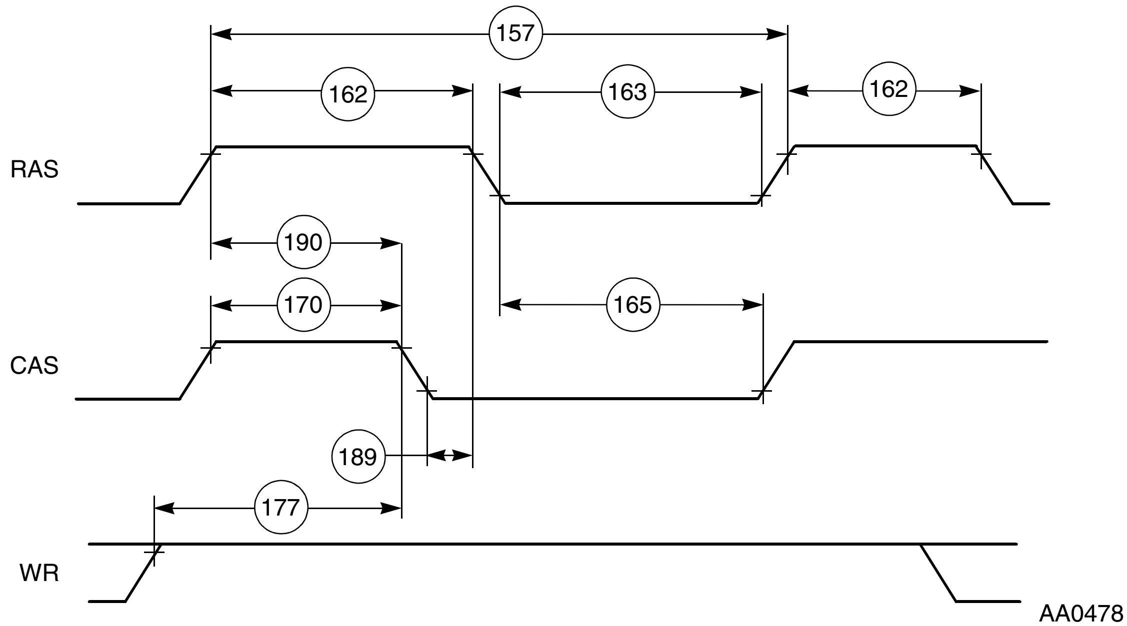


Figure 3-19 DRAM Refresh Access

3.10.3 Synchronous Timings (SRAM)

Table 3-17 External Bus Synchronous Timings (SRAM Access)[1]

No.	Characteristics	Expression[2, 3]	100 MHz		Unit
			Min	Max	
198	CLKOUT high to address, and AA valid[4]	$0.25 \times T_C + 4.0$	—	6.5	ns
199	CLKOUT high to address, and AA invalid[4]	$0.25 \times T_C$	2.5	—	ns
200	$\overline{TA}$ valid to CLKOUT high (setup time)		4.0	—	ns
201	CLKOUT high to $\overline{TA}$ invalid (hold time)		0.0	—	ns
202	CLKOUT high to data out active	$0.25 \times T_C$	2.5	—	ns
203	CLKOUT high to data out valid	$0.25 \times T_C + 4.0$	3.3	6.5	ns
204	CLKOUT high to data out invalid	$0.25 \times T_C$	2.5	—	ns
205	CLKOUT high to data out high impedance	$0.25 \times T_C$	—	2.5	ns
206	Data in valid to CLKOUT high (setup)		4.0	—	ns
207	CLKOUT high to data in invalid (hold)		0.0	—	ns
208	CLKOUT high to $\overline{RD}$ assertion	$0.75 \times T_C + 4.0$	8.2	11.5	ns

Table 3-17 External Bus Synchronous Timings (SRAM Access)[1] (continued)

No.	Characteristics	Expression[2, 3]	100 MHz		Unit
			Min	Max	
209	CLKOUT high to $\overline{RD}$ deassertion		0.0	4.0	ns
210	CLKOUT high to $\overline{WR}$ assertion[5]	$0.5 \times T_C + 4.3$ [WS = 1 or WS ≥ 4]	6.3	9.3	ns
		All frequencies: [2 ≤ WS ≤ 3]	1.3	4.3	
211	CLKOUT high to $\overline{WR}$ deassertion		0.0	3.8	ns

1 External bus synchronous timings should be used only for reference to the clock and *not* for relative timings.
2 WS is the number of wait states specified in the BCR.
3 The asynchronous delays specified in the expressions are valid for DSP56362.
4 T198 and T199 are valid for Address Trace mode if the ATE bit in the OMR is set. Use the status of $\overline{BR}$ (See T212) to determine whether the access referenced by A0–A23 is internal or external, when this mode is enabled
5 If WS > 1, $\overline{WR}$ assertion refers to the next rising edge of CLKOUT.

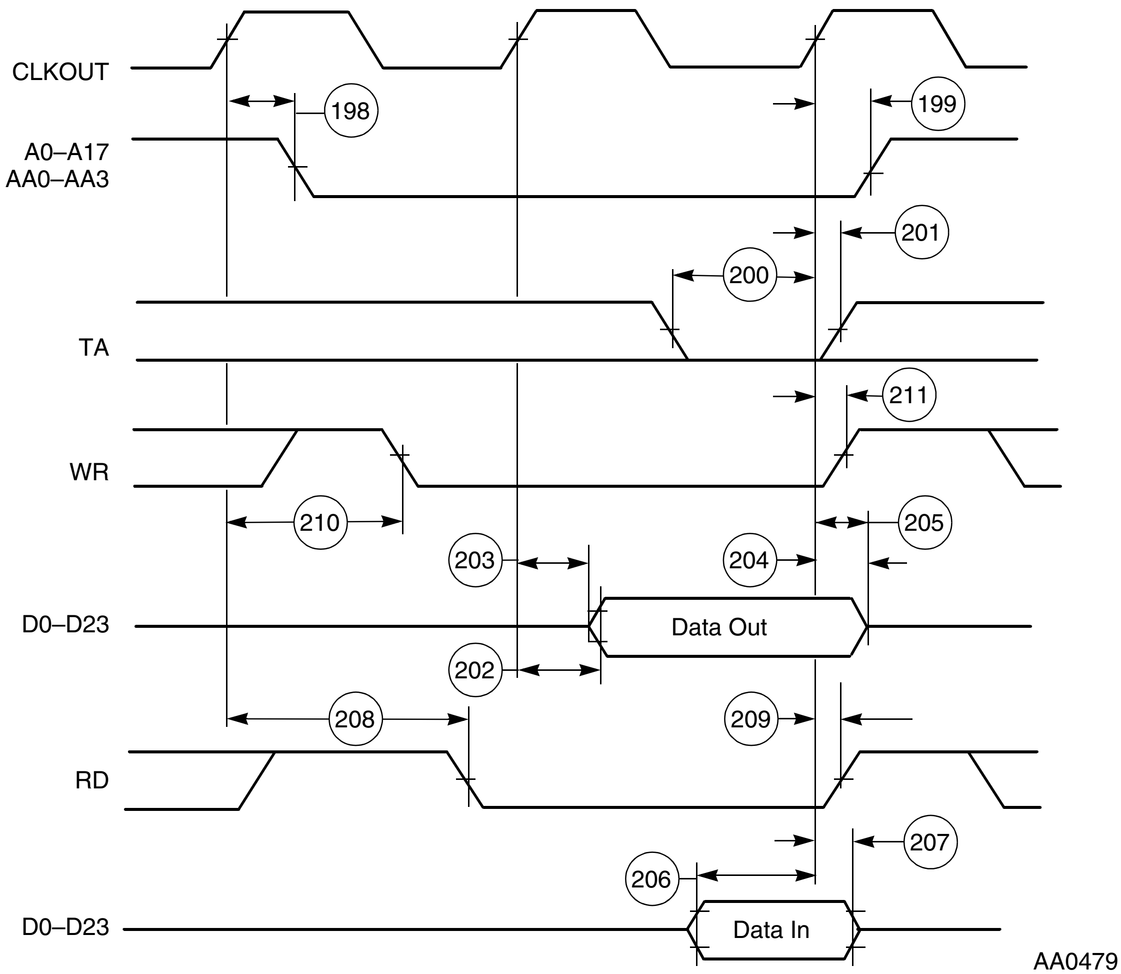


Figure 3-20 Synchronous Bus Timings SRAM 1 WS (BCR Controlled)

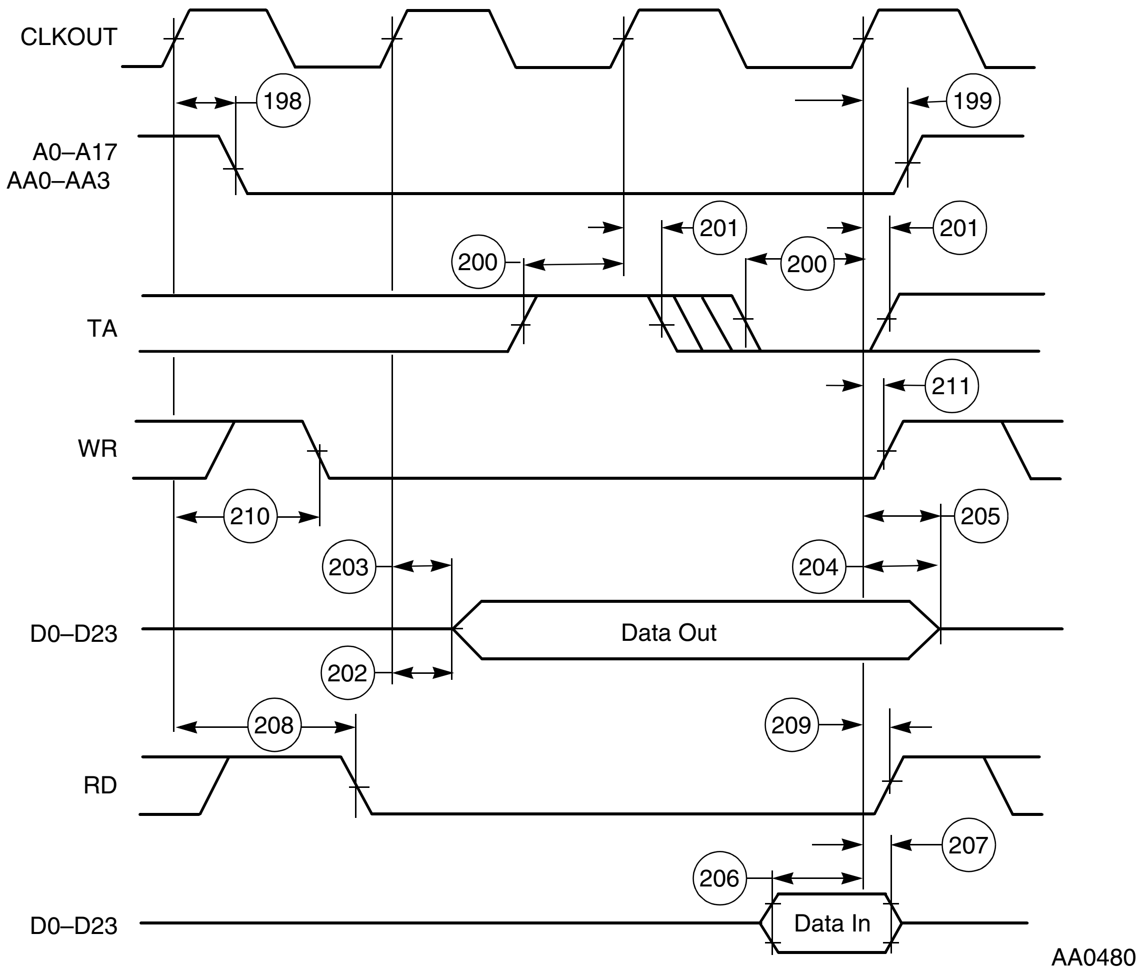


Figure 3-21 Synchronous Bus Timings SRAM 2 WS ($\overline{TA}$ Controlled)

3.10.4 Arbitration Timings

Table 3-18 Arbitration Bus Timings[1]

No.	Characteristics	Expression	100 MHz		Unit
			Min	Max	
212	CLKOUT high to $\overline{BR}$ assertion/deassertion[2]		1.0	4.0	ns
213	$\overline{BG}$ asserted/deasserted to CLKOUT high (setup)		4.0	—	ns
214	CLKOUT high to $\overline{BG}$ deasserted/asserted (hold)		0.0	—	ns
215	$\overline{BB}$ deassertion to CLKOUT high (input setup)		4.0	—	ns
216	CLKOUT high to $\overline{BB}$ assertion (input hold)		0.0	—	ns
217	CLKOUT high to $\overline{BB}$ assertion (output)		1.0	4.0	ns

Table 3-18 Arbitration Bus Timings[1] (continued)

No.	Characteristics	Expression	100 MHz		Unit
			Min	Max	
218	CLKOUT high to $\overline{BB}$ deassertion (output)		1.0	4.0	ns
219	$\overline{BB}$ high to $\overline{BB}$ high impedance (output)		—	4.5	ns
220	CLKOUT high to address and controls active	$0.25 \times T_C$	2.5	—	ns
221	CLKOUT high to address and controls high impedance	$0.25 \times T_C$	—	2.5	ns
222	CLKOUT high to AA active	$0.25 \times T_C$	2.5	—	ns
223	CLKOUT high to AA deassertion	$0.25 \times T_C + 4.0$	3.2	6.5	ns
224	CLKOUT high to AA high impedance	$0.75 \times T_C$	—	7.5	ns

1 The asynchronous delays specified in the expressions are valid for DSP56362.

2 T212 is valid for Address Trace mode when the ATE bit in the OMR is set. $\overline{BR}$ is deasserted for internal accesses and asserted for external accesses.

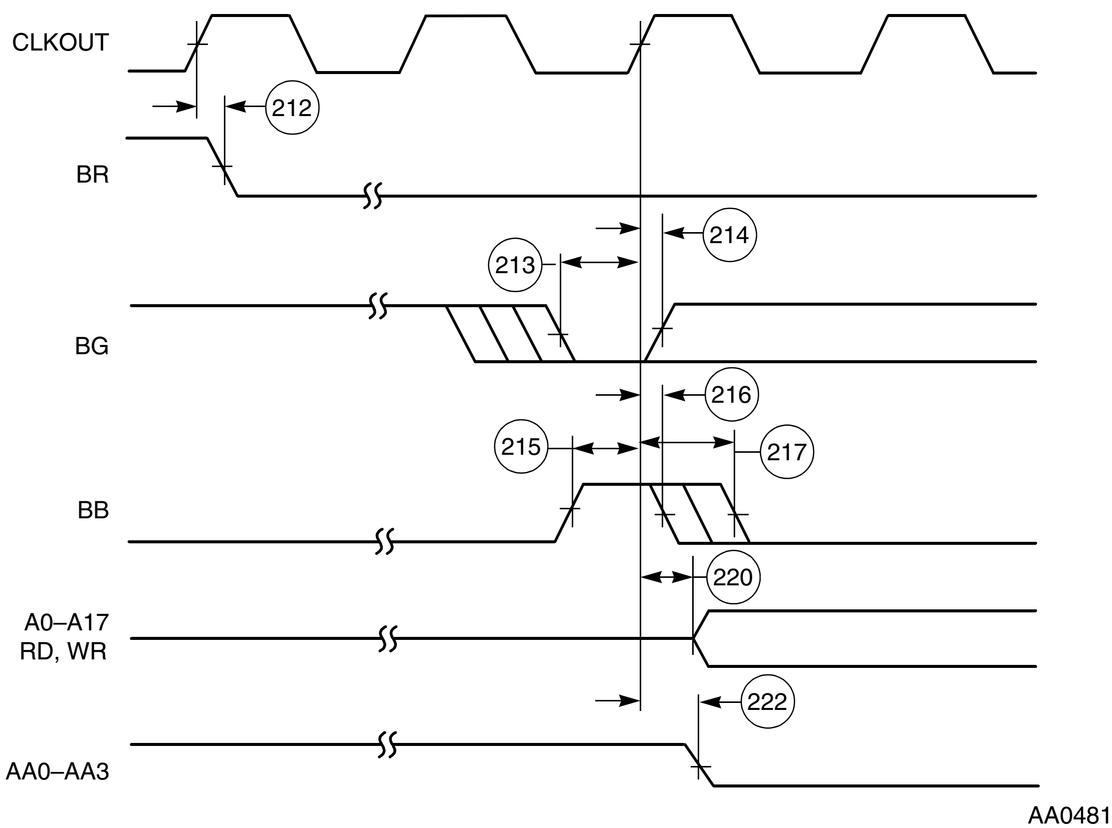


Figure 3-22 Bus Acquisition Timings

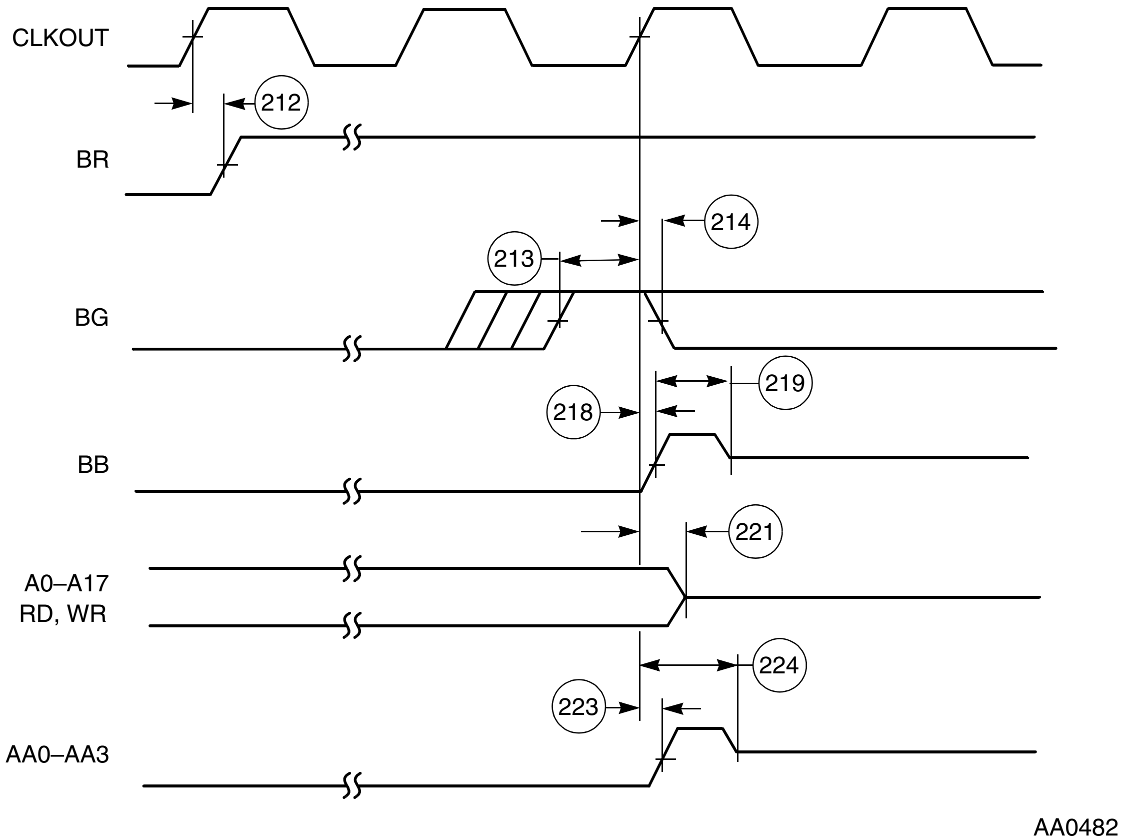


Figure 3-23 Bus Release Timings Case 1 (BRT Bit in OMR Cleared)

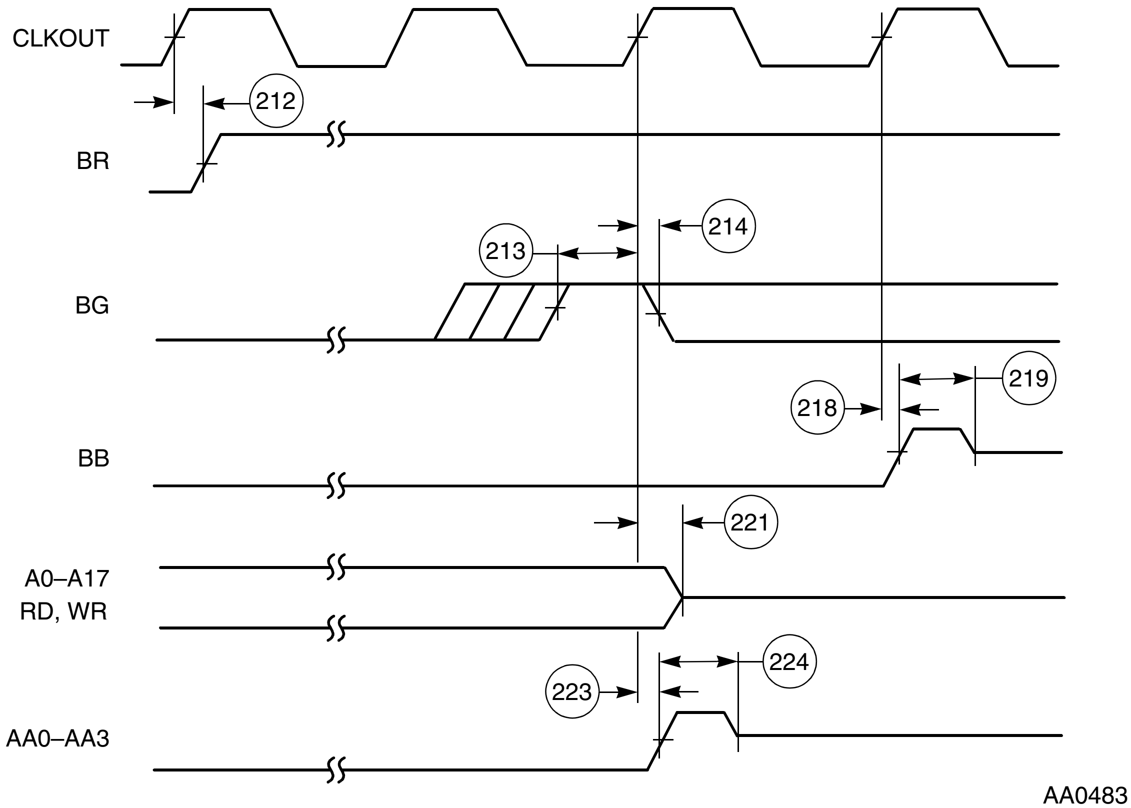


Figure 3-24 Bus Release Timings Case 2 (BRT Bit in OMR Set)

Table 3-19 Asynchronous Bus Arbitration timing

No.	Characteristics	Expression	100 MHz		Unit
			Min	Max	
250	BB assertion window from BG input negation.	2 .5* Tc + 5	—	20	ns
251	Delay from BB assertion to BG assertion	2 * Tc + 5	20	—	ns

Notes:
1. Bit 13 in the OMR register must be set to enter Asynchronous Arbitration mode
2. At 100 MHz it is recommended to use Asynchronous Arbitration mode.
3. If Asynchronous Arbitration mode is active, none of the timings in Table 3-19 is required.
4. In order to guarantee timings 250, and 251, it is recommended to assert BG inputs to different 56300 devices (on the same bus) in a non overlap manner as shown in Figure 3-25.

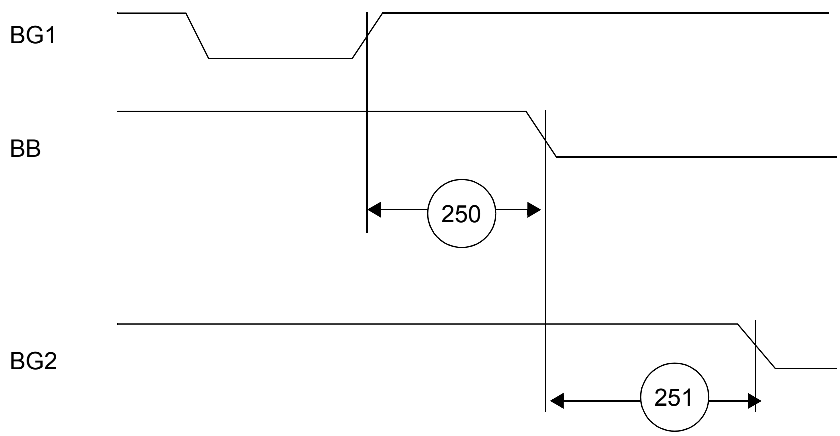


Figure 3-25 Asynchronous Bus Arbitration Timing

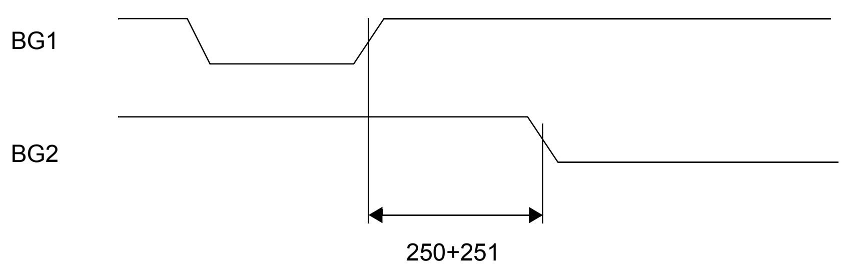


Figure 3-26 Asynchronous Bus Arbitration Timing

Background explanation for Asynchronous Bus Arbitration:

The asynchronous bus arbitration is enabled by internal synchronization circuits on $\overline{BG}$, and $\overline{BB}$ inputs. These synchronization circuits add delay from the external signal until it is exposed to internal logic. As a result of this delay, a 56300 part may assume mastership and assert $\overline{BB}$, for some time after $\overline{BG}$ is negated. This is the reason for timing 250.

Once $\overline{BB}$ is asserted, there is a synchronization delay from $\overline{BB}$ assertion to the time this assertion is exposed to other 56300 components which are potential masters on the same bus. If $\overline{BG}$ input is asserted before that time, a situation of $\overline{BG}$ asserted, and $\overline{BB}$ negated, may cause another 56300 component to assume mastership at the same time. Therefore some non-overlap period between one $\overline{BG}$ input active to another $\overline{BG}$ input active, is required. Timing 251 ensures that such a situation is avoided.

3.11 Parallel Host Interface (HDI08) Timing

Table 3-20 Host Interface (HDI08) Timing[1, 2]

No.	Characteristics[3]	Expression	100 MHz		Unit
			Min	Max	
317	Read data strobe assertion width[4] $\overline{HACK}$ read assertion width	$T_C + 9.9$	19.9	—	ns
318	Read data strobe deassertion width[4] $\overline{HACK}$ read deassertion width	—	9.9	—	ns
319	Read data strobe deassertion width[4] after "Last Data Register" reads[5, 6], or between two consecutive CVR, ICR, or ISR reads[7] $\overline{HACK}$ deassertion width after "Last Data Register" reads[5, 6]	$2.5 \times T_C + 6.6$	31.6	—	ns
320	Write data strobe assertion width[8]$\overline{HACK}$ write assertion width	—	13.2	—	ns
321	Write data strobe deassertion width[8] $\overline{HACK}$ write deassertion width after ICR, CVR and "Last Data Register" writes[5]	$2.5 \times T_C + 6.6$	31.6	—	ns
	after IVR writes, or after TXH:TXM writes (with HBE=0), or after TXL:TXM writes (with HBE=1)		16.5	—	
322	$\overline{HAS}$ assertion width	—	9.9	—	ns
323	$\overline{HAS}$ deassertion to data strobe assertion[9]	—	0.0	—	ns
324	Host data input setup time before write data strobe deassertion[8] Host data input setup time before $\overline{HACK}$ write deassertion	—	9.9	—	ns
325	Host data input hold time after write data strobe deassertion[8] Host data input hold time after $\overline{HACK}$ write deassertion	—	3.3	—	ns
326	Read data strobe assertion to output data active from high impedance[4] $\overline{HACK}$ read assertion to output data active from high impedance	—	3.3	—	ns
327	Read data strobe assertion to output data valid[4] $\overline{HACK}$ read assertion to output data valid	—	—	24.2	ns
328	Read data strobe deassertion to output data high impedance[4] $\overline{HACK}$ read deassertion to output data high impedance	—	—	9.9	ns
329	Output data hold time after read data strobe deassertion[4] Output data hold time after $\overline{HACK}$ read deassertion	—	3.3	—	ns
330	$\overline{HCS}$ assertion to read data strobe deassertion[4]	$T_C + 9.9$	19.9	—	ns
331	$\overline{HCS}$ assertion to write data strobe deassertion[8]	—	9.9	—	ns
332	$\overline{HCS}$ assertion to output data valid	—	—	19.1	ns

Table 3-20 Host Interface (HDI08) Timing[1, 2] (continued)

No.	Characteristics[3]	Expression	100 MHz		Unit
			Min	Max	
333	$\overline{HCS}$ hold time after data strobe deassertion[9]	—	0.0	—	ns
334	Address (AD7–AD0) setup time before $\overline{HAS}$ deassertion (HMUX=1)	—	4.7	—	ns
335	Address (AD7–AD0) hold time after $\overline{HAS}$ deassertion (HMUX=1)	—	3.3	—	ns
336	A10–A8 (HMUX=1), A2–A0 (HMUX=0), HR/$\overline{W}$ setup time before data strobe assertion[9] • Read • Write	—	 0 4.7	 — —	ns
337	A10–A8 (HMUX=1), A2–A0 (HMUX=0), HR/$\overline{W}$ hold time after data strobe deassertion[9]	—	3.3	—	ns
338	Delay from read data strobe deassertion to host request assertion for “Last Data Register” read[4, 5, 10]	T_C	10	—	ns
339	Delay from write data strobe deassertion to host request assertion for “Last Data Register” write[5, 8, 10]	$2 \times T_C$	20	—	ns
340	Delay from data strobe assertion to host request deassertion for “Last Data Register” read or write (HROD = 0)[5, 9, 10]	—	—	19.1	ns
341	Delay from data strobe assertion to host request deassertion for “Last Data Register” read or write (HROD = 1, open drain Host Request)[5, 9, 10, 11]	—	—	300.0	ns
342	Delay from DMA $\overline{HACK}$ deassertion to HOREQ assertion • For “Last Data Register” read[5] • For “Last Data Register” write[5] • For other cases	 $2 \times T_C + 19.1$ $1.5 \times T_C + 19.1$	 39.1 34.1 0.0	 — — —	ns
343	Delay from DMA $\overline{HACK}$ assertion to HOREQ deassertion • HROD = 0[5]	—	 —	 20.2	ns
344	Delay from DMA $\overline{HACK}$ assertion to HOREQ deassertion for “Last Data Register” read or write • HROD = 1, open drain Host Request[5, 11]	—	 —	 300.0	ns

1 See **Host Port Usage Considerations** in the DSP56362 User Design Manual.
2 In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.
3 $V_{CC} = 3.3$ V ± 0.16 V; $T_J = 0$°C to +100°C, $C_L = 50$ pF
4 The read data strobe is HRD in the dual data strobe mode and HDS in the single data strobe mode.
5 The “last data register” is the register at address \$7, which is the last location to be read or written in data transfers. This is RXL/TXL in the little endian mode (HBE = 0), or RXH/TXH in the big endian mode (HBE = 1).
6 This timing is applicable only if a read from the “last data register” is followed by a read from the RXL, RXM, or RXH registers without first polling RXDF or HREQ bits, or waiting for the assertion of the HOREQ signal.
7 This timing is applicable only if two consecutive reads from one of these registers are executed.

8 The write data strobe is HWR in the dual data strobe mode and HDS in the single data strobe mode.
9 The data strobe is host read (HRD) or host write (HWR) in the dual data strobe mode and host data strobe (HDS) in the single data strobe mode.
10 The host request is HOREQ in the single host request mode and HRRQ and HTRQ in the double host request mode.
11 In this calculation, the host request signal is pulled up by a 4.7 kΩ resistor in the open-drain mode.

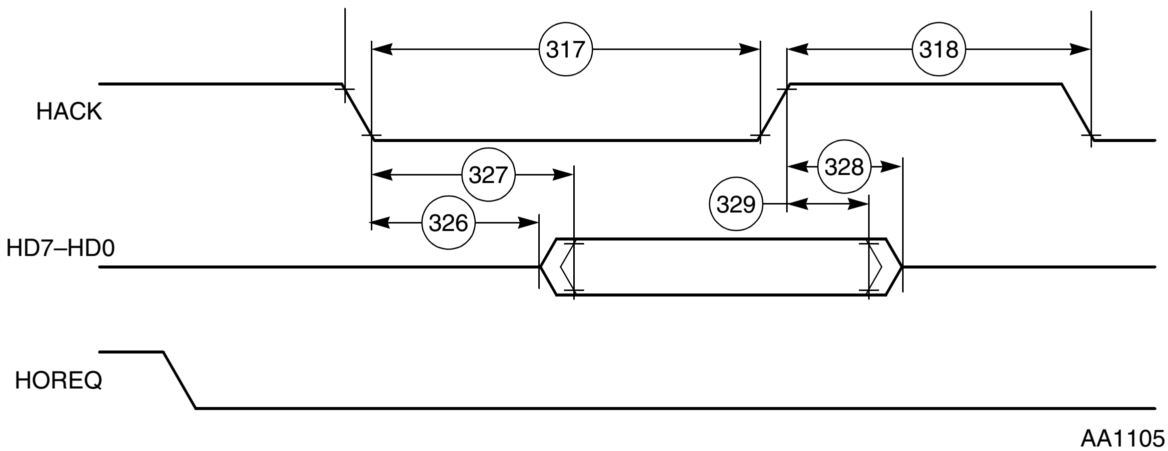


Figure 3-27 Host Interrupt Vector Register (IVR) Read Timing Diagram

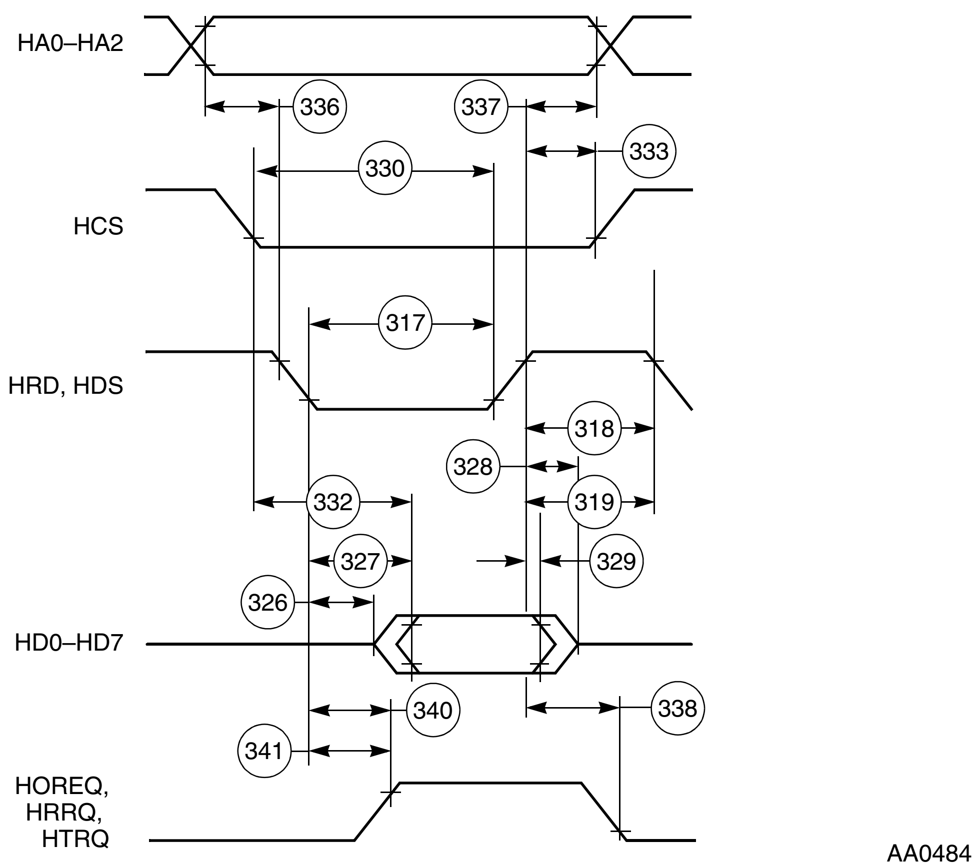


Figure 3-28 Read Timing Diagram, Non-Multiplexed Bus

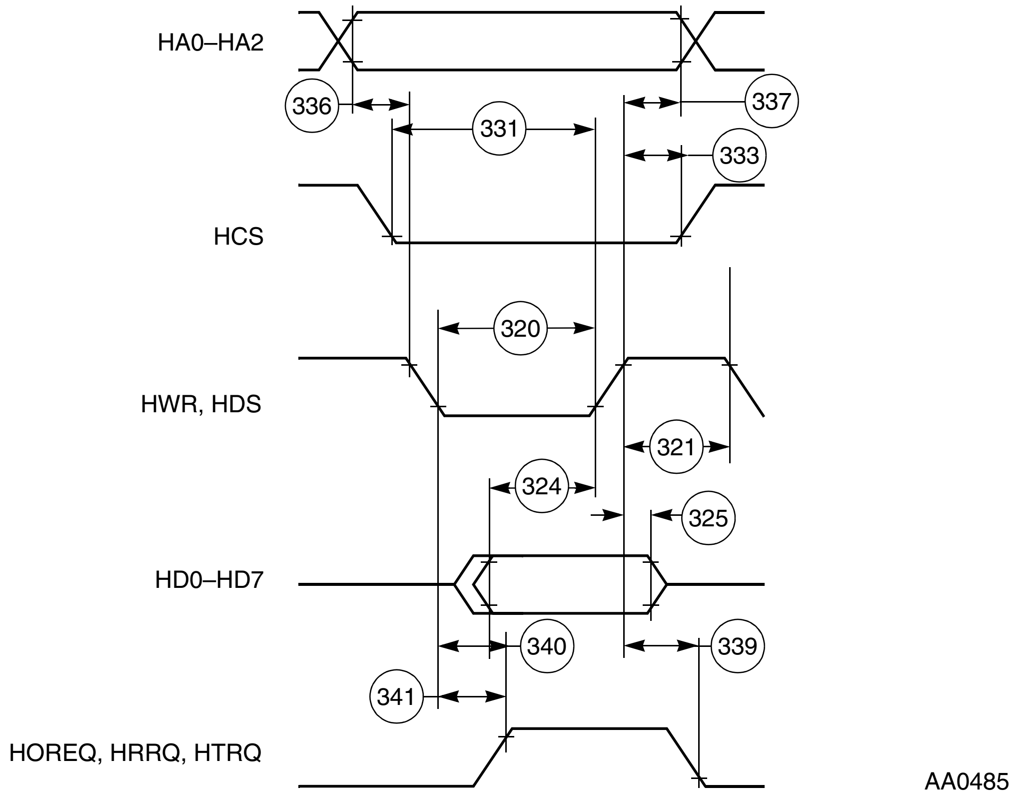


Figure 3-29 Write Timing Diagram, Non-Multiplexed Bus

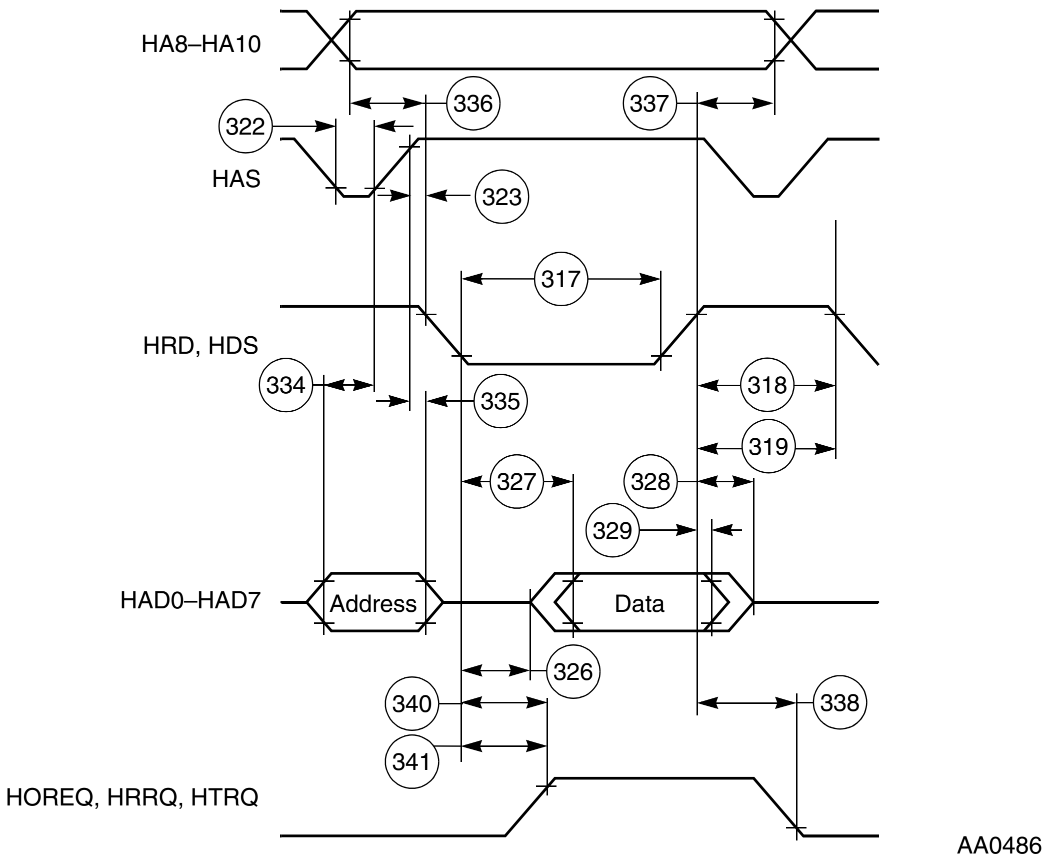


Figure 3-30 Read Timing Diagram, Multiplexed Bus

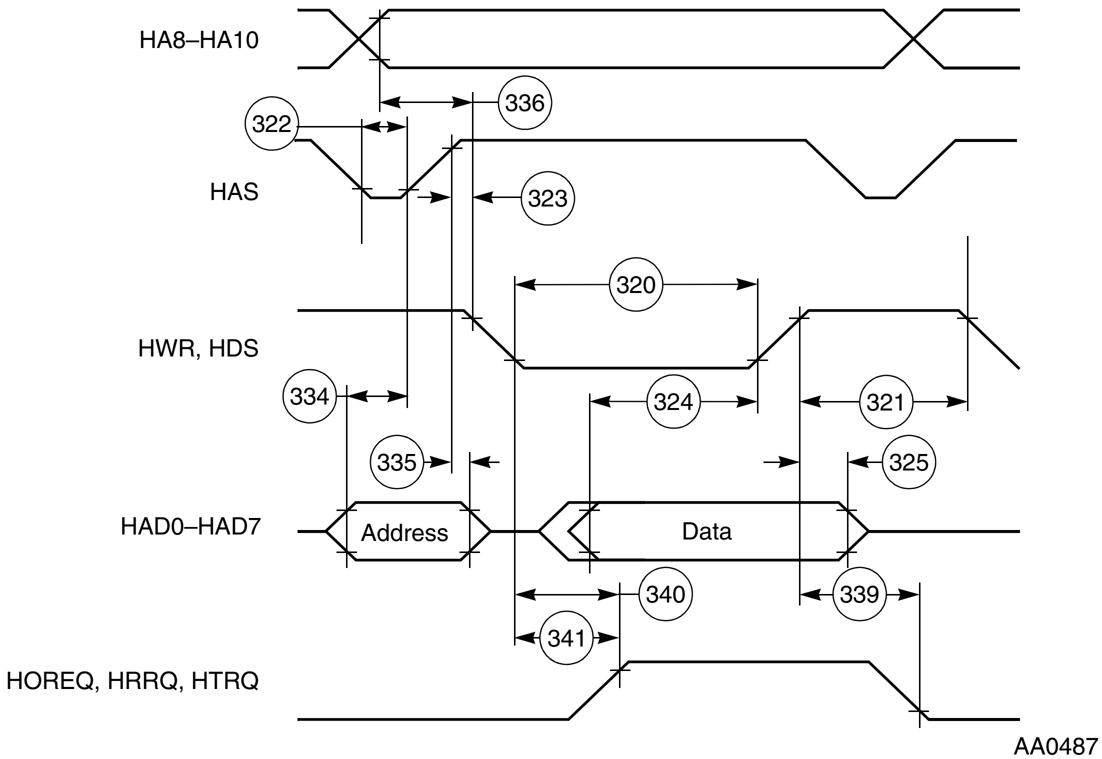


Figure 3-31 Write Timing Diagram, Multiplexed Bus

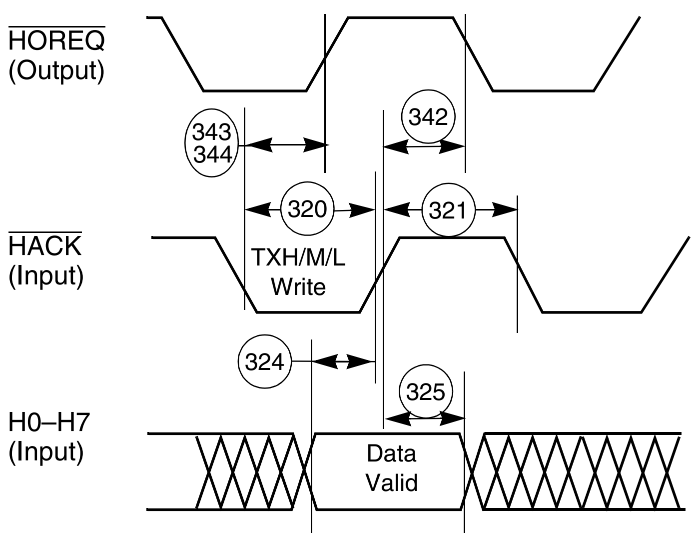


Figure 3-32 Host DMA Write Timing Diagram

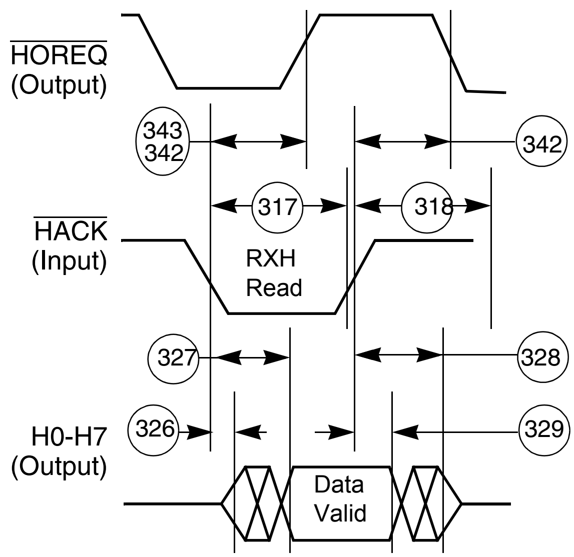


Figure 3-33 Host DMA Read Timing Diagram

3.12 Serial Host Interface SPI Protocol Timing

Table 3-21 Serial Host Interface SPI Protocol Timing

No.	Characteristics	Mode	Filter Mode	Expression	100MHz		Unit
					Min	Max	
140	Tolerable spike width on clock or data in	—	Bypassed Narrow Wide	—	— — —	0 50 100	ns
141	Minimum serial clock cycle = t_{SPICC}(min)	Master	Bypassed Narrow Wide	$6\times T_C+46$ $6\times T_C+152$ $6\times T_C+223$	106 212 283	— — —	ns
142	Serial clock high period	Master	Bypassed Narrow Wide	$0.5\times t_{SPICC}-10$ $0.5\times t_{SPICC}-10$ $0.5\times t_{SPICC}-10$	43 96 131	— — —	ns
		Slave	Bypassed Narrow Wide	$2.5\times T_C+12$ $2.5\times T_C+102$ $2.5\times T_C+189$	37 127 214	— — —	
143	Serial clock low period	Master	Bypassed Narrow Wide	$0.5\times t_{SPICC}-10$ $0.5\times t_{SPICC}-10$ $0.5\times t_{SPICC}-10$	43 96 131	— — —	ns
		Slave	Bypassed Narrow Wide	$2.5\times T_C+12$ $2.5\times T_C+102$ $2.5\times T_C+189$	37 127 214	— — —	

Table 3-21 Serial Host Interface SPI Protocol Timing (continued)

No.	Characteristics	Mode	Filter Mode	Expression	100MHz		Unit
					Min	Max	
144	Serial clock rise/fall time	Master	—	—	—	10	ns
		Slave	—	—	—	2000	
146	$\overline{SS}$ assertion to first SCK edge CPHA = 0	Slave	Bypassed Narrow Wide	$3.5 \times T_C + 15$ 0 0	50 0 0	— — —	ns
	CPHA = 1	Slave	Bypassed Narrow Wide	10 0 0	10 0 0	— — —	
147	Last SCK edge to $\overline{SS}$ not asserted	slave	Bypassed Narrow Wide	12 102 189	12 102 189	— — —	ns
148	Data input valid to SCK edge (data input set-up time)	Master/ Slave	Bypassed Narrow Wide	0 $MAX\{(20-T_C), 0\}$ $MAX\{(40-T_C), 0\}$	0 10 30	— — —	ns
149	SCK last sampling edge to data input not valid	Master/ Slave	Bypassed Narrow Wide	$2.5 \times T_C + 10$ $2.5 \times T_C + 30$ $2.5 \times T_C + 50$	35 55 75	— — —	ns
150	$\overline{SS}$ assertion to data out active	Slave	—	2	2	—	ns
151	$\overline{SS}$ deassertion to data high impedance	Slave	—	9	—	9	ns
152	SCK edge to data out valid (data out delay time)	Master/ Slave	Bypassed Narrow Wide	$2 \times T_C + 33$ $2 \times T_C + 123$ $2 \times T_C + 210$	— — —	53 143 230	ns
153	SCK edge to data out not valid (data out hold time)	Master/ Slave	Bypassed Narrow Wide	$T_C + 5$ $T_C + 55$ $T_C + 106$	15 65 116	— — —	ns
154	$\overline{SS}$ assertion to data out valid (CPHA = 0)	Slave	—	$T_C + 33$	—	43	ns
157	First SCK sampling edge to $\overline{HREQ}$ output deassertion	Slave	Bypassed Narrow Wide	$2.5 \times T_C + 30$ $2.5 \times T_C + 120$ $2.5 \times T_C + 217$	— — —	55 145 242	ns
158	Last SCK sampling edge to $\overline{HREQ}$ output not deasserted (CPHA = 1)	Slave	Bypassed Narrow Wide	$2.5 \times T_C + 30$ $2.5 \times T_C + 80$ $2.5 \times T_C + 136$	55 105 161	— — —	ns

Table 3-21 Serial Host Interface SPI Protocol Timing (continued)

No.	Characteristics	Mode	Filter Mode	Expression	100MHz		Unit
					Min	Max	
159	$\overline{SS}$ deassertion to $\overline{HREQ}$ output not deasserted (CPHA = 0)	Slave	—	$2.5 \times T_C + 30$	55	—	ns
160	$\overline{SS}$ deassertion pulse width (CPHA = 0)	Slave	—	$T_C + 6$	16	—	ns
161	$\overline{HREQ}$ in assertion to first SCK edge	Master	Bypassed Narrow Wide	$0.5 \times t_{SPICC} + 2.5 \times T_C + 43$ $0.5 \times t_{SPICC} + 2.5 \times T_C + 43$ $0.5 \times t_{SPICC} + 2.5 \times T_C + 43$	121 174 209	— — —	ns
162	$\overline{HREQ}$ in deassertion to last SCK sampling edge ($\overline{HREQ}$ in set-up time) (CPHA = 1)	Master	—	0	0	—	ns
163	First SCK edge to $\overline{HREQ}$ in not asserted ($\overline{HREQ}$ in hold time)	Master	—	0	0	—	ns
Note: Periodically sampled, not 100% tested							

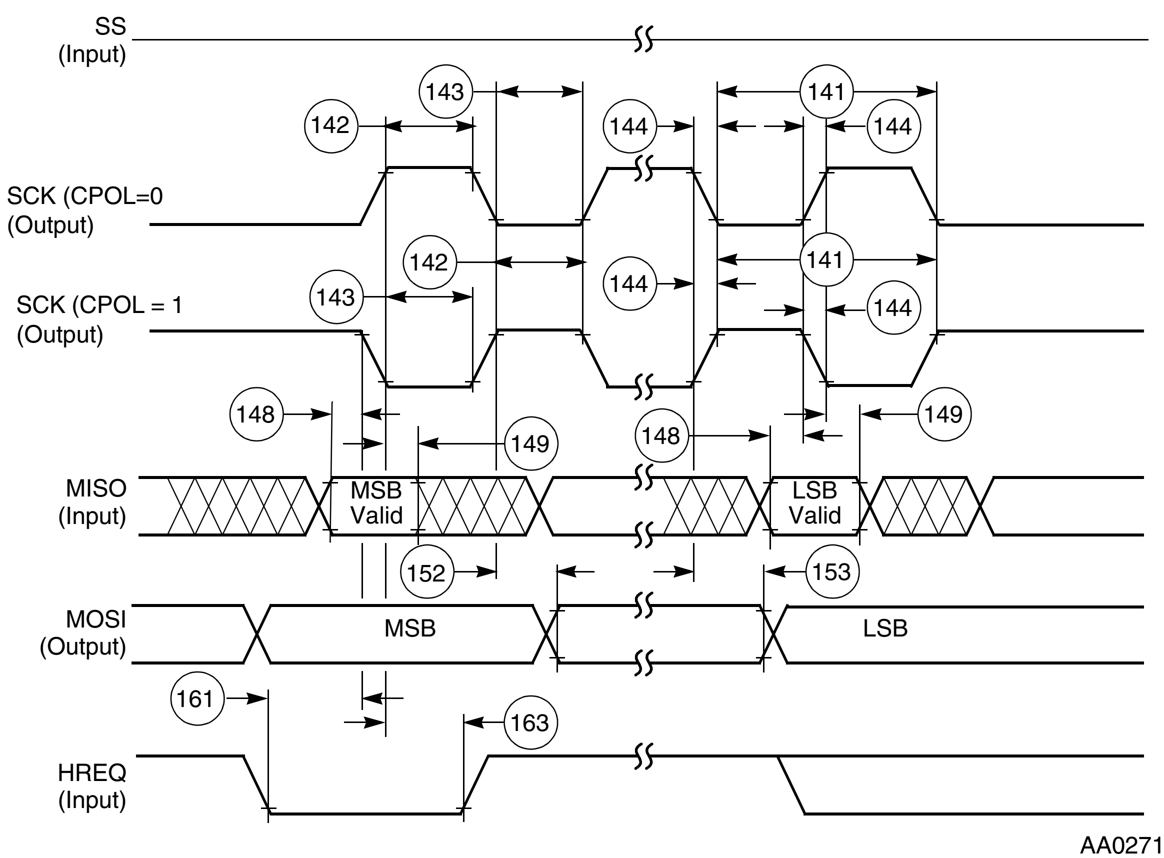


Figure 3-34 SPI Master Timing (CPHA = 0)

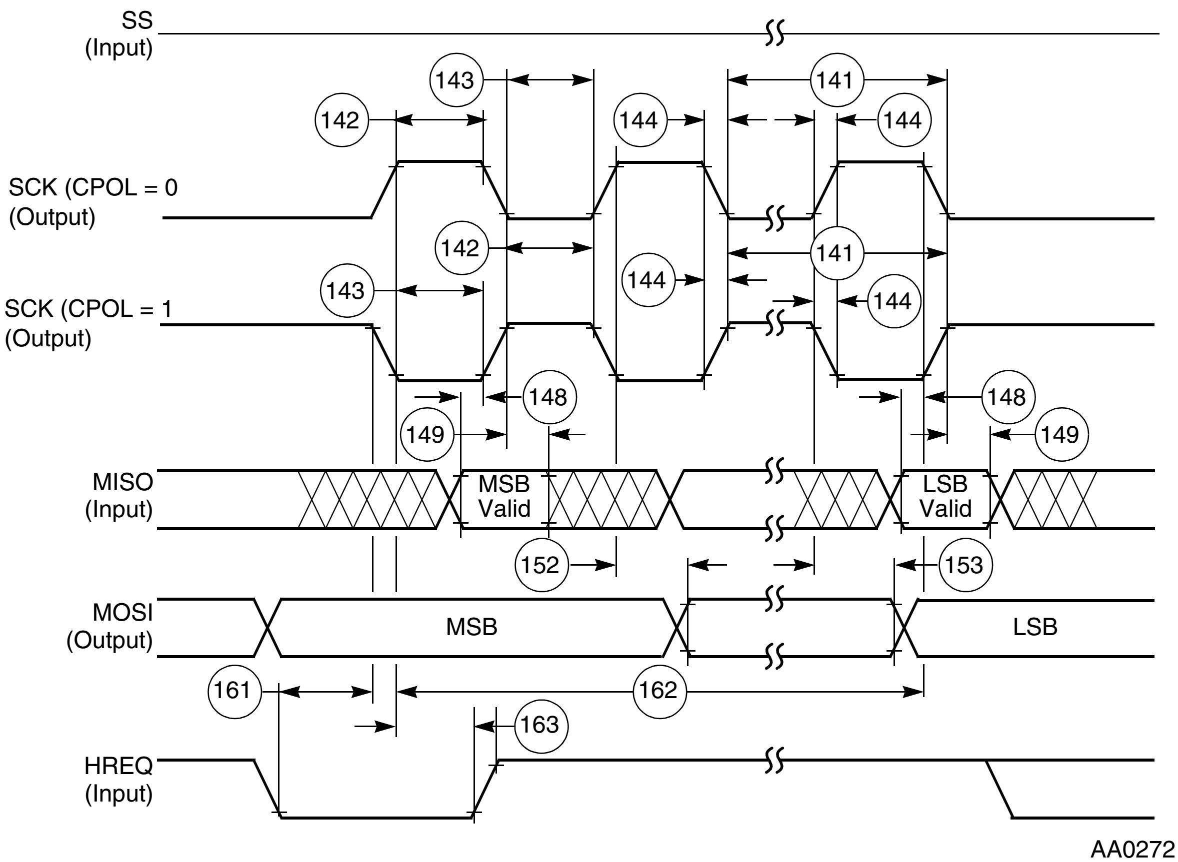


Figure 3-35 SPI Slave Timing (CPHA = 0)

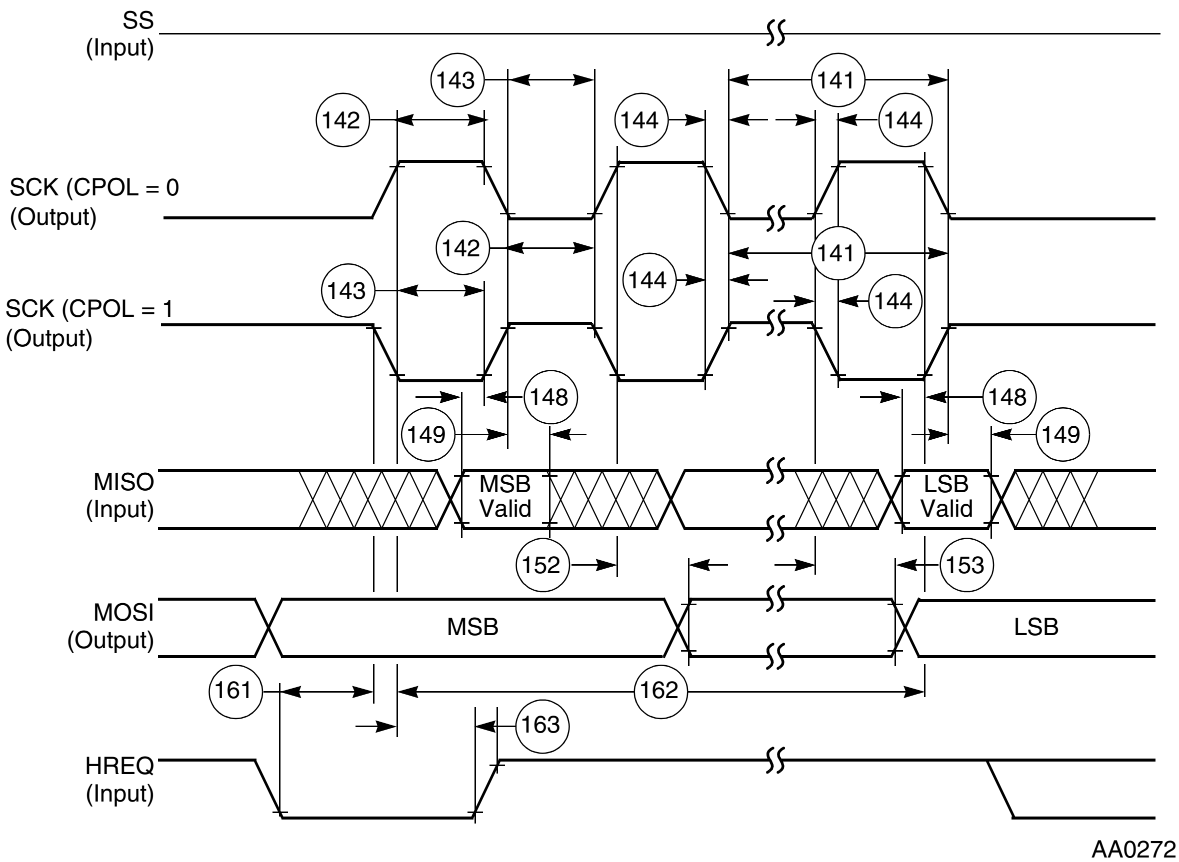


Figure 3-36 SPI Master Timing (CPHA = 1)

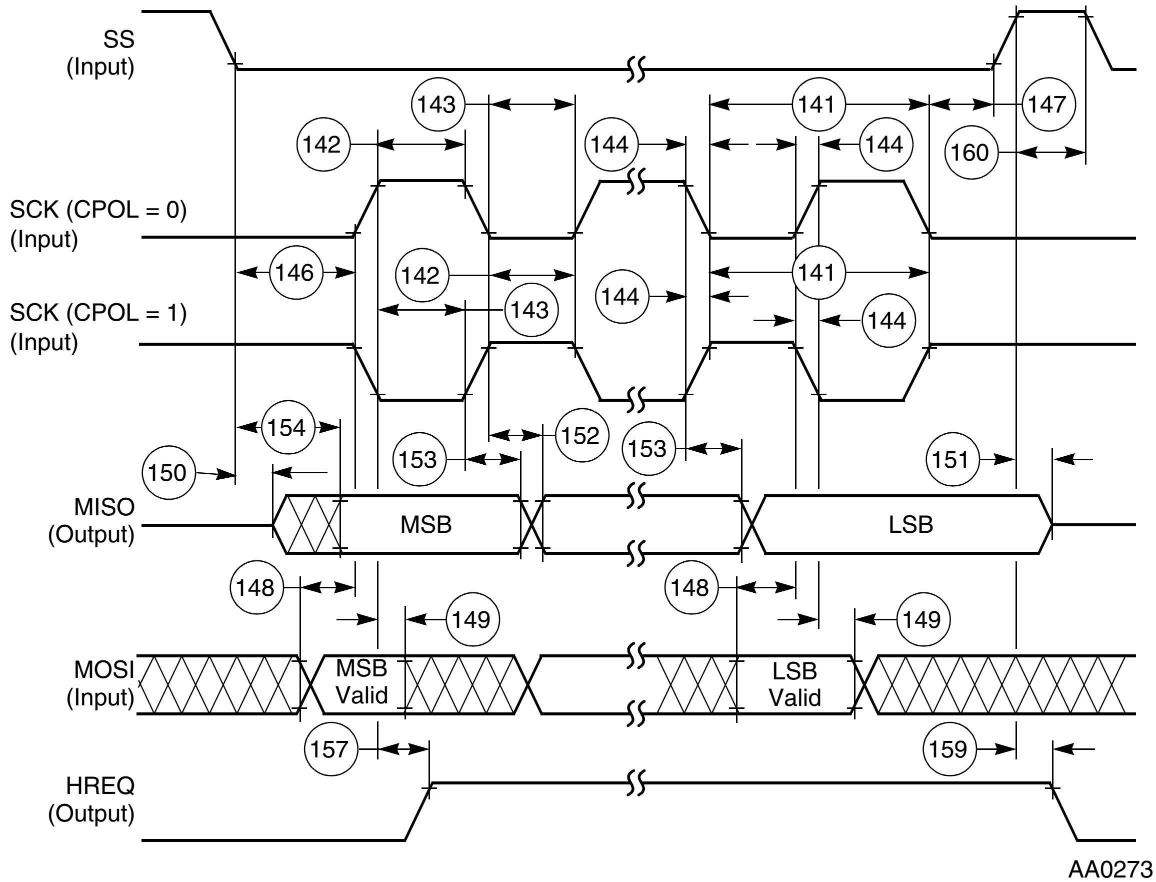


Figure 3-37 SPI Slave Timing (CPHA = 0)

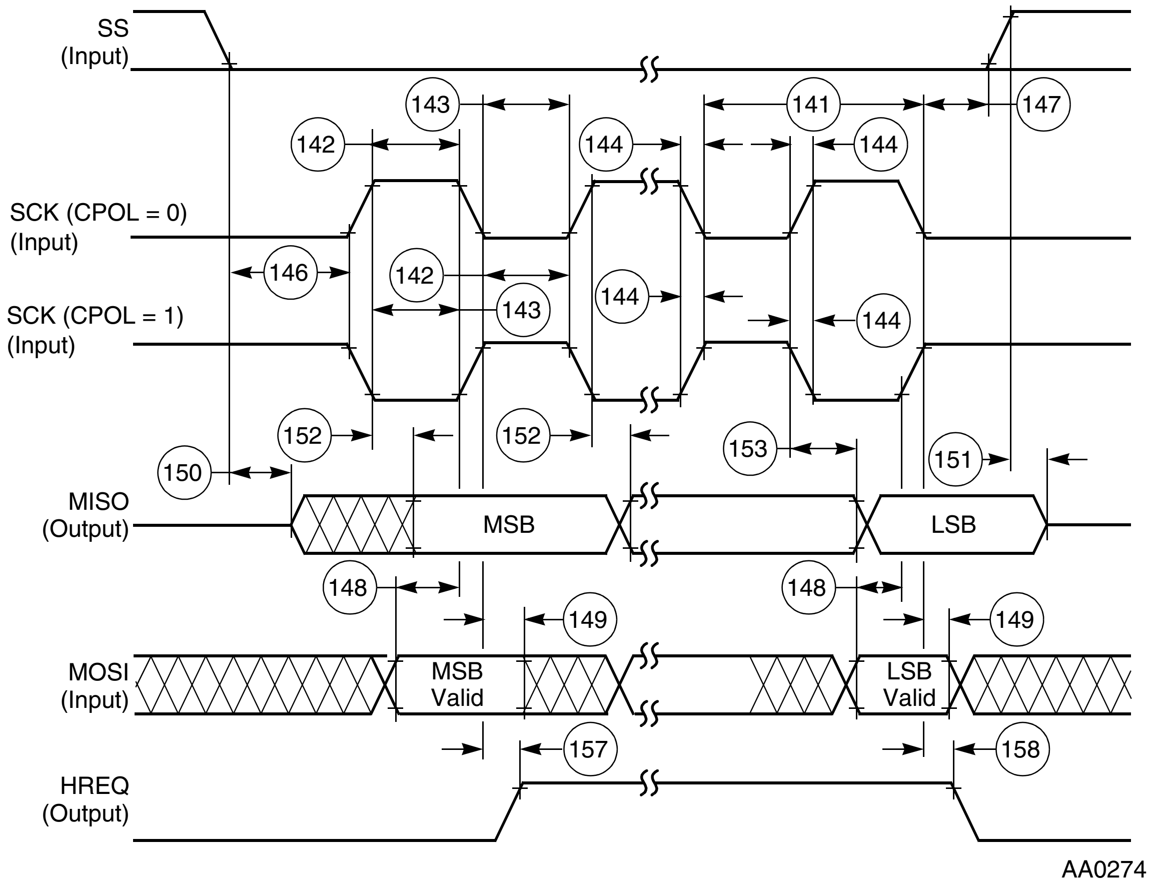


Figure 3-38 SPI Slave Timing (CPHA = 1)

3.13 Serial Host Interface (SHI) I²C Protocol Timing

Table 3-22 SHI I2C Protocol Timing

Standard I2C*							
No.	**Characteristics**	**Symbol/ Expression**	**Standard**		**Fast-Mode**		**Unit**
			Min	**Max**	**Min**	**Max**	
	Tolerable spike width on SCL or SDA Filters bypassed Narrow filters enabled Wide filters enabled	—	 — — —	 0 50 100	 — — —	 0 50 100	ns
171	SCL clock frequency	F_{SCL}	—	100	—	400	kHz
172	Bus free time	T_{BUF}	4.7	—	1.3	—	µs
173	Start condition set-up time	$T_{SU;STA}$	4.7	—	0.6	—	µs
174	Start condition hold time	$T_{HD;STA}$	4.0	—	0.6	—	µs
175	SCL low period	T_{LOW}	4.7	—	1.3	—	µs
176	SCL high period	T_{HIGH}	4.0	—	1.3	—	µs
177	SCL and SDA rise time	T_R	—	1000	$20 + 0.1 \times C_b$	300	ns
178	SCL and SDA fall time	T_F	—	300	$20 + 0.1 \times C_b$	300	ns
179	Data set-up time	$T_{SU;DAT}$	250	—	100	—	ns
180	Data hold time	$T_{HD;DAT}$	0.0	—	0.0	0.9	µs
181	Stop condition set-up time	$T_{SU;STO}$	4.0	—	0.6	—	µs
182	Capacitive load for each line	C_b	—	400	—	400	pF
183	DSP clock frequency Filters bypassed Narrow filters enabled Wide filters enabled	F_{DSP}	 10.6 11.8 13.1	 — — —	 28.5 39.7 61.0	 — — —	MHz
184	$\overline{HREQ}$ in deassertion to last SCL edge ($\overline{HREQ}$ in set-up time)	$t_{SU;RQI}$	0.0	—	0.0	—	ns
186	First SCL sampling edge to $\overline{HREQ}$ output deassertion Filters bypassed Narrow filters enabled Wide filters enabled	$T_{NG;RQO}$ $2 \times T_C + 30$ $2 \times T_C + 120$ $2 \times T_C + 208$	 — — —	 50 140 228	 — — —	 50 140 228	ns

Table 3-22 SHI I2C Protocol Timing (continued)

Standard I2C*							
No.	**Characteristics**	**Symbol/ Expression**	**Standard**		**Fast-Mode**		**Unit**
			Min	**Max**	**Min**	**Max**	
187	Last SCL edge to HREQ output not deasserted	$T_{AS;RQO}$					ns
	Filters bypassed	$2 \times T_C + 30$	50	—	50	—	
	Narrow filters enabled	$2 \times T_C + 80$	100	—	100	—	
	Wide filters enabled	$2 \times T_C + 135$	155	—	155	—	
188	HREQ in assertion to first SCL edge	$T_{AS;RQI}$					ns
	Filters bypassed	$0.5 \times T_{I2CCP}$	4327	—	927	—	
	Narrow filters enabled	—	4282	—	882	—	
	Wide filters enabled	$0.5 \times T_C$ - 21	4238	—	838	—	
Note: R_P (min) = 1.5 k¾							

3.13.1 Programming the Serial Clock

The programmed serial clock cycle, T_{I^2CCP}, is specified by the value of the HDM[5:0] and HRS bits of the HCKR (SHI clock control register).

The expression for T_{I^2CCP} is

$$T_{I^2CCP} = [T_C \times 2 \times (HDM[7:0] + 1) \times (7 \times (1 - HRS) + 1)]$$

where:

HRS is the prescaler rate select bit.

When HRS is cleared, the fixed divide-by-eight prescaler is operational.

When HRS is set, the prescaler is bypassed.

HDM[7:0] are the divider modulus select bits.

A divide ratio from 1 to 64 (HDM[5:0] = 0 to $3F) may be selected.

In I2C mode, the user may select a value for the programmed serial clock cycle from

$$6 \times T_C (\text{if } HDM[5:0] = \$02 \text{ and } HRS = 1)$$

to

$$4096 \times T_C (\text{if } HDM[7:0] = \$FF \text{ and } HRS = 0)$$

The programmed serial clock cycle (T_{I2CCP}), SCL rise time (T_R), and the filters selected should be chosen in order to achieve the desired SCL frequency, as shown in Table 3-23

Table 3-23 SCL Serial Clock Cycle generated as Master

Filters bypassed	$T_{I^2CCP} + 2.5 \times T_C + 45ns + T_R$
Narrow filters enabled	$T_{I^2CCP} + 2.5 \times T_C + 135ns + T_R$
Wide filters enabled	$T_{I^2CCP} + 2.5 \times T_C + 223ns + T_R$

EXAMPLE:

For DSP clock frequency of 100 MHz (i.e. T_C = 10ns), operating in a standard-mode I^{2}C environment (F_{SCL} = 100 KHz (i.e. T_{SCL} = 10µs), T_R = 1000ns), with filters bypassed

$$T_{I^2CCP} = 10\mu s - 2.5 \times 10ns - 45ns - 1000ns = 8930ns$$

Choosing HRS = 0 gives

$$HDM[7:0] = 8930ns/(2 \times 10ns \times 8) - 1 = 55.8$$

Thus the HDM[7:0] value should be programmed to \$38 (=56).

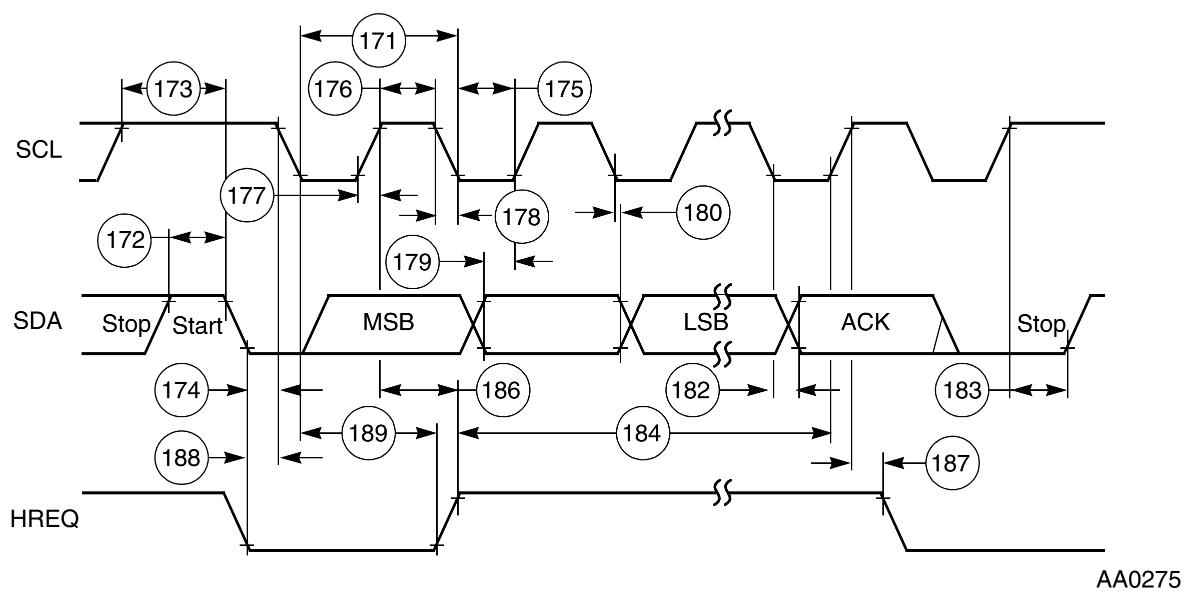


Figure 3-39 I^{2}C Timing

3.14 Enhanced Serial Audio Interface Timing

Table 3-24 Enhanced Serial Audio Interface Timing

No.	Characteristics[1, 2, 3]	Symbol	Expression	100 MHz		Condition[4]	Unit
				Min	Max		
430	Clock cycle[5]	t_{SSICC}	4 x T_C RXC:3 xT_C TXC:MAX [3xT_C;t_{454}]	40.0 30 40	— —	i ck x ck x ck	ns
431	Clock high period • For internal clock • For external clock	—	 $2 \times T_C - 10.0$ $1.5 \times T_C$	 10.0 15.0	 — —		ns
432	Clock low period • For internal clock • For external clock	—	 $2 \times T_C - 10.0$ $1.5 \times T_C$	 10.0 15.0	 — —		ns
433	RXC rising edge to FSR out (bl) high	—	—	— —	37.0 22.0	x ck i ck a	ns
434	RXC rising edge to FSR out (bl) low	—	—	— —	37.0 22.0	x ck i ck a	ns
435	RXC rising edge to FSR out (wr) high[6]	—	—	— —	39.0 24.0	x ck i ck a	ns
436	RXC rising edge to FSR out (wr) low[6]	—	—	 —	39.0 24.0	x ck i ck a	ns
437	RXC rising edge to FSR out (wl) high	—	—	— —	36.0 21.0	x ck i ck a	ns
438	RXC rising edge to FSR out (wl) low	—	—	— —	37.0 22.0	x ck i ck a	ns
439	Data in setup time before RXC (TXC in synchronous mode) falling edge	—	—	0.0 19.0	— —	x ck i ck	ns
440	Data in hold time after RXC falling edge	—	—	5.0 3.0	— —	x ck i ck	ns
441	FSR input (bl, wr) high before RXC falling edge[6]	—	—	23.0 1.0	— —	x ck i ck a	ns
442	FSR input (wl) high before RXC falling edge	—	—	1.0 23.0	— —	x ck i ck a	ns

Table 3-24 Enhanced Serial Audio Interface Timing (continued)

No.	Characteristics[1, 2, 3]	Symbol	Expression	100 MHz		Condition[4]	Unit
				Min	Max		
443	FSR input hold time after RXC falling edge	—	—	3.0 0.0	— —	x ck i ck a	ns
444	Flags input setup before RXC falling edge	—	—	0.0 19.0	— —	x ck i ck s	ns
445	Flags input hold time after RXC falling edge	—	—	6.0 0.0	— —	x ck i ck s	ns
446	TXC rising edge to FST out (bl) high	—	—	— —	29.0 15.0	x ck i ck	ns
447	TXC rising edge to FST out (bl) low	—	—	— —	31.0 17.0	x ck i ck	ns
448	TXC rising edge to FST out (wr) high[6]	—	—	— —	31.0 17.0	x ck i ck	ns
449	TXC rising edge to FST out (wr) low[6]	—	—	— —	33.0 19.0	x ck i ck	ns
450	TXC rising edge to FST out (wl) high	—	—	— —	30.0 16.0	x ck i ck	ns
451	TXC rising edge to FST out (wl) low	—	—	— —	31.0 17.0	x ck i ck	ns
452	TXC rising edge to data out enable from high impedance	—	—	— —	31.0 17.0	x ck i ck	ns
453	TXC rising edge to transmitter drive enable assertion	—	—	— —	34.0 20.0	x ck i ck	ns
454	TXC rising edge to data out valid	—	$23 + 0.5 \times T_C$ 21.0	— —	28.0 21.0	x ck i ck	ns
455	TXC rising edge to data out high impedance[7]	—	—	— —	31.0 16.0	x ck i ck	ns
456	TXC rising edge to transmitter drive enable deassertion[7]	—	—	— —	34.0 20.0	x ck i ck	ns
457	FST input (bl, wr) setup time before TXC falling edge[6]	—	—	2.0 21.0	— —	x ck i ck	ns

Table 3-24 Enhanced Serial Audio Interface Timing (continued)

No.	Characteristics[1, 2, 3]	Symbol	Expression	100 MHz		Condition[4]	Unit
				Min	Max		
458	FST input (wl) to data out enable from high impedance	—	—	—	27.0	—	ns
459	FST input (wl) to transmitter drive enable assertion	—	—	—	31.0	—	ns
460	FST input (wl) setup time before TXC falling edge	—	—	2.0 21.0	— —	x ck i ck	ns
461	FST input hold time after TXC falling edge	—	—	4.0 0.0	— —	x ck i ck	ns
462	Flag output valid after TXC rising edge	—	—	— —	32.0 18.0	x ck i ck	ns
463	HCKR/HCKT clock cycle	—	—	40.0	—		ns
464	HCKT input rising edge to TXC output	—	—	—	27.5		ns
465	HCKR input rising edge to RXC output	—	—	—	27.5		ns

1 V_{CC} = 3.3 V ± 0.16 V; T_J = 0°C to +100°C, C_L = 50 pF

2 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode (asynchronous implies that TXC and RXC are two different clocks)
i ck s = internal clock, synchronous mode (synchronous implies that TXC and RXC are the same clock)

3 bl = bit length
wl = word length
wr = word length relative

4 TXC(SCKT pin) = transmit clock
RXC(SCKR pin) = receive clock
FST(FST pin) = transmit frame sync
FSR(FSR pin) = receive frame sync
HCKT(HCKT pin) = transmit high frequency clock
HCKR(HCKR pin) = receive high frequency clock

5 For the internal clock, the clock cycle at the pin is defined by Icyc and the ESAI control registers.

6 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but spreads from one serial clock before first bit clock (same as bit length frame sync signal), until the one before last bit clock of the first word in frame.

7 Periodically sampled and not 100% tested.

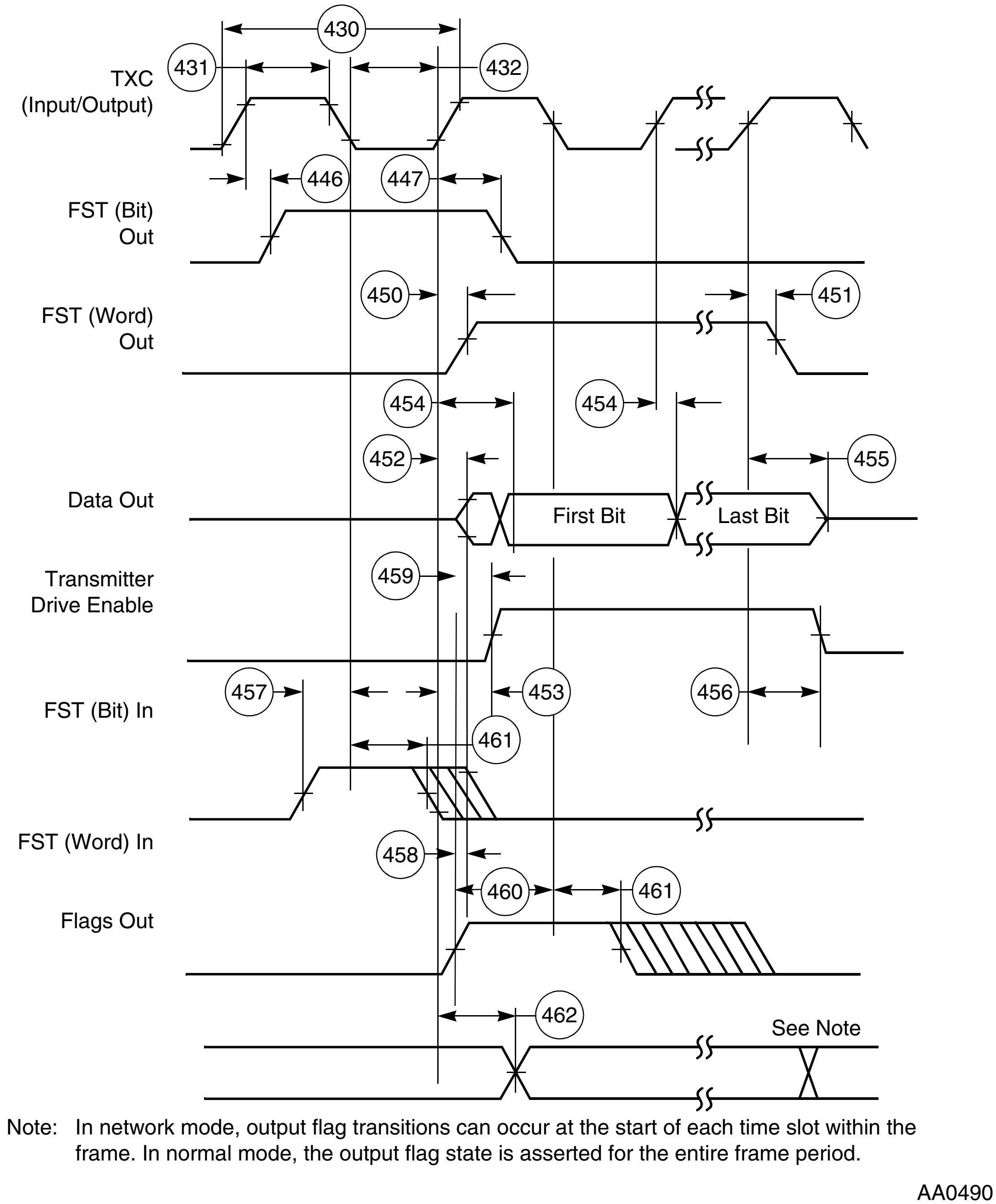


Figure 3-40 ESAI Transmitter Timing

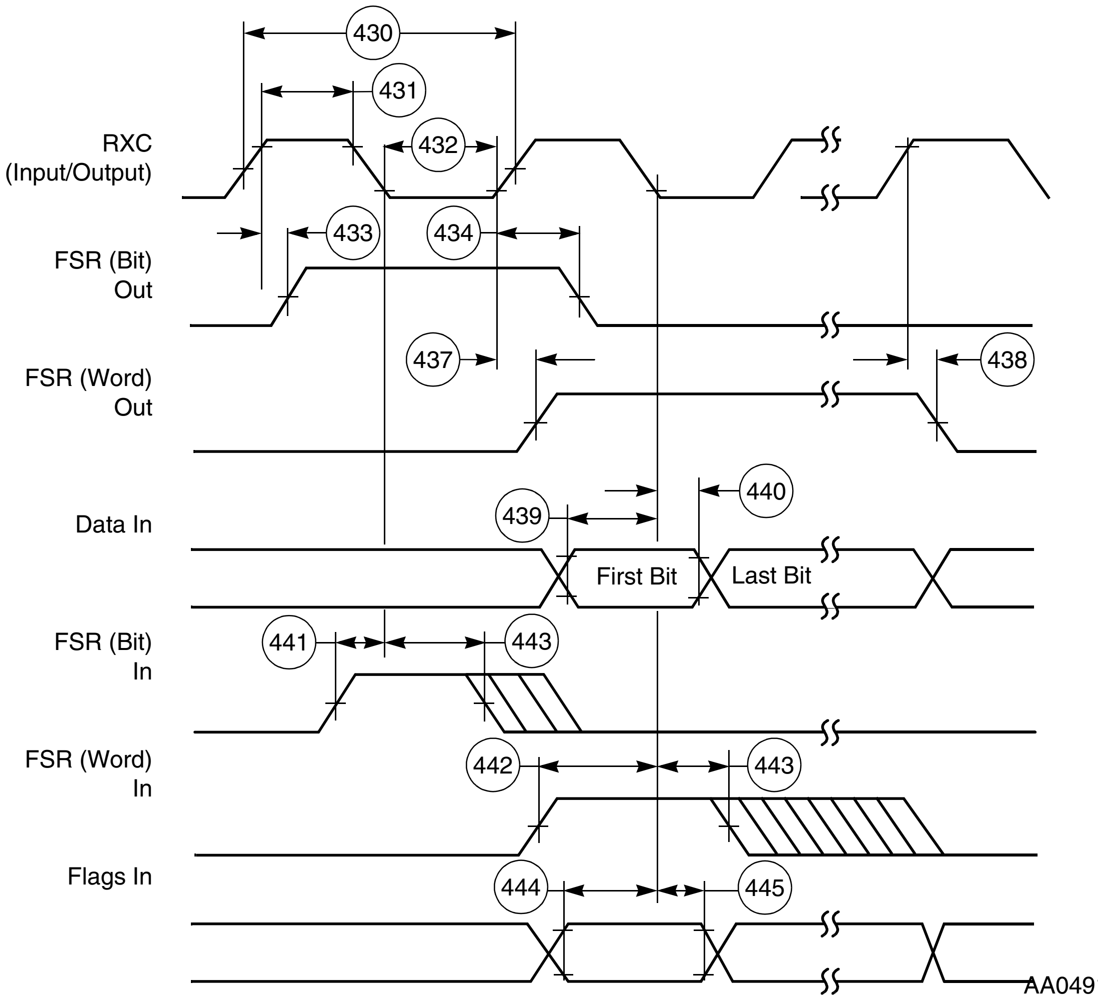


Figure 3-41 ESAI Receiver Timing

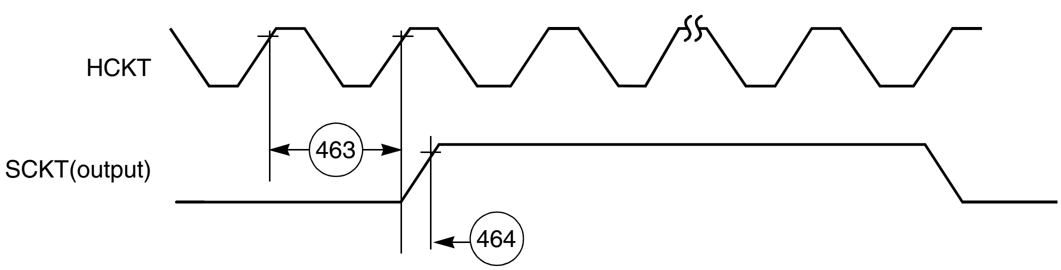


Figure 3-42 ESAI HCKT Timing

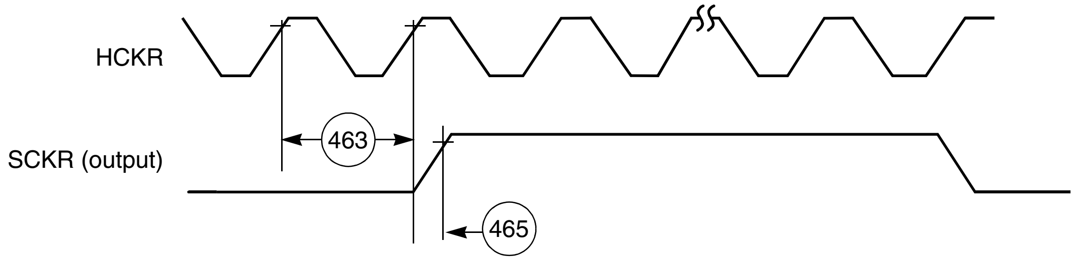


Figure 3-43 ESAI HCKR Timing

3.15 Digital Audio Transmitter Timing

Table 3-25 Digital Audio Transmitter Timing

No.	Characteristic	Expression	100 MHz		Unit
			Min	Max	
	ACI frequency[1]	—	—	50	MHz
220	ACI period	$2 \times T_C$	20	—	ns
221	ACI high duration	$0.5 \times T_C$	5	—	ns
222	ACI low duration	$0.5 \times T_C$	5	—	ns
223	ACI rising edge to ADO valid	$1.5 \times T_C$	—	15	ns

[1] In order to assure proper operation of the DAX, the ACI frequency should be less than 1/2 of the DSP56362 internal clock frequency. For example, if the DSP56362 is running at 100 MHz internally, the ACI frequency should be less than 50 MHz.

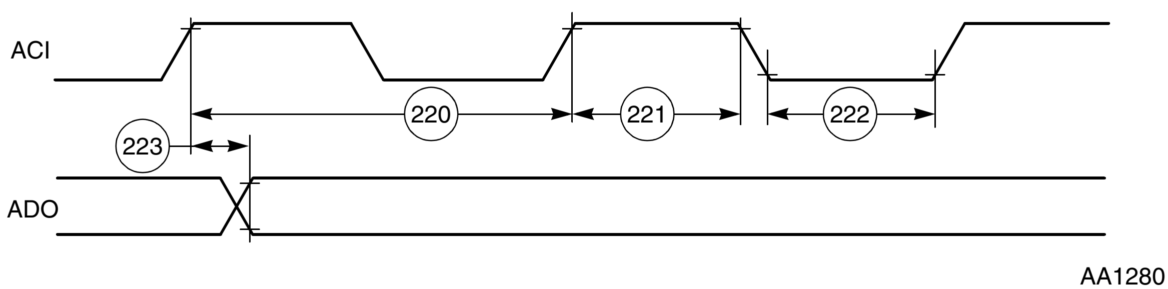


Figure 3-44 Digital Audio Transmitter Timing

3.16 Timer Timing

Table 3-26 Timer Timing[1]

No.	Characteristics	Expression	100 MHz		Unit
			Min	Max	
480	TIO Low	$2 \times T_C + 2.0$	22.0	—	ns
481	TIO High	$2 \times T_C + 2.0$	22.0	—	ns
482	Timer setup time from TIO (Input) assertion to CLKOUT rising edge		9.0	10.0	ns
483	Synchronous timer delay time from CLKOUT rising edge to the external memory access address out valid caused by first interrupt instruction execution	$10.25 \times T_C + 1.0$	103.5	—	ns
484	CLKOUT rising edge to TIO (Output) assertion • Minimum • Maximum	 $0.5 \times T_C + 3.5$ $0.5 \times T_C + 19.8$	 8.5 —	 — 24.8	ns
485	CLKOUT rising edge to TIO (Output) deassertion • Minimum • Maximum	 $0.5 \times T_C + 3.5$ $0.5 \times T_C + 19.0$	 8.5 —	 — 24.8	ns

[1] V_{CC} = 3.3 V ± 0.16 V; T_J = 0°C to +100°C, C_L = 50 pF

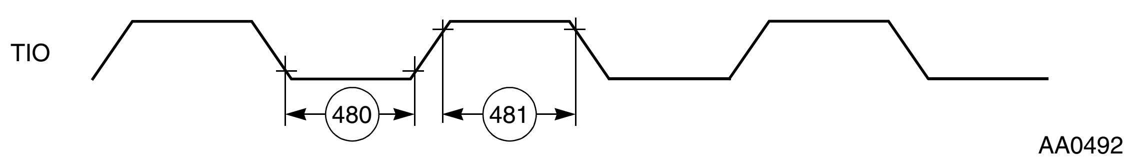


Figure 3-45 TIO Timer Event Input Restrictions

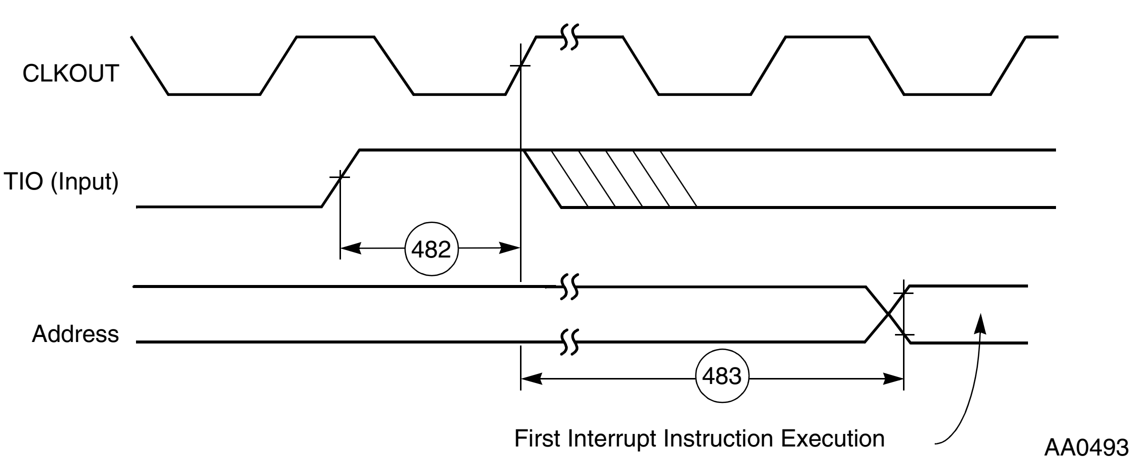


Figure 3-46 Timer Interrupt Generation

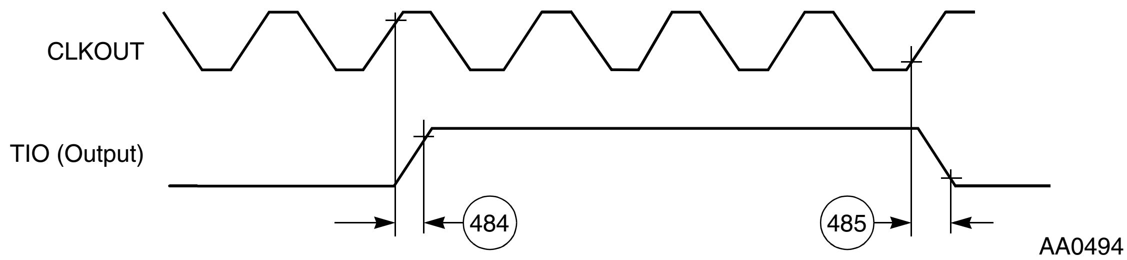


Figure 3-47 External Pulse Generation

3.17 GPIO Timing

Table 3-27 GPIO Timing[1]

No.	Characteristics	Expression	100 MHz		Unit
			Min	Max	
490	CLKOUT edge to GPIO out valid (GPIO out delay time)		—	31.0	ns
491	CLKOUT edge to GPIO out not valid (GPIO out hold time)		3.0	—	ns
492	GPIO In valid to CLKOUT edge (GPIO in set-up time)		12.0	—	ns
493	CLKOUT edge to GPIO in not valid (GPIO in hold time)		0.0	—	ns
494	Fetch to CLKOUT edge before GPIO change	$6.75 \times T_C$	67.5	—	ns
495	GPIO out rise time	—	—	13	ns
496	GPIO out fall time	—	—	13	ns

1 V_{CC} = 3.3 V ± 0.16 V; T_J = 0°C to +100°C, C_L = 50 pF

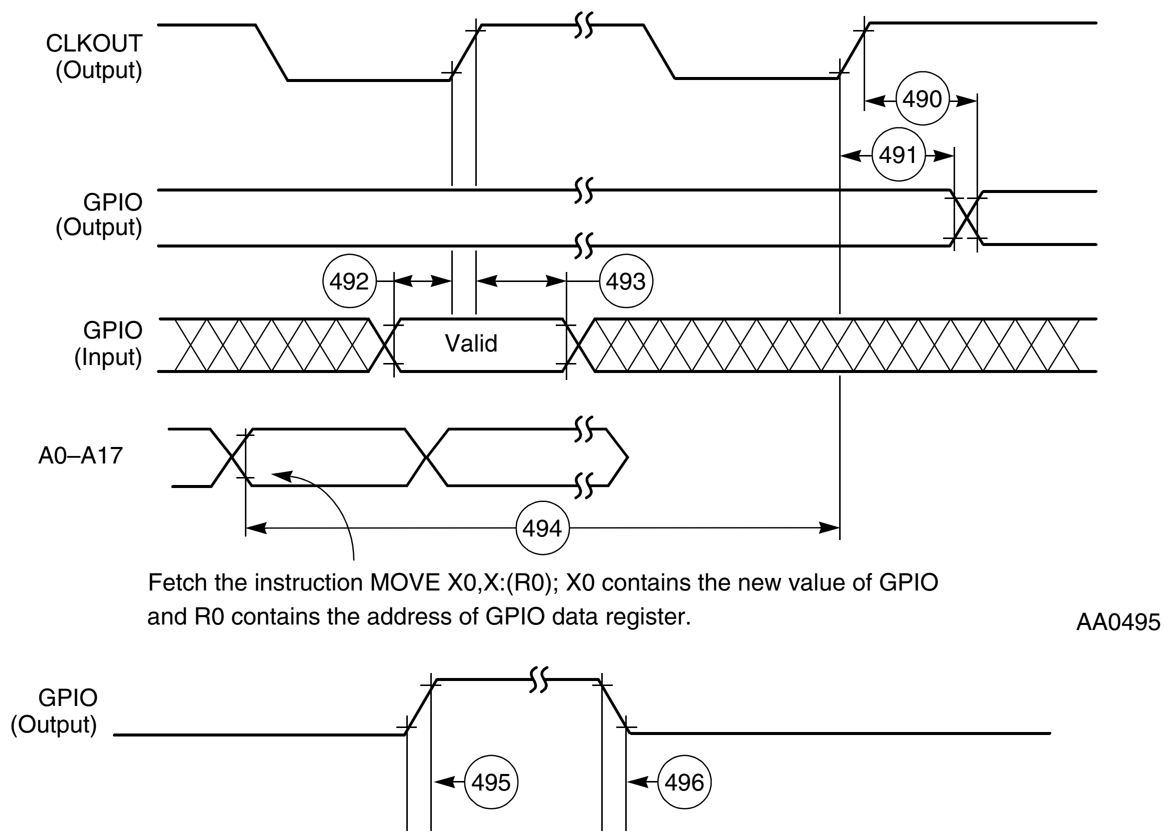


Figure 3-48 GPIO Timing

3.18 JTAG Timing

Table 3-28 JTAG Timing[1, 2]

No.	Characteristics	All Frequencies		Unit
		Min	Max	
500	TCK frequency of operation ($1/(T_C \times 3)$; maximum 22 MHz)	0.0	22.0	MHz
501	TCK cycle time in Crystal mode	45.0	—	ns
502	TCK clock pulse width measured at 1.5 V	20.0	—	ns
503	TCK rise and fall times	0.0	3.0	ns
504	Boundary scan input data setup time	5.0	—	ns
505	Boundary scan input data hold time	24.0	—	ns
506	TCK low to output data valid	0.0	40.0	ns
507	TCK low to output high impedance	0.0	40.0	ns

Table 3-28 JTAG Timing[1, 2] (continued)

No.	Characteristics	All Frequencies		Unit
		Min	Max	
508	TMS, TDI data setup time	5.0	—	ns
509	TMS, TDI data hold time	25.0	—	ns
510	TCK low to TDO data valid	0.0	44.0	ns
511	TCK low to TDO high impedance	0.0	44.0	ns
512	$\overline{\text{TRST}}$ assert time	100.0	—	ns
513	$\overline{\text{TRST}}$ setup time to TCK low	40.0	—	ns

1 V_{CC} = 3.3 V ± 0.16V; T_J = 0°C to +100°C, C_L = 50 pF
2 All timings apply to OnCE module data transfers because it uses the JTAG port as an interface.

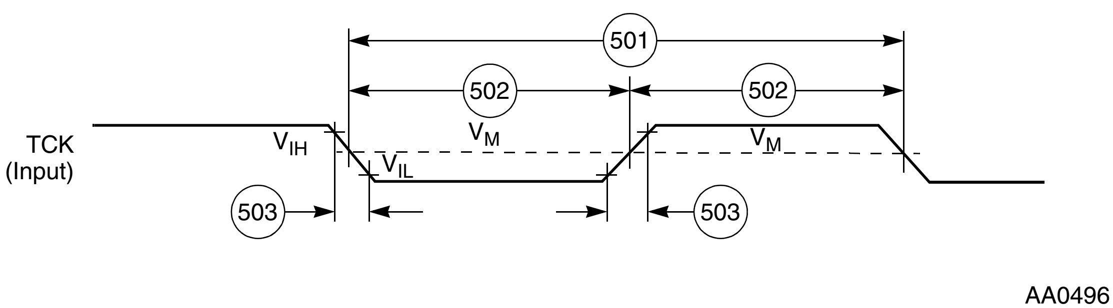


Figure 3-49 Test Clock Input Timing Diagram

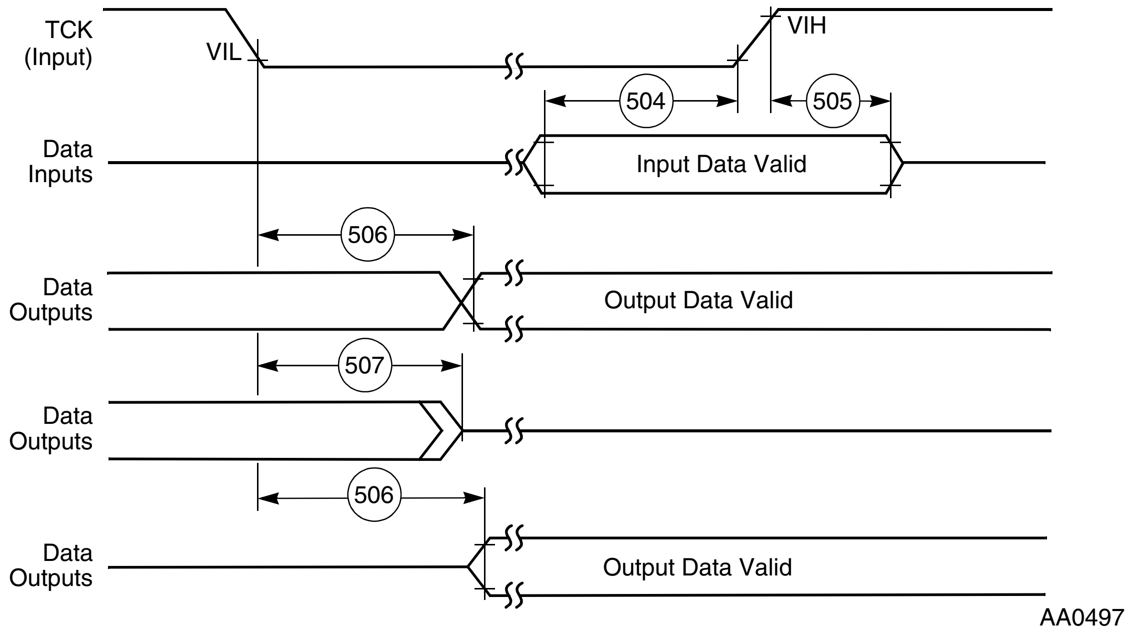


Figure 3-50 Boundary Scan (JTAG) Timing Diagram

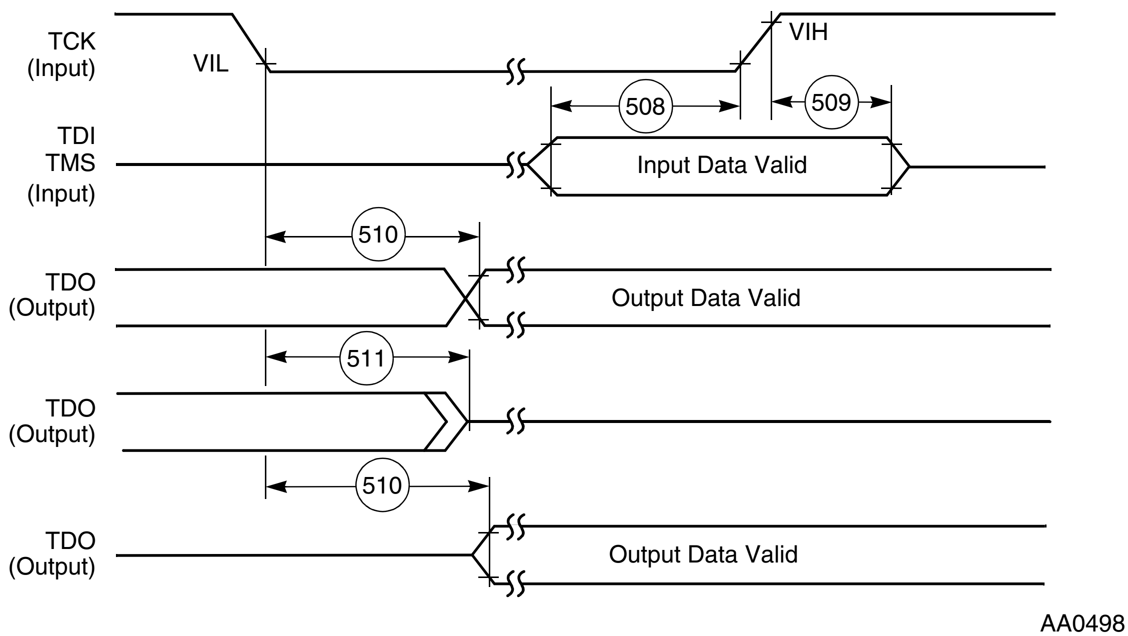


Figure 3-51 Test Access Port Timing Diagram

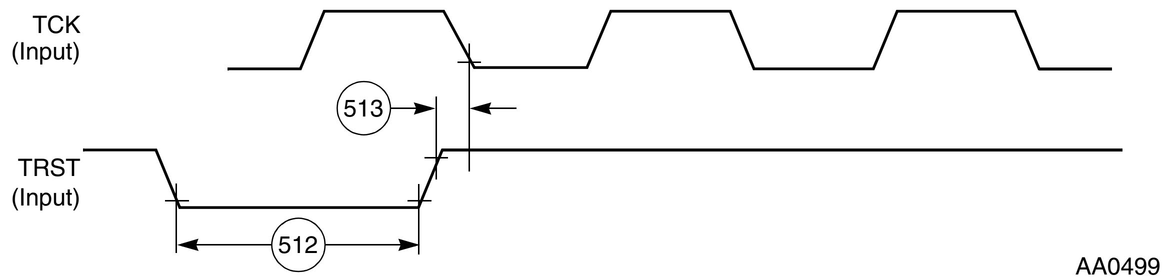


Figure 3-52 TRST Timing Diagram

3.19 OnCE Module TimIng

Table 3-29 OnCE Module Timing[1]

No.	Characteristics	Expression	100 MHz		Unit
			Min	Max	
500	TCK frequency of operation	$1/(T_C \times 3)$, max 22.0 MHz	0.0	22.0	MHz
514	DE assertion time in order to enter Debug mode	$1.5 \times T_C + 10.0$	25.0	—	ns
515	Response time when DSP56362 is executing NOP instructions from internal memory	$5.5 \times T_C + 30.0$	—	85.0	ns
516	Debug acknowledge assertion time	$3 \times T_C + 10.0$	40.0	—	ns

[1] V_{CC} = 3.3 V ± 0.16 V; T_J = 0°C to +100°C, C_L = 50 pF

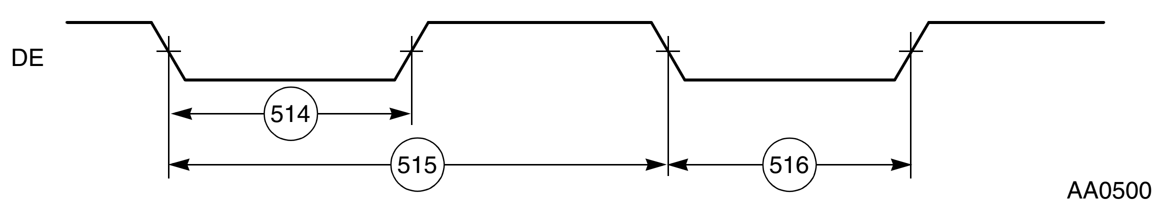


Figure 3-53 OnCE—Debug Request

NOTES

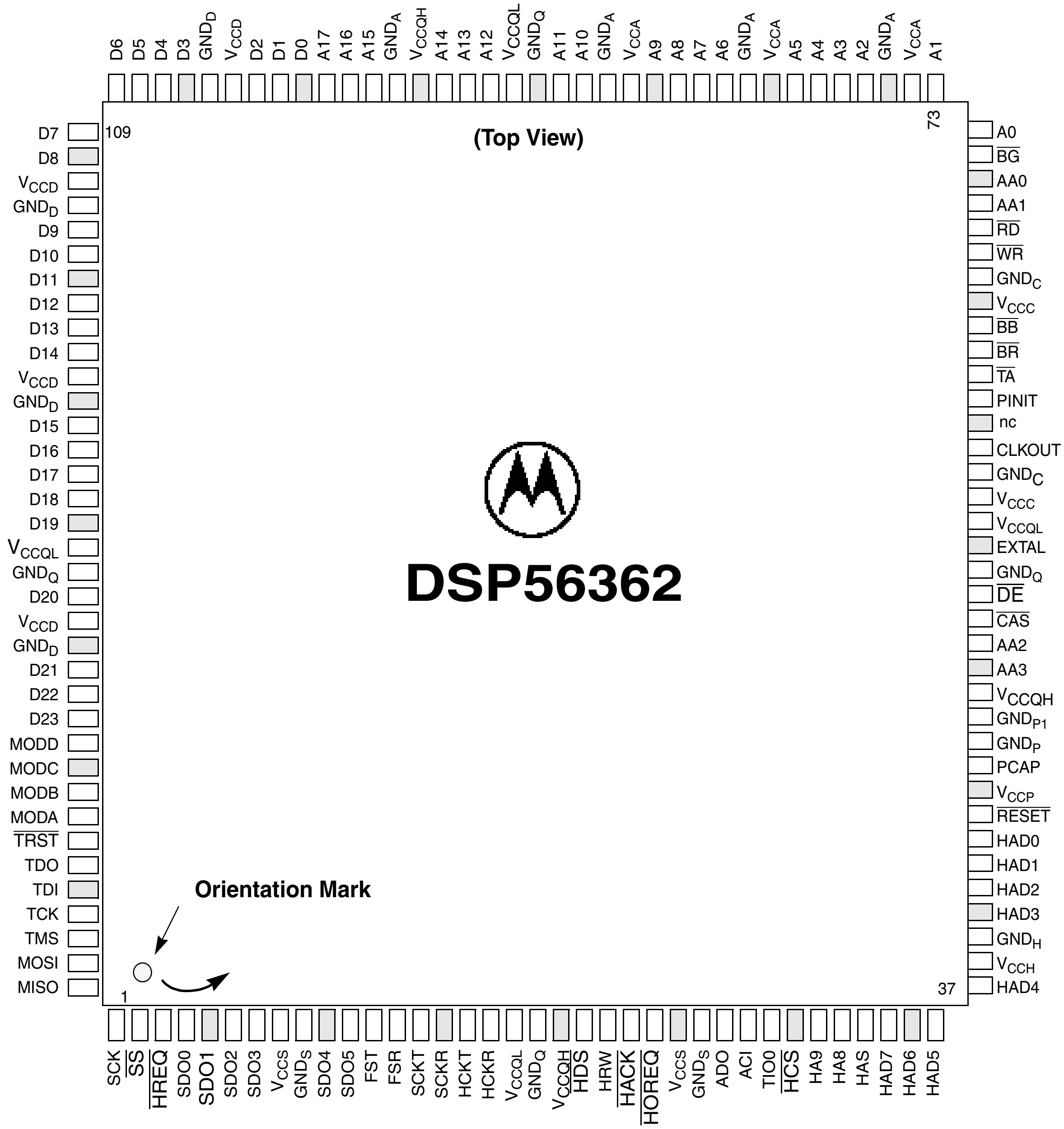
4 Packaging

4.1 Pin-out and Package Information

This section provides information about the available package for this product, including diagrams of the package pinouts and tables describing how the signals described in Section 2, "Signal/Connection Descriptions" are allocated for the package. The DSP56362 is available in a 144-pin LQFP package.

4.2 LQFP Package Description

Top view of the LQFP package is shown in Figure 4-1 with its pin-outs. The LQFP package mechanical drawing is shown in Figure 4-2.



Note: Because of size constraints in this figure, only one name is shown for multiplexed pins. Refer to Table 4-1 and Table 4-2 for detailed information about pin functions and signal names.

AA0301

Figure 4-1 DSP56362 Thin Quad Flat Pack (LQFP), Top View

Table 4-1 DSP56362 LQFP Signal Identification by Pin Number

Pin No.	Signal Name[1]	Pin No.	Signal Name[1]	Pin No.	Signal Name[1]
1	SCK/SCL	26	GND_{S}	51	AA2/$\overline{\text{RAS2}}$
2	$\overline{\text{SS}}$/HA2	27	ADO or PD1	52	$\overline{\text{CAS}}$
3	$\overline{\text{HREQ}}$	28	ACI or PD0	53	$\overline{\text{DE}}$
4	SDO0 or PC11	29	TIO0	54	GND_{Q}
5	$\overline{\text{SDO1}}$ or $\overline{\text{PC10}}$	30	$\overline{\text{HCS}}$/HCS, HA10, or PB13	55	EXTAL
6	SDO2/SDI3 or PC9	31	HA2, HA9, or PB10	56	V_{CCQL}
7	SDO3/SDI2 or PC8	32	HA1, HA8, or PB9	57	V_{CCC}
8	V_{CCS}	33	HA0, $\overline{\text{HAS}}$/HAS, or PB8	58	GND_{C}
9	GND_{S}	34	H7, HAD7, or PB7	59	CLKOUT
10	SDO4/SDI1 or PC7	35	H6, HAD6, or PB6	60	NC (not connected)
11	SDO5/SDI0 or PC6	36	H5, HAD5, or PB5	61	$\overline{\text{PINIT/NMI}}$
12	FST or PC4	37	H4, HAD4, or PB4	62	$\overline{\text{TA}}$
13	FSR or PC1	38	V_{CCH}	63	$\overline{\text{BR}}$
14	SCKT or PC3	39	GND_{H}	64	$\overline{\text{BB}}$
15	SCKR or PC0	40	H3, HAD3, or PB3	65	V_{CCC}
16	HCKT or PC5	41	H2, HAD2, or PB2	66	GND_{C}
17	HCKR or PC2	42	H1, HAD1, or PB1	67	$\overline{\text{WR}}$
18	V_{CCQL}	43	H0, HAD0, or PB0	68	$\overline{\text{RD}}$
19	GND_{Q}	44	$\overline{\text{RESET}}$	69	AA1/$\overline{\text{RAS1}}$
20	V_{CCQH}	45	V_{CCP}	70	AA0/$\overline{\text{RAS0}}$
21	$\overline{\text{HDS}}$/HDS, $\overline{\text{HWR}}$/HWR, or PB12	46	PCAP	71	$\overline{\text{BG}}$
22	HRW, $\overline{\text{HRD}}$/HRD, or PB11	47	GND_{P}	72	A0
23	$\overline{\text{HACK}}$/HACK, $\overline{\text{HRRQ}}$/HRRQ, or PB15	48	GND_{P1}	73	A1
24	$\overline{\text{HOREQ}}$/HOREQ, $\overline{\text{HTRQ}}$/HTRQ, or PB14	49	V_{CCQH}	74	V_{CCA}
25	V_{CCS}	50	AA3/$\overline{\text{RAS3}}$	75	GND_{A}

Table 4-1 DSP56362 LQFP Signal Identification by Pin Number (continued)

Pin No.	Signal Name[1]	Pin No.	Signal Name[1]	Pin No.	Signal Name[1]
76	A2	99	A17	122	D16
77	A3	100	D0	123	D17
78	A4	101	D1	124	D18
79	A5	102	D2	125	D19
80	V_{CCA}	103	V_{CCD}	126	V_{CCQL}
81	GND_A	104	GND_D	127	GND_Q
82	A6	105	D3	128	D20
83	A7	106	D4	129	V_{CCD}
84	A8	107	D5	130	GND_D
85	A9	108	D6	131	D21
86	V_{CCA}	109	D7	132	D22
87	GND_A	110	D8	133	D23
88	A10	111	V_{CCD}	134	MODD/$\overline{IRQD}$
89	A11	112	GND_D	135	MODC/$\overline{IRQC}$
90	GND_Q	113	D9	136	MODB/$\overline{IRQB}$
91	V_{CCQL}	114	D10	137	MODA/$\overline{IRQA}$
92	A12	115	D11	138	$\overline{TRST}$
93	A13	116	D12	139	TDO
94	A14	117	D13	140	TDI
95	V_{CCQH}	118	D14	141	TCK
96	GND_A	119	V_{CCD}	142	TMS
97	A15	120	GND_D	143	MOSI/HA0
98	A16	121	D15	144	MISO/SDA

1 Signal names are based on configured functionality. Most pins supply a single signal. Some pins provide a signal with dual functionality, such as the MODx/$\overline{IRQx}$ pins that select an operating mode after $\overline{RESET}$ is deasserted, but act as interrupt lines during operation. Some signals have configurable polarity; these names are shown with and without overbars, such as $\overline{HAS}$/HAS. Some pins have two or more configurable functions; names assigned to these pins indicate the function for a specific configuration. For example, pin 34 is data line H7 in nonmultiplexed bus mode, data/address line HAD7 in multiplexed bus mode, or GPIO line PB7 when the GPIO function is enabled for this pin.

Table 4-2 DSP56362 LQFP Signal Identification by Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
not connected	60	D13	117	GND_{P1}	48
A0	72	D14	118	GND_Q	19
A1	73	D15	121	GND_Q	54
A10	88	D16	122	GND_Q	90
A11	89	D17	123	GND_Q	127
A12	92	D18	124	GND_S	9
A13	93	D19	125	GND_S	26
A14	94	D2	102	H0	43
A15	97	D20	128	H1	42
A16	98	D21	131	H2	41
A17	99	D22	132	H3	40
A2	76	D23	133	H4	37
A3	77	D3	105	H5	36
A4	78	D4	106	H6	35
A5	79	D5	107	H7	34
A6	82	D6	108	HA0	33
A7	83	D7	109	HA0	143
A8	84	D8	110	HA1	32
A9	85	D9	113	HA10	30
AA0	70	$\overline{DE}$	53	HA2	2
AA1	69	EXTAL	55	HA2	31
AA2	51	FSR	13	HA8	32
AA3	50	FST	12	HA9	31
ACI	28	GND_A	75	$\overline{HACK}$/HACK	23
ADO	27	GND_A	81	HAD0	43
$\overline{BB}$	64	GND_A	87	HAD1	42
BG	71	GND_A	96	HAD2	41

Table 4-2 DSP56362 LQFP Signal Identification by Name (continued)

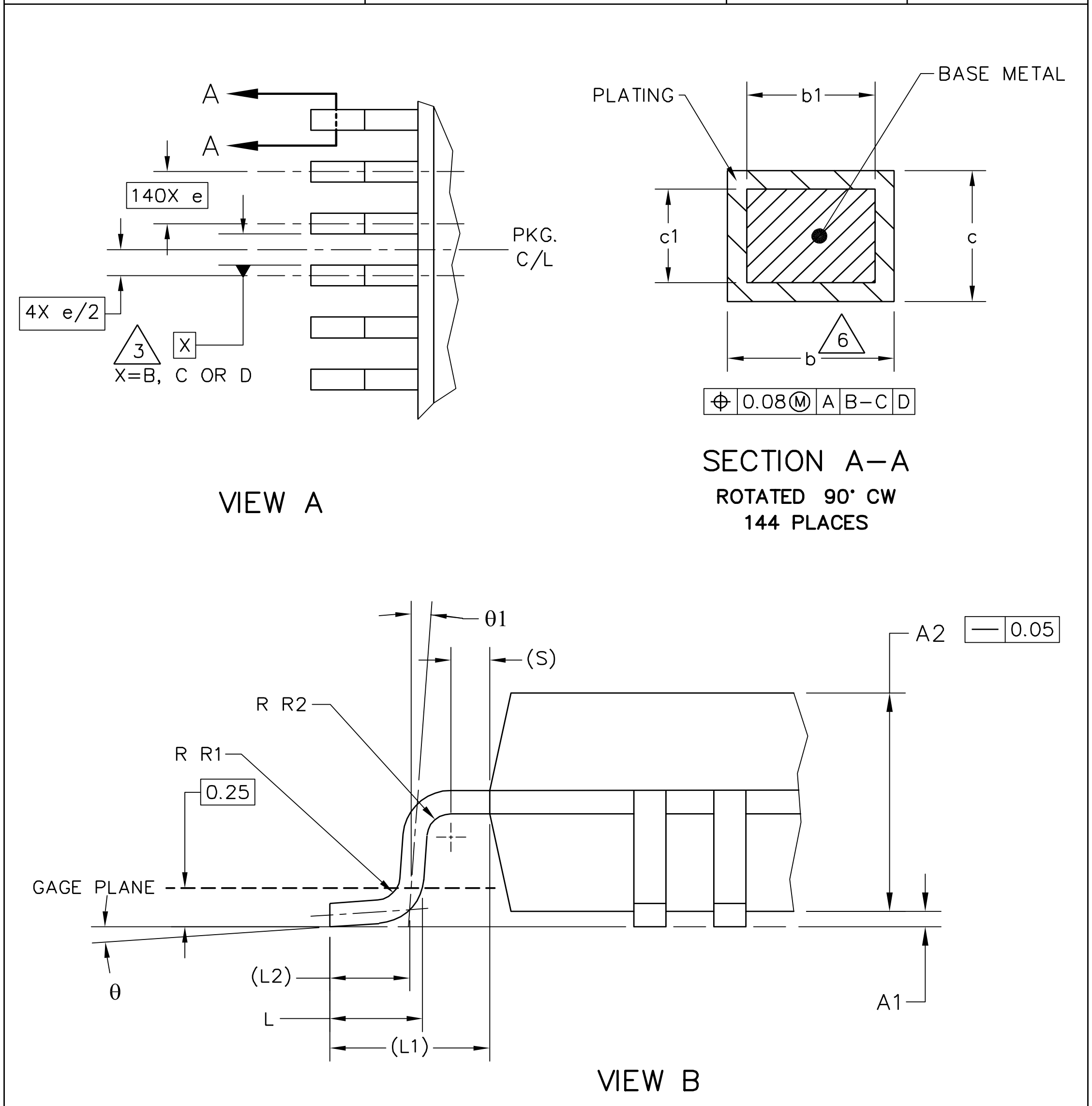
Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
$\overline{\text{BR}}$	63	GND_C	58	HAD3	40
$\overline{\text{CAS}}$	52	GND_C	66	HAD4	37
CLKOUT	59	GND_D	104	HAD5	36
D0	100	GND_D	112	HAD6	35
D1	101	GND_D	120	HAD7	34
D10	114	GND_D	130	$\overline{\text{HAS}}$/HAS	33
D11	115	GND_H	39	$\overline{\text{HCS}}$/HCS	30
D12	116	GND_P	47	$\overline{\text{HDS}}$/HDS	21
$\overline{\text{HOREQ}}$/HOREQ	24	PB9	32	SDO3	7
$\overline{\text{HRD}}$/HRD	22	PC0	15	SDO4	10
$\overline{\text{HREQ}}$	3	PC1	13	SDO5	11
$\overline{\text{HRRQ}}$/HRRQ	23	PC10	5	$\overline{\text{SS}}$	2
HRW	22	PC11	4	$\overline{\text{TA}}$	62
HCKR	17	PC2	17	TCK	141
HCKT	16	PC3	14	TDI	140
$\overline{\text{HTRQ}}$/HTRQ	24	PC4	12	TDO	139
$\overline{\text{HWR}}$/HWR	21	PC5	16	TIO0	29
$\overline{\text{IRQA}}$	137	PC6	11	TMS	142
$\overline{\text{IRQB}}$	136	PC7	10	$\overline{\text{TRST}}$	138
$\overline{\text{IRQC}}$	135	PC8	7	V_{CCA}	74
IRQD	134	PC9	6	V_{CCA}	80
MISO	144	PCAP	46	V_{CCA}	86
MODA	137	PD0	28	V_{CCC}	57
MODB	136	PD1	27	V_{CCC}	65
MODC	135	PINIT	61	V_{CCD}	103
MODD	134	$\overline{\text{RAS0}}$	70	V_{CCD}	111
MOSI	143	$\overline{\text{RAS1}}$	69	V_{CCD}	119

Table 4-2 DSP56362 LQFP Signal Identification by Name (continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
$\overline{\text{NMI}}$	61	$\overline{\text{RAS2}}$	52	V_{CCD}	129
PB0	43	$\overline{\text{RAS3}}$	51	V_{CCH}	38
PB1	42	$\overline{\text{RD}}$	68	V_{CCP}	45
PB10	31	RESET	44	V_{CCQH}	20
PB11	22	SCK	1	V_{CCQH}	49
PB12	21	SCKR	15	V_{CCQH}	95
PB13	30	SCKT	14	V_{CCQL}	18
PB14	24	SCL	1	V_{CCQL}	56
PB15	23	SDA	144	V_{CCQL}	91
PB2	41	SDI0	11	V_{CCQL}	126
PB3	40	SDI1	10	V_{CCS}	8
PB4	37	SDI2	7	V_{CCS}	25
PB5	36	SDI3	6	$\overline{\text{WR}}$	67
PB6	35	SDO0	4		
PB7	34	SDO1	5		
PB8	33	SDO2	6		

4.3 LQFP PACKAGE MECHANICAL DRAWING

MOTOROLA Semiconductor Products Sector COPYRIGHT MOTOROLA, INC. ALL RIGHTS RESERVED	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23177W	
		PAGE: 918	
ELECTRONIC VERSIONS ARE UNCONTROLLED EXCEPT WHEN ACCESSED DIRECTLY FROM THE FINAL MANUFACTURING STRATEGIC OPERATIONS WEB PAGE IN PDF FORMAT. PRINTED VERSIONS ARE UNCONTROLLED.	DO NOT SCALE THIS DRAWING	ISSUE: D	DATE: 22AUG00



TITLE: 144 LEAD LQFP 20 X 20, 0.5 PITCH, 1.4 THICK	CASE NUMBER: 918−03	
	STANDARD: MOTOROLA	
	PACKAGE CODE: 8259	SHEET: 2 OF 3

Figure 4-2 DSP56362 144-pin LQFP Package

5 Design Considerations

5.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, in °C can be obtained from the following equation:

$$T_J = T_A + (P_D \times R_{\theta JA})$$

Where:

T_A = ambient temperature °C

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W

P_D = power dissipation in package W

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W

$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W

$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on a PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages.

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to where the leads are attached to the case.
- If the temperature of the package case (T_T) is determined by a thermocouple, the thermal resistance is computed using the value obtained by the equation

  $(T_J – T_T)/P_D$.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual temperature. Hence, the new thermal metric, thermal characterization parameter or Ψ_{JT}, has been defined to be $(T_J – T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

5.2 Electrical Design Considerations

CAUTION

> This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). The suggested value for a pullup or pulldown resistor is 10 k ohm.

Use the following list of recommendations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each V_{CC} pin on the DSP and from the board ground to each GND pin.
- Use at least six 0.01–0.1 µF bypass capacitors positioned as close as possible to the four sides of the package to connect the V_{CC} power source to GND.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{CC} and GND pins are less than 1.2 cm (0.5 inch) per capacitor lead.
- Use at least a four-layer PCB with two inner layers for V_{CC} and GND.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal. This recommendation particularly applies to the address and data buses as well as the $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{TA}$, and $\overline{BG}$ pins. Maximum PCB trace lengths on the order of 15 cm (6 inches) are recommended.

- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- All inputs must be terminated (i.e., not allowed to float) using CMOS levels, except for the pins with internal pull-up resistors ($\overline{TRST}$, TMS, $\overline{DE}$, TCK, and TDI).
- Take special care to minimize noise levels on the V_{CCP}, GND_P, and GND_{P1} pins.
- If multiple DSP56362 devices are on the same board, check for cross-talk or excessive spikes on the supplies due to synchronous operation of the devices.
- RESET must be asserted when the chip is powered up. A stable EXTAL signal should be supplied before deassertion of RESET.
- At power-up, ensure that the voltage difference between the 5 V tolerant pins and the chip V_{CC} never exceeds 3.95 V.

5.3 Power Consumption Considerations

Power dissipation is a key issue in portable DSP applications. Some of the factors which affect current consumption are described in this section. Most of the current consumed by CMOS devices is alternating current (ac), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by the following formula:

$$I = C \times V \times f$$

where:

C = node/pin capacitance

V = voltage swing

f = frequency of node/pin toggle

Example 1. Current Consumption

For a Port A address pin loaded with 50 pF capacitance, operating at 3.3 V, and with a 100 MHz clock, toggling at its maximum possible rate (50 MHz), the current consumption is

$$I = 50 \times 10^{-12} \times 3.3 \times 50 \times 10^{6} = 8.25 \text{mA}$$

The maximum internal current (I_{CCI}max) value reflects the typical possible switching of the internal buses on best-case operation conditions, which is not necessarily a real application case. The typical internal current (I_{CCItyp}) value reflects the average switching of the internal buses on typical operating conditions.

For applications that require very low current consumption, do the following:

- Set the EBD bit when not accessing external memory.
- Minimize external memory accesses and use internal memory accesses.
- Minimize the number of pins that are switching.
- Minimize the capacitive load on the pins.
- Connect the unused inputs to pull-up or pull-down resistors.

- Disable unused peripherals.
- Disable unused pin activity (e.g., CLKOUT, XTAL).

One way to evaluate power consumption is to use a current per MIPS measurement methodology to minimize specific board effects (i.e., to compensate for measured board current not caused by the DSP). A benchmark power consumption test algorithm is listed in **Appendix A**. Use the test algorithm, specific test current measurements, and the following equation to derive the current per MIPS value.

$$1\text{MIPS} = 1\text{MHz} = (I_{typF2} - I_{typF1}) \times (F2 - F1)$$

where :

I_{typF2} = current at F2

I_{typF1} = current at F1

F2 = high frequency (any specified operating frequency)

F1 = low frequency (any specified operating frequency lower than F2)

NOTE

F1 should be significantly less than F2. For example, F2 could be 66 MHz and F1 could be 33 MHz. The degree of difference between F1 and F2 determines the amount of precision with which the current rating can be determined for an application.

5.4 PLL Performance Issues

The following explanations should be considered as general observations on expected PLL behavior. There is no testing that verifies these exact numbers. These observations were measured on a limited number of parts and were not verified over the entire temperature and voltage ranges.

5.4.1 Phase Skew Performance

The phase skew of the PLL is defined as the time difference between the falling edges of EXTAL and CLKOUT for a given capacitive load on CLKOUT, over the entire process, temperature, and voltage ranges. As defined in Figure 3-1, for input frequencies greater than 15 MHz and the MF ≤ 4, this skew is greater than or equal to 0.0 ns and less than 1.8 ns; otherwise, this skew is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this skew is between –1.4 ns and +3.2 ns.

5.4.2 Phase Jitter Performance

The phase jitter of the PLL is defined as the variations in the skew between the falling edges of EXTAL and CLKOUT for a given device in specific temperature, voltage, input frequency, MF, and capacitive load on CLKOUT. These variations are a result of the PLL locking mechanism. For input frequencies greater than 15 MHz and MF ≤ 4, this jitter is less than ±0.6 ns; otherwise, this jitter is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this jitter is less than ±2 ns.

5.4.3 Frequency Jitter Performance

The frequency jitter of the PLL is defined as the variation of the frequency of CLKOUT. For small MF (MF < 10) this jitter is smaller than 0.5%. For mid-range MF (10 < MF < 500) this jitter is between 0.5% and approximately 2%. For large MF (MF > 500), the frequency jitter is 2–3%.

5.4.4 Input (EXTAL) Jitter Requirements

The allowed jitter on the frequency of EXTAL is 0.5%. If the rate of change of the frequency of EXTAL is slow (i.e., it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (i.e., it does not stay at an extreme value for a long time), then the allowed jitter can be 2%. The phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed values.

5.5 Host Port Considerations

Careful synchronization is required when reading multi-bit registers that are written by another asynchronous system. This synchronization is a common problem when two asynchronous systems are connected, as they are in the host interface. The following paragraphs present considerations for proper operation.

5.5.1 Host Programming Considerations

- **Unsynchronized Reading of Receive Byte Registers**—When reading the receive byte registers, receive register high (RXH), receive register middle (RXM), or receive register low (RXL), the host interface programmer should use interrupts or poll the receive register data full (RXDF) flag that indicates whether data is available. This ensures that the data in the receive byte registers will be valid.
- **Overwriting Transmit Byte Registers**—The host interface programmer should not write to the transmit byte registers, transmit register high (TXH), transmit register middle (TXM), or transmit register low (TXL), unless the transmit register data empty (TXDE) bit is set, indicating that the transmit byte registers are empty. This ensures that the transmit byte registers will transfer valid data to the host receive (HRX) register.
- **Synchronization of Status Bits from DSP to Host**—HC, $\overline{\text{HOREQ}}$, DMA, HF3, HF2, TRDY, TXDE, and RXDF status bits are set or cleared from inside the DSP and read by the host processor (refer to the user’s manual for descriptions of these status bits). The host can read these status bits very quickly without regard to the clock rate used by the DSP, but the state of the bit could be changing during the read operation. This is not generally a system problem, because the bit will be read correctly in the next pass of any host polling routine.

  However, if the host asserts $\overline{\text{HEN}}$ for more than timing number 31, with a minimum cycle time of timing number 31 + 32, then these status bits are guaranteed to be stable. Exercise care when reading status bits HF3 and HF2 as an encoded pair. If the DSP changes HF3 and HF2 from 00 to 11, there is a small probability that the host could read the bits during the transition and receive 01 or 10 instead of 11. If the combination of HF3 and HF2 has significance, the host could read the wrong combination. Therefore, read the bits twice and check for consensus.

- **Overwriting the Host Vector**—The host interface programmer should change the host vector (HV) register only when the host command (HC) bit is clear. This ensures that the DSP interrupt control logic will receive a stable vector.
- **Cancelling a Pending Host Command Exception**—The host processor may elect to clear the HC bit to cancel the host command exception request at any time before it is recognized by the DSP. Because the host does not know exactly when the exception will be recognized (due to exception processing synchronization and pipeline delays), the DSP may execute the host command exception after the HC bit is cleared. For these reasons, the HV bits must not be changed at the same time that the HC bit is cleared.
- **Variance in the Host Interface Timing**—The host interface (HDI) may vary (e.g. due to the PLL lock time at reset). Therefore, a host which attempts to load (bootstrap) the DSP should first make sure that the part has completed its HI port programming (e.g., by setting the INIT bit in ICR then polling it and waiting it to be cleared, then reading the ISR or by writing the TREQ/RREQ together with the INIT and then polling INIT, ISR, and the $\overline{\text{HOREQ}}$ pin).

5.5.2 DSP Programming Considerations

- **Synchronization of Status Bits from Host to DSP**—DMA, HF1, HF0, HCP, HTDE, and HRDF status bits are set or cleared by the host processor side of the interface. These bits are individually synchronized to the DSP clock. (Refer to the user’s manual for descriptions of these status bits.)
- **Reading HF0 and HF1 as an Encoded Pair**—Care must be exercised when reading status bits HF0 and HF1 as an encoded pair, (i.e., the four combinations 00, 01, 10, and 11 each have significance). A very small probability exists that the DSP will read the status bits synchronized during transition. Therefore, HF0 and HF1 should be read twice and checked for consensus.

6 Ordering Information

Consult a Freescale Semiconductor, Inc. sales office or authorized distributor to determine product availability and to place an order.

For information on ordering this and all DSP Audio products, review the SG1004 selector guide at http://www.freescale.com.

NOTES

Appendix A Power Consumption Benchmark

The following benchmark program permits evaluation of DSP power usage in a test situation. It enables the PLL, disables the external clock, and uses repeated multiply-accumulate instructions with a set of synthetic DSP application data to emulate intensive sustained DSP operation.

```
;********************************************************************;*********
************************************************************

;* ;* CHECKS   Typical Power Consumption

;********************************************************************
          page     200,55,0,0,0
          nolist

I_VEC EQU $000000  ; Interrupt vectors for program debug only
START EQU $8000    ; MAIN (external) program starting address
INT_PROG  EQU $100 ; INTERNAL program memory starting address
INT_XDAT  EQU $0   ; INTERNAL X-data memory starting address
INT_YDAT  EQU $0   ; INTERNAL Y-data memory starting address

          INCLUDE "ioequ.asm"
          INCLUDE "intequ.asm"

          list

          org      P:START
;
          movep #$0123FF,x:M_BCR; BCR: Area 3 : 1 w.s (SRAM)
; Default: 1 w.s (SRAM)
;
          movep    #$0d0000,x:M_PCTL           ; XTAL disable
                                ; PLL enable
                                ; CLKOUT disable
;
; Load the program
;
          move     #INT_PROG,r0
          move     #PROG_START,r1
          do       #(PROG_END-PROG_START),PLOAD_LOOP
          move     p:(r1)+,x0
          move     x0,p:(r0)+
          nop
PLOAD_LOOP
;
; Load the X-data
;
          move     #INT_XDAT,r0
          move     #XDAT_START,r1
```

```
          do        #(XDAT_END-XDAT_START),XLOAD_LOOP
          move      p:(r1)+,x0
          move      x0,x:(r0)+
XLOAD_LOOP
;
; Load the Y-data
;
          move      #INT_YDAT,r0
          move      #YDAT_START,r1
          do        #(YDAT_END-YDAT_START),YLOAD_LOOP
          move      p:(r1)+,x0
          move      x0,y:(r0)+
YLOAD_LOOP
;

          jmp       INT_PROG

PROG_START
          move      #$0,r0
          move      #$0,r4
          move      #$3f,m0
          move      #$3f,m4
;
          clr       a
          clr       b
          move      #$0,x0
          move      #$0,x1
          move      #$0,y0
          move      #$0,y1
          bset      #4,omr              ; ebd
;
sbr       dor       #60,_end
          mac       x0,y0,a   x:(r0)+,x1          y:(r4)+,y1
          mac       x1,y1,a   x:(r0)+,x0          y:(r4)+,y0
          add       a,b
          mac       x0,y0,a   x:(r0)+,x1
          mac       x1,y1,a                       y:(r4)+,y0
          move      b1,x:$ff
_end
          bra       sbr
          nop
          nop
          nop
          nop
PROG_END
          nop
          nop


XDAT_START
;         org       x:0
          dc        $262EB9
          dc        $86F2FE
          dc        $E56A5F
          dc        $616CAC
```

```
dc      $8FFD75
dc      $9210A
dc      $A06D7B
dc      $CEA798
dc      $8DFBF1
dc      $A063D6
dc      $6C6657
dc      $C2A544
dc      $A3662D
dc      $A4E762
dc      $84F0F3
dc      $E6F1B0
dc      $B3829
dc      $8BF7AE
dc      $63A94F
dc      $EF78DC
dc      $242DE5
dc      $A3E0BA
dc      $EBAB6B
dc      $8726C8
dc      $CA361
dc      $2F6E86
dc      $A57347
dc      $4BE774
dc      $8F349D
dc      $A1ED12
dc      $4BFCE3
dc      $EA26E0
dc      $CD7D99
dc      $4BA85E
dc      $27A43F
dc      $A8B10C
dc      $D3A55
dc      $25EC6A
dc      $2A255B
dc      $A5F1F8
dc      $2426D1
dc      $AE6536
dc      $CBBC37
dc      $6235A4
dc      $37F0D
dc      $63BEC2
dc      $A5E4D3
dc      $8CE810
dc      $3FF09
dc      $60E50E
dc      $CFFB2F
dc      $40753C
dc      $8262C5
dc      $CA641A
dc      $EB3B4B
dc      $2DA928
dc      $AB6641
dc      $28A7E6
dc      $4E2127
```

```
            dc          $482FD4
            dc          $7257D
            dc          $E53C72
            dc          $1A8C3
            dc          $E27540
XDAT_END

YDAT_START
;           org         y:0
            dc          $5B6DA
            dc          $C3F70B
            dc          $6A39E8
            dc          $81E801
            dc          $C666A6
            dc          $46F8E7
            dc          $AAEC94
            dc          $24233D
            dc          $802732
            dc          $2E3C83
            dc          $A43E00
            dc          $C2B639
            dc          $85A47E
            dc          $ABFDDF
            dc          $F3A2C
            dc          $2D7CF5
            dc          $E16A8A
            dc          $ECB8FB
            dc          $4BED18
            dc          $43F371
            dc          $83A556
            dc          $E1E9D7
            dc          $ACA2C4
            dc          $8135AD
            dc          $2CE0E2
            dc          $8F2C73
            dc          $432730
            dc          $A87FA9
            dc          $4A292E
            dc          $A63CCF
            dc          $6BA65C
            dc          $E06D65
            dc          $1AA3A
            dc          $A1B6EB
            dc          $48AC48
            dc          $EF7AE1
            dc          $6E3006
            dc          $62F6C7
            dc          $6064F4
            dc          $87E41D
            dc          $CB2692
            dc          $2C3863
            dc          $C6BC60
            dc          $43A519
            dc          $6139DE
            dc          $ADF7BF
```

```
                dc          $4B3E8C
                dc          $6079D5
                dc          $E0F5EA
                dc          $8230DB
                dc          $A3B778
                dc          $2BFE51
                dc          $E0A6B6
                dc          $68FFB7
                dc          $28F324
                dc          $8F2E8D
                dc          $667842
                dc          $83E053
                dc          $A1FD90
                dc          $6B2689
                dc          $85B68E
                dc          $622EAF
                dc          $6162BC
                dc          $E4A245
YDAT_END
```

NOTES

Appendix B IBIS Model

```
[IBIS ver]       2.1
[File name]     56362.ibs
[File Rev]      0.0
[Date]         29/6/2000
[Component]    56362
[Manufacturer]  Freescale
[Package]
|variable       typ                    min                   max
R_pkg            45m                    22m                   75m
L_pkg            2.5nH                  1.1nH                 4.3nH
C_pkg            1.3pF                  1.2pF                 1.4pF


[Pin]signal_name model_name
1 sck               ip5b_io
2 ss_               ip5b_io
3 hreq_               ip5b_io
4 sdo0               ip5b_io
5 sdo1               ip5b_io
6 sdoi23               ip5b_io
7 sdoi32               ip5b_io
8 svcc               power
9 sgnd               gnd
10 sdoi41               ip5b_io
11 sdoi50               ip5b_io
12 fst               ip5b_io
13 fsr               ip5b_io
14 sckt               ip5b_io
15 sckr               ip5b_io
16 hsckt               ip5b_io
17 hsckr               ip5b_io
18 qvccl               power
19 gnd               gnd
20 qvcch               power
21 hp12               ip5b_io
22 hp11               ip5b_io
23 hp15               ip5b_io
24 hp14               ip5b_io
25 svcc               power
26 sgnd               gnd
27 ado               ip5b_io
28 aci               ip5b_io
29 tio               ip5b_io
30 hp13               ip5b_io
31 hp10               ip5b_io
32 hp9               ip5b_io
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33	hp8	ip5b_io
34	hp7	ip5b_io
35	hp6	ip5b_io
36	hp5	ip5b_io
37	hp4	ip5b_io
38	svcc	power
39	sgnd	gnd
40	hp3	ip5b_io
41	hp2	ip5b_io
42	hp1	ip5b_io
43	hp0	ip5b_io
44	ires_	ip5b_i
45	pvcc	power
46	pcap	power
47	pgnd	gnd
48	pgnd1	gnd
49	qvcch	power
50	aa3	icbc_o
51	aa2	icbc_o
52	cas_	icbc_o
53	de_	ipbw_io
54	qgnd	gnd
55	cxtldis_	iexlh_i
56	qvccl	power
57	cvcc	power
58	cgnd	gnd
59	clkout	icba_o
61	nmi_	ipbw_i
62	ta_	icbc_o
63	br_	icbc_o
64	bb_	icbc_o
65	cvcc	power
66	cgnd	gnd
67	wr_	icbc_o
68	rd_	icbc_o
69	aa1	icbc_o
70	aa0	icbc_o
71	bg_	icbc_o
72	eab0	icba_o
73	eab1	icba_o
74	avcc	power
75	agnd	gnd
76	eab2	icba_o
77	eab3	icba_o
78	eab4	icba_o
79	eab5	icba_o
80	avcc	power
81	agnd	gnd
82	eab6	icba_o
83	eab7	icba_o
84	eab8	icba_o
85	eab9	icba_o
86	avcc	power
87	agnd	gnd
88	eab10	icba_o

89	eab11	icba_o
90	qgnd	gnd
91	qvcc	power
92	eab12	icba_o
93	eab13	icba_o
94	eab14	icba_o
95	qvcch	power
96	agnd	gnd
97	eab15	icba_o
98	eab16	icba_o
99	eab17	icba_o
100	edb0	icba_io
101	edb1	icba_io
102	edb2	icba_io
103	dvcc	power
104	dgnd	gnd
105	edb3	icba_io
106	edb4	icba_io
107	edb5	icba_io
108	edb6	icba_io
109	edb7	icba_io
110	edb8	icba_io
111	dvcc	power
112	dgnd	gnd
113	edb9	icba_io
114	edb10	icba_io
115	edb11	icba_io
116	edb12	icba_io
117	edb13	icba_io
118	edb14	icba_io
119	dvcc	power
120	dgnd	gnd
121	edb15	icba_io
122	edb16	icba_io
123	edb17	icba_io
124	edb18	icba_io
125	edb19	icba_io
126	qvccl	power
127	qgnd	gnd
128	edb20	icba_io
129	dvcc	power
130	dgnd	gnd
131	edb21	icba_io
132	edb22	icba_io
133	edb23	icba_io
134	irqd_	ip5b_i
135	irqc_	ip5b_i
136	irqb_	ip5b_i
137	irqa_	ip5b_i
138	trst_	ip5b_i
139	tdo	ip5b_o
140	tdi	ip5b_i
141	tck	ip5b_i
142	tms	ip5b_i
143	mosi	ip5b_io

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144 sda                ip5b_io
|
[Model]         ip5b_i
Model_type         Input
Polarity         Non-Inverting
Vinl= 0.8000v
Vinh= 2.000v
C_comp         5.00pF         5.00pF         5.00pF
|
|
[Voltage Range]       3.3v       3v       3.6v
[GND_clamp]
|voltage         I(typ)         I(min)         I(max)
|
-3.30e+00   -5.21e+02   -3.65e+02   -5.18e+02
-3.10e+00   -4.69e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.16e+02
-2.70e+00   -3.67e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.14e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.63e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.12e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.61e+02
-1.70e+00   -1.13e+02   -9.25e+01   -1.10e+02
-1.50e+00   -7.83e+01   -6.88e+01   -7.58e+01
-1.30e+00   -4.43e+01   -4.52e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.67e+00
-9.00e-01   -9.69e-03   -1.18e+00   -7.81e-03
-7.00e-01   -2.83e-04   -5.70e-03   -8.42e-04
-5.00e-01   -1.35e-06   -4.53e-05   -1.00e-05
-3.00e-01   -1.31e-09   -3.74e-07   -8.58e-09
-1.00e-01   -2.92e-11   -3.00e-09   -3.64e-11
0.000e+00   -2.44e-11   -5.14e-10   -2.79e-11
|
|
[Model]         ip5b_io
Model_type         I/O
Polarity         Non-Inverting
Vinl= 0.8000v
Vinh= 2.000v
C_comp         5.00pF         5.00pF         5.00pF
|
|
[Voltage Range]       3.3v       3v       3.6v
[Pulldown]
|voltage         I(typ)         I(min)         I(max)
|
-3.30e+00   -5.21e+02   -3.65e+02   -5.18e+02
-3.10e+00   -4.69e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.16e+02
-2.70e+00   -3.67e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.14e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.63e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.12e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.61e+02
-1.70e+00   -1.13e+02   -9.25e+01   -1.10e+02
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-1.50e+00    -7.83e+01    -6.88e+01    -7.58e+01
-1.30e+00    -4.43e+01    -4.52e+01    -4.17e+01
-1.10e+00    -1.02e+01    -2.15e+01    -7.69e+00
-9.00e-01    -5.10e-02    -1.18e+00    -5.63e-02
-7.00e-01    -3.65e-02    -2.25e-02    -4.28e-02
-5.00e-01    -2.65e-02    -1.38e-02    -3.12e-02
-3.00e-01    -1.62e-02    -8.35e-03    -1.91e-02
-1.00e-01    -5.49e-03    -2.80e-03    -6.52e-03
1.000e-01    5.377e-03    2.744e-03    6.427e-03
3.000e-01    1.516e-02    7.871e-03    1.823e-02
5.000e-01    2.370e-02    1.252e-02    2.869e-02
7.000e-01    3.098e-02    1.667e-02    3.776e-02
9.000e-01    3.700e-02    2.026e-02    4.544e-02
1.100e+00    4.175e-02    2.324e-02    5.171e-02
1.300e+00    4.531e-02    2.553e-02    5.660e-02
1.500e+00    4.779e-02    2.709e-02    6.023e-02
1.700e+00    4.935e-02    2.803e-02    6.271e-02
1.900e+00    5.013e-02    2.851e-02    6.419e-02
2.100e+00    5.046e-02    2.876e-02    6.494e-02
2.300e+00    5.063e-02    2.892e-02    6.525e-02
2.500e+00    5.075e-02    2.904e-02    6.540e-02
2.700e+00    5.085e-02    2.912e-02    6.549e-02
2.900e+00    5.090e-02    2.876e-02    6.555e-02
3.100e+00    4.771e-02    2.994e-02    6.561e-02
3.300e+00    4.525e-02    3.321e-02    6.182e-02
3.500e+00    4.657e-02    3.570e-02    6.049e-02
3.700e+00    4.904e-02    3.801e-02    6.178e-02
3.900e+00    5.221e-02    4.029e-02    6.450e-02
4.100e+00    5.524e-02    4.253e-02    6.659e-02
4.300e+00    5.634e-02    4.463e-02    6.867e-02
4.500e+00    5.751e-02    4.645e-02    6.970e-02
4.700e+00    5.634e-02    4.786e-02    6.938e-02
4.900e+00    5.648e-02    4.881e-02    6.960e-02
5.100e+00    5.664e-02    4.912e-02    6.983e-02
5.300e+00    5.679e-02    4.795e-02    7.005e-02
5.500e+00    5.693e-02    4.679e-02    7.026e-02
5.700e+00    5.707e-02    4.688e-02    7.049e-02
5.900e+00    5.722e-02    4.700e-02    7.074e-02
6.100e+00    5.741e-02    4.712e-02    7.105e-02
6.300e+00    5.766e-02    4.723e-02    7.147e-02
6.500e+00    5.801e-02    4.733e-02    7.205e-02
6.600e+00    5.824e-02    4.737e-02    7.242e-02
|
[Pullup]
|voltage        I(typ)         I(min)         I(max)
|
-3.30e+00    2.922e-04    2.177e-04    4.123e-04
-3.10e+00    2.881e-04    2.175e-04    4.021e-04
-2.90e+00    2.853e-04    2.173e-04    3.946e-04
-2.70e+00    2.836e-04    2.172e-04    3.893e-04
-2.50e+00    2.825e-04    2.171e-04    3.857e-04
-2.30e+00    2.819e-04    2.170e-04    3.834e-04
-2.10e+00    2.815e-04    2.169e-04    3.820e-04
-1.90e+00    2.813e-04    2.167e-04    3.812e-04
-1.70e+00    2.812e-04    2.520e-04    3.808e-04
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-1.50e+00   2.811e-04   3.078e-02   3.806e-04
-1.30e+00   2.810e-04   2.684e-02   3.804e-04
-1.10e+00   2.809e-04   2.277e-02   3.802e-04
-9.00e-01   2.808e-04   1.864e-02   3.801e-04
-7.00e-01   2.997e-04   1.447e-02   3.799e-04
-5.00e-01   1.750e-02   1.031e-02   3.797e-04
-3.00e-01   1.048e-02   6.181e-03   3.776e-04
-1.00e-01   3.487e-03   2.084e-03   4.568e-03
1.000e-01   -3.40e-03   -2.03e-03   -4.22e-03
3.000e-01   -9.69e-03   -5.71e-03   -1.24e-02
5.000e-01   -1.52e-02   -8.99e-03   -1.95e-02
7.000e-01   -2.02e-02   -1.19e-02   -2.61e-02
9.000e-01   -2.46e-02   -1.43e-02   -3.21e-02
1.100e+00   -2.84e-02   -1.62e-02   -3.73e-02
1.300e+00   -3.14e-02   -1.77e-02   -4.18e-02
1.500e+00   -3.37e-02   -1.88e-02   -4.55e-02
1.700e+00   -3.55e-02   -1.95e-02   -4.85e-02
1.900e+00   -3.68e-02   -2.00e-02   -5.09e-02
2.100e+00   -3.78e-02   -2.04e-02   -5.27e-02
2.300e+00   -3.85e-02   -2.07e-02   -5.41e-02
2.500e+00   -3.91e-02   -2.10e-02   -5.51e-02
2.700e+00   -3.96e-02   -2.12e-02   -5.60e-02
2.900e+00   -4.01e-02   -2.15e-02   -5.67e-02
3.100e+00   -4.04e-02   -2.17e-02   -5.74e-02
3.300e+00   -4.08e-02   -2.18e-02   -5.79e-02
3.500e+00   -4.11e-02   -2.20e-02   -5.84e-02
3.700e+00   -4.14e-02   -2.78e-02   -5.89e-02
3.900e+00   -4.17e-02   -1.20e+00   -5.94e-02
4.100e+00   -4.32e-02   -2.15e+01   -5.98e-02
4.300e+00   -4.08e-01   -4.52e+01   -6.10e-02
4.500e+00   -2.73e+01   -6.89e+01   -6.84e-02
4.700e+00   -6.13e+01   -9.25e+01   -7.73e+00
4.900e+00   -9.54e+01   -1.17e+02   -4.18e+01
5.100e+00   -1.38e+02   -1.52e+02   -7.59e+01
5.300e+00   -1.89e+02   -1.88e+02   -1.11e+02
5.500e+00   -2.40e+02   -2.23e+02   -1.61e+02
5.700e+00   -2.91e+02   -2.59e+02   -2.12e+02
5.900e+00   -3.42e+02   -2.94e+02   -2.63e+02
6.100e+00   -3.93e+02   -3.30e+02   -3.14e+02
6.300e+00   -4.44e+02   -3.65e+02   -3.65e+02
6.500e+00   -4.95e+02   -4.01e+02   -4.16e+02
6.600e+00   -5.21e+02   -4.18e+02   -4.41e+02
|
[GND_clamp]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   -5.21e+02   -3.65e+02   -5.18e+02
-3.10e+00   -4.69e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.16e+02
-2.70e+00   -3.67e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.14e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.63e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.12e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.61e+02
-1.70e+00   -1.13e+02   -9.25e+01   -1.10e+02
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-1.50e+00   -7.83e+01   -6.88e+01   -7.58e+01
-1.30e+00   -4.43e+01   -4.52e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.67e+00
-9.00e-01   -9.69e-03   -1.18e+00   -7.81e-03
-7.00e-01   -2.83e-04   -5.70e-03   -8.42e-04
-5.00e-01   -1.35e-06   -4.53e-05   -1.00e-05
-3.00e-01   -1.31e-09   -3.74e-07   -8.58e-09
-1.00e-01   -2.92e-11   -3.00e-09   -3.64e-11
0.000e+00   -2.44e-11   -5.14e-10   -2.79e-11
|
[Ramp]
R_load = 50.00
|voltage        I(typ)         I(min)         I(max)
|
|
dV/dt_r        1.030/0.465    0.605/0.676    1.320/0.366
|
|
dV/dt_f        1.290/0.671    0.829/0.122    1.520/0.431
|
|
[Model]        ip5b_o
Model_type        3-state
Polarity        Non-Inverting
C_comp        5.00pF        5.00pF        5.00pF
|
|
[Voltage Range]      3.3v      3v      3.6v
[Pulldown]
|voltage        I(typ)         I(min)         I(max)
|
-3.30e+00   -5.21e+02   -3.65e+02   -5.18e+02
-3.10e+00   -4.69e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.16e+02
-2.70e+00   -3.67e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.14e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.63e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.12e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.61e+02
-1.70e+00   -1.13e+02   -9.25e+01   -1.10e+02
-1.50e+00   -7.83e+01   -6.88e+01   -7.58e+01
-1.30e+00   -4.43e+01   -4.52e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.69e+00
-9.00e-01   -5.10e-02   -1.18e+00   -5.63e-02
-7.00e-01   -3.65e-02   -2.25e-02   -4.28e-02
-5.00e-01   -2.65e-02   -1.38e-02   -3.12e-02
-3.00e-01   -1.62e-02   -8.35e-03   -1.91e-02
-1.00e-01   -5.49e-03   -2.80e-03   -6.52e-03
1.000e-01   5.377e-03   2.744e-03   6.427e-03
3.000e-01   1.516e-02   7.871e-03   1.823e-02
5.000e-01   2.370e-02   1.252e-02   2.869e-02
7.000e-01   3.098e-02   1.667e-02   3.776e-02
9.000e-01   3.700e-02   2.026e-02   4.544e-02
1.100e+00   4.175e-02   2.324e-02   5.171e-02
1.300e+00   4.531e-02   2.553e-02   5.660e-02
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1.500e+00    4.779e-02    2.709e-02    6.023e-02
1.700e+00    4.935e-02    2.803e-02    6.271e-02
1.900e+00    5.013e-02    2.851e-02    6.419e-02
2.100e+00    5.046e-02    2.876e-02    6.494e-02
2.300e+00    5.063e-02    2.892e-02    6.525e-02
2.500e+00    5.075e-02    2.904e-02    6.540e-02
2.700e+00    5.085e-02    2.912e-02    6.549e-02
2.900e+00    5.090e-02    2.876e-02    6.555e-02
3.100e+00    4.771e-02    2.994e-02    6.561e-02
3.300e+00    4.525e-02    3.321e-02    6.182e-02
3.500e+00    4.657e-02    3.570e-02    6.049e-02
3.700e+00    4.904e-02    3.801e-02    6.178e-02
3.900e+00    5.221e-02    4.029e-02    6.450e-02
4.100e+00    5.524e-02    4.253e-02    6.659e-02
4.300e+00    5.634e-02    4.463e-02    6.867e-02
4.500e+00    5.751e-02    4.645e-02    6.970e-02
4.700e+00    5.634e-02    4.786e-02    6.938e-02
4.900e+00    5.648e-02    4.881e-02    6.960e-02
5.100e+00    5.664e-02    4.912e-02    6.983e-02
5.300e+00    5.679e-02    4.795e-02    7.005e-02
5.500e+00    5.693e-02    4.679e-02    7.026e-02
5.700e+00    5.707e-02    4.688e-02    7.049e-02
5.900e+00    5.722e-02    4.700e-02    7.074e-02
6.100e+00    5.741e-02    4.712e-02    7.105e-02
6.300e+00    5.766e-02    4.723e-02    7.147e-02
6.500e+00    5.801e-02    4.733e-02    7.205e-02
6.600e+00    5.824e-02    4.737e-02    7.242e-02
|
[Pullup]
|voltage          I(typ)         I(min)         I(max)
|
-3.30e+00    2.922e-04    2.177e-04    4.123e-04
-3.10e+00    2.881e-04    2.175e-04    4.021e-04
-2.90e+00    2.853e-04    2.173e-04    3.946e-04
-2.70e+00    2.836e-04    2.172e-04    3.893e-04
-2.50e+00    2.825e-04    2.171e-04    3.857e-04
-2.30e+00    2.819e-04    2.170e-04    3.834e-04
-2.10e+00    2.815e-04    2.169e-04    3.820e-04
-1.90e+00    2.813e-04    2.167e-04    3.812e-04
-1.70e+00    2.812e-04    2.520e-04    3.808e-04
-1.50e+00    2.811e-04    3.078e-02    3.806e-04
-1.30e+00    2.810e-04    2.684e-02    3.804e-04
-1.10e+00    2.809e-04    2.277e-02    3.802e-04
-9.00e-01    2.808e-04    1.864e-02    3.801e-04
-7.00e-01    2.997e-04    1.447e-02    3.799e-04
-5.00e-01    1.750e-02    1.031e-02    3.797e-04
-3.00e-01    1.048e-02    6.181e-03    3.776e-04
-1.00e-01    3.487e-03    2.084e-03    4.568e-03
1.000e-01    -3.40e-03    -2.03e-03    -4.22e-03
3.000e-01    -9.69e-03    -5.71e-03    -1.24e-02
5.000e-01    -1.52e-02    -8.99e-03    -1.95e-02
7.000e-01    -2.02e-02    -1.19e-02    -2.61e-02
9.000e-01    -2.46e-02    -1.43e-02    -3.21e-02
1.100e+00    -2.84e-02    -1.62e-02    -3.73e-02
1.300e+00    -3.14e-02    -1.77e-02    -4.18e-02
```

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1.500e+00    -3.37e-02    -1.88e-02    -4.55e-02
1.700e+00    -3.55e-02    -1.95e-02    -4.85e-02
1.900e+00    -3.68e-02    -2.00e-02    -5.09e-02
2.100e+00    -3.78e-02    -2.04e-02    -5.27e-02
2.300e+00    -3.85e-02    -2.07e-02    -5.41e-02
2.500e+00    -3.91e-02    -2.10e-02    -5.51e-02
2.700e+00    -3.96e-02    -2.12e-02    -5.60e-02
2.900e+00    -4.01e-02    -2.15e-02    -5.67e-02
3.100e+00    -4.04e-02    -2.17e-02    -5.74e-02
3.300e+00    -4.08e-02    -2.18e-02    -5.79e-02
3.500e+00    -4.11e-02    -2.20e-02    -5.84e-02
3.700e+00    -4.14e-02    -2.78e-02    -5.89e-02
3.900e+00    -4.17e-02    -1.20e+00    -5.94e-02
4.100e+00    -4.32e-02    -2.15e+01    -5.98e-02
4.300e+00    -4.08e-01    -4.52e+01    -6.10e-02
4.500e+00    -2.73e+01    -6.89e+01    -6.84e-02
4.700e+00    -6.13e+01    -9.25e+01    -7.73e+00
4.900e+00    -9.54e+01    -1.17e+02    -4.18e+01
5.100e+00    -1.38e+02    -1.52e+02    -7.59e+01
5.300e+00    -1.89e+02    -1.88e+02    -1.11e+02
5.500e+00    -2.40e+02    -2.23e+02    -1.61e+02
5.700e+00    -2.91e+02    -2.59e+02    -2.12e+02
5.900e+00    -3.42e+02    -2.94e+02    -2.63e+02
6.100e+00    -3.93e+02    -3.30e+02    -3.14e+02
6.300e+00    -4.44e+02    -3.65e+02    -3.65e+02
6.500e+00    -4.95e+02    -4.01e+02    -4.16e+02
6.600e+00    -5.21e+02    -4.18e+02    -4.41e+02
|
[GND_clamp]
|voltage          I(typ)         I(min)         I(max)
|
-3.30e+00    -5.21e+02    -3.65e+02    -5.18e+02
-3.10e+00    -4.69e+02    -3.30e+02    -4.67e+02
-2.90e+00    -4.18e+02    -2.94e+02    -4.16e+02
-2.70e+00    -3.67e+02    -2.59e+02    -3.65e+02
-2.50e+00    -3.16e+02    -2.23e+02    -3.14e+02
-2.30e+00    -2.65e+02    -1.88e+02    -2.63e+02
-2.10e+00    -2.14e+02    -1.52e+02    -2.12e+02
-1.90e+00    -1.63e+02    -1.17e+02    -1.61e+02
-1.70e+00    -1.13e+02    -9.25e+01    -1.10e+02
-1.50e+00    -7.83e+01    -6.88e+01    -7.58e+01
-1.30e+00    -4.43e+01    -4.52e+01    -4.17e+01
-1.10e+00    -1.02e+01    -2.15e+01    -7.67e+00
-9.00e-01    -9.69e-03    -1.18e+00    -7.81e-03
-7.00e-01    -2.83e-04    -5.70e-03    -8.42e-04
-5.00e-01    -1.35e-06    -4.53e-05    -1.00e-05
-3.00e-01    -1.31e-09    -3.74e-07    -8.58e-09
-1.00e-01    -2.92e-11    -3.00e-09    -3.64e-11
0.000e+00    -2.44e-11    -5.14e-10    -2.79e-11
|
[Ramp]
R_load = 50.00
|voltage          I(typ)         I(min)         I(max)
|
|
```

```
dV/dt_r        1.030/0.465    0.605/0.676    1.320/0.366
|
|
dV/dt_f        1.290/0.671    0.829/0.122    1.520/0.431
|
|
[Model]        icba_io
Model_type        I/O
Polarity        Non-Inverting
Vinl= 0.8000v
Vinh= 2.000v
C_comp        5.00pF        5.00pF        5.00pF
|
|
[Voltage Range]      3.3v      3v      3.6v
[Pulldown]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   -5.20e+02   -3.65e+02   -5.18e+02
-3.10e+00   -4.69e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.16e+02
-2.70e+00   -3.67e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.14e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.63e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.12e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.60e+02
-1.70e+00   -1.13e+02   -9.25e+01   -1.10e+02
-1.50e+00   -7.83e+01   -6.88e+01   -7.58e+01
-1.30e+00   -4.43e+01   -4.52e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.68e+00
-9.00e-01   -2.70e-02   -1.19e+00   -2.90e-02
-7.00e-01   -1.32e-02   -1.25e-02   -1.63e-02
-5.00e-01   -9.33e-03   -4.69e-03   -1.10e-02
-3.00e-01   -5.75e-03   -2.81e-03   -6.76e-03
-1.00e-01   -1.97e-03   -9.48e-04   -2.32e-03
1.000e-01   1.945e-03   9.285e-04   2.307e-03
3.000e-01   5.507e-03   2.640e-03   6.599e-03
5.000e-01   8.649e-03   4.168e-03   1.048e-02
7.000e-01   1.136e-02   5.504e-03   1.393e-02
9.000e-01   1.364e-02   6.636e-03   1.693e-02
1.100e+00   1.547e-02   7.551e-03   1.950e-02
1.300e+00   1.688e-02   8.240e-03   2.162e-02
1.500e+00   1.299e-01   6.458e-02   2.331e-02
1.700e+00   1.366e-01   6.746e-02   1.755e-01
1.900e+00   1.404e-01   6.916e-02   1.847e-01
2.100e+00   1.423e-01   7.006e-02   1.907e-01
2.300e+00   1.433e-01   7.059e-02   1.940e-01
2.500e+00   1.440e-01   7.098e-02   1.958e-01
2.700e+00   1.445e-01   7.128e-02   1.970e-01
2.900e+00   1.450e-01   7.154e-02   1.979e-01
3.100e+00   1.454e-01   7.176e-02   1.986e-01
3.300e+00   1.458e-01   7.196e-02   1.993e-01
3.500e+00   1.461e-01   7.223e-02   1.999e-01
3.700e+00   1.464e-01   8.810e-02   2.004e-01
3.900e+00   1.469e-01   2.589e+00   2.009e-01
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4.100e+00   1.490e-01   1.451e+01   2.015e-01
4.300e+00   1.501e+00   2.658e+01   2.030e-01
4.500e+00   1.813e+01   3.866e+01   2.385e-01
4.700e+00   3.540e+01   5.076e+01   9.563e+00
4.900e+00   5.269e+01   6.461e+01   2.682e+01
5.100e+00   7.541e+01   8.261e+01   4.409e+01
5.300e+00   1.012e+02   1.006e+02   6.258e+01
5.500e+00   1.270e+02   1.186e+02   8.836e+01
5.700e+00   1.527e+02   1.366e+02   1.141e+02
5.900e+00   1.785e+02   1.546e+02   1.399e+02
6.100e+00   2.043e+02   1.726e+02   1.657e+02
6.300e+00   2.301e+02   1.906e+02   1.915e+02
6.500e+00   2.559e+02   2.086e+02   2.173e+02
6.600e+00   2.688e+02   2.176e+02   2.302e+02
|
[Pullup]
|voltage        I(typ)         I(min)         I(max)
|
-3.30e+00   2.686e+02   1.905e+02   2.686e+02
-3.10e+00   2.428e+02   1.725e+02   2.428e+02
-2.90e+00   2.170e+02   1.545e+02   2.170e+02
-2.70e+00   1.912e+02   1.365e+02   1.912e+02
-2.50e+00   1.655e+02   1.185e+02   1.655e+02
-2.30e+00   1.397e+02   1.005e+02   1.397e+02
-2.10e+00   1.139e+02   8.253e+01   1.139e+02
-1.90e+00   8.814e+01   6.454e+01   8.814e+01
-1.70e+00   6.237e+01   5.068e+01   6.237e+01
-1.50e+00   4.389e+01   3.859e+01   4.389e+01
-1.30e+00   2.662e+01   2.651e+01   2.662e+01
-1.10e+00   9.360e+00   1.444e+01   9.362e+00
-9.00e-01   4.275e-02   2.518e+00   4.663e-02
-7.00e-01   8.208e-03   2.012e-02   1.070e-02
-5.00e-01   5.635e-03   3.518e-03   7.068e-03
-3.00e-01   3.370e-03   2.053e-03   4.233e-03
-1.00e-01   1.118e-03   6.789e-04   1.410e-03
1.000e-01   -1.09e-03   -6.56e-04   -1.38e-03
3.000e-01   -3.12e-03   -1.86e-03   -3.99e-03
5.000e-01   -4.96e-03   -2.93e-03   -6.39e-03
7.000e-01   -6.60e-03   -3.87e-03   -8.59e-03
9.000e-01   -8.04e-03   -4.66e-03   -1.06e-02
1.100e+00   -9.26e-03   -5.30e-03   -1.23e-02
1.300e+00   -1.03e-02   -6.55e-02   -1.38e-02
1.500e+00   -1.25e-01   -6.93e-02   -1.70e-01
1.700e+00   -1.31e-01   -7.19e-02   -1.82e-01
1.900e+00   -1.36e-01   -7.38e-02   -1.91e-01
2.100e+00   -1.40e-01   -7.53e-02   -1.97e-01
2.300e+00   -1.42e-01   -7.65e-02   -2.03e-01
2.500e+00   -1.44e-01   -7.76e-02   -2.07e-01
2.700e+00   -1.46e-01   -7.85e-02   -2.10e-01
2.900e+00   -1.48e-01   -7.93e-02   -2.13e-01
3.100e+00   -1.49e-01   -8.00e-02   -2.15e-01
3.300e+00   -1.50e-01   -8.06e-02   -2.17e-01
3.500e+00   -1.52e-01   -8.13e-02   -2.19e-01
3.700e+00   -1.53e-01   -8.84e-02   -2.21e-01
3.900e+00   -1.54e-01   -1.26e+00   -2.22e-01
```

```
4.100e+00   -1.57e-01   -2.16e+01   -2.24e-01
4.300e+00   -5.25e-01   -4.53e+01   -2.27e-01
4.500e+00   -2.74e+01   -6.89e+01   -2.38e-01
4.700e+00   -6.14e+01   -9.26e+01   -7.90e+00
4.900e+00   -9.55e+01   -1.17e+02   -4.20e+01
5.100e+00   -1.38e+02   -1.52e+02   -7.60e+01
5.300e+00   -1.89e+02   -1.88e+02   -1.11e+02
5.500e+00   -2.40e+02   -2.23e+02   -1.61e+02
5.700e+00   -2.91e+02   -2.59e+02   -2.12e+02
5.900e+00   -3.42e+02   -2.94e+02   -2.63e+02
6.100e+00   -3.93e+02   -3.30e+02   -3.14e+02
6.300e+00   -4.44e+02   -3.65e+02   -3.65e+02
6.500e+00   -4.95e+02   -4.01e+02   -4.16e+02
6.600e+00   -5.21e+02   -4.19e+02   -4.42e+02
|
[GND_clamp]
|voltage        I(typ)         I(min)         I(max)
|
-3.30e+00   -5.20e+02   -3.65e+02   -5.18e+02
-3.10e+00   -4.69e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.16e+02
-2.70e+00   -3.67e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.14e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.63e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.12e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.60e+02
-1.70e+00   -1.13e+02   -9.25e+01   -1.10e+02
-1.50e+00   -7.83e+01   -6.88e+01   -7.58e+01
-1.30e+00   -4.43e+01   -4.52e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.67e+00
-9.00e-01   -1.22e-02   -1.18e+00   -1.17e-02
-7.00e-01   -5.18e-04   -6.62e-03   -1.56e-03
-5.00e-01   -2.43e-06   -6.64e-05   -1.80e-05
-3.00e-01   -2.33e-09   -6.35e-07   -1.54e-08
-1.00e-01   -2.10e-11   -6.31e-09   -2.99e-11
0.000e+00   -1.70e-11   -1.95e-09   -1.91e-11
|
[POWER_clamp]
|voltage        I(typ)         I(min)         I(max)
|
-3.30e+00   2.686e+02   1.905e+02   2.686e+02
-3.10e+00   2.428e+02   1.725e+02   2.428e+02
-2.90e+00   2.170e+02   1.545e+02   2.170e+02
-2.70e+00   1.912e+02   1.365e+02   1.912e+02
-2.50e+00   1.655e+02   1.185e+02   1.655e+02
-2.30e+00   1.397e+02   1.005e+02   1.397e+02
-2.10e+00   1.139e+02   8.253e+01   1.139e+02
-1.90e+00   8.814e+01   6.454e+01   8.814e+01
-1.70e+00   6.236e+01   5.068e+01   6.237e+01
-1.50e+00   4.389e+01   3.859e+01   4.389e+01
-1.30e+00   2.662e+01   2.651e+01   2.662e+01
-1.10e+00   9.358e+00   1.444e+01   9.359e+00
-9.00e-01   3.399e-02   2.517e+00   3.554e-02
-7.00e-01   3.426e-04   1.577e-02   9.211e-04
-5.00e-01   2.840e-06   7.857e-05   1.655e-05
```

```
-3.00e-01   3.401e-09   6.836e-07   1.946e-08
-1.00e-01   6.162e-11   7.379e-09   7.622e-11
0.000e+00   5.758e-11   2.438e-09   6.240e-11
|
[Ramp]
R_load = 50.00
|voltage        I(typ)         I(min)         I(max)
|
|
dV/dt_r         1.680/0.164    1.360/0.329    1.900/0.124
|
|
dV/dt_f         1.690/0.219    1.310/0.442    1.880/0.155
|
|
[Model]         icba_o
Model_type         3-state
Polarity        Non-Inverting
C_comp         5.00pF         5.00pF         5.00pF
|
|
[Voltage Range]      3.3v      3v      3.6v
[Pulldown]
|voltage        I(typ)         I(min)         I(max)
|
-3.30e+00   -5.20e+02   -3.65e+02   -5.18e+02
-3.10e+00   -4.69e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.16e+02
-2.70e+00   -3.67e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.14e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.63e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.12e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.60e+02
-1.70e+00   -1.13e+02   -9.25e+01   -1.10e+02
-1.50e+00   -7.83e+01   -6.88e+01   -7.58e+01
-1.30e+00   -4.43e+01   -4.52e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.68e+00
-9.00e-01   -2.70e-02   -1.19e+00   -2.90e-02
-7.00e-01   -1.32e-02   -1.25e-02   -1.63e-02
-5.00e-01   -9.33e-03   -4.69e-03   -1.10e-02
-3.00e-01   -5.75e-03   -2.81e-03   -6.76e-03
-1.00e-01   -1.97e-03   -9.48e-04   -2.32e-03
1.000e-01   1.945e-03   9.285e-04   2.307e-03
3.000e-01   5.507e-03   2.640e-03   6.599e-03
5.000e-01   8.649e-03   4.168e-03   1.048e-02
7.000e-01   1.136e-02   5.504e-03   1.393e-02
9.000e-01   1.364e-02   6.636e-03   1.693e-02
1.100e+00   1.547e-02   7.551e-03   1.950e-02
1.300e+00   1.688e-02   8.240e-03   2.162e-02
1.500e+00   1.299e-01   6.458e-02   2.331e-02
1.700e+00   1.366e-01   6.746e-02   1.755e-01
1.900e+00   1.404e-01   6.916e-02   1.847e-01
2.100e+00   1.423e-01   7.006e-02   1.907e-01
2.300e+00   1.433e-01   7.059e-02   1.940e-01
2.500e+00   1.440e-01   7.098e-02   1.958e-01
```

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2.700e+00   1.445e-01   7.128e-02   1.970e-01
2.900e+00   1.450e-01   7.154e-02   1.979e-01
3.100e+00   1.454e-01   7.176e-02   1.986e-01
3.300e+00   1.458e-01   7.196e-02   1.993e-01
3.500e+00   1.461e-01   7.223e-02   1.999e-01
3.700e+00   1.464e-01   8.810e-02   2.004e-01
3.900e+00   1.469e-01   2.589e+00   2.009e-01
4.100e+00   1.490e-01   1.451e+01   2.015e-01
4.300e+00   1.501e+00   2.658e+01   2.030e-01
4.500e+00   1.813e+01   3.866e+01   2.385e-01
4.700e+00   3.540e+01   5.076e+01   9.563e+00
4.900e+00   5.269e+01   6.461e+01   2.682e+01
5.100e+00   7.541e+01   8.261e+01   4.409e+01
5.300e+00   1.012e+02   1.006e+02   6.258e+01
5.500e+00   1.270e+02   1.186e+02   8.836e+01
5.700e+00   1.527e+02   1.366e+02   1.141e+02
5.900e+00   1.785e+02   1.546e+02   1.399e+02
6.100e+00   2.043e+02   1.726e+02   1.657e+02
6.300e+00   2.301e+02   1.906e+02   1.915e+02
6.500e+00   2.559e+02   2.086e+02   2.173e+02
6.600e+00   2.688e+02   2.176e+02   2.302e+02
|
[Pullup]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   2.686e+02   1.905e+02   2.686e+02
-3.10e+00   2.428e+02   1.725e+02   2.428e+02
-2.90e+00   2.170e+02   1.545e+02   2.170e+02
-2.70e+00   1.912e+02   1.365e+02   1.912e+02
-2.50e+00   1.655e+02   1.185e+02   1.655e+02
-2.30e+00   1.397e+02   1.005e+02   1.397e+02
-2.10e+00   1.139e+02   8.253e+01   1.139e+02
-1.90e+00   8.814e+01   6.454e+01   8.814e+01
-1.70e+00   6.237e+01   5.068e+01   6.237e+01
-1.50e+00   4.389e+01   3.859e+01   4.389e+01
-1.30e+00   2.662e+01   2.651e+01   2.662e+01
-1.10e+00   9.360e+00   1.444e+01   9.362e+00
-9.00e-01   4.275e-02   2.518e+00   4.663e-02
-7.00e-01   8.208e-03   2.012e-02   1.070e-02
-5.00e-01   5.635e-03   3.518e-03   7.068e-03
-3.00e-01   3.370e-03   2.053e-03   4.233e-03
-1.00e-01   1.118e-03   6.789e-04   1.410e-03
1.000e-01   -1.09e-03   -6.56e-04   -1.38e-03
3.000e-01   -3.12e-03   -1.86e-03   -3.99e-03
5.000e-01   -4.96e-03   -2.93e-03   -6.39e-03
7.000e-01   -6.60e-03   -3.87e-03   -8.59e-03
9.000e-01   -8.04e-03   -4.66e-03   -1.06e-02
1.100e+00   -9.26e-03   -5.30e-03   -1.23e-02
1.300e+00   -1.03e-02   -6.55e-02   -1.38e-02
1.500e+00   -1.25e-01   -6.93e-02   -1.70e-01
1.700e+00   -1.31e-01   -7.19e-02   -1.82e-01
1.900e+00   -1.36e-01   -7.38e-02   -1.91e-01
2.100e+00   -1.40e-01   -7.53e-02   -1.97e-01
2.300e+00   -1.42e-01   -7.65e-02   -2.03e-01
2.500e+00   -1.44e-01   -7.76e-02   -2.07e-01
```

```
2.700e+00   -1.46e-01   -7.85e-02   -2.10e-01
2.900e+00   -1.48e-01   -7.93e-02   -2.13e-01
3.100e+00   -1.49e-01   -8.00e-02   -2.15e-01
3.300e+00   -1.50e-01   -8.06e-02   -2.17e-01
3.500e+00   -1.52e-01   -8.13e-02   -2.19e-01
3.700e+00   -1.53e-01   -8.84e-02   -2.21e-01
3.900e+00   -1.54e-01   -1.26e+00   -2.22e-01
4.100e+00   -1.57e-01   -2.16e+01   -2.24e-01
4.300e+00   -5.25e-01   -4.53e+01   -2.27e-01
4.500e+00   -2.74e+01   -6.89e+01   -2.38e-01
4.700e+00   -6.14e+01   -9.26e+01   -7.90e+00
4.900e+00   -9.55e+01   -1.17e+02   -4.20e+01
5.100e+00   -1.38e+02   -1.52e+02   -7.60e+01
5.300e+00   -1.89e+02   -1.88e+02   -1.11e+02
5.500e+00   -2.40e+02   -2.23e+02   -1.61e+02
5.700e+00   -2.91e+02   -2.59e+02   -2.12e+02
5.900e+00   -3.42e+02   -2.94e+02   -2.63e+02
6.100e+00   -3.93e+02   -3.30e+02   -3.14e+02
6.300e+00   -4.44e+02   -3.65e+02   -3.65e+02
6.500e+00   -4.95e+02   -4.01e+02   -4.16e+02
6.600e+00   -5.21e+02   -4.19e+02   -4.42e+02
|
[GND_clamp]
|voltage         I(typ)         I(min)         I(max)
|
-3.30e+00   -5.20e+02   -3.65e+02   -5.18e+02
-3.10e+00   -4.69e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.16e+02
-2.70e+00   -3.67e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.14e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.63e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.12e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.60e+02
-1.70e+00   -1.13e+02   -9.25e+01   -1.10e+02
-1.50e+00   -7.83e+01   -6.88e+01   -7.58e+01
-1.30e+00   -4.43e+01   -4.52e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.67e+00
-9.00e-01   -1.22e-02   -1.18e+00   -1.17e-02
-7.00e-01   -5.18e-04   -6.62e-03   -1.56e-03
-5.00e-01   -2.43e-06   -6.64e-05   -1.80e-05
-3.00e-01   -2.33e-09   -6.35e-07   -1.54e-08
-1.00e-01   -2.10e-11   -6.31e-09   -2.99e-11
0.000e+00   -1.70e-11   -1.95e-09   -1.91e-11
|
[POWER_clamp]
|voltage         I(typ)         I(min)         I(max)
|
-3.30e+00   2.686e+02   1.905e+02   2.686e+02
-3.10e+00   2.428e+02   1.725e+02   2.428e+02
-2.90e+00   2.170e+02   1.545e+02   2.170e+02
-2.70e+00   1.912e+02   1.365e+02   1.912e+02
-2.50e+00   1.655e+02   1.185e+02   1.655e+02
-2.30e+00   1.397e+02   1.005e+02   1.397e+02
-2.10e+00   1.139e+02   8.253e+01   1.139e+02
-1.90e+00   8.814e+01   6.454e+01   8.814e+01
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-1.70e+00   6.236e+01   5.068e+01   6.237e+01
-1.50e+00   4.389e+01   3.859e+01   4.389e+01
-1.30e+00   2.662e+01   2.651e+01   2.662e+01
-1.10e+00   9.358e+00   1.444e+01   9.359e+00
-9.00e-01   3.399e-02   2.517e+00   3.554e-02
-7.00e-01   3.426e-04   1.577e-02   9.211e-04
-5.00e-01   2.840e-06   7.857e-05   1.655e-05
-3.00e-01   3.401e-09   6.836e-07   1.946e-08
-1.00e-01   6.162e-11   7.379e-09   7.622e-11
0.000e+00   5.758e-11   2.438e-09   6.240e-11
|
[Ramp]
R_load = 50.00
|voltage         I(typ)         I(min)         I(max)
|
|
dV/dt_r        1.680/0.164    1.360/0.329    1.900/0.124
|
|
dV/dt_f        1.690/0.219    1.310/0.442    1.880/0.155
|
|
[Model]        icbc_o
Model_type        3-state
Polarity         Non-Inverting
C_comp         5.00pF         5.00pF         5.00pF
|
|
[Voltage Range]      3.3v      3v      3.6v
[Pulldown]
|voltage         I(typ)         I(min)         I(max)
|
-3.30e+00   -5.20e+02   -3.65e+02   -5.18e+02
-3.10e+00   -4.69e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.16e+02
-2.70e+00   -3.67e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.14e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.63e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.11e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.60e+02
-1.70e+00   -1.13e+02   -9.25e+01   -1.10e+02
-1.50e+00   -7.83e+01   -6.88e+01   -7.58e+01
-1.30e+00   -4.42e+01   -4.51e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.67e+00
-9.00e-01   -2.51e-02   -1.18e+00   -2.65e-02
-7.00e-01   -1.30e-02   -1.16e-02   -1.58e-02
-5.00e-01   -9.33e-03   -4.67e-03   -1.10e-02
-3.00e-01   -5.75e-03   -2.81e-03   -6.76e-03
-1.00e-01   -1.97e-03   -9.48e-04   -2.32e-03
1.000e-01   1.945e-03   9.285e-04   2.307e-03
3.000e-01   5.507e-03   2.640e-03   6.599e-03
5.000e-01   8.649e-03   4.168e-03   1.048e-02
7.000e-01   1.136e-02   5.504e-03   1.393e-02
9.000e-01   1.364e-02   6.636e-03   1.693e-02
1.100e+00   1.547e-02   7.551e-03   1.950e-02
```

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1.300e+00   1.688e-02   8.240e-03   2.162e-02
1.500e+00   9.632e-02   4.783e-02   2.331e-02
1.700e+00   1.012e-01   4.994e-02   1.302e-01
1.900e+00   1.039e-01   5.118e-02   1.369e-01
2.100e+00   1.053e-01   5.184e-02   1.412e-01
2.300e+00   1.060e-01   5.223e-02   1.436e-01
2.500e+00   1.065e-01   5.251e-02   1.449e-01
2.700e+00   1.069e-01   5.274e-02   1.458e-01
2.900e+00   1.073e-01   5.293e-02   1.464e-01
3.100e+00   1.076e-01   5.309e-02   1.470e-01
3.300e+00   1.078e-01   5.324e-02   1.475e-01
3.500e+00   1.081e-01   5.344e-02   1.479e-01
3.700e+00   1.083e-01   6.705e-02   1.483e-01
3.900e+00   1.086e-01   2.529e+00   1.487e-01
4.100e+00   1.103e-01   1.438e+01   1.491e-01
4.300e+00   1.437e+00   2.638e+01   1.503e-01
4.500e+00   1.800e+01   3.839e+01   1.810e-01
4.700e+00   3.519e+01   5.041e+01   9.452e+00
4.900e+00   5.241e+01   6.419e+01   2.664e+01
5.100e+00   7.505e+01   8.210e+01   4.384e+01
5.300e+00   1.007e+02   1.000e+02   6.224e+01
5.500e+00   1.264e+02   1.179e+02   8.794e+01
5.700e+00   1.522e+02   1.359e+02   1.136e+02
5.900e+00   1.779e+02   1.538e+02   1.394e+02
6.100e+00   2.036e+02   1.717e+02   1.651e+02
6.300e+00   2.293e+02   1.896e+02   1.908e+02
6.500e+00   2.550e+02   2.075e+02   2.165e+02
6.600e+00   2.678e+02   2.165e+02   2.293e+02
|
[Pullup]
|voltage         I(typ)          I(min)          I(max)
|
-3.30e+00   2.677e+02   1.896e+02   2.677e+02
-3.10e+00   2.420e+02   1.716e+02   2.420e+02
-2.90e+00   2.163e+02   1.537e+02   2.163e+02
-2.70e+00   1.906e+02   1.358e+02   1.906e+02
-2.50e+00   1.649e+02   1.179e+02   1.649e+02
-2.30e+00   1.392e+02   9.996e+01   1.392e+02
-2.10e+00   1.135e+02   8.205e+01   1.135e+02
-1.90e+00   8.778e+01   6.413e+01   8.778e+01
-1.70e+00   6.208e+01   5.035e+01   6.208e+01
-1.50e+00   4.368e+01   3.834e+01   4.368e+01
-1.30e+00   2.649e+01   2.633e+01   2.649e+01
-1.10e+00   9.302e+00   1.433e+01   9.303e+00
-9.00e-01   3.838e-02   2.477e+00   4.183e-02
-7.00e-01   8.115e-03   1.789e-02   1.045e-02
-5.00e-01   5.634e-03   3.503e-03   7.064e-03
-3.00e-01   3.370e-03   2.053e-03   4.233e-03
-1.00e-01   1.118e-03   6.789e-04   1.410e-03
1.000e-01   -1.09e-03   -6.56e-04   -1.38e-03
3.000e-01   -3.12e-03   -1.86e-03   -3.99e-03
5.000e-01   -4.96e-03   -2.93e-03   -6.39e-03
7.000e-01   -6.60e-03   -3.87e-03   -8.59e-03
9.000e-01   -8.04e-03   -4.66e-03   -1.06e-02
1.100e+00   -9.26e-03   -5.30e-03   -1.23e-02
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1.300e+00   -1.03e-02   -4.75e-02   -1.41e-02
1.500e+00   -9.03e-02   -5.02e-02   -1.23e-01
1.700e+00   -9.49e-02   -5.21e-02   -1.31e-01
1.900e+00   -9.84e-02   -5.34e-02   -1.38e-01
2.100e+00   -1.01e-01   -5.45e-02   -1.43e-01
2.300e+00   -1.03e-01   -5.54e-02   -1.47e-01
2.500e+00   -1.05e-01   -5.62e-02   -1.50e-01
2.700e+00   -1.06e-01   -5.68e-02   -1.52e-01
2.900e+00   -1.07e-01   -5.74e-02   -1.54e-01
3.100e+00   -1.08e-01   -5.79e-02   -1.56e-01
3.300e+00   -1.09e-01   -5.84e-02   -1.57e-01
3.500e+00   -1.10e-01   -5.89e-02   -1.59e-01
3.700e+00   -1.11e-01   -6.49e-02   -1.60e-01
3.900e+00   -1.11e-01   -1.23e+00   -1.61e-01
4.100e+00   -1.14e-01   -2.16e+01   -1.62e-01
4.300e+00   -4.76e-01   -4.52e+01   -1.64e-01
4.500e+00   -2.73e+01   -6.89e+01   -1.73e-01
4.700e+00   -6.14e+01   -9.25e+01   -7.82e+00
4.900e+00   -9.54e+01   -1.17e+02   -4.19e+01
5.100e+00   -1.38e+02   -1.52e+02   -7.59e+01
5.300e+00   -1.89e+02   -1.88e+02   -1.11e+02
5.500e+00   -2.40e+02   -2.23e+02   -1.61e+02
5.700e+00   -2.91e+02   -2.59e+02   -2.12e+02
5.900e+00   -3.42e+02   -2.94e+02   -2.63e+02
6.100e+00   -3.93e+02   -3.30e+02   -3.14e+02
6.300e+00   -4.44e+02   -3.65e+02   -3.65e+02
6.500e+00   -4.95e+02   -4.01e+02   -4.16e+02
6.600e+00   -5.20e+02   -4.18e+02   -4.41e+02
|
[GND_clamp]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   -5.20e+02   -3.65e+02   -5.18e+02
-3.10e+00   -4.69e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.16e+02
-2.70e+00   -3.67e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.14e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.63e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.11e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.60e+02
-1.70e+00   -1.13e+02   -9.25e+01   -1.10e+02
-1.50e+00   -7.83e+01   -6.88e+01   -7.58e+01
-1.30e+00   -4.42e+01   -4.51e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.66e+00
-9.00e-01   -1.03e-02   -1.17e+00   -9.27e-03
-7.00e-01   -3.74e-04   -5.73e-03   -1.14e-03
-5.00e-01   -1.72e-06   -5.06e-05   -1.28e-05
-3.00e-01   -1.67e-09   -4.65e-07   -1.10e-08
-1.00e-01   -2.03e-11   -4.80e-09   -2.71e-11
0.000e+00   -1.69e-11   -1.61e-09   -1.89e-11
|
[POWER_clamp]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   2.677e+02   1.896e+02   2.677e+02
```

```
-3.10e+00   2.420e+02   1.716e+02   2.420e+02
-2.90e+00   2.163e+02   1.537e+02   2.163e+02
-2.70e+00   1.906e+02   1.358e+02   1.906e+02
-2.50e+00   1.649e+02   1.179e+02   1.649e+02
-2.30e+00   1.392e+02   9.996e+01   1.392e+02
-2.10e+00   1.135e+02   8.205e+01   1.135e+02
-1.90e+00   8.778e+01   6.413e+01   8.778e+01
-1.70e+00   6.208e+01   5.035e+01   6.208e+01
-1.50e+00   4.368e+01   3.834e+01   4.368e+01
-1.30e+00   2.649e+01   2.633e+01   2.649e+01
-1.10e+00   9.300e+00   1.433e+01   9.301e+00
-9.00e-01   2.962e-02   2.475e+00   3.075e-02
-7.00e-01   2.501e-04   1.354e-02   6.708e-04
-5.00e-01   2.066e-06   6.280e-05   1.204e-05
-3.00e-01   2.487e-09   5.128e-07   1.417e-08
-1.00e-01   5.672e-11   5.639e-09   6.832e-11
0.000e+00   5.334e-11   1.992e-09   5.783e-11
|
[Ramp]
R_load = 50.00
|voltage        I(typ)         I(min)         I(max)
|
|
dV/dt_r        1.570/0.200    1.210/0.411    1.810/0.149
|
|
dV/dt_f        1.590/0.304    1.170/0.673    1.800/0.205
|
|
[Model]        ipbw_i
Model_type        Input
Polarity        Non-Inverting
Vinl= 0.8000v
Vinh= 2.000v
C_comp        5.00pF        5.00pF        5.00pF
|
|
[Voltage Range]      3.3v      3v      3.6v
[GND_clamp]
|voltage        I(typ)         I(min)         I(max)
|
-3.30e+00   -5.20e+02   -3.65e+02   -5.17e+02
-3.10e+00   -4.69e+02   -3.29e+02   -4.66e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.15e+02
-2.70e+00   -3.67e+02   -2.58e+02   -3.64e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.13e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.62e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.11e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.60e+02
-1.70e+00   -1.13e+02   -9.24e+01   -1.10e+02
-1.50e+00   -7.82e+01   -6.87e+01   -7.57e+01
-1.30e+00   -4.42e+01   -4.51e+01   -4.16e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.64e+00
-9.00e-01   -7.17e-03   -1.16e+00   -4.87e-03
-7.00e-01   -1.14e-04   -4.39e-03   -3.03e-04
```

```
-5.00e-01   -4.86e-07   -2.55e-05   -2.73e-06
-3.00e-01   -5.19e-10   -1.91e-07   -2.57e-09
-1.00e-01   -1.91e-11   -2.47e-09   -2.19e-11
0.000e+00   -1.68e-11   -1.17e-09   -1.84e-11
|
[POWER_clamp]
|voltage         I(typ)         I(min)         I(max)
|
-3.30e+00   2.667e+02   1.885e+02   2.667e+02
-3.10e+00   2.411e+02   1.707e+02   2.411e+02
-2.90e+00   2.155e+02   1.528e+02   2.155e+02
-2.70e+00   1.898e+02   1.350e+02   1.898e+02
-2.50e+00   1.642e+02   1.172e+02   1.642e+02
-2.30e+00   1.386e+02   9.935e+01   1.386e+02
-2.10e+00   1.130e+02   8.152e+01   1.130e+02
-1.90e+00   8.739e+01   6.369e+01   8.739e+01
-1.70e+00   6.178e+01   4.999e+01   6.178e+01
-1.50e+00   4.346e+01   3.806e+01   4.346e+01
-1.30e+00   2.634e+01   2.613e+01   2.634e+01
-1.10e+00   9.237e+00   1.421e+01   9.237e+00
-9.00e-01   2.454e-02   2.430e+00   2.488e-02
-7.00e-01   8.741e-05   1.104e-02   2.050e-04
-5.00e-01   6.316e-07   4.079e-05   2.961e-06
-3.00e-01   8.479e-10   2.484e-07   3.721e-09
-1.00e-01   4.420e-11   3.001e-09   4.943e-11
0.000e+00   4.215e-11   1.346e-09   4.543e-11
|
|
[Model]         ipbw_io
Model_type         I/O
Polarity         Non-Inverting
Vinl= 0.8000v
Vinh= 2.000v
C_comp        5.00pF        5.00pF        5.00pF
|
|
[Voltage Range]      3.3v      3v      3.6v
[Pulldown]
|voltage         I(typ)         I(min)         I(max)
|
-3.30e+00   -5.20e+02   -3.65e+02   -5.17e+02
-3.10e+00   -4.69e+02   -3.29e+02   -4.66e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.15e+02
-2.70e+00   -3.67e+02   -2.58e+02   -3.64e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.13e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.62e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.11e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.60e+02
-1.70e+00   -1.13e+02   -9.24e+01   -1.10e+02
-1.50e+00   -7.82e+01   -6.87e+01   -7.57e+01
-1.30e+00   -4.42e+01   -4.51e+01   -4.17e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.66e+00
-9.00e-01   -3.69e-02   -1.17e+00   -3.79e-02
-7.00e-01   -2.52e-02   -1.67e-02   -2.81e-02
-5.00e-01   -1.83e-02   -9.77e-03   -2.04e-02
```

```
-3.00e-01   -1.11e-02   -5.89e-03   -1.24e-02
-1.00e-01   -3.77e-03   -1.98e-03   -4.20e-03
1.000e-01   3.729e-03   1.940e-03   4.177e-03
3.000e-01   1.076e-02   5.578e-03   1.216e-02
5.000e-01   1.723e-02   8.907e-03   1.965e-02
7.000e-01   2.311e-02   1.191e-02   2.663e-02
9.000e-01   2.836e-02   1.455e-02   3.305e-02
1.100e+00   3.292e-02   1.680e-02   3.887e-02
1.300e+00   3.675e-02   1.862e-02   4.404e-02
1.500e+00   3.979e-02   1.997e-02   4.850e-02
1.700e+00   4.205e-02   2.085e-02   5.223e-02
1.900e+00   4.347e-02   2.136e-02   5.518e-02
2.100e+00   4.413e-02   2.162e-02   5.728e-02
2.300e+00   4.445e-02   2.176e-02   5.843e-02
2.500e+00   4.465e-02   2.186e-02   5.899e-02
2.700e+00   4.479e-02   2.194e-02   5.931e-02
2.900e+00   4.492e-02   2.200e-02   5.953e-02
3.100e+00   4.502e-02   2.206e-02   5.971e-02
3.300e+00   4.511e-02   2.211e-02   5.986e-02
3.500e+00   4.519e-02   2.219e-02   5.999e-02
3.700e+00   4.526e-02   3.324e-02   6.010e-02
3.900e+00   4.536e-02   2.452e+00   6.021e-02
4.100e+00   4.614e-02   1.423e+01   6.032e-02
4.300e+00   1.344e+00   2.615e+01   6.065e-02
4.500e+00   1.783e+01   3.808e+01   8.548e-02
4.700e+00   3.495e+01   5.001e+01   9.298e+00
4.900e+00   5.208e+01   6.371e+01   2.640e+01
5.100e+00   7.463e+01   8.154e+01   4.352e+01
5.300e+00   1.002e+02   9.937e+01   6.184e+01
5.500e+00   1.259e+02   1.172e+02   8.745e+01
5.700e+00   1.515e+02   1.350e+02   1.131e+02
5.900e+00   1.771e+02   1.529e+02   1.387e+02
6.100e+00   2.027e+02   1.707e+02   1.643e+02
6.300e+00   2.283e+02   1.885e+02   1.899e+02
6.500e+00   2.539e+02   2.064e+02   2.155e+02
6.600e+00   2.667e+02   2.153e+02   2.283e+02
|
[Pullup]
|voltage        I(typ)         I(min)         I(max)
|
-3.30e+00   2.667e+02   1.885e+02   2.667e+02
-3.10e+00   2.411e+02   1.707e+02   2.411e+02
-2.90e+00   2.155e+02   1.528e+02   2.155e+02
-2.70e+00   1.898e+02   1.350e+02   1.898e+02
-2.50e+00   1.642e+02   1.172e+02   1.642e+02
-2.30e+00   1.386e+02   9.935e+01   1.386e+02
-2.10e+00   1.130e+02   8.152e+01   1.130e+02
-1.90e+00   8.739e+01   6.369e+01   8.739e+01
-1.70e+00   6.178e+01   4.999e+01   6.178e+01
-1.50e+00   4.346e+01   3.806e+01   4.346e+01
-1.30e+00   2.635e+01   2.613e+01   2.635e+01
-1.10e+00   9.243e+00   1.421e+01   9.245e+00
-9.00e-01   5.536e-02   2.435e+00   6.260e-02
-7.00e-01   2.847e-02   2.689e-02   3.437e-02
-5.00e-01   2.025e-02   1.265e-02   2.451e-02
```

```
-3.00e-01   1.208e-02   7.503e-03   1.467e-02
-1.00e-01   3.994e-03   2.474e-03   4.868e-03
1.000e-01   -3.88e-03   -2.38e-03   -4.76e-03
3.000e-01   -1.11e-02   -6.76e-03   -1.37e-02
5.000e-01   -1.76e-02   -1.06e-02   -2.20e-02
7.000e-01   -2.35e-02   -1.40e-02   -2.95e-02
9.000e-01   -2.86e-02   -1.69e-02   -3.63e-02
1.100e+00   -3.30e-02   -1.93e-02   -4.23e-02
1.300e+00   -3.65e-02   -2.10e-02   -4.75e-02
1.500e+00   -3.92e-02   -2.22e-02   -5.17e-02
1.700e+00   -4.12e-02   -2.29e-02   -5.51e-02
1.900e+00   -4.26e-02   -2.35e-02   -5.77e-02
2.100e+00   -4.36e-02   -2.38e-02   -5.97e-02
2.300e+00   -4.43e-02   -2.42e-02   -6.11e-02
2.500e+00   -4.49e-02   -2.44e-02   -6.22e-02
2.700e+00   -4.54e-02   -2.47e-02   -6.31e-02
2.900e+00   -4.58e-02   -2.49e-02   -6.38e-02
3.100e+00   -4.61e-02   -2.50e-02   -6.44e-02
3.300e+00   -4.65e-02   -2.52e-02   -6.49e-02
3.500e+00   -4.68e-02   -2.54e-02   -6.54e-02
3.700e+00   -4.70e-02   -2.99e-02   -6.58e-02
3.900e+00   -4.73e-02   -1.19e+00   -6.62e-02
4.100e+00   -4.81e-02   -2.15e+01   -6.66e-02
4.300e+00   -4.00e-01   -4.51e+01   -6.72e-02
4.500e+00   -2.72e+01   -6.87e+01   -7.21e-02
4.700e+00   -6.12e+01   -9.24e+01   -7.70e+00
4.900e+00   -9.52e+01   -1.17e+02   -4.17e+01
5.100e+00   -1.37e+02   -1.52e+02   -7.57e+01
5.300e+00   -1.88e+02   -1.88e+02   -1.10e+02
5.500e+00   -2.39e+02   -2.23e+02   -1.60e+02
5.700e+00   -2.90e+02   -2.58e+02   -2.11e+02
5.900e+00   -3.41e+02   -2.94e+02   -2.62e+02
6.100e+00   -3.92e+02   -3.29e+02   -3.13e+02
6.300e+00   -4.43e+02   -3.65e+02   -3.64e+02
6.500e+00   -4.94e+02   -4.00e+02   -4.15e+02
6.600e+00   -5.20e+02   -4.18e+02   -4.41e+02
|
[GND_clamp]
|voltage        I(typ)         I(min)         I(max)
|
-3.30e+00   -5.20e+02   -3.65e+02   -5.17e+02
-3.10e+00   -4.69e+02   -3.29e+02   -4.66e+02
-2.90e+00   -4.18e+02   -2.94e+02   -4.15e+02
-2.70e+00   -3.67e+02   -2.58e+02   -3.64e+02
-2.50e+00   -3.16e+02   -2.23e+02   -3.13e+02
-2.30e+00   -2.65e+02   -1.88e+02   -2.62e+02
-2.10e+00   -2.14e+02   -1.52e+02   -2.11e+02
-1.90e+00   -1.63e+02   -1.17e+02   -1.60e+02
-1.70e+00   -1.13e+02   -9.24e+01   -1.10e+02
-1.50e+00   -7.82e+01   -6.87e+01   -7.57e+01
-1.30e+00   -4.42e+01   -4.51e+01   -4.16e+01
-1.10e+00   -1.02e+01   -2.15e+01   -7.64e+00
-9.00e-01   -7.17e-03   -1.16e+00   -4.87e-03
-7.00e-01   -1.14e-04   -4.39e-03   -3.03e-04
-5.00e-01   -4.86e-07   -2.55e-05   -2.73e-06
```

```
-3.00e-01   -5.19e-10   -1.91e-07   -2.57e-09
-1.00e-01   -1.91e-11   -2.47e-09   -2.19e-11
0.000e+00   -1.68e-11   -1.17e-09   -1.84e-11
|
[POWER_clamp]
|voltage         I(typ)         I(min)         I(max)
|
-3.30e+00   2.667e+02   1.885e+02   2.667e+02
-3.10e+00   2.411e+02   1.707e+02   2.411e+02
-2.90e+00   2.155e+02   1.528e+02   2.155e+02
-2.70e+00   1.898e+02   1.350e+02   1.898e+02
-2.50e+00   1.642e+02   1.172e+02   1.642e+02
-2.30e+00   1.386e+02   9.935e+01   1.386e+02
-2.10e+00   1.130e+02   8.152e+01   1.130e+02
-1.90e+00   8.739e+01   6.369e+01   8.739e+01
-1.70e+00   6.178e+01   4.999e+01   6.178e+01
-1.50e+00   4.346e+01   3.806e+01   4.346e+01
-1.30e+00   2.634e+01   2.613e+01   2.634e+01
-1.10e+00   9.237e+00   1.421e+01   9.237e+00
-9.00e-01   2.454e-02   2.430e+00   2.488e-02
-7.00e-01   8.741e-05   1.104e-02   2.050e-04
-5.00e-01   6.316e-07   4.079e-05   2.961e-06
-3.00e-01   8.479e-10   2.484e-07   3.721e-09
-1.00e-01   4.420e-11   3.001e-09   4.943e-11
0.000e+00   4.215e-11   1.346e-09   4.543e-11
|
[Ramp]
R_load = 50.00
|voltage         I(typ)         I(min)         I(max)
|
|
dV/dt_r        1.140/0.494    0.699/0.978    1.400/0.354
|
|
dV/dt_f        1.150/0.505    0.642/0.956    1.350/0.350
|
|
[Model]        iexlh_i
Model_type        Input
Polarity        Non-Inverting
Vinl= 0.8000v
Vinh= 2.000v
C_comp        5.00pF        5.00pF        5.00pF
|
|
[Voltage Range]      3.3v      3v      3.6v
[GND_clamp]
|voltage         I(typ)         I(min)         I(max)
|
-3.30e+00   -5.21e+02   -3.66e+02   -5.18e+02
-3.10e+00   -4.70e+02   -3.30e+02   -4.67e+02
-2.90e+00   -4.19e+02   -2.95e+02   -4.16e+02
-2.70e+00   -3.68e+02   -2.59e+02   -3.65e+02
-2.50e+00   -3.17e+02   -2.24e+02   -3.14e+02
-2.30e+00   -2.66e+02   -1.89e+02   -2.63e+02
```

```
-2.10e+00   -2.15e+02   -1.53e+02   -2.12e+02
-1.90e+00   -1.64e+02   -1.18e+02   -1.61e+02
-1.70e+00   -1.14e+02   -9.34e+01   -1.11e+02
-1.50e+00   -7.93e+01   -6.98e+01   -7.68e+01
-1.30e+00   -4.53e+01   -4.62e+01   -4.28e+01
-1.10e+00   -1.13e+01   -2.26e+01   -8.78e+00
-9.00e-01   -7.94e-03   -1.87e+00   -3.77e-03
-7.00e-01   -1.62e-06   -5.11e-03   -7.69e-07
-5.00e-01   -3.45e-10   -1.40e-05   -1.72e-10
-3.00e-01   -1.29e-11   -3.90e-08   -1.38e-11
-1.00e-01   -1.10e-11   -8.67e-10   -1.19e-11
0.000e+00   -1.01e-11   -7.13e-10   -1.10e-11
|
[POWER_clamp]
|voltage        I(typ)        I(min)        I(max)
|
-3.30e+00   2.653e+02   1.870e+02   2.653e+02
-3.10e+00   2.398e+02   1.693e+02   2.398e+02
-2.90e+00   2.143e+02   1.516e+02   2.143e+02
-2.70e+00   1.888e+02   1.339e+02   1.888e+02
-2.50e+00   1.633e+02   1.162e+02   1.633e+02
-2.30e+00   1.378e+02   9.847e+01   1.378e+02
-2.10e+00   1.123e+02   8.076e+01   1.123e+02
-1.90e+00   8.682e+01   6.305e+01   8.682e+01
-1.70e+00   6.133e+01   4.947e+01   6.133e+01
-1.50e+00   4.313e+01   3.766e+01   4.313e+01
-1.30e+00   2.614e+01   2.585e+01   2.614e+01
-1.10e+00   9.145e+00   1.404e+01   9.145e+00
-9.00e-01   1.797e-02   2.364e+00   1.797e-02
-7.00e-01   3.667e-06   7.589e-03   3.667e-06
-5.00e-01   7.730e-10   2.072e-05   7.748e-10
-3.00e-01   2.293e-11   5.767e-08   2.476e-11
-1.00e-01   2.096e-11   1.163e-09   2.278e-11
0.000e+00   2.004e-11   9.618e-10   2.186e-11
|
[End]
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