70-V Fault-Protected RS-485 Transceiver With Cable Invert

Check for Samples: SN65HVD1794, SN65HVD1795, SN65HVD1796

FEATURES

- **Bus-Pin Fault Protection to > ±70 V**
- **Cable Invert Function Allows Correction for Reversed Bus Pins**
- **Common-Mode Voltage Range (–20 V to 25 V) More Than Doubles TIA/EIA 485 Requirement**
- **Bus I/O Protection**
  - **±16 kV JEDEC HBM Protection**
- **Reduced Unit Load for Up to 256 Nodes**
- **Failsafe Receiver for Open-Circuit, Short-Circuit and Idle-Bus Conditions**
- **Low Power Consumption**
  - **I_{CC} 5 mA Quiescent During Operation**
- **Power-Up, Power-Down Glitch-Free Operation**

APPLICATIONS

- **Designed for RS-485 and RS-422 Networks**

DESCRIPTION

These devices are designed to survive overvoltage faults such as direct shorts to power supplies, mis-wiring faults, connector failures, cable crushes, and tool mis-applications. They are also robust to ESD events, with high levels of protection to human-body model specifications.

These devices combine a differential driver and a differential receiver, which operate from a single power supply. The driver differential outputs and the receiver differential inputs are connected internally to for a bus port suitable for half-duplex (two-wire bus) communication. A cable invert pin (INV) allows active correction of mis-wires that may occur during installation. Upon detecting communication errors, the user can apply a logic HIGH to the INV pin, effectively inverting the polarity of the differential bus port, thereby correcting for the reversed bus wires.

These devices feature a wide common-mode voltage range, making them suitable for multi-point applications over long cable runs. These devices are characterized from –40°C to 105°C.

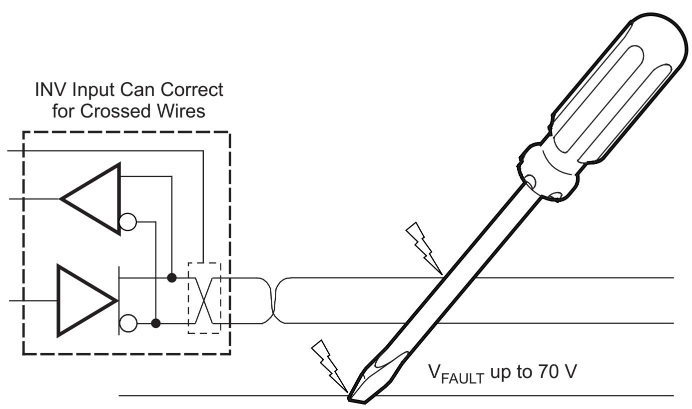


Table 1. PRODUCT SELECTION GUIDE

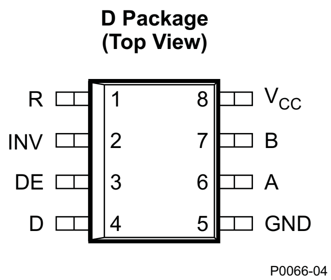
PART NUMBER	DUPLEX	SIGNALING RATE	NODES	CABLE LENGTH
SN65HVD1794	Half	115 kbps	Up to 256	1500 m
SN65HVD1795 PREVIEW	Half	1 Mbps	Up to 256	150 m
SN65HVD1796 PREVIEW	Half	10 Mbps	Up to 64	50 m

For similar features with 3.3 V supply operation, see the SN65HVD1781 (SLLS877).

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DEVICE INFORMATION



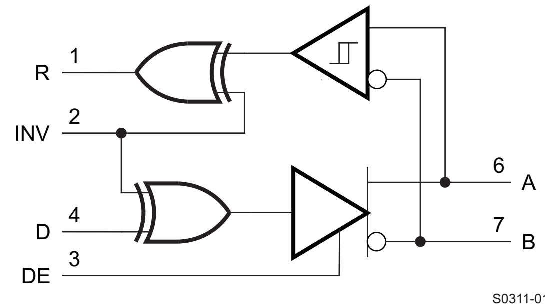


Figure 1. SN65HVD17xx With Inverting Feature to Correct for Miswired Cables

DRIVER FUNCTION TABLE

INPUT	ENABLE	INVERT	OUTPUTS		
D	DE	INV	A	B	
H	H	L	H	L	Actively drive normal bus High
L	H	L	L	H	Actively drive normal bus Low
H	H	H	L	H	Actively drive inverted bus High (drive normal bus Low)
L	H	H	H	L	Actively drive inverted bus Low (drive normal bus High)
X	L	X	Z	Z	Driver disabled
X	OPEN	X	Z	Z	Driver disabled by default
OPEN	H	L	H	L	Actively drive bus High by default
OPEN	H	H	L	H	Actively drive bus Low by default (inverted cable)

RECEIVER FUNCTION TABLE

DIFFERENTIAL INPUT	INVERT	OUTPUT	
$V_{ID} = V_A - V_B$	INV	R	
$V_{IT+} < V_{ID}$	L or OPEN	H	Receive valid bus High
	H	L	Receive inverted bus Low
$V_{IT-} < V_{ID} < V_{IT+}$	X	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L or OPEN	L	Receive valid bus Low
	H	H	Receive inverted bus High
Open-circuit bus	L or OPEN	H	Fail-safe high output
	H	L	Failsafe inverted output
Short-circuit bus	L or OPEN	H	Fail-safe high output
	H	L	Failsafe inverted output
Idle (terminated) bus	L or OPEN	H	Fail-safe high output
	H	L	Failsafe inverted output

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
V_{CC}	Supply voltage	–0.5 to 7	V
	Voltage range at A and B pins with respect to GND	–70 to 70	V
	Voltage range across A and B pins (differential)	–70 to 70	V
	Input voltage range at any logic pin	–0.3 to V_{CC} + 0.3	V
	Voltage input range, transient pulse, A and B, through 100 Ω	–100 to 100	V
	Receiver output current	–24 to 24	mA
T_J	Junction temperature	170	°C
	Continuous total power dissipation	See Dissipation Rating Table	
	IEC 60749-26 ESD (human-body model), bus terminals and GND	±16	kV
	JEDEC Standard 22, Test Method A114 (human-body model), bus terminals and GND	±16	kV
	JEDEC Standard 22, Test Method A114 (human-body model), all pins	±4	kV
	JEDEC Standard 22, Test Method C101 (charged-device model), all pins	±2	kV
	JEDEC Standard 22, Test Method A115 (machine model), all pins	±400	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE DISSIPATION RATINGS

PACKAGE	JEDEC THERMAL MODEL	T_A < 25°C RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C RATING	T_A = 105°C RATING
SOIC (D) 8-pin	High-K	905 mW	7.25 mW/°C	470 mW	325 mW
	Low-K	516 mW	4.1 mW/°C	268 mW	186 mW
PDIP (P) 8-pin	High-K	2119 mW	16.9 mW/°C	1100 mW	763 mW
	Low-K	976 mW	7.8 mW/°C	508 mW	352 mW

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)(1)		–20		25	V
V_{IH}	High-level input voltage (driver, driver enable, and invert inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver enable, and invert inputs)		0		0.8	V
V_{ID}	Differential input voltage		–25		25	V
I_O	Output current, driver		–60		60	mA
	Output current, receiver		–8		8	mA
R_L	Differential load resistance		54	60		Ω
C_L	Differential load capacitance			50		pF
$1/t_{UI}$	Signaling rate	HVD1794			115	kbps
		HVD1795			1	Mbps
		HVD1796			10	
T_A	Operating free-air temperature (See application section for thermal information)		–40		105	°C
T_J	Junction temperature		–40		150	°C

(1) By convention, the least positive (most negative) limit is designated as minimum in this data sheet.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$\lvert V_{OD}\rvert$	Driver differential output voltage magnitude	RS-485 with common-mode load, V_{CC} > 4.75 V, see Figure 2	T_A ≤ 85°C		1.5			V
			T_A ≤ 105°C		1.4			
		R_L = 54 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V			1.5	2		
		R_L = 100 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V			2	2.5		
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of driver differential output voltage	R_L = 54 Ω			–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage				1	V_{CC}/2	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage				–100	0	100	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors, See Figure 3				500		mV
C_{OD}	Differential output capacitance					23		pF
V_{IT+}	Positive-going receiver differential input voltage threshold	V_{CM} = –20 V to 25 V				–100	–10	mV
$V_{IT–}$	Negative-going receiver differential input voltage threshold				–200	–150		mV
V_{HYS}	Receiver differential input voltage threshold hysteresis (V_{IT+} – $V_{IT–}$)				30	50		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA			2.4	V_{CC} – 0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA	T_A ≤ 85°C			0.2	0.4	V
			T_A ≤ 105°C			0.2	0.5	
I_I	Driver input, driver enable, and invert input current				–100		100	μA
I_{OS}	Driver short-circuit output current				–250		250	mA
I_I	Bus input current (disabled driver)	V_{CC} = 4.5 to 5.5 V or V_{CC} = 0 V, DE at 0 V	94, 95	V_I = 12 V		75	125	μA
				V_I = –7 V	–100	–40		
			96	V_I = 12 V			500	
				V_I = –7 V	–400			
I_{CC}	Supply current (quiescent)	Driver enabled	DE = 5V			4	6	mA
		Driver disabled	DE = GND			2	4	
	Supply current (dynamic)	See TYPICAL CHARACTERISTICS section						

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER (HVD1794)							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, See Figure 4		0.4	1.7	2.6	μs
t_{PHL}, t_{PLH}	Driver propagation delay				0.8	2	μs
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} – t_{PLH}\|$				20	250	ns
t_{PHZ}, t_{PLZ}	Driver disable time	See Figure 5 and Figure 6			0.1	5	μs
t_{PZH}, t_{PZL}	Driver enable time				0.2	3	μs
DRIVER (HVD1795)							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, See Figure 4		50		300	ns
t_{PHL}, t_{PLH}	Driver propagation delay					200	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} – t_{PLH}\|$					25	ns
t_{PHZ}, t_{PLZ}	Driver disable time	See Figure 5 and Figure 6				3	μs
t_{PZH}, t_{PZL}	Driver enable time					500	ns
DRIVER (HVD1796)							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, See Figure 4		3		30	ns
t_{PHL}, t_{PLH}	Driver propagation delay					50	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} – t_{PLH}\|$					10	ns
t_{PHZ}, t_{PLZ}	Driver disable time	See Figure 5 and Figure 6				3	μs
t_{PZH}, t_{PZL}	Driver enable time					500	ns
RECEIVER (ALL DEVICES UNLESS OTHERWISE NOTED)							
t_r, t_f	Receiver output rise/fall time	C_L = 15 pF, See Figure 7			4	15	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time		94, 95		100	200	ns
			96			70	
$t_{SK(P)}$	Receiver output pulse skew, $\|t_{PHL} – t_{PLH}\|$		94, 95		6	20	ns
			96			5	

THERMAL INFORMATION

PARAMETER		TEST CONDITIONS	VALUE	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance (no airflow)	SOIC-8	JEDEC high-K model	138	°C/W
		JEDIC low-K model	242	
	DIP-8	JEDEC high-K model	59	
		JEDIC low-K model	128	
$R_{\theta JB}$ Junction-to-board thermal resistance	SOIC-8		62	°C/W
	DIP-8		39	
$R_{\theta JC}$ Junction-to-case thermal resistance	SOIC-8		61	°C/W
	DIP-8		61	
P_D Power dissipation	94	V_{CC} = 5.5 V, T_J = 150°C, R_L = 300 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, unterminated(1)	290	mW
	94	V_{CC} = 5.5 V, T_J = 150°C, R_L = 100 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, RS-422 load(1)		
	95		320	
	96			
	94	V_{CC} = 5.5 V, T_J = 150°C, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, RS-485 load(1)	400	
	95			
	96			
T_{SD} Thermal-shutdown junction temperature			170	°C

(1) Driver enabled, 50% duty cycle square-wave signal at signaling rate: 115 kbps for HVD1794, 1 Mbps for HVD1795, 10 Mbps for HVD1796

PARAMETER MEASUREMENT INFORMATION

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50 Ω.

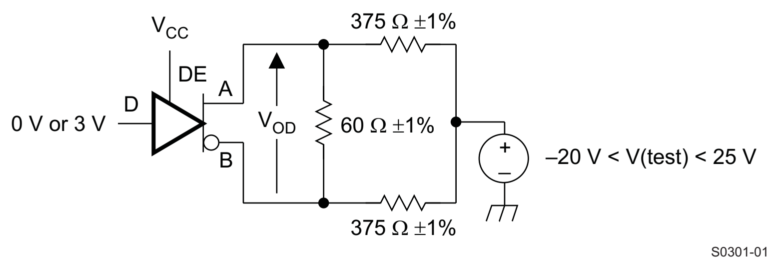


Figure 2. Measurement of Driver Differential Output Voltage With Common-Mode Load

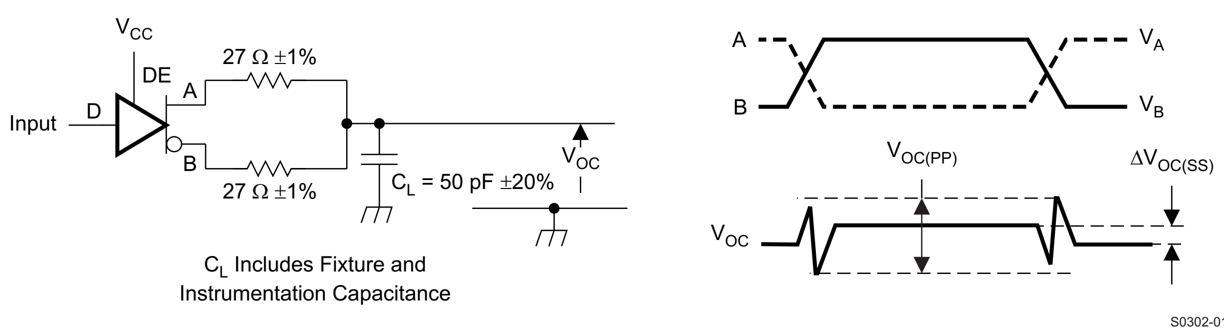


Figure 3. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

PARAMETER MEASUREMENT INFORMATION (continued)

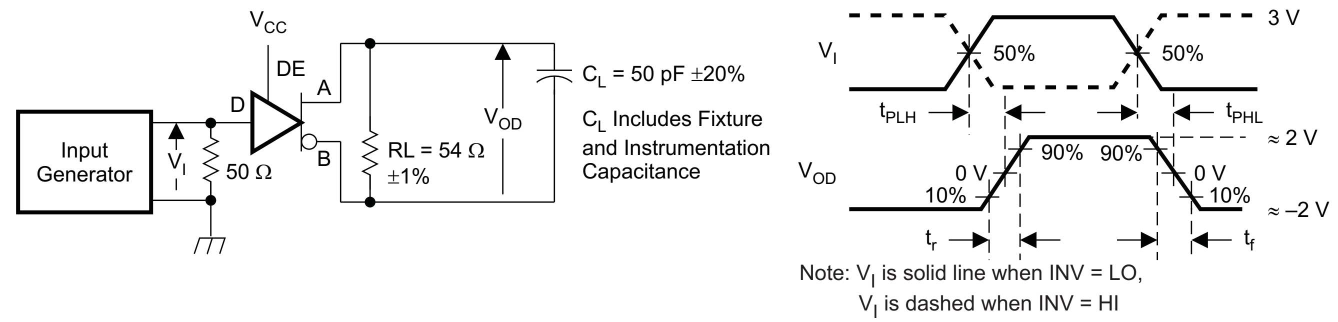
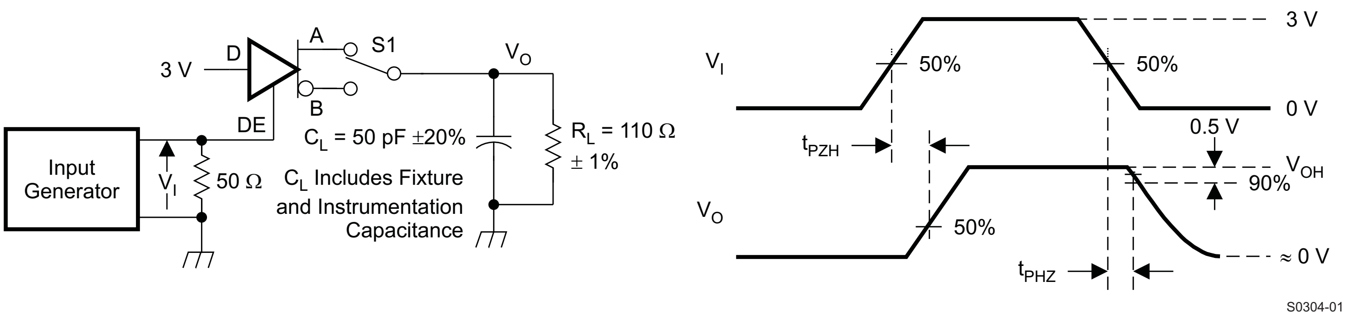
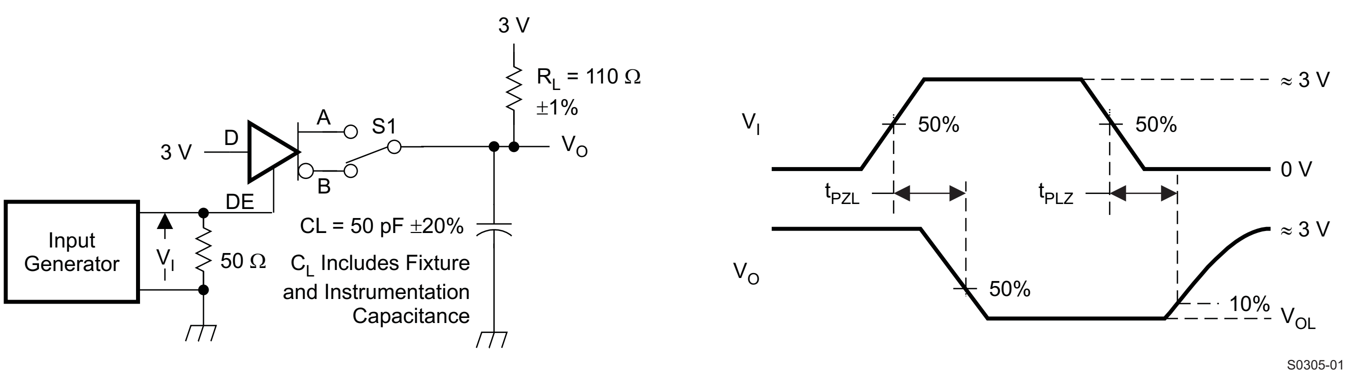


Figure 4. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



NOTE: D at 3 V to test non-inverting output, D at 0 V to test inverting output.

Figure 5. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load



NOTE: D at 0 V to test non-inverting output, D at 3 V to test inverting output.

Figure 6. Measurement of Driver Enable and Disable Times With Active-Low Output and Pullup Load

PARAMETER MEASUREMENT INFORMATION (continued)

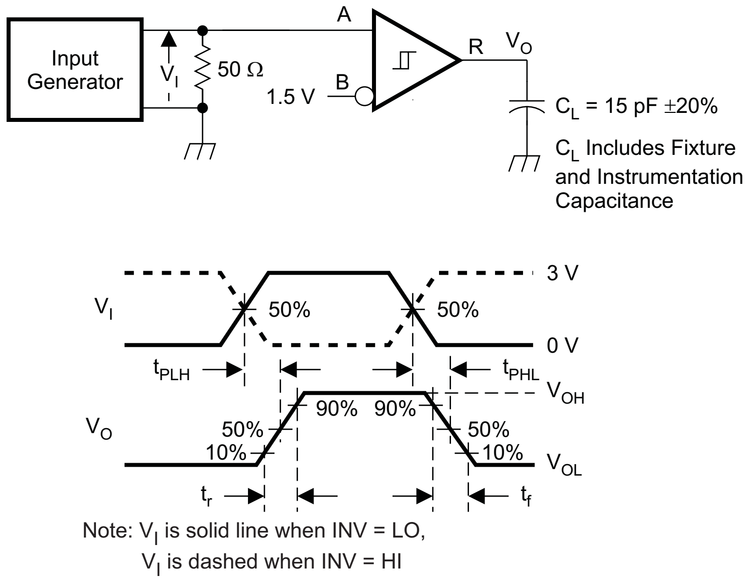


Figure 7. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

TYPICAL CHARACTERISTICS

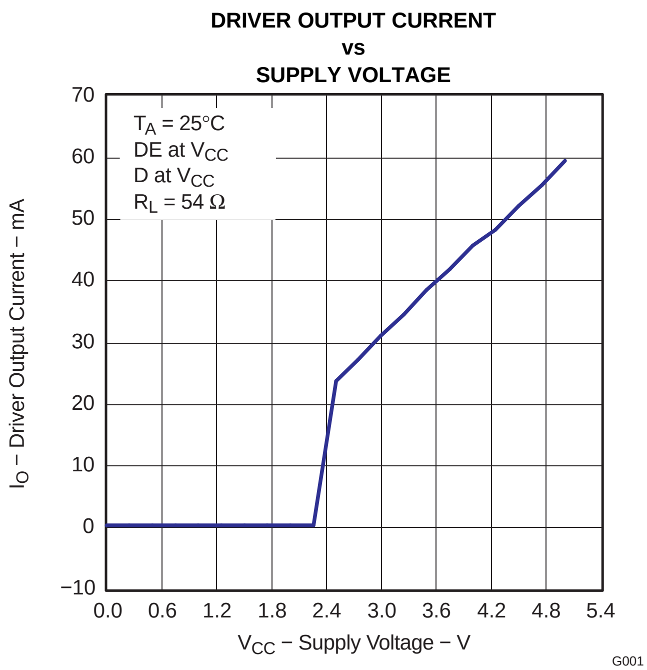


Figure 8.

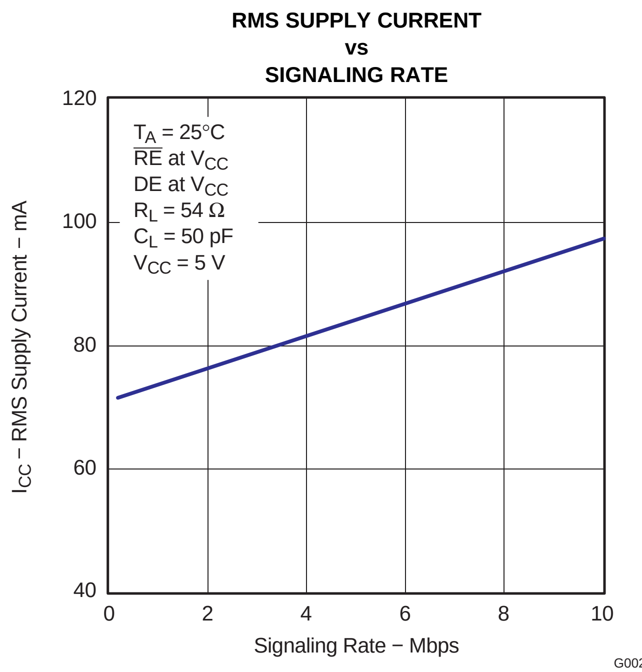


Figure 9.

TYPICAL CHARACTERISTICS (continued)

**BUS PIN CURRENT
vs
BUS PIN VOLTAGE**

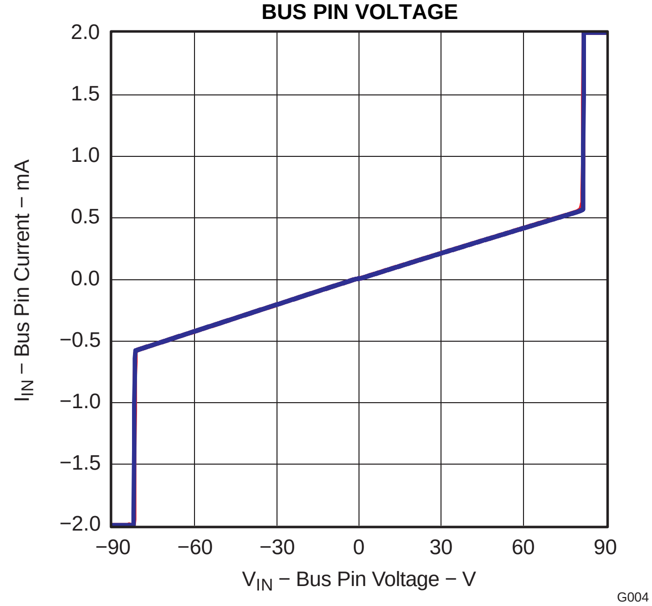


Figure 10.

**DIFFERENTIAL OUTPUT VOLTAGE
vs
DIFFERENTIAL LOAD CURRENT**

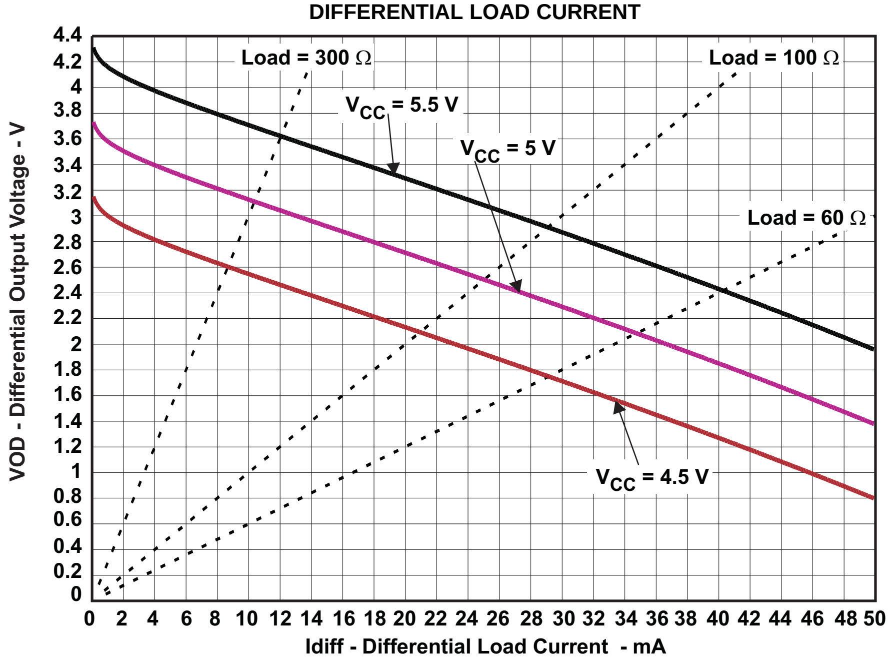
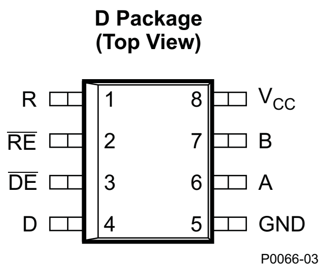


Figure 11.

ADDITIONAL OPTIONS

The SN65HVD17xx family also has options for J1708 applications, for always-enabled full-duplex versions (industry-standard SN65LBC179 footprint) and for inverting-polarity versions, which allow users to correct a reversal of the bus wires without re-wiring. Contact your local Texas Instruments representative for information on these options.

PART NUMBER	SN65HVD17xx		
FOOTPRINT/FUNCTION	**SLOW**	**MEDIUM**	**FAST**
Half-duplex (176 pinout)	85	86	87
Full-duplex no enables (179 pinout)	88	89	90
Full-duplex with enables (180 pinout)	91	92	93
Half-duplex with cable invert	94	95	96
Full-duplex with cable invert and enables	97	98	99
J1708	08	09	10



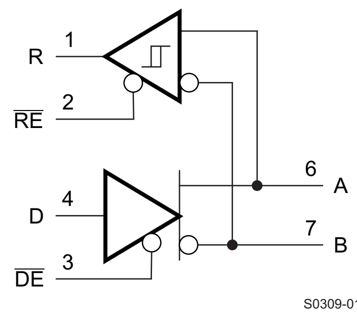
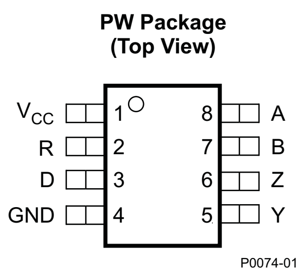


Figure 12. SN65HVD1708E Transceiver for J1708 Applications



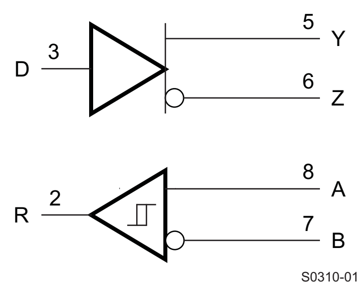


Figure 13. SN65HVD17xx Always-Enabled Driver Receiver

APPLICATION INFORMATION

Hot-Plugging

These devices are designed to operate in "hot swap" or "hot pluggable" applications. Key features for hot-pluggable applications are power-up, power-down glitch free operation, default disabled input/output pins, and receiver failsafe. As shown in Figure 8, an internal Power-On Reset circuit keeps the driver outputs in a high-impedance state until the supply voltage has reached a level at which the device will reliably operate. This ensures that no spurious transitions (glitches) will occur on the bus pin outputs as the power supply turns on or turns off.

As shown in the device **FUNCTION TABLE**, the *ENABLE* inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device will neither drive the bus nor report data on the R pin until the associated controller actively drives the enable pins.

Likewise, the receiver output is "failsafe" to open-circuit, short-circuit, or idle (terminated only) bus conditions. This eliminates false transitions on the receiver output until a valid RS-485 signal is applied to the receiver input pins.

Cable Invert

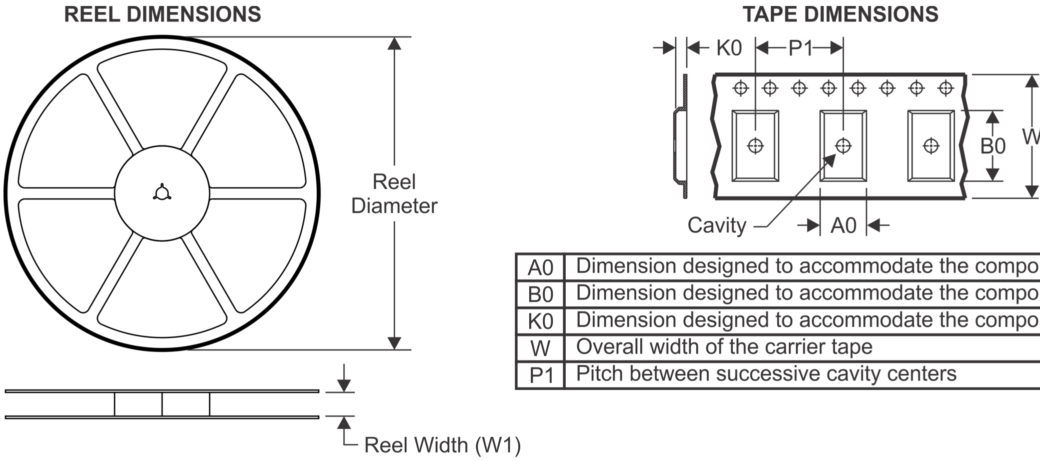
For many RS-485 applications, wiring of data cables takes place during equipment installation, and the possibility of miss-wiring is a significant issue. When the twisted-pair wires are reversed due to installation mistakes, normal RS-485 communication is not possible. The Cable Invert (INV) pin allows designers to compensate for this installation mistake. Under normal circumstances, the INV pin can be set to logic LOW, and the transceiver operates with normal polarity. If, after initial network start-up, a node cannot communicate properly, the local controller can set the INV pin high, which will invert the polarity of the A and B differential bus pins. This will compensate for a reversal of the bus wires, allowing proper communication.

Receiver Failsafe

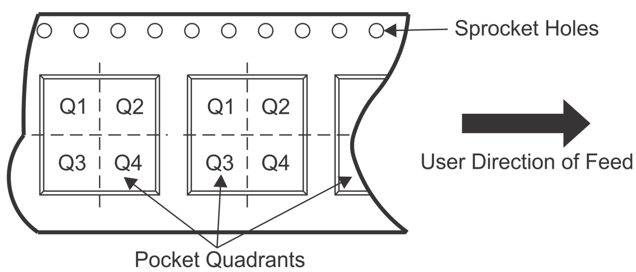
The differential receiver is “failsafe” to invalid bus states caused by open bus conditions such as a disconnected connector, shorted bus conditions such as cable damage shorting the twisted-pair together or idle bus conditions that occur when no driver is actively driving a valid RS-485 bus state on the network. In any of these cases, the differential receiver outputs a failsafe state, so that small noise signals do not cause spurious transitions at the receiver output. When INV is logic Low or Open (normal operation), the receiver output will be failsafe High. When INV is logic High to correct for a twisted-pair reversal, the receiver output will be failsafe Low under those fault conditions.

Changes from Original (August 2008) to Revision A **Page**

TAPE AND REEL INFORMATION

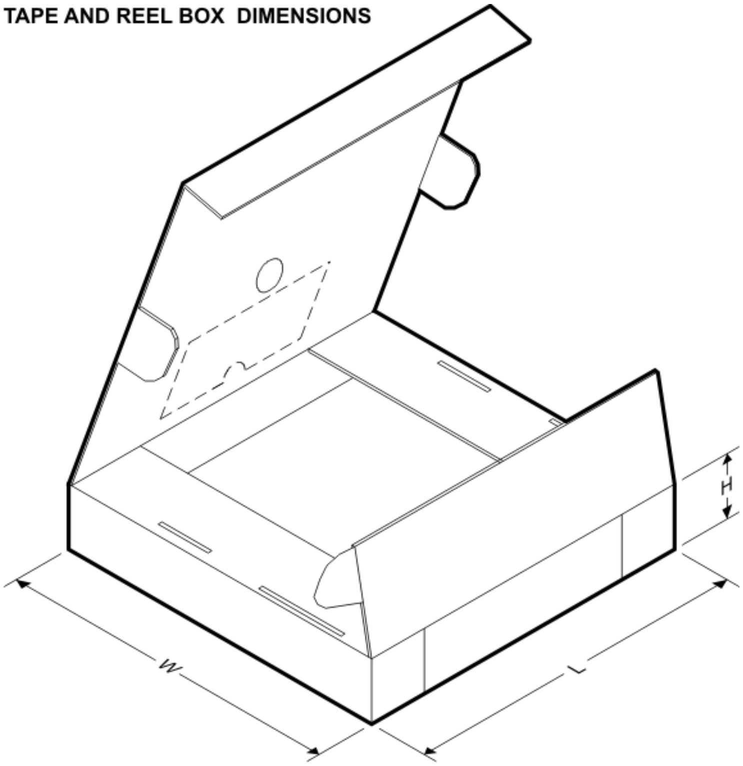


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



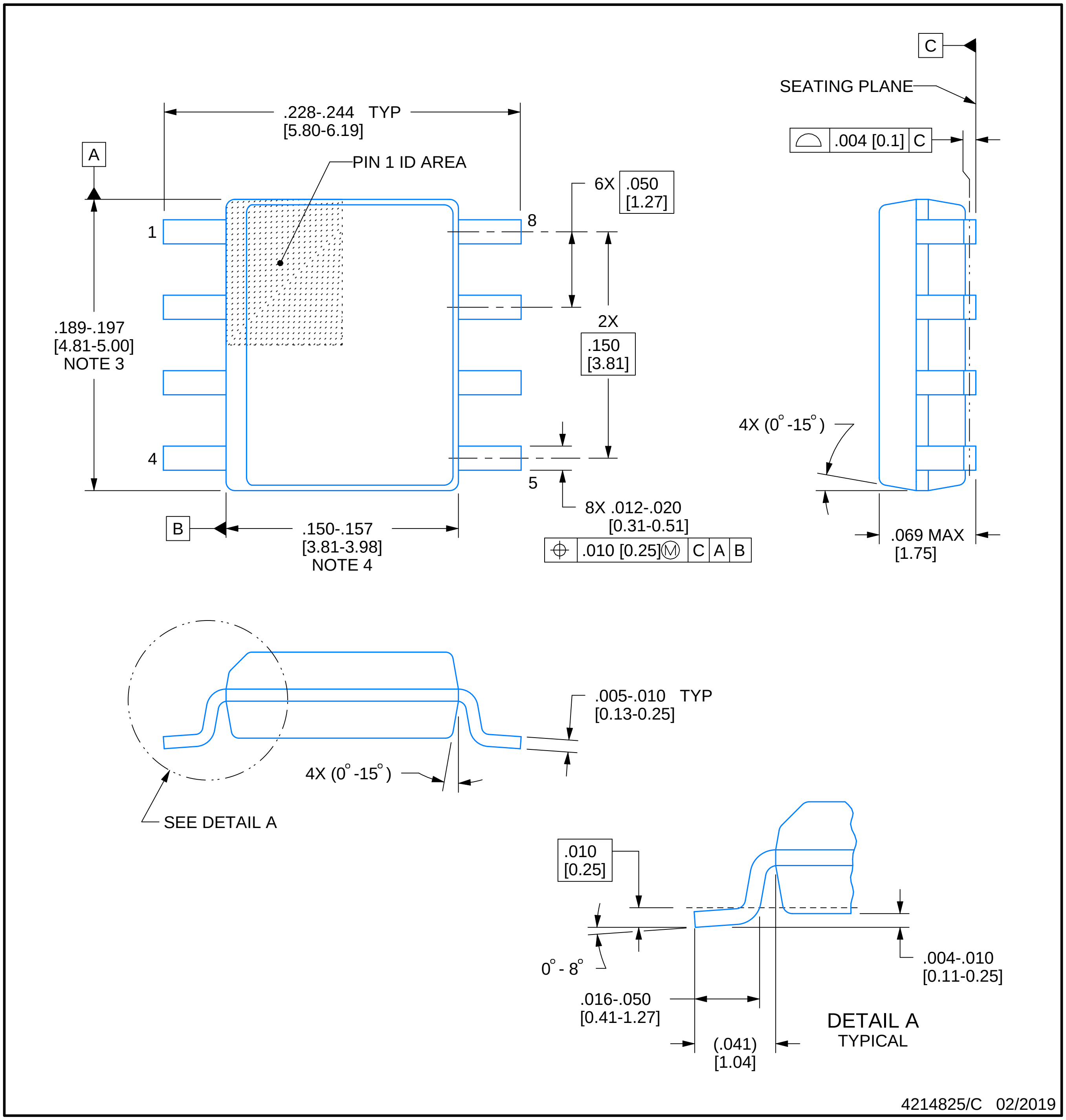
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1794DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



*All dimensions are nominal

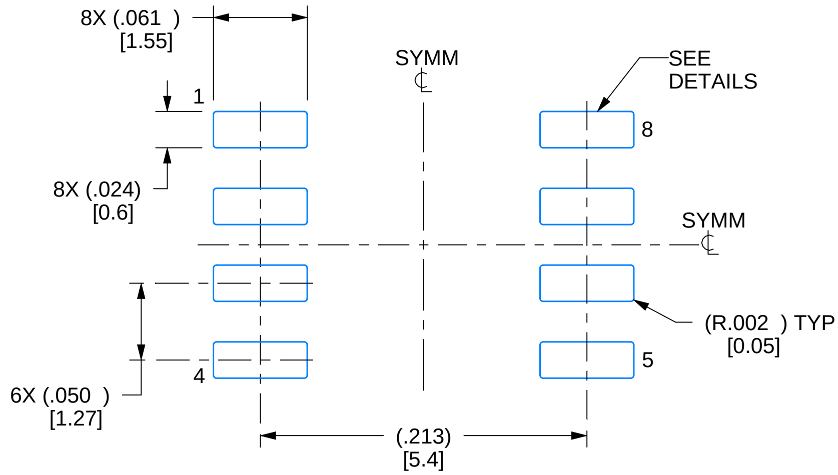
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1794DR	SOIC	D	8	2500	367.0	367.0	35.0



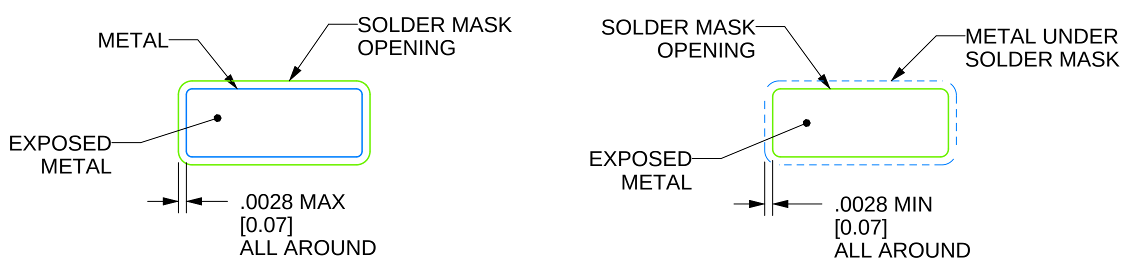
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

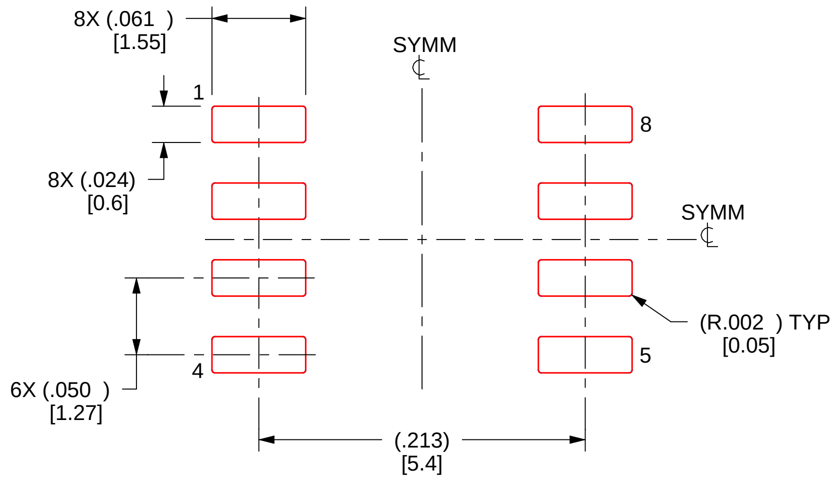
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



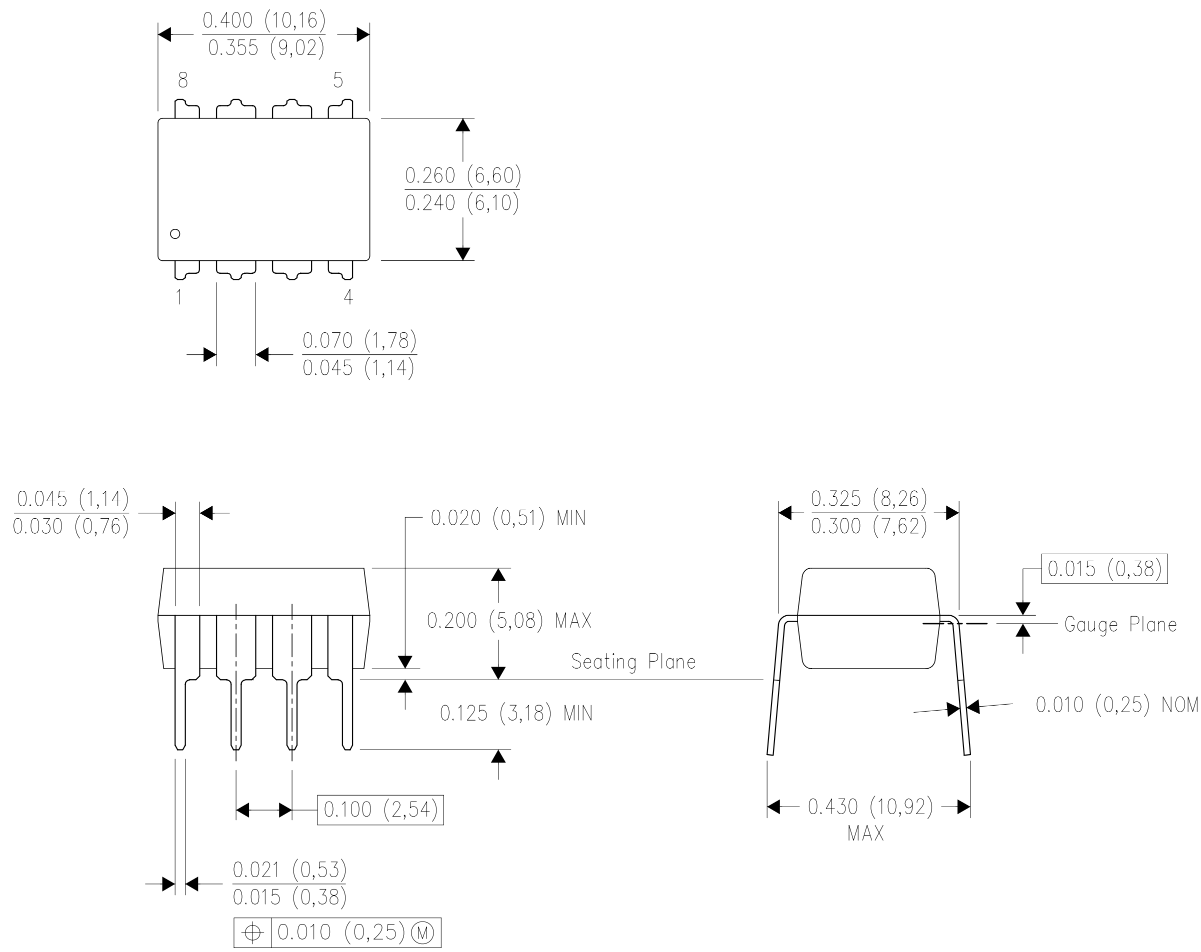
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.