TPS54362-Q1 3-A, 60-V Step-Down DC-DC Converter With Low $I_{(q)}$

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C5
- Withstands Transients up to 60 V With an Operating Range of 3.6 V to 48 V
- Asynchronous Switch-Mode Regulator With External Components (L and C), Load Current up to 3 A (max.)
- 0.8 V ± 1.5% Voltage Reference
- 200-kHz to 2.2-MHz Switching Frequency
- High-Voltage-Tolerant Enable Input for ON/OFF State
- Soft Start on Enable Cycle
- Slew-Rate Control on Internal Power Switch
- External Clock Input for Synchronization
- Pulse-Skip Mode (PFM) During Light Output Loads With Quiescent Current = 65 µA Typical (LPM Operation)
- External Compensation for Wide-Bandwidth Error Amplifier
- Internal Undervoltage Lockout, UVLO
- Programmable Reset Power-On Delay
- Reset-Function Filter Time for Fast Negative Transients
- Programmable Overvoltage Output Monitoring
- Programmable Undervoltage Output Monitoring, Issuance of Reset if Output Falls Below Threshold
- Thermal Shutdown During Excessive Power Dissipation
- Switch Current-Limit Protection
- Short-Circuit and Overcurrent Protection of FET
- Junction Temperature Range: –40°C to 150°C
- 20-Pin HTSSOP PowerPAD™ Package
- Qualified for Automotive Applications

2 Applications

- Automotive Telematics
- Navigation Systems
- In-Dash Instrumentation
- Battery-Powered Applications

3 Description

The TPS54362-Q1 device is a step-down switch-mode power supply with a low-power mode and a programmable voltage supervisor. Integrated input voltage-line feed-forward topology improves line transient regulation of the voltage-mode buck regulator. The regulator has a cycle-by-cycle current limit. Pulse-skip mode operation under no load reduces the supply current to 65 µA. Using the enable pin reduces the supply shutdown current to 1 µA.

An open-drain reset signal indicates when the nominal output drops below the threshold set by an external resistor-divider network. A soft-start capacitor controls the output voltage start-up ramp. The device activates an internal undervoltage shutdown when the input supply ramps down to 2.6 V.

Frequency foldback operation protects the device during an overload conditions on the output. The device also has thermal shutdown protection due to excessive power dissipation.

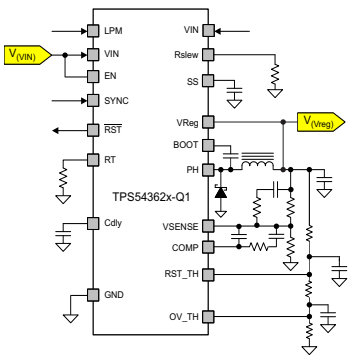
The B-revision has an improved leakage current parameter, and improved discharged function while in disable mode.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54362-Q1	HTSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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4 Revision History

Changes from Revision F (May 2014) to Revision G **Page**

- Added AEC-Q100 qualification features to the *Features* section ... 1
- Added product improvements for B-revision silicon under the Product Description section ... 1
- Increased the max output voltage value for the SS pin in the *Absolute Maximum Ratings* table ... 5
- Changed column in Thermal Table from TPS54362A, to TPS54362x ... 6
- Changed the II_{KG} row in Elec Chara Table from TPS54362A-Q1 to A-revision and TPS54362B-Q1 to B-revision ... 7
- Increased the maximum I_{lkg} value for both B-revision test conditions in the *Electrical Characteristics* table ... 7
- Changed in CAUTION: TPS54362A-Q1 to TPS54362Ax-Q1 and deleted TPS54362B-Q1 ... 16
- Changed in Soft-Start Capacitor paragraph TPS54362A-Q1 to TPS54362Ax-Q1 and deleted TPS54362B-Q1 ... 26
- Changed Power Supply Recommendations section: TPS54362A-Q1 to TPS54362Ax-Q1 and deleted TPS54362B-Q1 .. 30

Changes from Revision E (May 2013) to Revision F **Page**

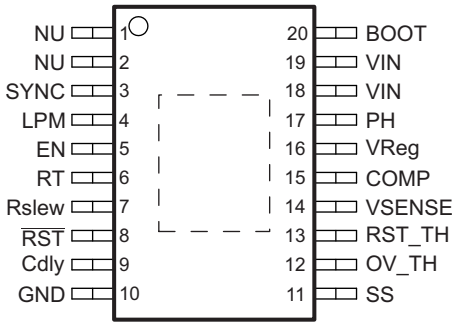
- Changed all text, tables and graphics to the new data sheet template. ... 1
- Changed pinout drawing ... 4
- Changed parameter symbols for JEDEC compliance throughout the data sheet ... 4
- Added a row for the Rslew pin to the *Absolute Maximum Ratings* table ... 5
- Changed symbol for thermal resistance from θ to R_θ in the *Thermal Information* table ... 6
- Added I_{lkg} parameters for EN pin on TPS54362B-Q1 device ... 7
- Revised Figure 22 ... 22
- Changed value of R4 in *Output Voltage and Feedback Resistor Selection* section ... 25
- Changed several values in the *Overvoltage Resistor Selection* section ... 25
- Changed several values in the *Reset-Threshold Resistor Selection* section ... 25
- Changed the voltage value in the *Undervoltage Threshold for Low-Power Mode and Load-Transient Operation* section . 26
- Added the TPS54362B-Q1 part number to the text of the *Soft-Start Capacitor* section ... 26
- Changed calculated values for loop compensation components ... 27

Changes from Revision D (October 2011) to Revision E **Page**

- Removed TPS54362-Q1 and TPS54362 from data sheet; added -Q1 to TPS54362A part numbers. 1
- Removed Ordering Information table; see Package Option Addendum for ordering information. 1
- Removed items 3 and 4 from the *Soft Start (SS)* section, also removed the sentence: Item 3 and item 4 are not applicable for TPS54362A-Q1. 15
- Removed the following sentence from the *Soft-Start Capacitor* section: Equation 4 has to be satisfied in addition to the other conditions stated in the soft start section of this document (not applicable for TPS54362A-Q1). 26

5 Pin Configuration and Functions

PWP 20-Pin Package
20-Pin HTSSOP With Thermal Pad
Top View



NU – Make no external connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	20	O	External bootstrap capacitor to PH to drive the gate of the internal switching FET
Cdly	9	I/O	External capacitor to ground to program power-on-reset delay.
COMP	15	I/O	Error-amplifier output to connect external compensation components
EN	5	I	Enable pin, internally pulled up. This pin requires an external pullup or pulldown to enable or disable the device.
GND	10	O	Ground pin
LPM	4	I	Low-power mode control using digital input signal. An internal pulldown resistor of 62 kΩ (typical) connects to ground.
NU	1	—	Connect to ground
	2		
OV_TH	12	I	Sense input for overvoltage detection on regulated output. This pin monitors the $V_{(Vreg)}$ output voltage as divided by the external resistor network connecting between the VReg pin and ground. The resistor network programs the threshold voltage.
PH	17	O	Source of the internal switching FET
Rslew	7	O	External resistor to ground to control the slew rate of the internal switching FET
$\overline{RST}$	8	O	Active-low, open-drain reset output connected to external bias voltage through a resistor, asserted high after the device starts regulating
RST_TH	13	I	Sense input for undervoltage and reset voltage detection on regulated output to initiate a reset-output signal. This pin monitors the $V_{(Vreg)}$ output voltage as divided by the external resistor network connecting between the VReg pin and ground. The resistor network programs the threshold voltage.
RT	6	O	External resistor to ground to program the internal oscillator frequency
SS	11	I/O	External capacitor to ground to program soft-start time
SYNC	3	I	External synchronization clock input to override the internal oscillator clock. An internal pulldown resistor of 62 kΩ (typical) connects to ground.
VIN	18	I	Unregulated input voltage. Connect pin 18 and pin 19 together externally.
	19		
VReg	16	I	Internal low-side FET to load output during start-up or limit overshoot
VSENSE	14	I	Inverting node of error amplifier for voltage-mode control
Thermal pad		—	The thermal pad connects electrically to exposed ground pad on PCB for proper thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

			MIN	MAX	UNIT
Input voltage	EN		–0.3	60	V
	VIN		–0.3	60	
	VReg		–0.3	20	
	LPM		–0.3	5.5	
	OV_TH		–0.3	5.5	
	RST_TH		–0.3	5.5	
	SYNC		–0.3	5.5	
	VSENSE		–0.3	5.5	
Output voltage	BOOT		–0.3	65	V
	PH		–0.3	60	
		30 ns	–2	60	
		200 ns	–1	60	
		T_J = –40	–0.85	60	
		T_J = 125	–0.5	60	
	RT		–0.3	5.5	V
	$\overline{RST}$		–0.3	5.5	
	Rslew		–0.3	5.5	
	Cdly		–0.3	8	
	SS		–0.3	8	
	COMP		–0.3	7	
T_J	Operating virtual junction temperature range		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	165	°C
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	–2	2	kV
		Charged-device model (CDM), per AEC Q100-011	–750	750	V

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
V_I	Unregulated buck supply input voltage (VIN, EN)	3.6	48	V
$V_{(VReg)}$	Regulator voltage range	0.9	18	V
	Power up in low-power mode (LPM) or discontinuous mode (DCM)	0.9	5.5	
	Logic level inputs ($\overline{RST}$, VSENSE, OV_TH, RST_TH, SYNC, RT)	0	5.25	V
	Logic level inputs (SS, Cdly, COMP)	0	6.5	V
T_J	Operating junction temperature range(1)	–40	150	°C

(1) This assumes $T_A = T_J$ – Power dissipation × $R_{\theta JA}$ (junction-to-ambient).

6.4 Thermal Information

THERMAL METRIC(1)		TPS54362-Q1 PWP 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	18.5	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	18.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.2	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

$V_{(VIN)}$ = 7 V to 48 V, $V_{(EN)}$ = $V_{(VIN)}$, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST(1)
INPUT POWER SUPPLY								
$V_{(VIN)}$	Supply voltage on VIN pin	Normal mode–buck mode after initial start-up		3.6		48	V	Info
		Low-power mode	Falling threshold (LPM disabled)		8		V	
			Rising threshold (LPM activated)		8.5			
			High-voltage threshold (LPM disabled)	25	27	30		
$I_{(q\text{-}Normal)}$	Quiescent current, normal mode	Open-loop test – maximum duty cycle $V_{(VIN)}$ = 7 V to 48 V			5	10	mA	PT
$I_{(q\text{-}LPM)}$	Quiescent current; low-power mode	$I_{(VReg)}$ < 1 mA, $V_{(VIN)}$ = 12 V, T_A = 25°C			65	75	µA	PT
		$I_{(VReg)}$ < 1 mA, $V_{(VIN)}$ = 12 V, –40 < T_J < 150°C				75		
		$I_{(VReg)}$ < 1 mA, $V_{(VIN)}$ = 24 V, T_A = 25°C				85		
		$I_{(VReg)}$ < 1 mA, $V_{(VIN)}$ = 24 V, –40 < T_J < 150°C				85		
$I_{(SD)}$	Shutdown	$V_{(EN)}$ = 0 V, device is OFF, T_A = –40°C to 125°C, $V_{(VIN)}$ = 24 V				10	µA	PT
		$V_{(EN)}$ = 0 V, device is OFF, T_A = 25°C, $V_{(VIN)}$ = 12 V			1	4		
TRANSITION TIMES (LOW-POWER AND NORMAL MODES)								
$t_{d(1)}$	Transition delay from normal mode to low-power mode	$V_{(VIN)}$ = 12 V, $V_{(VReg)}$ = 5 V, $I_{(VReg)}$ = 1 A to 1 mA			100		µs	CT
$t_{d(2)}$	Transition delay from low-power mode to normal mode	$V_{(VIN)}$ = 12 V, $V_{(VReg)}$ = 5 V, $I_{(VReg)}$ = 1 mA to 1 A			5		µs	CT
SWITCH-MODE SUPPLY (VReg)								
$V_{(VReg)}$	Regulator output	$V_{(VSENSE)}$ = 0.8-V reference		0.9		18	V	Info
$V_{(VSENSE)}$	Feedback voltage	$V_{(VReg)}$ = 0.9 V to 18 V, $V_{(VIN)}$ = 7 V to 48 V		0.788	0.8	0.812	V	CT
$r_{DS(on)}$	Internal switch resistance	Measured across VIN and PH, $I_{(VReg)}$ = 500 mA				500	mΩ	PT
$I_{(CL)}$	Switch current limit, cycle-by-cycle	$V_{(VIN)}$ = 12 V		4	6	8	A	Info
$t_{(ON\text{-}Min)}$	Duty-cycle pulse duration (ON)			50	100	150	ns	Info
$t_{(OFF\text{-}Min)}$	Duty-cycle pulse duration (OFF)			100	200	250	ns	Info
$f_{(SW)}$	Switch-mode frequency	Set using external resistor on RT pin		0.2		2.2	MHz	PT
	Accuracy of $f_{(SW)}$			–10%		10%		PT
$I_{(Sink)}$	Sink current in start-up condition	$V_{(OV\_TH)}$ = 0 V, $V_{(VReg)}$ = 10 V				1	mA	Info
$I_{(Limit)}$	Sink-current limit	0 V < $V_{(OV\_TH)}$ < 0.8 V, $V_{(VReg)}$ = 10 V				80	mA	Info
ENABLE (EN)								
V_{IL}	Low input threshold					0.7	V	PT
V_{IH}	High input threshold			1.7			V	PT
I_{lkg}	Leakage into EN pin	A-revision, $V_{(EN)}$ = 60 V			100	135	µA	PT
		A-revision,, $V_{(EN)}$ = 12 V			8	15		
		B-revision, $V_{(EN)}$ = 60 V				10		
		B-revision, $V_{(EN)}$ = 12 V				2		
RESET DELAY (Cdly)								
I_O	External capacitor charge current	$V_{(EN)}$ = high		1.4	2	2.6	µA	PT
$V_{Threshold}$	Switching threshold	Output voltage in regulation			2		V	PT
LOW-POWER MODE (LPM)								
V_{IL}	Low input threshold	$V_{(VIN)}$ = 12 V				0.7	V	PT
V_{IH}	High input threshold	$V_{(VIN)}$ = 12 V		1.7			V	PT
I_{lkg}	Leakage into LPM pin	$V_{(LPM)}$ = 5 V			65	95	µA	PT
RESET OUTPUT ($\overline{RST}$)								
$V_{(RST\_TH)}$	Reset threshold for RST_TH pin			0.768		0.832	V	PT
SOFT START (SS)								
$I_{(SS)}$	Soft-start source current			40	50	60	µA	PT

(1) PT = Production tested; CT = Characterization tested only, not production tested; Info = User information only, not production tested

Electrical Characteristics (continued)

$V_{(VIN)}$ = 7 V to 48 V, $V_{(EN)}$ = $V_{(VIN)}$, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST(1)
SYNCHRONIZATION (SYNC)(2)							
$V_{IL(SYNC)}$	Low input threshold				0.7	V	PT
$V_{IH(SYNC)}$	High input threshold		1.7			V	PT
I_{lkg}	Leakage	SYNC = 5 V		65	95	µA	PT
$Duty_{(min)}$	Minimum duty cycle		30%				CT
$Duty_{(miax)}$	Maximum duty cycle				70%		CT
Rslew							
$I_{(Rslew)}$	Output current	Rslew = 50 kΩ		20		µA	CT
		Rslew = 10 kΩ		100			
OVERVOLTAGE SUPERVISORS (OV_TH)							
$V_{(OV\_TH)}$	Threshold for OV_TH pin during OV	Internal switch is OFF.	0.768		0.832	V	PT
	Internal pulldown current on OV_TH pin	OV_TH = 1 V, $V_{(VReg)}$ = 5 V		70		mA	
THERMAL SHUTDOWN							
$T_{(SD)}$	Thermal shutdown junction temperature			175		°C	CT
$T_{(HYS)}$	Temperature hysteresis			30		°C	CT

(2) The SYNC input clock can have a maximum frequency of 2× the programmed clock frequency up to a maximum value of 1.1 MHz.

6.6 Timing Requirements

$V_{(VIN)}$ = 7 V to 48 V, $V_{(EN)}$ = $V_{(VIN)}$, T_J = –40°C to 150°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT	TEST(1)
SYNCHRONIZATION (SYNC)(2)							
$t_{(trans-ItoE)}$	Internal clock to external clock	External clock = 1 MHz, $V_{(VIN)}$ = 12 V, $V_{(VReg)}$ = 5 V		2.5		µs	Info
$f_{(SYNC)}$	Input clock	$V_{(VIN)}$ = 12 V, $V_{(VReg)}$ = 5 V, $f_{(sw)} < f_{(ext)} < 2 \times f_{(sw)}$	180		2200	kHz	CT
RESET OUTPUT ($\overline{RST}$)							
$t_{d(POR)}$	POR delay timer	C2 = 4.7 nF	3.6		7	ms	PT
$t_{d(RSTdly)}$	Filter time		10	20	35	µs	PT

(1) PT = Production tested; CT = Characterization tested only, not production tested; Info = User information only, not production tested
(2) The SYNC input clock can have a maximum frequency of 2× the programmed clock frequency up to a maximum value of 1.1 MHz.

6.7 Switching Characteristics

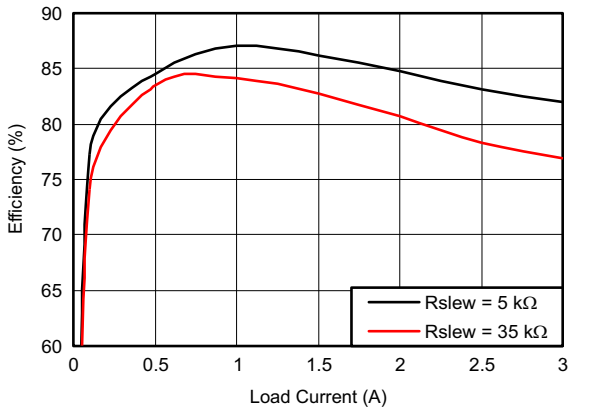
$V_{(VIN)}$ = 7 V to 48 V, $V_{(EN)}$ = $V_{(VIN)}$, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST(1)
SYNCHRONIZATION (SYNC)(2)							
$t_{(trans-EtoI)}$	External clock to internal clock	Remove external clock, $V_{(VIN)}$ = 12 V, $V_{(VReg)}$ = 5 V		32		µs	Info

(1) PT = Production tested; CT = Characterization tested only, not production tested; Info = User information only, not production tested
(2) The SYNC input clock can have a maximum frequency of 2× the programmed clock frequency up to a maximum value of 1.1 MHz.

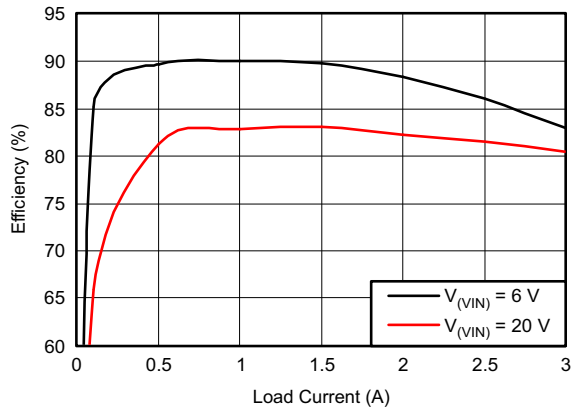
6.8 Typical Characteristics

6.8.1 Efficiency Data of Power Supply



$V_{(VIN)}$ = 12 V $V_{(VReg)}$ = 5 V $f_{(SW)}$ = 500 kHz
L = 22 µH C4 (output) = 100 µF T_A = 25ºC

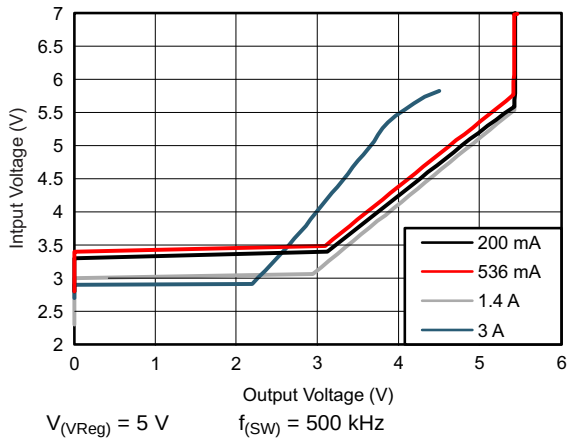
Figure 1. FET Switching (Slow Slew Rate)



$V_{(VReg)}$ = 5 V $f_{(SW)}$ = 500 kHz L = 22 µH
C4 (output) = 100 µF Rslew = 5 kΩ T_A = 25ºC

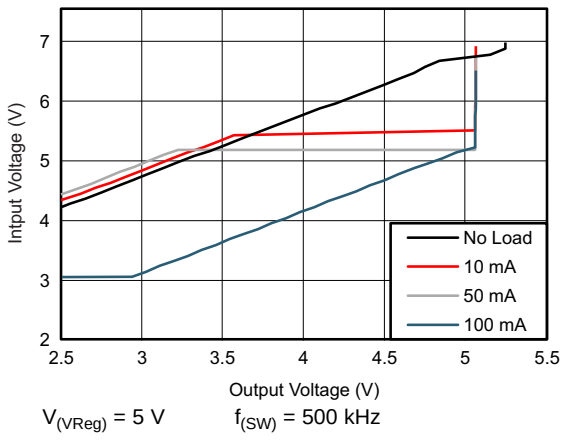
Figure 2. Fast Slew Rate on Switching FET

6.8.2 Output Voltage Dropout



$V_{(VReg)}$ = 5 V $f_{(SW)}$ = 500 kHz

Figure 3. Load Current > 100 mA



$V_{(VReg)}$ = 5 V $f_{(SW)}$ = 500 kHz

Figure 4. Load Current < 100 mA

Output Voltage Dropout (continued)

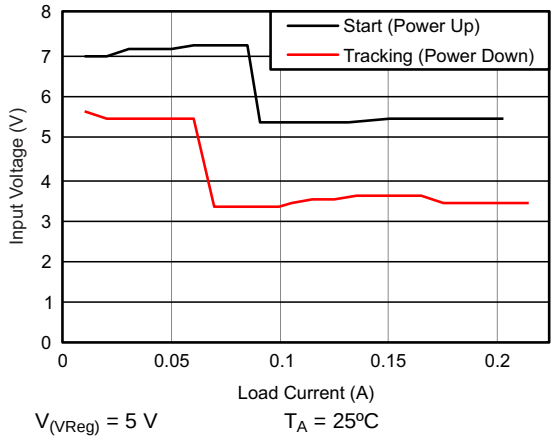


Figure 5. Output-Voltage Tracking

NOTE

Tracking: The input voltage at which the output voltage drops approximately –0.7 V of the regulated voltage or for low input voltages (tracking function) over the load range.

Start: The input voltage required to achieve 5-V regulation on power up with the stated load currents.

6.8.3 Quiescent and Standby Current

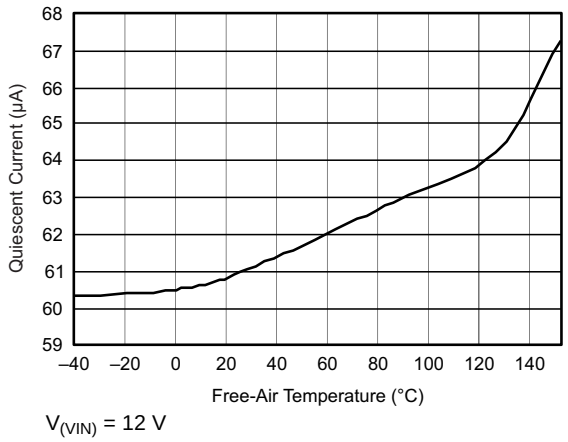


Figure 6. LPM, Quiescent Current Variation With Temperature

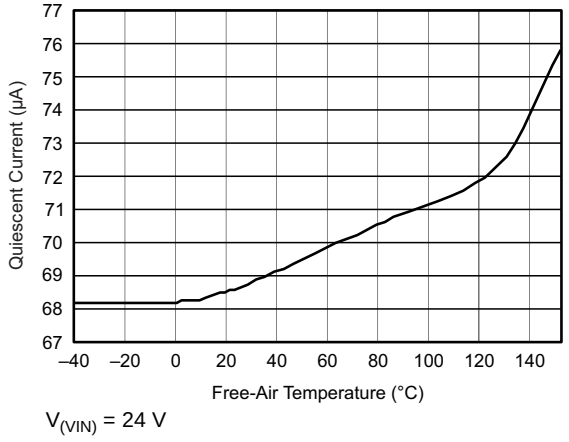
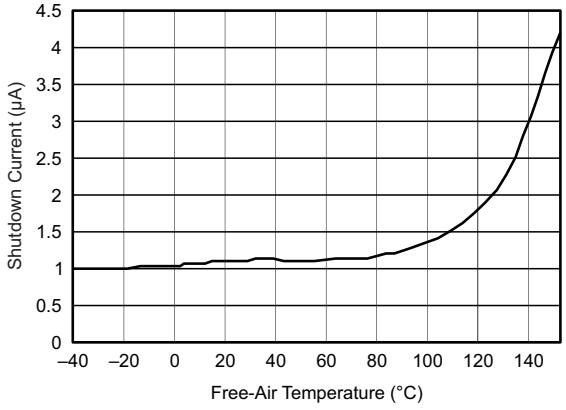


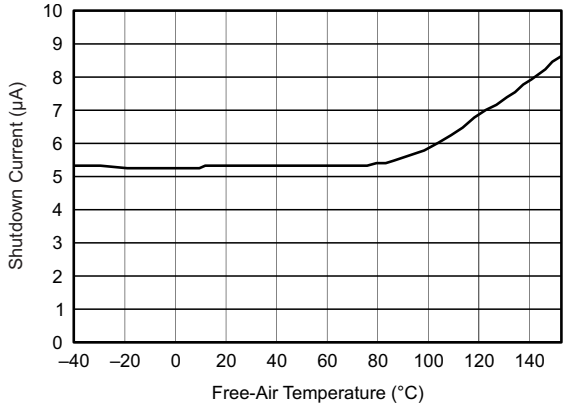
Figure 7. LPM, Quiescent Current Variation with Temperature

Quiescent and Standby Current (continued)



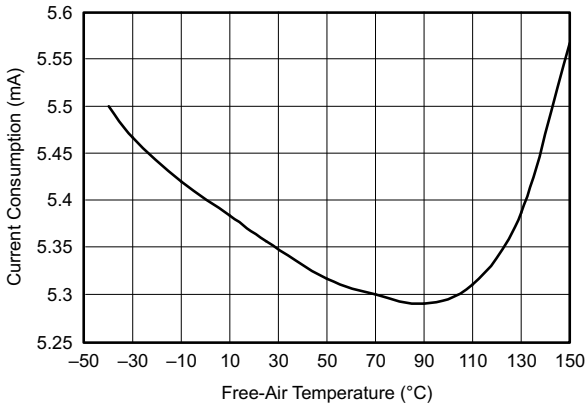
$V_{(VIN)}$ = 12 V

Figure 8. Shutdown Current



$V_{(VIN)}$ = 24 V

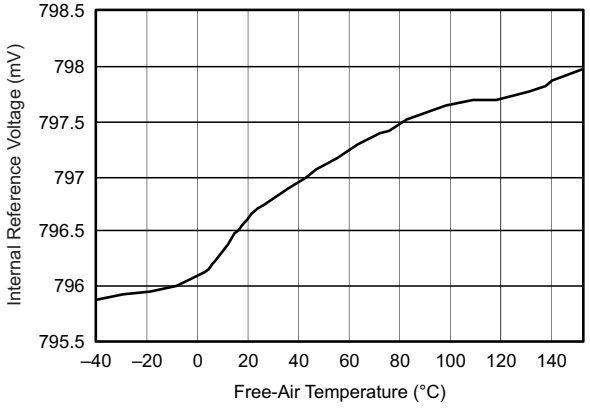
Figure 9. Shutdown Current



EN = High $V_{(VIN)}$ = 12 V

Figure 10. Current Consumption vs Temperature

6.8.4 Reference Voltages



$V_{(VIN)}$ = 12 V

Figure 11. Internal Reference Voltage

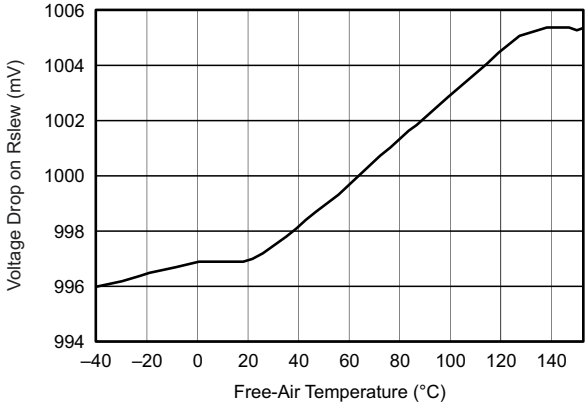


Figure 12. Voltage Drop on Rslew for Current Reference

7 Detailed Description

7.1 Overview

The TPS54362-Q1 device is a 60-V, 3-A DC-DC step-down (buck) converter using a voltage-control-mode scheme. The device features a supervisory function for power-on-reset during system power on. When the output voltage has exceeded the threshold set by the resistor network connected to the RST_TH pin, a delay of 1 ms per nF (based on the capacitor value on the RSTDLY pin) occurs before the release to high of the $\overline{\text{RST}}$ pin. Conversely on power down, once the output voltage falls below the same set threshold, the device pulls $\overline{\text{RST}}$ low only after a de-glitch filter of approximately 20 µs (typical) expires. The implementation of this function prevents the triggering of $\overline{\text{RST}}$ due to fast transient line noise on the output supply.

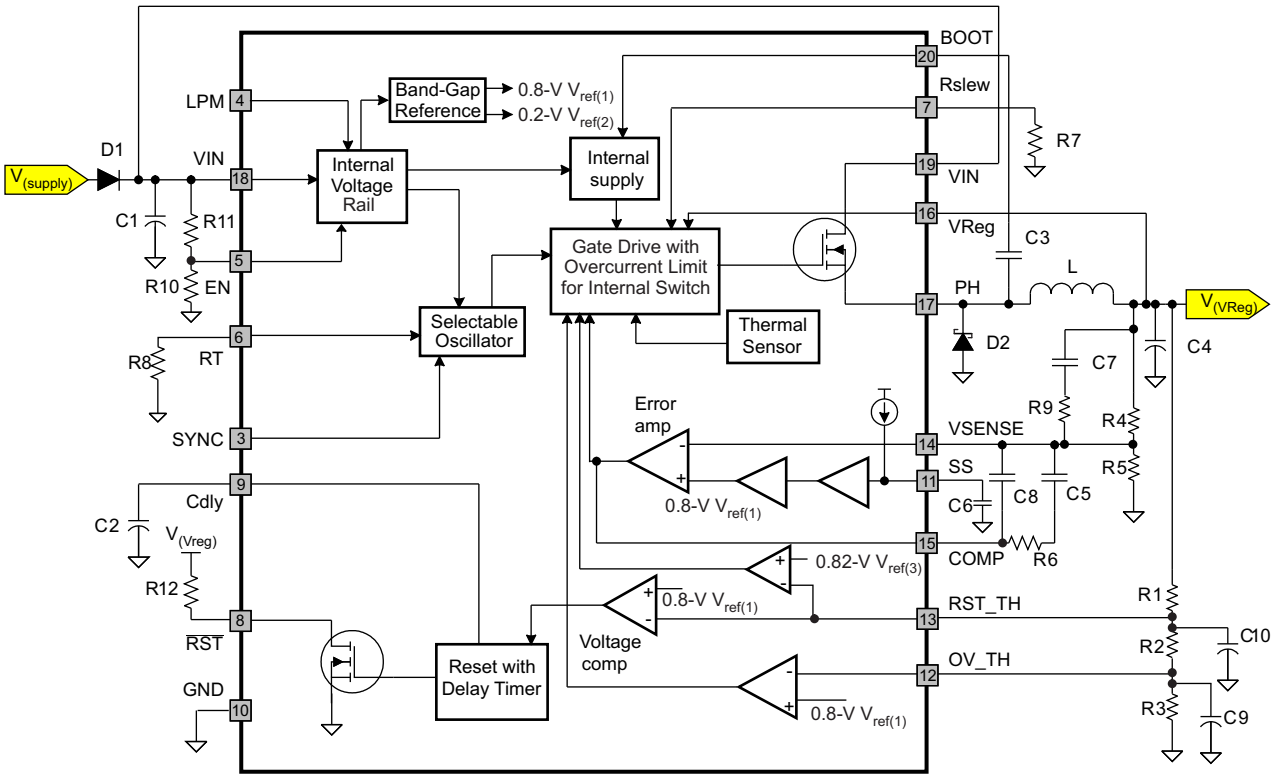
An overvoltage monitor function limits output voltage to the threshold set by OV_TH. The external resistor network sets both the RST_TH and OV_TH monitoring voltages to be a pre-scale of the output voltage, and the internal bias voltages of the voltage comparators (0.8 V typical) are the basis of the thresholds.

The RST_TH setting is the basis for detection of undervoltage on the output, which invokes low assertion of the $\overline{\text{RST}}$ pin. The OV_TH setting is the basis for detection of overvoltage on the output, which does not invoke low assertion of the $\overline{\text{RST}}$ pin. However, the device commands the internal switch to turn OFF.

In systems where power consumption is critical, implementation of low-power mode reduces the non-switching quiescent current during light load conditions. The system entering discontinuous current mode (DCM) for at least 100 µs determines PFM operation. When the device enters discontinuous mode depends on the selection of external components.

If excessive power dissipation causes invocation of thermal shutdown, the device disables the internal switch, and the regulated output voltage starts to decrease. Depending on the load line, the regulated voltage could decay and the RST_TH threshold may assert the $\overline{\text{RST}}$ output low.

7.2 Functional Block Diagram



7.3 Feature Description

The TPS54362-Q1 device is a DC-DC converter using a voltage-control-mode scheme with an input voltage feed-forward technique. The device is programmable for a range of output voltages with a wide input-voltage range. The following are details with regard to the pin functionality.

7.3.1 Input Voltage

The VIN pin is the input power source for the TPS54362-Q1 device. This pin requires external protection against voltage levels greater than 60 V and reverse battery. In buck mode, the device draws pulsed input current from this pin, with fast rise and fall times. Therefore, this input line requires a filter capacitor to minimize noise. Additionally, for EMI considerations, the line may also require an input-filter inductor.

7.3.2 Function Mode

FUNCTION	OPERATING VOLTAGE RANGE	OUTPUT CURRENT CAPABILITY	COMMENTS
Buck	3.6 V to 48 V	$V_{(VReg)}$ = 0.9 V to 18 V and $I_{(VReg)}$ up to 3 A; however, at higher output power the device requires derating for maximum temperature rating.	Optimum performance: always set $V_{(VIN)}$-to-$V_{(VReg)}$ ratios such that the minimum required duty cycle pulse ($t_{(ON-Min)}$) > 150 ns. The minimum off-time is 250 ns for all conditions.

7.3.3 Output Voltage $V_{(VReg)}$

The converter supplied from battery voltage $V_{(VIN)}$ and the external components (L, C) generate the output voltage, $V_{(VReg)}$. The VSENSE pin senses the output through an external resistor divider and compares it with an internal reference voltage.

Selecting the external resistors according to the relationship in Equation 1 selects the value of the adjustable output voltage between 0.9 V and 18 V in buck mode. Reference designators for the resistors in the following equations refer to the *Functional Block Diagram*.

$$V_{(VReg)} = V_{ref} \ (1 + R4 / R5) \quad (1)$$

where

- R5 and R4 are feedback resistors
- V_{ref} = 0.8 V (typical)

The internal reference voltage has a ±1.5% tolerance. The overall output voltage tolerance depends on the external feedback resistors. To determine the overall output voltage tolerance, use the following relationship:

$$V_{(VReg\text{-}tol)} = V_{(VRef\text{-}tol)} + (R4 / (R4 + R5)) \times (R4\text{-}tol + R5\text{-}tol) \quad (2)$$

where

- R4 and R5 are feedback resistors
- V_{ref} = 0.8 V (typical)

The VReg pin also connects internally to a load of 100 Ω, which turns ON in the following conditions:

- During startup conditions, when the device is powered up with no load, or whenever EN is toggled, the internal load connected to the VReg pin turns ON for about 100 µs to charge the bootstrap capacitor to provide gate drive voltage to the switching transistor.
- During normal operating conditions, when the regulated output voltage exceeds the overvoltage threshold (preset by external resisitors R1, R2, and R3), the internal load turns ON, pulling this pin down to bring the regulated output voltage down.

Typically, the output uses a capacitor within the range of 10 µF to 400 µF. This pin must have a filter capacitor with low ESR characteristics in order to minimize output ripple voltage.

7.3.4 Oscillator Frequency (RT)

Oscillator frequency is selectable by means of a resistor placed at the RT pin. The switching frequency ($f_{(SW)}$) can be set in the range of 200 kHz–2200 kHz. In addition, a clock signal ($f_{(ext)}$) at the SYNC pin with $f_{(SW)} < f_{(ext)} < 2 \times f_{(SW)}$ can externally impose the switching frequency. In this case, the external clock overrides the switching frequency determined by the RT pin, and the external synchronization signal clocks the internal oscillator.

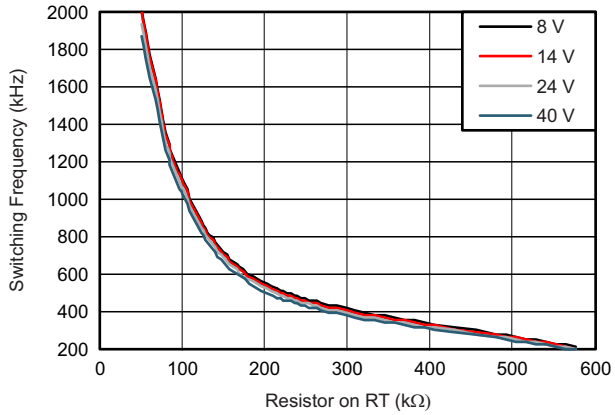


Figure 13. Switching Frequency vs Resistor Value

7.3.5 Synchronization (SYNC)

The SYNC pin is an external input signal to synchronize the switching frequency using an external clock signal. The synchronization input overrides the internally fixed oscillator signal. The synchronization signal must be valid for approximately 2 clock cycles (pulses) before the transition is made for synchronization with the external frequency input. If the external clock input does NOT transition low or high for 32 µS (typical), the system defaults to the internal clock set by the RT pin. The SYNC input clock can have a maximum frequency of 2× the programmed clock frequency up to a maximum value of 2.2 MHz.

7.3.6 Enable or Shutdown (EN)

The enable pin provides electrical on-off control of the regulator. Once the enable pin voltage exceeds the threshold voltage, the regulator starts operation, and the internal soft start begins to ramp. Pulling the enable pin voltage below the threshold voltage stops the regulator from switching, and the internal soft start resets. Connecting the pin to ground or to any voltage less than 0.7 V disables the regulator and activates the shutdown mode. This pin must have an external pullup or pulldown to change the state of the device.

7.3.7 Reset Delay (Cdly)

The reset-delay pin sets the desired delay time to assert the RESET pin high after the supply has exceeded the programmed VReg_RST voltage. One can program the delay in the range of 2.2 ms to 200 ms using capacitors in the range of 2.2 nF to 200 nF. Use Equation 3 to calculate the delay time.

$$t_{d(POR)} = 1 \text{ ms / nF} \times C \quad (3)$$

where

- C = capacitance on the Cdly pin

7.3.8 Reset Pin ($\overline{\text{RST}}$)

The $\overline{\text{RST}}$ pin is an open-drain output. The device asserts the power-on-reset output low until the output voltage exceeds the programmed VReg_RST voltage threshold and the reset delay timer has expired. Additionally, whenever the EN pin is low or open, the device immediately asserts $\overline{\text{RST}}$ low regardless of the output voltage. A reset filter timer prevents reset being invoked because of short negative transients on the output line. If a thermal shutdown occurs due to excessive thermal conditions, the device asserts this pin low when the switching FET is OFF and output falls below the reset threshold.

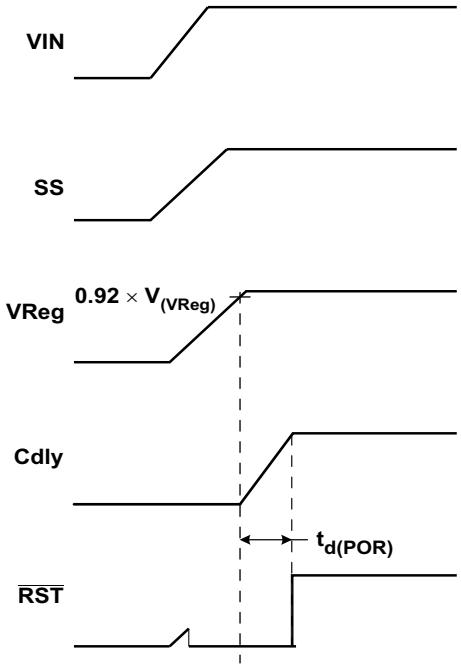


Figure 14. Power-On Condition, Reset Line

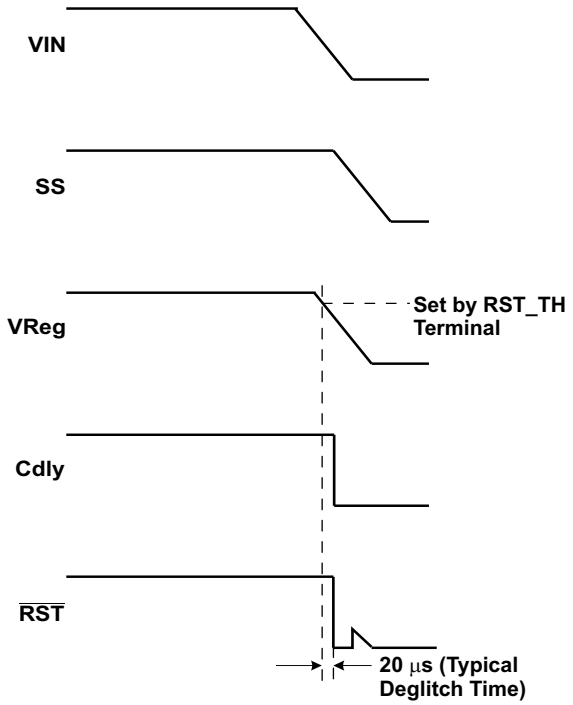


Figure 15. Power-Down Condition, Reset Line

7.3.9 Boost Capacitor (BOOT)

This capacitor provides the gate-drive voltage for the internal MOSFET switch. TI recommends X7R or X5R grade dielectrics because of the stable values over temperature of these dielectrics. Decreasing the value of the boost capacitor for low-Vreg applications, high-frequency applications, or combination applications may be necessary. Increasing the value of the boost capacitor for high-Vreg applications, low-frequency applications, or combination applications may be necessary (for example, 100 nF for 500 kHz at 5 V or 220 nF for 500 kHz at 8 V).

7.3.10 Soft Start (SS)

On power up or after a short-circuit event , TI recommends the following conditions:

- $V_{(VIN)} – V_{(VReg)} > 2.5$ V
- Load current < 1 A, until $\overline{RST}$ goes high

$C_{(SS)}$ is 1 nF to 220 nF. If the buck converter starts up with output shorted to ground, the value of $C_{(SS)}$ must be a minimum of 150 nF.

7.3.11 Short-Circuit Protection

The TPS54362-Q1 device features output short-circuit protection. Detection of short-circuit conditions is by monitoring RST_TH, and when the voltage on this node drops below 0.2 V, the switching frequency decreases and the current limit folds back to protect the device. The switching frequency folds back to approximately 25 kHz and the current limit reduces to 30% of the current-limit typical value.

7.3.12 Overcurrent Protection

Implementation of overcurrent protection is by sensing the current through the NMOS switch FET and a comparison of the sensed current to a current reference level representing the overcurrent threshold limit. Sensed current exceeding the overcurrent threshold limit sets the overcurrent indicator to true. The system ignores the overcurrent indicator for the leading edge blanking time at the beginning of each cycle to avoid any turnon-noise glitches.

Setting the overcurrent indicator to true triggers overcurrent protection. The MOSFET turns off for the rest of the cycle after a propagation delay. The name of the overcurrent protection scheme is cycle-by-cycle current limiting. If the sensed current continues to increase during cycle-by-cycle current limiting, the temperature of the device starts rising. At the temperature limit, thermal shutdown (TSD) kicks in and shuts down switching until the device cools sufficiently.

CAUTION

In certain conditions, device damage may occur under a shorted load condition, depending on the supply voltage. The design of the TPS54362-Q1 devices is for protection from damage due to a shorted load condition using a cycle-by-cycle current limit, the short-circuit protection function, and/or the thermal shutdown function.

Short-circuit detection protects the device from damage when encountering a 0-Ω short-circuit condition. However, damage to a device may occur when the shorted load has some resistivity and the output level stays higher than the short-circuit detection level of 0.2 V. In this case, the inductor current increases until the junction temperature of the device hits the thermal shutdown threshold, but damage to the switching FET may occur before thermal shutdown.

This failure only occurs during an output short circuit with some resistivity when the supply voltage is above 18 V.

7.3.13 Slew Rate Control (Rslew)

The Rslew pin controls the switching slew rate of the internal power NMOS. An external resistor with a slew-rate range for rise and fall times as shown in Figure 16 and Figure 17 sets the slew rate. The range of rise time t_r = 15 ns to 35 ns, and fall time t_f = 15 ns to 200 ns, with Rslew range of 10 kΩ to 50 kΩ (see Figure 16 and Figure 17).

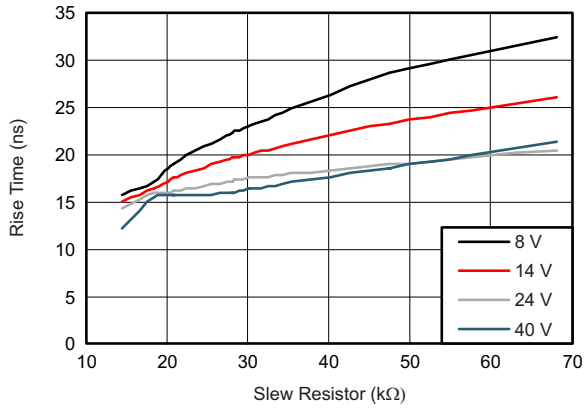


Figure 16. FET Rise Time

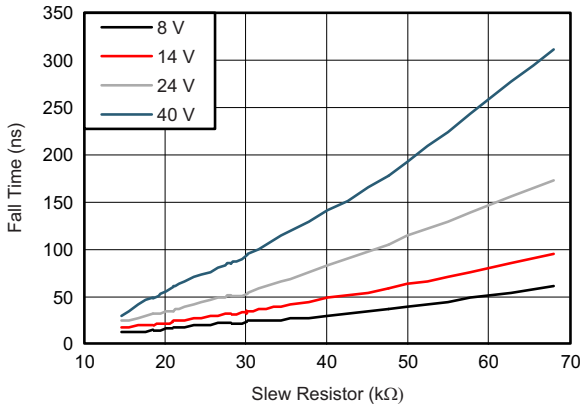


Figure 17. FET Fall Time

7.3.14 Thermal Shutdown

The TPS54362-Q1 device protects itself from overheating with an internal thermal-shutdown circuit. If the junction temperature exceeds the thermal-shutdown trip point, the MOSFET turns off. The device restarts automatically under control of the slow-start circuit when the junction temperature drops below the thermal-shutdown hysteretic trip point. Operating in low-power mode disables the thermal-shutdown sensing circuitry for low current consumption. Asserting $\overline{RST}$ or $V_{(VReg\_UV)}$ low activates thermal-shutdown monitoring.

7.3.15 Regulation Voltage (VSENSE)

Use of the VSENSE pin is for programming the regulated output voltage based on a resistor feedback network monitoring the $V_{(VReg)}$ output voltage. The selected ratio of R4 to R5 sets the VReg voltage.

7.3.16 RESET Threshold (RST_TH)

This pin is programmable for setting the undervoltage threshold level ($V_{(VReg\_UV)}$) for proper regulation in low-power mode and the reset threshold level ($V_{(VReg\_RST)}$) to initiate a reset-output signal. The resistor combination of R1 to R3 programs the threshold for detection of undervoltage. Voltage bias on R2 + R3 sets the reset threshold.

Undervoltage for transient and low-power-mode operation:

$$V_{(VReg\_UV)} = 0.82\ V \times (R1 + R2 + R3 / (R2 + R3) \quad (4)$$

$$\text{Reset threshold} = V_{(VReg\_RST)} = 0.8\ V \times (R1 + R2 + R3 / (R2 + R3) \quad (5)$$

Recommended range: 70% to 92% of the regulation voltage

7.3.17 Overvoltage Supervisor for $V_{(VReg)}$ (OV_TH)

This pin is programmable to set the overvoltage monitoring of the regulated output voltage. The resistor combination of R1 to R3 programs the threshold for detection of overvoltage. The bias voltage of R3 sets the OV threshold and the output voltage accuracy in hysteretic mode during transient events.

$$\text{Overvoltage reference} = V_{(VReg\_OV)} = 0.8\ V \times (R1 + R2 + R3) / (R3) \quad (6)$$

Recommended range: 106% to 110% of the regulation voltage

7.3.18 Noise Filter on RST_TH and OV_TH Pins

Some noise sensitivity exists on the RST_TH and OV_TH pins, and added capacitance filters this noise. The noise is more pronounced with fast falling edges on the PH pin. So a smaller Rslew resistor (minimum recommended value is 10 kΩ) may require more capacitance on RST_TH and OV_TH. Users should use the smallest capacitance necessary, because larger values increase the loop response time and degrade short-circuit protection and transient response. The 2-µs maximum time constant seen on OV_TH and RST_TH when $V_{(VReg)}$ = 0 V (that is, [R2 + R3] × [C9 + C10] < 2 µs) determines the upper limit. The noise in the RST_TH and OV_TH resistor chain may change with PCB layout or application setup, so there may not be a requirement for the RST_TH and/or OV_TH capacitor in all applications. Users can place the footprint and then populate it only if necessary.

Example:

R1 = 36 kΩ
R2 = 600 Ω
R3 = 6.6 kΩ

$$V_{(VReg\_RST)} = 0.8 \times (43.2\ k\Omega) / 7.2\ k\Omega = 4.8\ V \quad (7)$$

$$V_{(VReg\_OV)} = 0.8 \times (43.2\ k\Omega) / 6.6\ k\Omega) = 5.24\ V \quad (8)$$

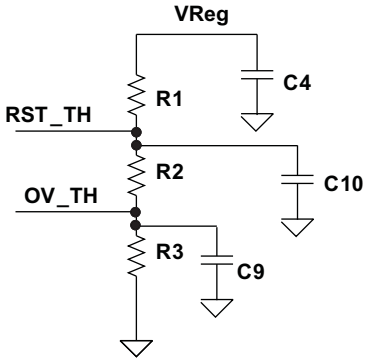


Figure 18. Resistor Network and Noise Filters

Typical values for the RST_TH and OV_TH capacitors are in the 10-pF to 100-pF range for total resistance on the RST_TH-OV_TH divider of < 200 kΩ.

7.3.19 Output Tolerances Based on Modes of Operation

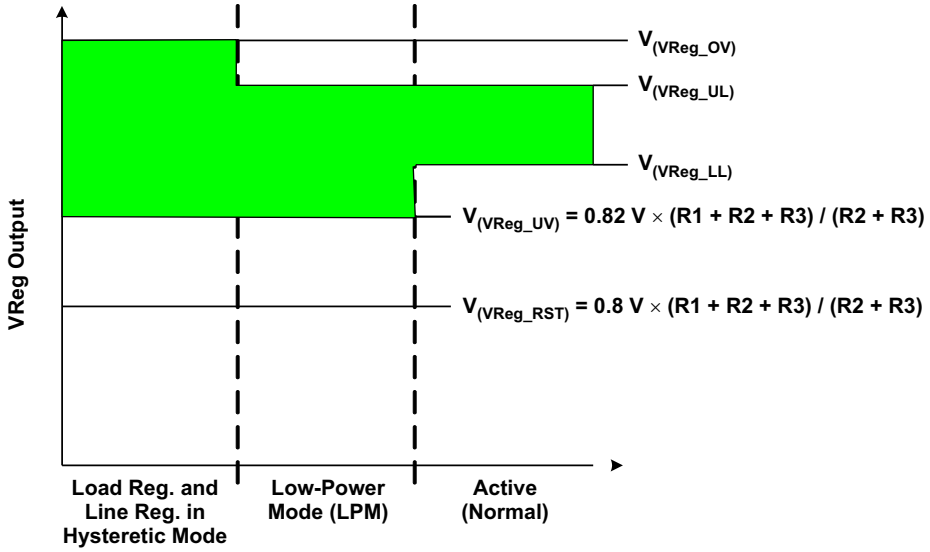


Figure 19. Modes of Operation

Table 1. Values for Threshold Voltages in Each Mode of Operation

MODE OF OPERATION	$V_{(VReg)}$ - LOWER LIMIT	$V_{(VReg)}$ – UPPER LIMIT	COMMENTS
Hysteretic mode	0.82 V × (R1 + R2 + R3) / (R2 + R3)	0.8 V × (R1 + R2 + R3) / (R3)	Minimum to maximum ripple on output
Low-power mode	0.82 V × (R1 + R2 + R3) / (R2 + R3)	$V_{(VReg)} + V_{(VReg\text{-}tol)}$	Minimum to maximum ripple on output
Active (normal)	$V_{(VReg)} – V_{(VReg\text{-}tol)}$	$V_{(VReg)} + V_{(VReg\text{-}tol)}$	Minimum to maximum ripple on output

Table 2. Values for Threshold Voltages of Voltage Supervisors

SUPERVISOR THRESHOLDS	$V_{(VReg)}$ - TYPICAL VALUE	TOLERANCE	COMMENTS
Overvoltage	0.8 V × (R1 + R2 + R3) / (R3)	± ($V_{(VRef\text{-}tol)}$ + (R1 + R2 / [R1 + R2 + R3]) × (R1-tol + R2-tol + R3-tol)	Overvoltage threshold setting
Reset	0.8 V × (R1 + R2 + R3) / (R2 + R3)	± ($V_{(VRef\text{-}tol)}$ + (R1 / [R1 + R2 + R3]) × (R1-tol + R2-tol + R3-tol)	Reset threshold setting

7.3.20 Load Regulation and Line Regulation in Hysteretic Mode

This mode of operation is when a load or line transient step occurs in the application. The converter goes into a hysteretic mode of operation until the error amplifier stabilizes and controls the output regulation to a tighter output tolerance. During the load step, $V_{(VReg\_OV)}$ sets the regulator upper threshold and the $V_{(VReg\_UV)}$ limit sets the lower threshold.

The converter enters this mode of operation during load- or line-transient events if the main control loop cannot respond to regulate within the specified tolerances. The regulator exits this mode once the main control loop responds.

7.3.21 Internal Undervoltage Lockout (UVLO)

On power up, the internal band-gap and bias currents attaining stability, which is typically at $V_{(VIN)}$ = 3.4 V (minimum), enables the IC. On power down, disabling the internal circuitry occurs at $V_{(VIN)}$ = 2.6 V (maximum).

7.3.22 Loop-Control Frequency Compensation

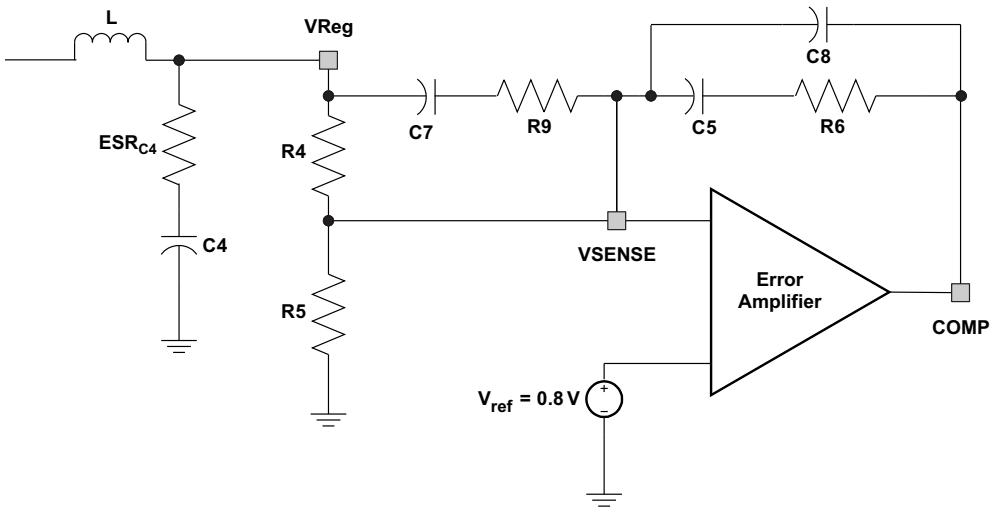


Figure 20. Type III Compensation

7.3.22.1 Type III Compensation

$f_{(c)} = f_{(SW)} \times 0.1$ (unity-gain frequency is the name of the cutoff frequency when the gain is 1).
$f_{(c)}$ is typically 1/5 to 1/10 of the switching frequency, and is typically greater than five times the double-pole frequency of the LC filter.

Equation 9 and Equation 10 derive the modulator break frequencies as a function of the output LC filter. The LC output filter gives a double pole, which has a –180 degree phase shift.

$$f_{(LC)} = \frac{1}{2\pi (L \times C4)^{1/2}} \tag{9}$$

The ESR of the output capacitor C gives a *zero* that has a 90° phase shift.

$$f_{(ESR)} = \frac{1}{2\pi \times C4 \times ESR_{C4}} \tag{10}$$

$$V_{(Vreg)} = V_{ref} \times \frac{(R4 + R5)}{R5} \tag{11}$$

$$\frac{V_{(Vreg)}}{0.8\ V} = \frac{(R4 + R5)}{R5} \tag{12}$$

The $V_{(VIN)}$ / $V_{(ramp)}$ modulator gain is about 10 for 8 V < VIN < 50 V. $V_{(ramp)}$ is fixed at 1 V for $V_{(VIN)}$ < 8 V and at 5 V for $V_{(VIN)}$ > 48 V.

Note that the $V_{(VIN)}$ / $V_{(ramp)}$ gain ($A_{(mod)}$) is not precise and has a tolerance of about 20%.

$$V_{(ramp)} = \frac{V_{(VIN)}}{10}$$

$$\text{Gain (dB)} = 20 \times \log \left(\frac{V_{(VIN)}}{V_{(ramp)}} \right) \tag{13}$$

$$\text{Gain} = 20 \times \log 10 = 20\ \text{dB} \tag{14}$$

$$f_{(p1)} = \frac{(C5 + C8)}{2\pi \times R6 \times (C5 \times C8)} \quad (15)$$

$$f_{(p2)} = \frac{1}{2\pi \times R9 \times C7} \quad (16)$$

$$f_{(z1)} = \frac{1}{2\pi \times R6 \times C5} \quad (17)$$

$$f_{(z2)} = \frac{1}{2\pi \times (R4 + R9) \times C7} \quad (18)$$

7.3.23 Bode Plot of Converter Gain

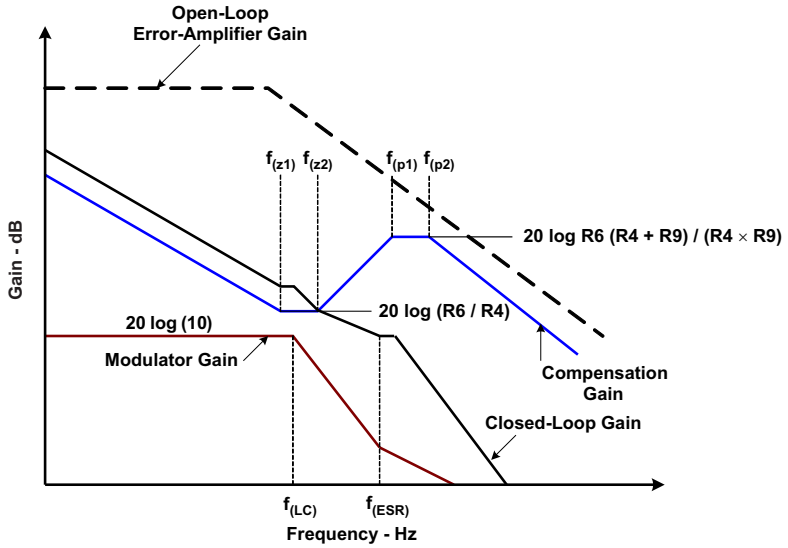


Figure 21. Bode Plot of Converter Gain

7.4 Device Functional Modes

7.4.1 Low-Power Mode (LPM)

The TPS54362-Q1 device automatically enters low-power mode once the regulation goes into discontinuous mode. The internal control circuitry for any transition from low-power mode to high-power mode occurs within 5 µs (typical). In low-power mode, the converter operates as a hysteretic controller with the threshold limits set by $V_{(VReg\_UV)}$ = 0.82 × (R1 + R2 +R3 / (R2 + R3) for the lower limit and approximately $V_{(VReg)}$ for the upper limit. To ensure tight regulation in the low-power mode, set the R2 and R3 values accordingly.

The device operates with both automatic and digitally controlled low-power mode. The digital low-power mode can override the automatic low-power mode function by applying the appropriate signal on the LPM pin. The device goes into active or normal mode for at least 100 µs on the tripping of RST_TH or VREG_UV. Operating in active mode or normal mode enables all blocks, including the OV function.

Being in LPM disables the OV function.

Active or normal mode: When the device is in DCM with LPM = High or in CCM with LPM = High or Low
LPM: When part is in DCM with LPM = Low

Automatic and Digital

LPM high:	LPM high forces the device to normal mode at fixed frequency, even at light load current (the device does pulse skipping to keep output voltage in regulation at light loads).

Device Functional Modes (continued)

LPM low or open: The device automatically changes between normal and low-power mode depending on load current.

7.4.2 Buck-Mode Low-Power-Mode Operation

When operating in low-power mode (buck regulator) with the output shorted to ground, the device asserts a reset. The thermal-shutdown and current-limiting circuitry activates to protect the device.

Low-power-mode operation begins once the converter enters the discontinuous mode of operation.

7.4.3 External LPM Operation

The low-power mode (LPM) is active-low; if there is an open on this pin the IC enters the low-power mode (internal pulldown).

To allow low-power mode operation, the load current must be low with the LPM pin set to ground.

To inhibit low-power mode, the microcontroller must drive the pin high, and the converter must not be in discontinuous mode of operation.

The device can only power up in LPM or DCM if $V_{(VReg)} < 5.5$ V and $V_{(VIN)} - V_{(VReg)} > 2.5$ V.

In active mode. the device powers up when $V_{(VIN)} > 3.6$ V (minimum).

NOTE

Being in LPM prevents enabling of the OV_TH circuit.

Active or normal mode: When the device is in CCM or DCM with LPM = High

LPM: When the device is in DCM with LPM = Low

8 Application and Implementation

8.1 Application Information

This section is a starting point, with theoretical representation of the values used for the application. Improving the performance of the device may require further optimization of the component values.

8.2 Typical Application

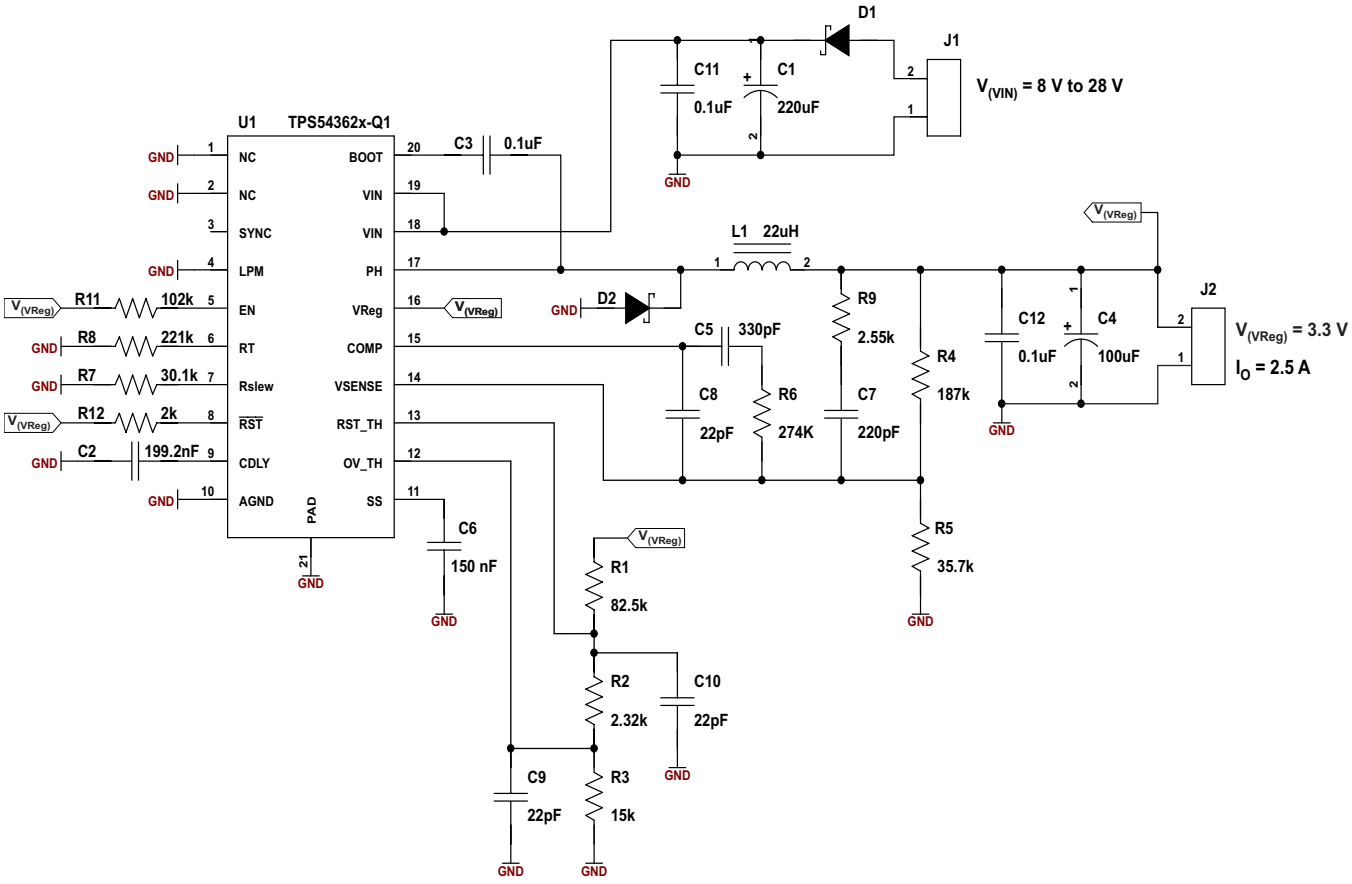


Figure 22. Schematic of Typical Application

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 3.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage, V_I	8 V to 28 V
Output voltage, V_O	5 V ± 2%
Maximum output current, $I_{O\text{-}max}$	3 A
Transient response 0.25-A to 2.25-A load step	ΔV_O = 5%
Reset threshold	92% of output voltage
Overvoltage threshold	106% of output voltage
Undervoltage threshold	95% of output voltage

8.2.2 Detailed Design Procedure

8.2.2.1 Selecting the Switching Frequency

The user selects the switching frequency based on the minimum on-time of the internal power switch, the maximum input voltage, the minimum output voltage, and the frequency-shift limitations. Use Equation 19 to find the maximum frequency for the regulator. Determine the value of the resistor to connect to the RT pin to set this frequency from Figure 13.

$$f_{(SW-max)} = \frac{\left(\frac{V_{O(min)}}{V_{I(max)}}\right)}{t_{(ON-Min)}} \text{ (Hz)} \quad (19)$$

where

- $f_{(SW-max)}$ = 770 kHz
- $t_{(ON-Min)}$ = 150 ns from the *Electrical Characteristics* table

Because the oscillator can vary 10%, decrease the frequency by 10%. Further, to keep the switching frequency outside the AM band, one can select $f_{(sw)}$ as 400 kHz (500 kHz in the application example).

8.2.2.2 Output Inductor Selection (L_O)

Calculate the minimum inductor value using Equation 21.

$k_{(IND)}$ is the coefficient that represents the amount of inductor ripple current relative to the maximum output current. Calculate the ripple using Equation 20.

The output capacitor filters the inductor ripple current, and so the typical range of this ripple current is in the range calculated with $k_{(IND)}$ = 0.2 to 0.3, depending on the ESR and the ripple-current rating of the output capacitor. The minimum inductor value calculated is 14.5 µH; choose an inductor ≈ 22 µH.

$$I_{(Ripple)} = k_{(IND)} \times I_O \quad (20)$$

where

- $I_{(Ripple)}$ = 0.2 × 2.5 = 0.5 A (peak-to-peak)

Calculate inductor $L_{(O)}$:

$$L_{(O-min)} = \frac{\left(V_{I(max)} - V_O\right) \times V_O}{f_{(SW)} \times I_{(Ripple)} \times V_{I(max)}} \text{ (Henries)} \quad (21)$$

where

- $f_{(SW)}$ is the regulator switching frequency
- $I_{(Ripple)}$ = Allowable ripple current in the inductor, typically 20% of maximum I_O

The RMS (root-mean-square) and peak current flowing in the inductor is:

$$I_{L(RMS)} = \sqrt{(I_O)^2 + \frac{(I_{(Ripple)})^2}{12}} \text{ (Amperes)} \quad (22)$$

Inductor peak current:

$$I_{L(pk)} = I_O + \frac{I_{(Ripple)}}{2} \text{ (Amperes)} \quad (23)$$

8.2.2.3 Output Capacitor (C_O)

The selection of the output capacitor determines several parameters in the operation of the converter, the modulator pole, voltage droop on the output capacitor, and the output ripple.

During a load step from no load to full load or changes in the input voltage, the output capacitor must hold up the output voltage above a certain level for a specified time and not issue a reset, until the main regulator control loop responds to the change. Equation 25 determines the minimum output capacitance required to allow sufficient droop on the output voltage without issuing a reset.

The capacitance value determines the modulator pole and the rolloff frequency due to the LC output filter double pole – Equation 9.

The output ripple voltage is a product of the output capacitor ESR and ripple current – Equation 27.

Using Equation 24, the minimum capacitance needed to maintain the desired output voltage during a high-to-low load transition and prevent overshoot is 157 µF.

$$C_{(O)} = \frac{L \times \left[I_{O(max)}^{2} - I_{O(min)}^{2} \right]}{V_{O(max)}^{2} - V_{O(min)}^{2}} \quad \text{(Farads)}$$

where

- $I_{O(max)}$ is the maximum output current
- $I_{O(min)}$ is the minimum output current

The difference between the output current maximum-to-minimum is the worst-case load step in the system

- $V_{O(max)}$ is maximum tolerance of regulated output voltage
- $V_{O(min)}$ is the minimum tolerance of regulated output voltage (24)

The calculation of minimum capacitance needed for transient load response, using Equation 25, yields 53 µF.

$$C_{(O)} > \frac{2 \times \Delta I_O}{f_{(SW)} \times \Delta V_O} \quad \text{(Farads)} \tag{25}$$

The calculation of minimum capacitance needed for output voltage ripple specification, using Equation 26, yields 1.18 µF.

$$C_{(O)} > \frac{1}{8 \times f_{(SW)}} \times \frac{1}{\left(\frac{V_{O(Ripple)}}{I_{(Ripple)}} \right)} \quad \text{(Farads)} \tag{26}$$

The most critical condition based on the foregoing calculations indicates that the output capacitance must be a minimum of 157 µF to keep the output voltage in regulation during load transients.

Factoring in additional capacitance de-ratings for temperature, aging, and dc bias yields a value of 220 µF. Equation 27 calculates the ESR required to meet the ripple-voltage tolerance of the system, but for system stability the ESR should not exceed 100 mΩ.

Maximum ESR of the out capacitor based on output ripple voltage specification is:

$$R_{(ESR)} < \frac{V_{O(Ripple)}}{I_{(Ripple)}} \quad \text{(Ohms)} \tag{27}$$

Output capacitor root-mean-square (rms) ripple current. This is to prevent excess heating or failure due to high ripple currents. This parameter is sometimes specified by the manufacturers.

$$I_{O(RMS)} = \frac{V_O \times \left(V_{I(max)} - V_O \right)}{\sqrt{12} \times V_{I(max)} \times L_{(O)} \times f_{(SW)}} \quad \text{(Amperes)} \tag{28}$$

8.2.2.4 Flyback Schottky Diode

The TPS54362-Q1 device requires an external Schottky diode connected between the PH pin and the power ground termination. The absolute voltage at the PH pin should not go beyond the values mentioned in *Absolute Maximum Ratings*. The Schottky diode conducts the output current during the off state of the internal power switch. This Schottky diode must have a reverse breakdown higher than the maximum input voltage of the application. The low forward voltage of a Schottky diode makes it ideal for this situation. Select the Schottky diode based on the appropriate power rating, which factors in the dc conduction losses and the ac losses due to the high switching frequencies; Equation 29 determines the power requirement.

$$P_{(diode)} = \left(\frac{\left[V_{I(max)} - V_O \right] \times I_O \times V_{(fd)}}{V_{I(max)}} \right) + \left(\frac{\left[V_I - V_{(fd)} \right]^2 \times f_{(SW)} \times C_j}{2} \right) \quad \text{(Watts)}$$

where

- V_F = forward conducting voltage of Schottky diode
- C_j = junction capacitance of the Schottky diode (29)

The recommended part numbers of the Flyback Schottky diodes are PDS360 and SBR8U60P5.

8.2.2.5 Input Capacitor, $C_{(I)}$

The requires an input ceramic decoupling capacitor with type X5R or X7R dielectric, and bulk capacitance to minimize input ripple voltage. The dc voltage rating of this input capacitance must be greater than the maximum input voltage. The capacitor must have an input ripple current rating higher than the maximum input ripple current of the converter for the application; Equation 30 determines the ripple current.

The input capacitors for power regulators are chosen to have reasonable capacitance-to-volume ratio and fairly stable over temperature. The value of the input capacitance also determines the input ripple voltage of the regulator, shown by Equation 31.

$$I_{I(RMS)} = I_O \times \sqrt{\frac{V_O}{V_{I(min)}} \times \frac{V_{I(min)} - V_O}{V_{I(min)}}} \quad \text{(Amperes)} \tag{30}$$

$$\Delta V_I = \frac{I_{O(max)} \times 0.25}{C_{(I)} \times f_{(SW)}} \quad \text{(Volts)} \tag{31}$$

8.2.2.6 Output Voltage and Feedback Resistor Selection

In the design example, the R4 selection is 187 kΩ; using Equation 1, R4 calculates as 35.7 kΩ. To minimize the effect of leakage current on the VSENSE pin, the current flowing through the feedback network should be greater than 5 µA in order to maintain output accuracy. Higher resistor values help improve the converter efficiency at low output currents, but may introduce noise immunity problems.

8.2.2.7 Overvoltage Resistor Selection

Use Equation 6 to determine the value of R3 to set the overvoltage threshold at 1.06 × 5.5 V. The total resistor network from the VReg output to ground is approximately 100 kΩ (this is R1 + R2 +R3). The calculated value of R3 is then 15.09 kΩ. Use the nearest standard value, which is 15 kΩ. This pin may require a noise decoupling capacitor to ensure proper operation; the value chosen for this design is 56 pF.

8.2.2.8 Reset-Threshold Resistor Selection

Using Equation 5, calculate the value of R2 + R3, and then knowing R3 from the OV_TH setting, determine R2. The value of R2 + R3 yields 17.39 kΩ, which means R2 is approximately 2.32 kΩ. This sets the reset threshold at 0.92 × 5 V. This pin may require a noise-decoupling capacitor to ensure proper operation; the value chosen for this design is 15 pF. The value determined for R1 is 82.5 kΩ.

8.2.2.9 Low-Power Mode Threshold

To obtain an approximation of the output load current at which the converter is operating in discontinuous mode, use Equation 32. The values used in the equation for minimum and maximum input voltage affect the duty cycle and the overall discontinuous-mode (DCM) load current. With a maximum input voltage of 28 V, the output load current for DCM is 165.8 mA, and for minimum input voltage of 8 V, the DCM-mode load current is 111.7 mA. These are nominal values, calculated without taking into consideration other factors like external component variations with temperature and aging.

$$I_{L(DCM)} = I_{L(LPM)} = \frac{(1 - D) \times V_O}{2 \times f_{(SW)} \times L_{(O)}} \quad \text{(Amperes) (with } \pm 30\% \text{ hysteresis)}$$

where

- $I_{L(DCM)}$ = Output load current at which the converter is operating in discontinuous mode
- $I_{L(LPM)}$ = Output load current at which the converter is operating in low-power mode
- D = Duty cycle (32)

8.2.2.10 Undervoltage Threshold for Low-Power Mode and Load-Transient Operation

Setting the undervoltage threshold above the reset threshold ensures the regulator operates within the specified tolerances during output load transients of low load to high load and during discontinuous conduction mode. Using Equation 4, determine the typical voltage threshold.

In this design, the value for this threshold is 0.95 × 5 V.

8.2.2.11 Soft-Start Capacitor

The soft-start capacitor determines the minimum time to reach the desired output voltage during a power-up cycle. This time is important when a load requires a controlled voltage-slew rate. Soft starting helps to limit the current draw from the input voltage supply line. This design requires a 4.7-nF capacitor to meet the soft-start criteria. If the buck converter starts up with output shorted to ground, the circuit requires a TPS54362-Q1 device and a minimum 150-nF $C_{(SS)}$.

8.2.2.12 Bootstrap Capacitor Selection

Connect a 0.1-µF ceramic capacitor between the PH and BOOT pins for the converter to operate and regulate the desired output voltage. TI recommends using a capacitor with X5R or better-grade dielectric material, and a voltage rating on this capacitor of at least 25 V to allow for derating.

8.2.2.13 Guidelines for Compensation Components

Make the two zeroes close to the double pole (LC), for example, $f_{(z1)} \approx f_{(z2)} \approx \frac{1}{2 \times \pi \sqrt{LC_O}}$.

1. Make the first zero below the filter double pole (approximately 50% to 75% of $f_{(LC)}$).
2. Make the second zero at the filter double pole ($f_{(LC)}$).

Make the two poles above the crossover frequency $f_{(c)}$,

1. Make the first pole at the ESR frequency ($f_{(ESR)}$).
2. Make the second pole at 0.5 the switching frequency (0.5 × $f_{(SW)}$).

Select R4 = 187 kΩ

$$R5 = \frac{(R4 \times 0.8)}{(V_O - 0.8)} \quad (33)$$

$$R6 = \frac{f_{(c)} \times V_{(ramp)} \times R4}{(f_{(LC)} \times V_I)} \quad (34)$$

Calculate C5 based on placing a zero at 50% to 75% of the output-filter double-pole frequency.

$$C5 = \frac{1}{\pi \times R6 \times f_{(LC)}} \quad (35)$$

Calculate C8 by placing the first pole at the ESR zero frequency.

$$C8 = \frac{C5}{(2\pi \times R6 \times C5 \times f_{(ESR)} - 1)} \quad (36)$$

Set the second pole at 0.5 times the switching frequency, and also set the second zero at the output-filter double-pole frequency.

$$R9 = \frac{R4}{\frac{f_{(SW)}}{2 \times f_{(LC)}} - 1} \quad (37)$$

$$C7 = \frac{1}{\pi \times R9 \times f_{(SW)}} \quad (38)$$

8.2.2.14 Compensation

8.2.2.14.1 Calculate the Loop Compensation

DC modulator gain ($A_{(mod)}$) = 8 / $V_{(ramp)}$
$V_{(ramp)}$ = 0.8 V
$A_{(mod)}$ (dB) = 20 log (10) = 20 dB

Output filter due to LC_O poles and C_O ESR zeros from Equation 9 and Equation 10.

$f_{(LC)}$ = 3.4 kHz for LC_O = 22 µH, C_O = 100 µF
$f_{(ESR)}$ = 15.9 kHz for C_O = 100 µF, ESR = 100 mΩ
Choose R4 = 187 kΩ.

Calculate the poles and zeros for a type III network using equations Equation 33 to Equation 38.

R5 = 35.7 kΩ (use standard value 35.7 kΩ)
R6 = 276 kΩ (use standard value 274 kΩ)
C5 = 340 pF (use standard value 330 pF)
C8 = 40.6 pF (use standard value 22 pF)
R9 = 2.57 kΩ (use standard value 2.55 kΩ)
C7 = 247 pF (use standard value 220 pF)

Calculate the poles and zeros based on these compensation values, using Equation 15 through Equation 18.

8.2.2.14.2 Power Dissipation

The power dissipation losses applicable for continuous-conduction-mode operation (CCM) are:

$$P_{(CON)} = I_O^2 \times r_{DS(on)} \times \frac{V_O}{V_I} \quad \text{(Conduction losses)} \quad (39)$$

$$P_{(SW)} = 1/2 \times V_I \times I_O \times (t_r + t_f) \times f_{(SW)} \quad \text{(Switching losses)} \quad (40)$$

$$P_{(Gate)} = V_{(drive)} \times Q_g \times f_{(SW)} \quad \text{(Gate drive losses) where } Q_g = 1 \times 10^{-9} \text{ (nC)} \quad (41)$$

$$P_{(IC)} = V_I \times I_{(q\text{-}normal)} \quad \text{(Supply losses)} \quad (42)$$

$$P_T = P_{(CON)} + P_{(SW)} + P_{(Gate)} + P_{(IC)} \quad \text{(Watts)} \quad (43)$$

where:

V_O = Output voltage
V_I = Input voltage
I_O = Output current
t_r = FET switching rise time (maximum t_r = 40 ns)
t_f = FET switching fall time
$V_{(drive)}$ = FET gate-drive voltage (typically $V_{(drive)}$ = 6 V and maximum $V_{(drive)}$ = 8 V)
$f_{(sw)}$ = Switching frequency

For a given operating ambient temperature T_A

$$T_J = T_A + R_{\theta JA} \times P_T \quad (44)$$

For a given maximum junction temperature $T_{J\text{-}Max}$ = 150°C

$$T_{A(Max)} = T_{J(Max)} - R_{\theta JA} \times P_T \quad (45)$$

where:

P_T = Total power dissipation (watts)
T_A = Ambient temperature in °C
T_J = Junction temperature in °C

$T_{A(Max)}$ = Maximum ambient temperature in °C
$T_{J(Max)}$ = Maximum junction temperature in °C
$R_{\theta JA}$ = Thermal resistance of package in (°C/W)

Other factors not included in the preceding information which affect the overall efficiency and power losses are:

- Inductor ac and dc losses
- Trace resistance and losses associated with the copper trace routing and connections
- Flyback catch diode

The output current rating for the regulator may require derating for ambient temperatures above 85°C. The derating value depends on the calculated worst-case power dissipation and the thermal management implementation in the application.

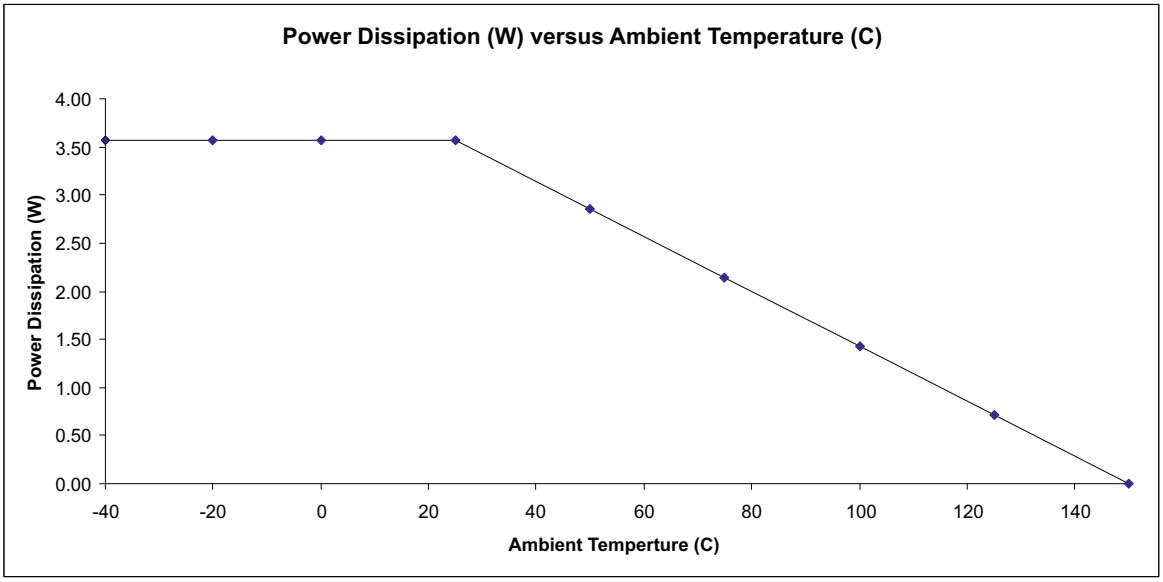
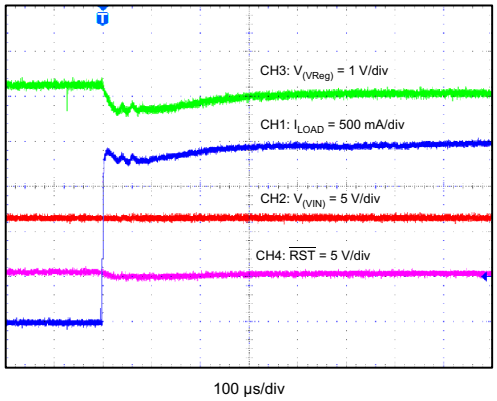


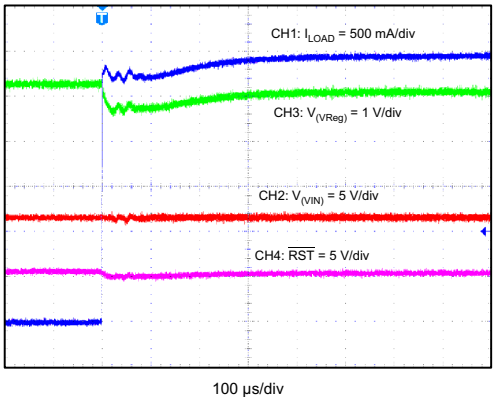
Figure 23. Power Dissipation Derating

8.2.3 Application Curves



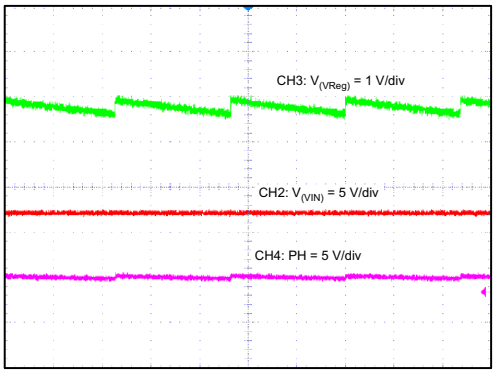
CH1: I_O CH2: VIN CH3: Vreg
CH4: $\overline{RST}$ $V_{(VIN)}$ = 12 V $V_{(VReg)}$ = 5 V

Figure 24. Transition Response (I_O from 0 A to 2 A)



CH1: I_O CH2: VIN CH3: Vreg
CH4: $\overline{RST}$ $V_{(VIN)}$ = 12 V $V_{(VReg)}$ = 5 V

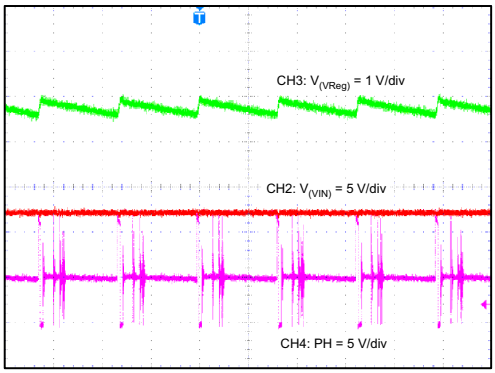
Figure 25. Transition Response (I_O from 0 A to 3 A)



100 ms/div

CH2: VIN $V_{(VIN)}$ = 12 V | CH3: Vreg $V_{(VReg)}$ = 5 V | CH4: PH (100 ms/div) CH4 = 1.905 kHz

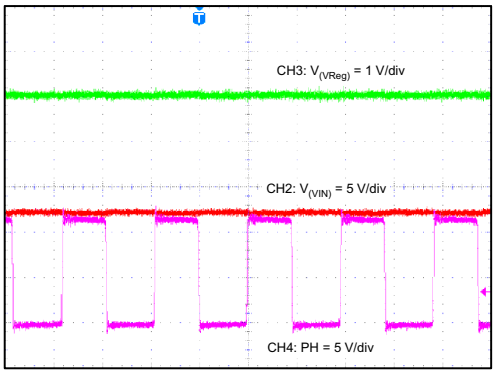
Figure 26. Output Ripple (I_O = 0 A)



200 µs/div

CH2: VIN $V_{(VIN)}$ = 12 V | CH3: Vreg $V_{(VReg)}$ = 5 V | CH4: PH (200 µs/div) CH4 = 45.7 kHz

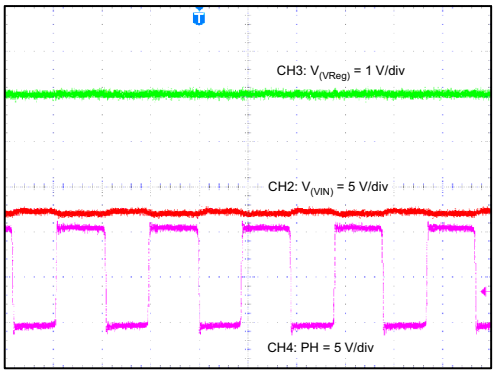
Figure 27. Output Ripple (I_O = 100 mA)



1 µs/div

CH2: VIN $V_{(VIN)}$ = 12 V | CH3: Vreg $V_{(VReg)}$ = 5 V | CH4: PH (1 µs/div) CH4 = 519.1 kHz

Figure 28. Output Ripple (I_O = 1 A)



1 µs/div

CH2: VIN $V_{(VIN)}$ = 12 V | CH3: Vreg $V_{(VReg)}$ = 5 V | CH4: PH (1 µs/div) CH4 = 523.5 kHz

Figure 29. Output Ripple (I_O = 3 A)

9 Power Supply Recommendations

The design of the TPS54362-Q1 devices is for operation using an input supply range from 3.6 V to 48 V. This input supply should be well regulated. If there is a possibility for a reverse-voltage condition to occur, place a series Schottky diode in the power routing.

10 Layout

10.1 Layout Guidelines

TI recommends the following guidelines for PCB layout of the TPS54362-Q1 device.

10.1.1 Inductor

Use a low-EMI inductor with a ferrite-type shielded core. Other types of inductors may be used; however, they must have low-EMI characteristics and be located away from the low-power traces and components in the circuit.

10.1.2 Input Filter Capacitors

Input ceramic filter capacitors should be located in close proximity to the VIN pin. TI recommends surface-mount capacitors to minimize lead length and reduce noise coupling.

10.1.3 Feedback

Route the feedback trace such that there is minimum interaction with any noise sources associated with the switching components. Recommended practice is to place the inductor away from the feedback trace to prevent EMI noise.

10.1.4 Traces and Ground Plane

All power (high-current) traces should be thick and as short as possible. The inductor and output capacitors should be as close to each other as possible. This reduces the EMI radiated by the power traces due to high switching currents.

In a two-sided PCB, TI recommends having ground planes on both sides of the PCB to help reduce noise and ground-loop errors. Connect the ground connection for the input and output capacitors and IC ground to this ground plane.

In a multilayer PCB, the ground plane separates the power plane (where high switching currents and components are placed) from the signal plane (where the feedback trace and components are) for improved performance.

Also, arrange the components such that the switching-current loops curl in the same direction. Place the high-current components such that during conduction the current path is in the same direction. Doing so prevents magnetic field reversal caused by the traces between the two half cycles, helping to reduce radiated EMI.

10.2 Layout Example

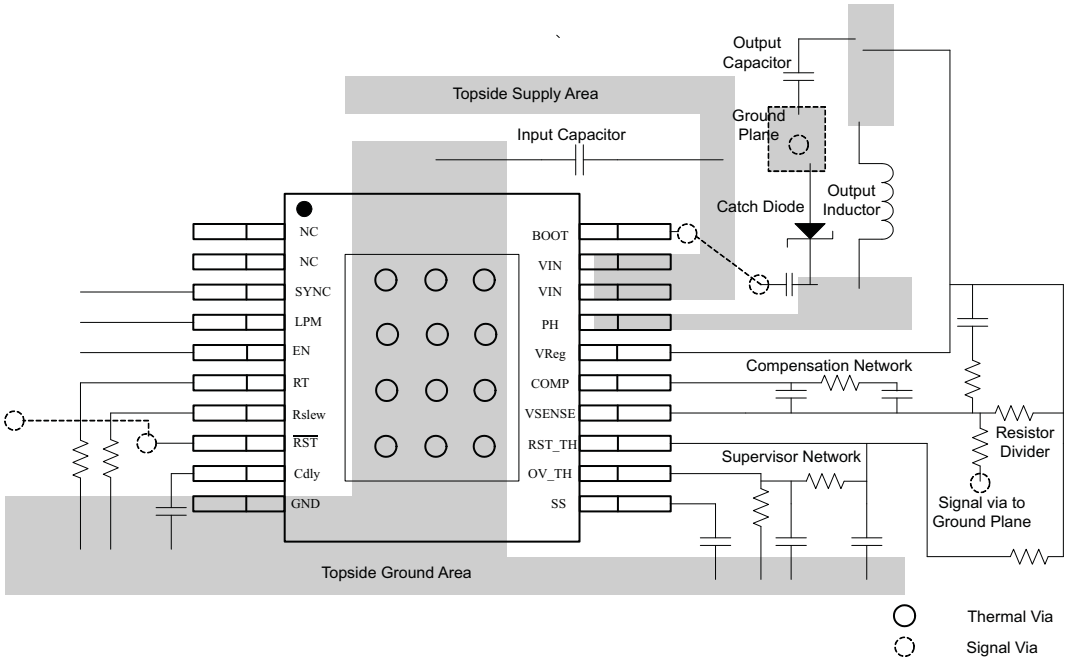


Figure 30. PCB Layout Example

11 Device and Documentation Support

11.1 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54362AQPWPRQ1	NRND	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	54362AQ1	
TPS54362BQPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	54362BQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

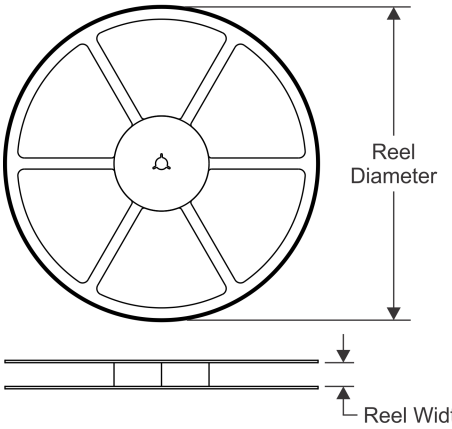
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS54362-Q1 :

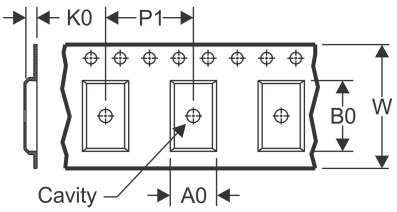
NOTE: Qualified Version Definitions:

TAPE AND REEL INFORMATION

REEL DIMENSIONS

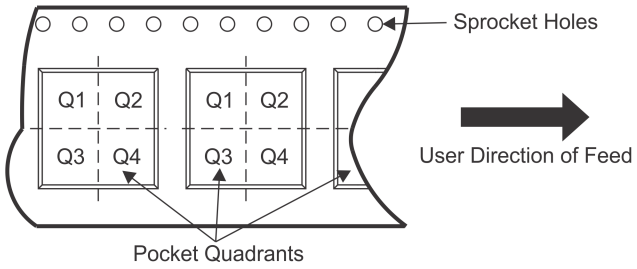


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

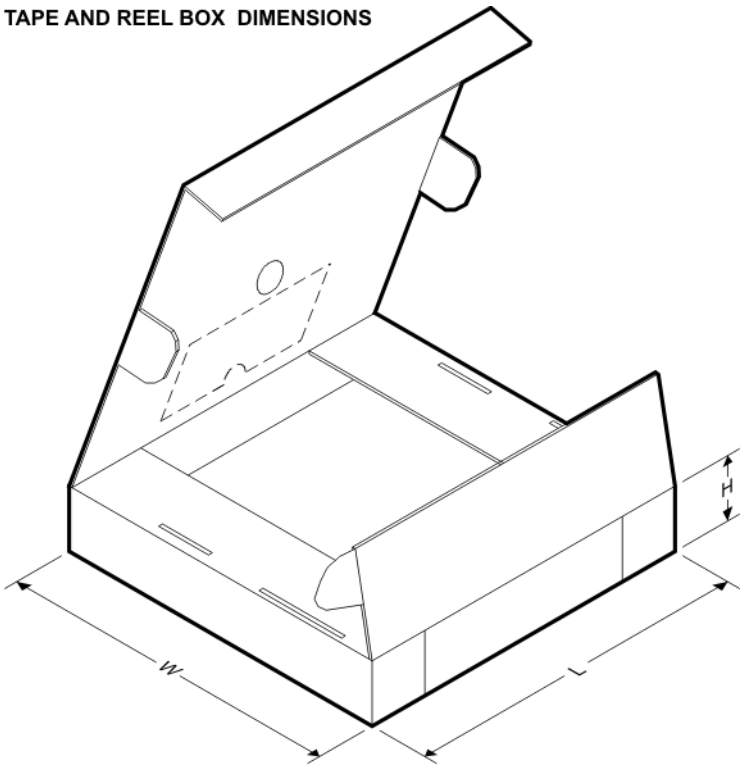
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54362AQPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS54362BQPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

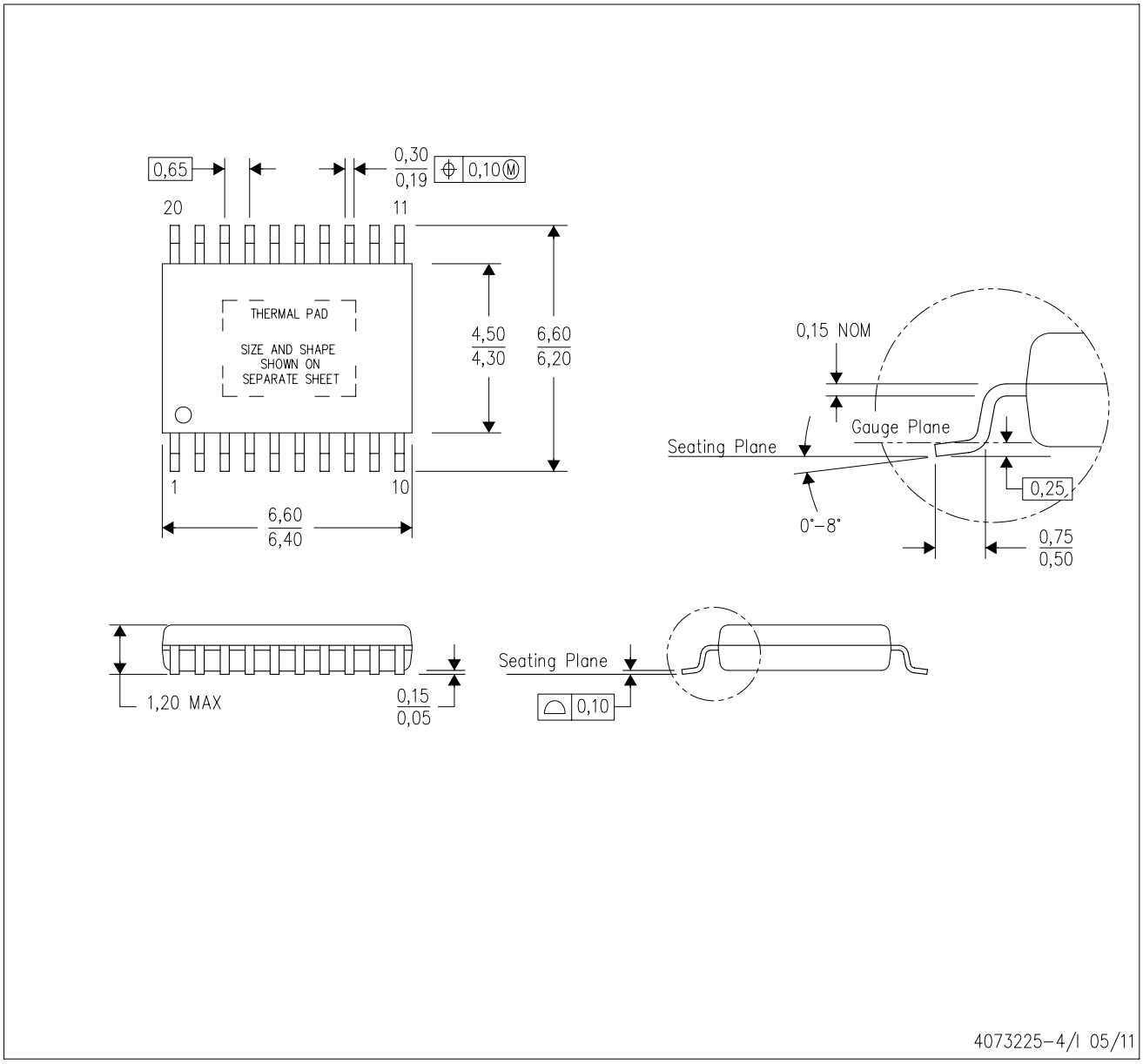
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54362AQPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS54362BQPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

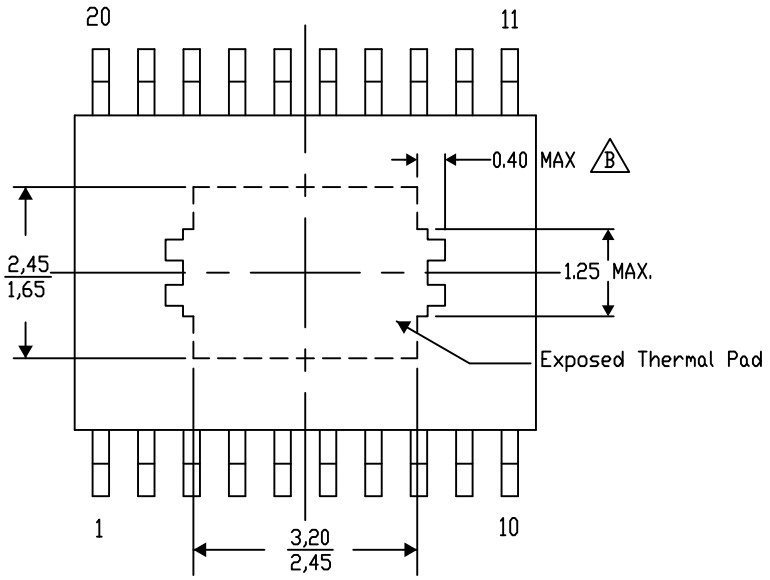
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–18/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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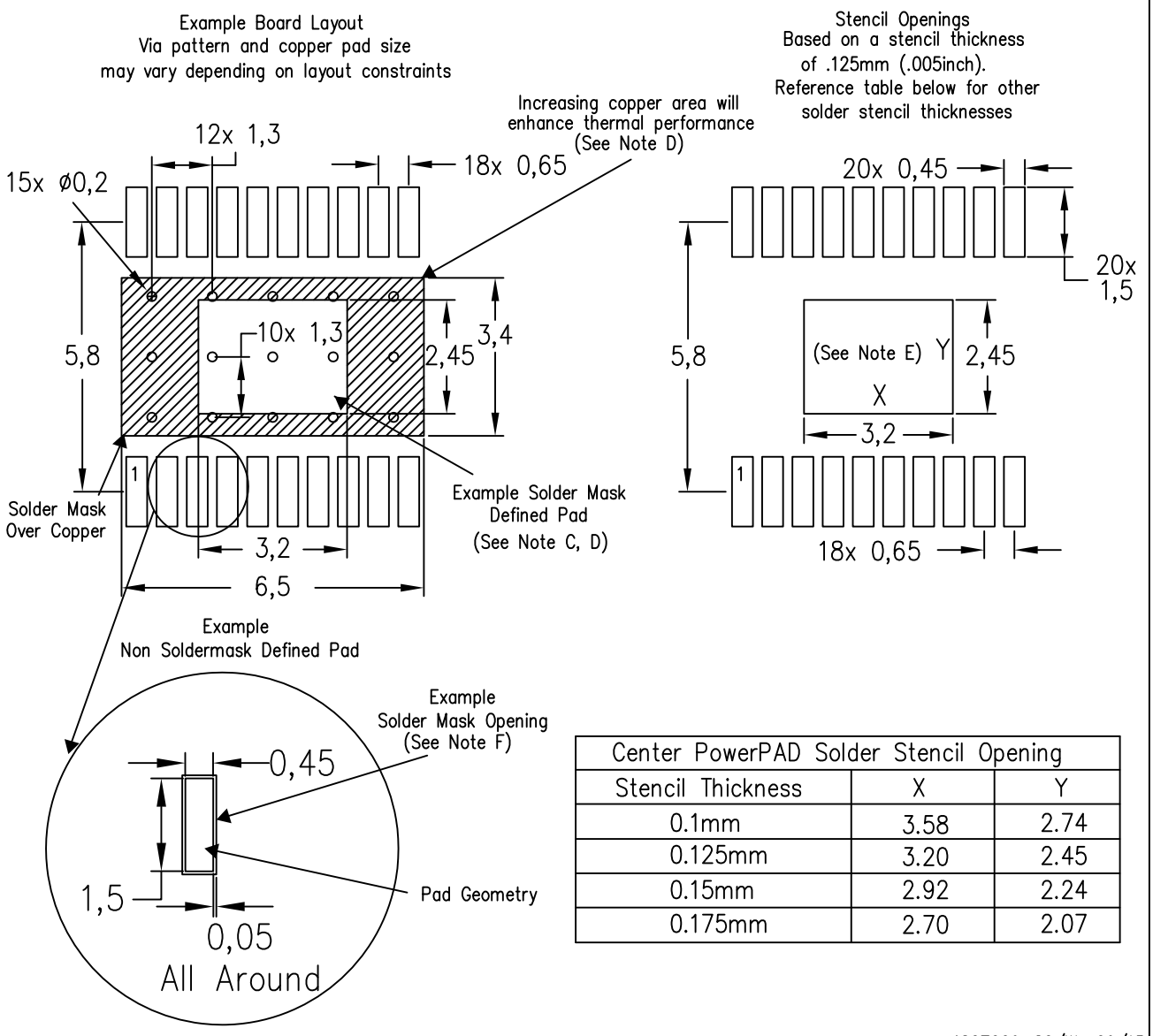
PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center PowerPAD Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.58	2.74
0.125mm	3.20	2.45
0.15mm	2.92	2.24
0.175mm	2.70	2.07

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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