HDMI™ Switch with non-blocking EQ Circuitry

Features

- Differential channel 3:1 Mux/DeMux for TDMS signals
- 3:1 Mux/DeMux for DDC signals
- non-EQ blocking circuitry to utilize ideal EQ found in main receiver chipset
- Low power consumption to support Energy Star Compliance
- Data rate support up to 3.4Gbps (16bit color depth per channel)
- 2 pin control for port selection
- 3.3V power and 5V standby power
- ESD protection on all I/O pins
  → ±8kV contact per IEC61000-4-2
  → 7kV HBM per JESD22
- Packaging (Pb-free & Green): 72 - Contact TQFN

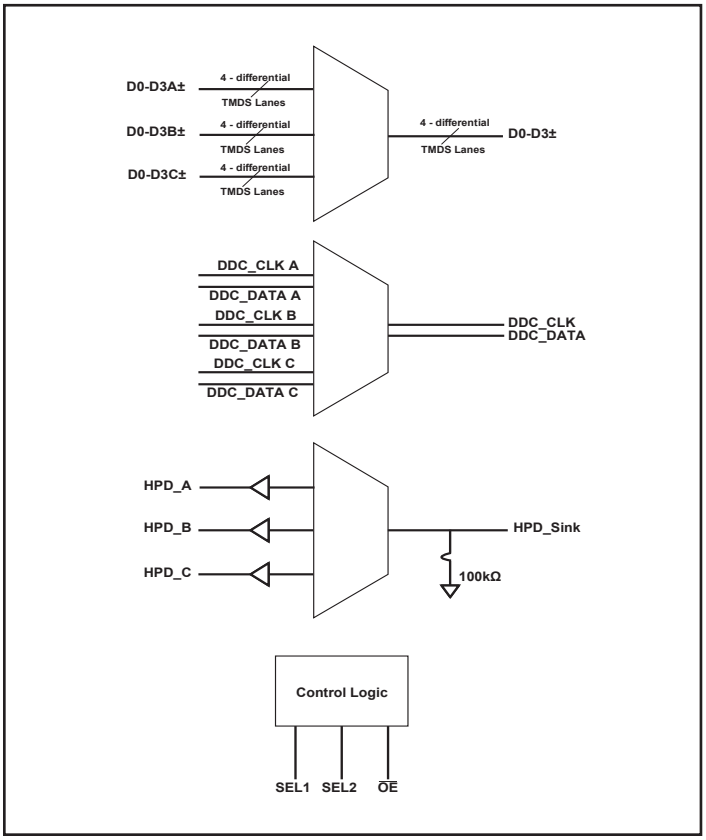
Description

Pericom Semiconductor's PI3HDMI™ series of switch circuits are targeted for high-resolution video networks that are based on DVI/HDMI standards. The PI3HDMI1310-A is a 3-to-1 HDMI Mux/DeMux Switch. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation. The maximum DVI/HDMI data rate of 3.4Gbps provides the resolution required by next generation HDTV and PC graphics. Three differential channels are used for data (video signals for DVI or audio/video signals for HDMI), and one differential channel is used for Clock for decoding the TMDS signals at the outputs.

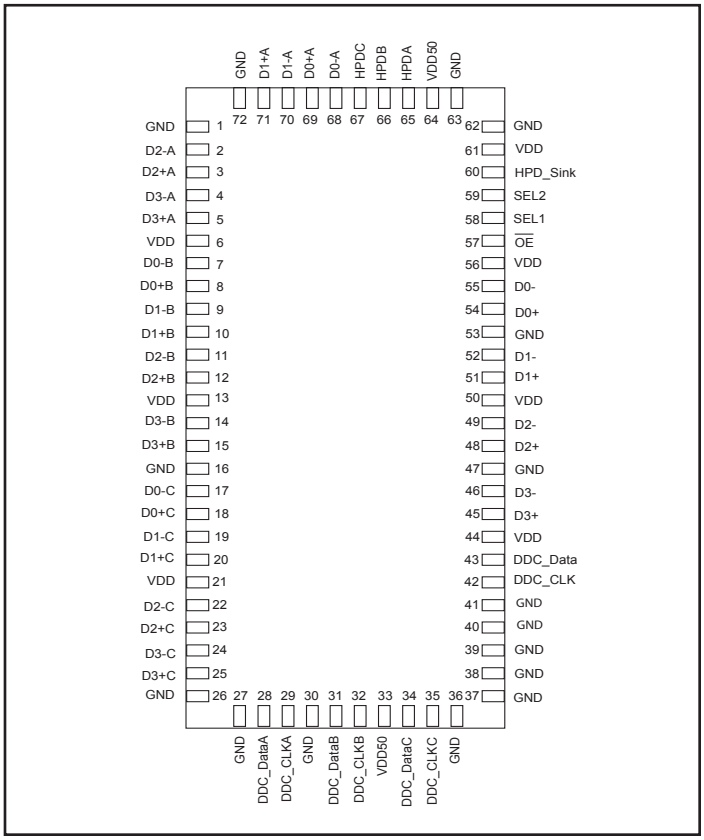
PI3HDMI1310-A was designed specifically to meet ATC-Sink requirement for the HPD ports. The high speed video ports and DDC ports can be either source or sink.

All TMDS I/O pins are protected with Pericom's ESD protection circuits, supporting protection against ESD damage as high as ±8kV contact per IEC6000-4-2 spec.

Block Diagram



Pin Configuration (Top View)



Pin Description

Pin #	Pin Name	Pin Type	Description
69, 68, 71, 70, 3, 2, 5, 4,	Dx±A (X = 0, 1, 2, 3)	I/O	Port A High Speed inputs
8, 7, 10, 9, 12, 11, 15, 14	Dx±B (X = 0, 1, 2, 3)	I/O	Port B High Speed inputs
18, 17, 20, 19, 23, 22, 25, 24	Dx±C (X = 0, 1, 2, 3)	I/O	Port C High Speed inputs
65, 66, 67	HPDA, HPDB, HPDC	Output	HPD open-drain outputs for each port. Logic will follow truth table on page 7. External 1Kohm pull-up to 5V is required
33, 64	VDD50	Power	5.0V voltage rail from HDMI/DVI connector. Used during standby-mode.
60	HPD_Sink	Input	GP I/O pin from SCALAR. Internal 100Kohm pull-down.
29, 28, 32, 31, 35, 34, 42, 43	DDC_CLKx, DDC_Datax	I/O	I^2C signals for DDC communication on TMDS ports
55, 54, 53, 52, 51, 49, 48, 46, 45	DX± (x = 0, 1, 2, 3)	I/O	4-differential high speed Output signals
58, 59	SEL1, SEL2	Inputs	Selection for D0-D3 and DDC signals (Select Pins, see truth tables on page 5)
6, 13, 21, 44, 50, 56, 61	V_{DD}	Power	3.3V Power Supply
1, 16, 26, 27, 30, 36, 37, 38, 39, 40, 41, 53, 62, 63, 72	GND	Power	Ground.
57	$\overline{OE}$	Input	Output enable (Active LOW). When HIGH, all outputs are Hi-Z and chip is placed into Standby Mode. Under Standby Mode, the current supply is from VDD50.

BLOCK DIAGRAM EXPLANATION

DDC Switch Block

Passive NMOS based 3:1 mux for DDC channels from each HDMI/DVI input connector. This section can remain active even when 3.3V supply is gone, as long as 5.0V from TMDS connector is connected to the PI3HDMI1310-A IC.

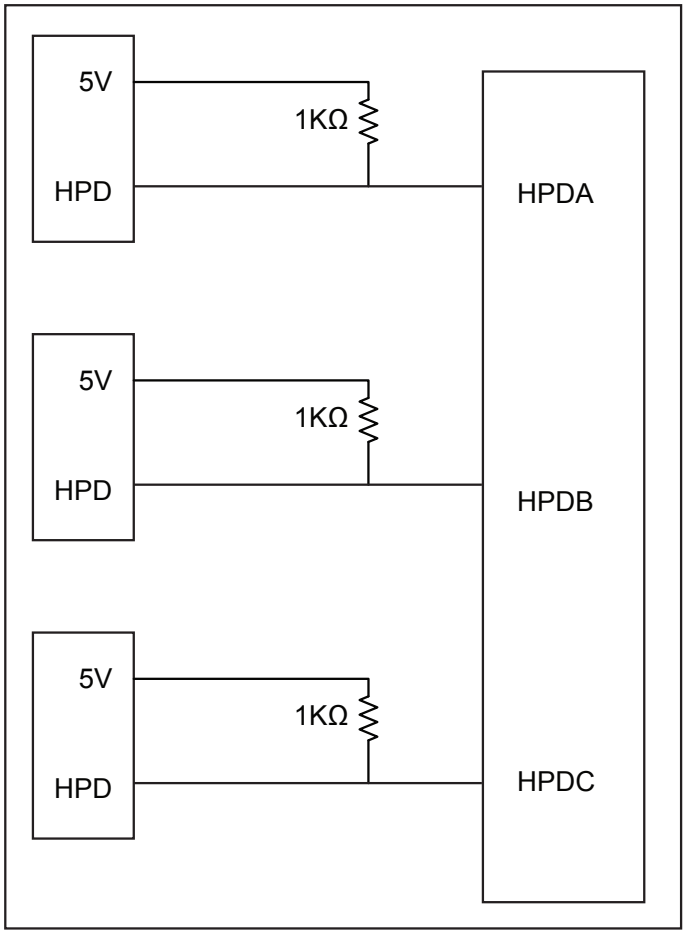
3:1 High speed Differential Channel Block

4-differential channels per port. 3 channels are targeted for high speed data channels (250Mbps to 3.4Gbps) and 1 channel is targeted for high speed clock signal (25MHz to 340MHz).

HPD Control Channels Block

Drives each HPD channels through the input pin, HPD_Sink.

This signal will need to drive external pull-down transistor circuit before connecting to the HDMI/DVI connector. The external pull down circuit will look like the following:



Truth table for D0-D3 and DDC Signals

SEL1	SEL2	Output Port
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Hi-Z

Truth table for HPDx signals

Control Pins				Hot Plug Detect Status		
$\overline{OE}$	SEL1	SEL2	HPD_Sink	HPD A	HPD B	HPD C
x	L	L	L	Hi-Z	Hi-Z	Hi-Z
x	L	L	H	L	Hi-Z	Hi-Z
x	L	H	L	Hi-Z	Hi-Z	Hi-Z
x	L	H	H	Hi-Z	L	Hi-Z
x	H	L	L	Hi-Z	Hi-Z	Hi-Z
x	H	L	H	Hi-Z	Hi-Z	L
x	H	H	L	Hi-Z	Hi-Z	Hi-Z
x	H	H	H	Hi-Z	Hi-Z	Hi-Z

*All Hi-Z will become H if external pull-up connected at the output.

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C
Supply Voltage to Ground Potential .....–0.5V to +4.0V
DC Input Voltage .....–0.5V to 4.0V
DC Output Current 120mA
Power Dissipation 0.5W

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics for Switching over Operating Range (T_A = –40°C to +85°C, V_{DD} = 3.3V ±10%)

Parameter	Description	Test Conditions[1]	Min	Typ[2]	Max	Units
V_{IH}	Input HIGH Voltage	Guaranteed HIGH level	1.5			V
V_{IL}	Input LOW Voltage	Guaranteed LOW level	–0.5		0.65	
V_{IK} [3]	Clamp Diode Voltage	V_{DD} = Max., I_{IN} = –18mA		–0.7	–1.2	

DC Electrical Characteristics for Switching over Operating Range (T_A = –40°C to +85°C, V_{DD} = 3.3V ±10%)

Parameter	Description	Test Conditions[1]	Min	Typ[2]	Max	Units
I_{IH}	Input HIGH Current	V_{DD} = Max., V_{IN} = V_{DD}			±5	µA
I_{IL}	Input LOW Current	V_{DD} = Max., V_{IN} = GND			±5	
I_{OFF}	Off Leakage Current, for high speed channels only	Vinput = 3.6V, V_{DD} = 0V			50	
Status Pins (HPD_SINK)						
V_{IH}	LVTTL Input HIGH Voltage		2		5.3	V
V_{IL}	LVTTL Input LOW Voltage		GND		0.8	
R_P	Pull-down Resistance	V_{DD}50 = 5.0V		100k		Ohm

Power Supply Characteristics

Parameters	Description	Test Conditions[1]	Min.	Typ.[2]	Max.	Units
I_{DD}	Operating Power Supply Current	V_{DD} = Max., V_{SELx} = GND or V_{DD}		6	10	mA
I_{DDQ}	Standby Supply Current	$\overline{OE}$ - High		3	5	

Dynamic Electrical Characteristics Over the Operating Range (T_A= -40° to +85°C, V_{DD} = 3.3V ±10%, GND=0V)

Parameter	Description	Test Conditions		Min	Typ.[2]	Max	Units
X_{TALK}	Crosstalk on High Speed Channels	See Fig. 3 for Measurement Setup	f= 1.13 GHz		-34		dB
			f = 825 MHz		-36		
O_{IRR}	OFF Isolation on High Speed Channels	See Fig. 2 for Measurement Setup	f= 1.13 GHz		-28		
			f = 825 MHz		-32		
I_{LOSS}	Differential Insertion Loss on High Speed Channels (see figure 1)	DR = 1.54Gbps DR = 2.0Gbps DR = 2.25Gbps DR = 3.0Gbps DR = 3.4Gbps			-1.5 -1.73 -1.82 -1.99 -2.08		dB
BW	-3dB BW for TMDS channels				3.0		GHz
Status Pins (HPD) - open drain output buffer							
$V_{OL(TTL)}$	TTL Low-level output voltage	I_{OL} = 4mA				0.4	V

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.
3. Substrate diode voltage drop. For testing reference.

Fig.1 **Differential Insertion Loss and Return Loss Test Circuit**

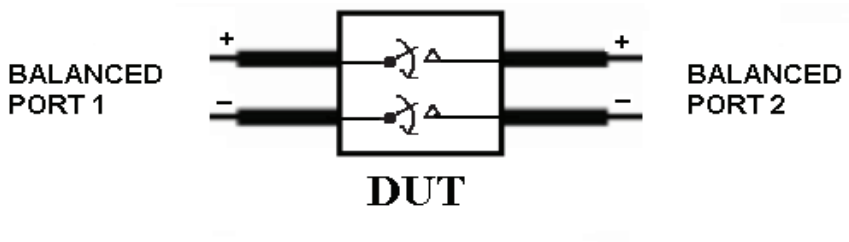


Fig.2 **Differential Off Isolation Test Circuit**

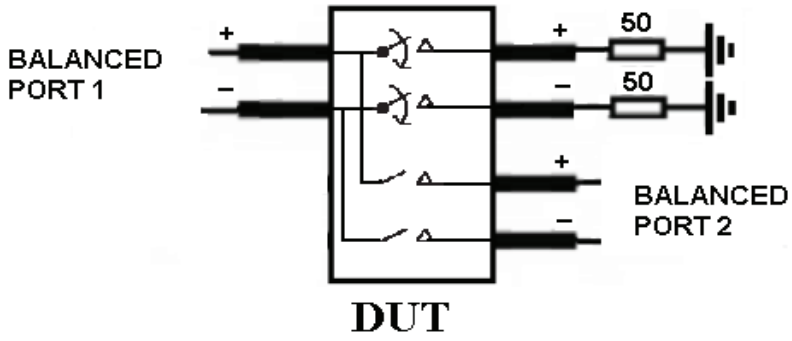
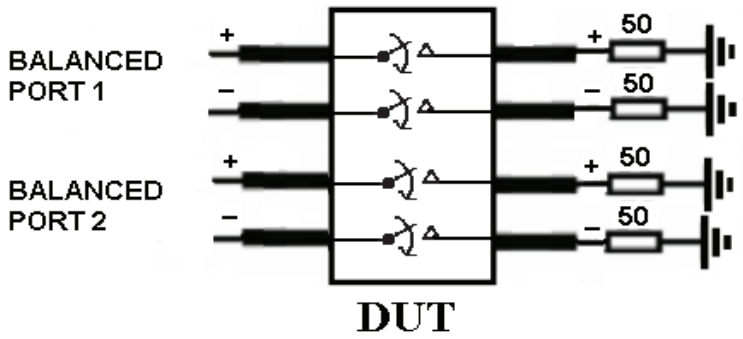


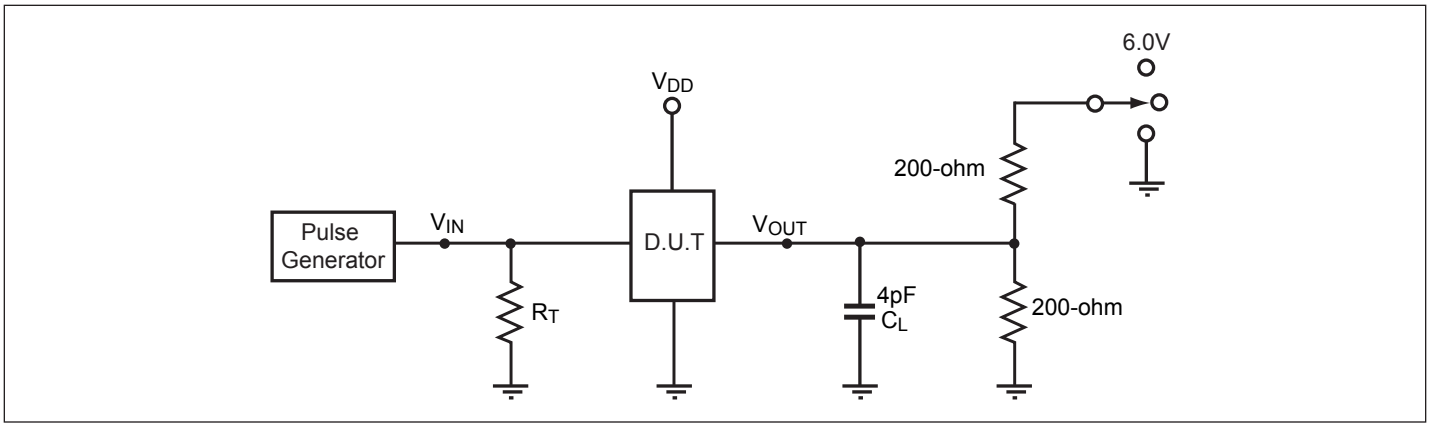
Fig.3 **Differential Near End Crosstalk Test Circuit**



Switching Characteristics (T_A= -40° to +85°C, V_{DD} = 3.3V±10%)

Parameter	Description	Min.	Max.	Units
t_{PZH}, t_{PZL}	Line Enable Time	0.5	25	ns
t_{PHZ}, t_{PLZ}	Line Disable Time	0.5	25	
$t_{b\text{-}b}$	Bit-to-bit skew within the same differential pair		15	ps
$t_{ch\text{-}ch}$	Channel-to-channel skew		35	

Test Circuit for Electrical Characteristics(1-5)



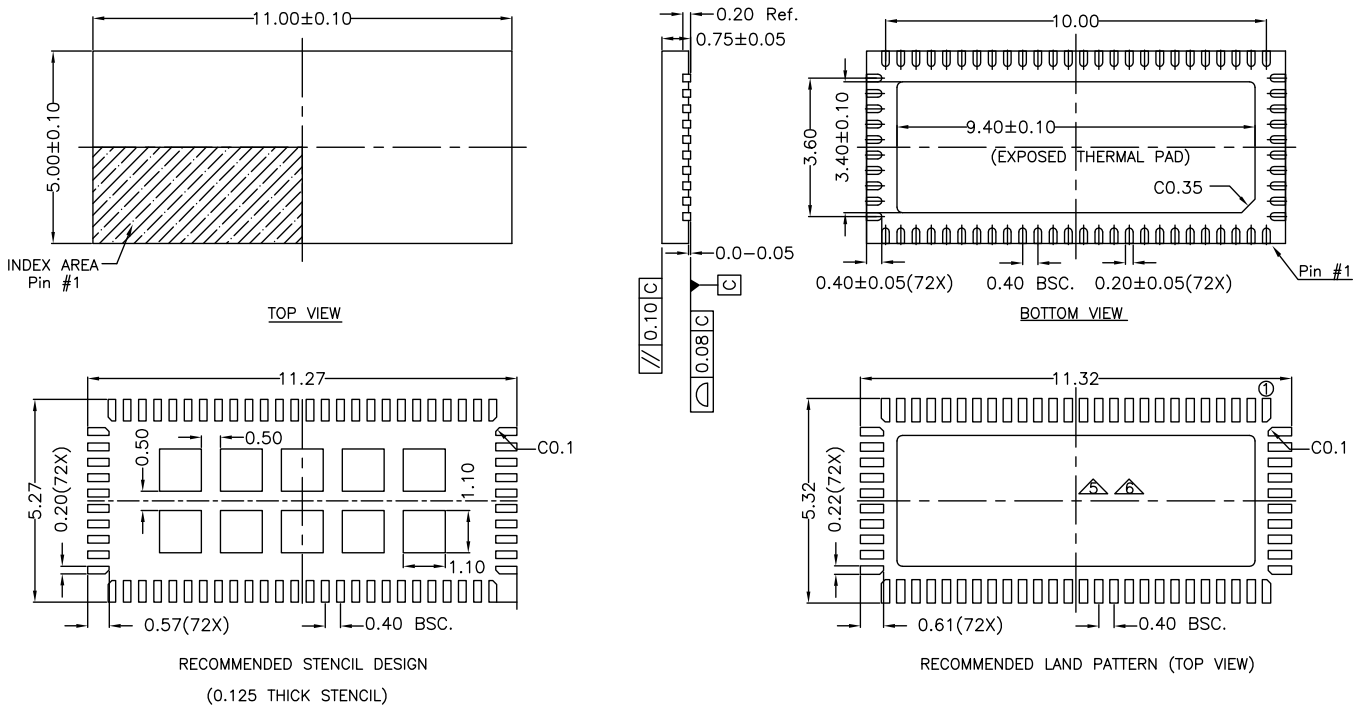
Notes:

1. C_L = Load capacitance: includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
3. Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control. output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, Z_O = 50Ω, t_R ≤ 2.5ns, t_F ≤ 2.5ns.
5. The outputs are measured one at a time with one transition per measurement.

Switch Positions

Test	Switch
t_{PLZ}, t_{PZL} (output on B-side)	6.0V
t_{PHZ}, t_{PZH} (output on B-side)	GND
Prop Delay	Open

Packaging Mechanical: 72-Contact TQFN



Notes:
1. All dimensions are in mm. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals.
3. Refer JEDEC MO-220
4. Recommended land pattern is for reference only.
5. Thermal pad soldering area.
6. Recommended thermal via diameter (drill size) is 0.3mm and via pitch is 1.27mm.

PERICOM Enabling Serial Connectivity

DATE: 06/10/11

DESCRIPTION: 72-contact, Very Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZL72

DOCUMENT CONTROL #: PD-2075 **REVISION: B**

11-0119

Note:
For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Code	Package Code	Package Description
PI3HDMI1310-AZLE	ZL	Pb-free and Green 72-contact TQFN

Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging

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