

1. General description

High voltage, high speed planar passivated NPN power switching transistor in a SOT428 (DPAK) surface mountable plastic package.

2. Features and benefits

- Fast switching
- Low thermal resistance
- Surface mountable package
- Very high voltage capability
- Very low switching and conduction losses

3. Applications

- DC-to-DC converters
- High frequency electronic lighting ballasts
- Inverters
- Motor control systems

4. Quick reference data

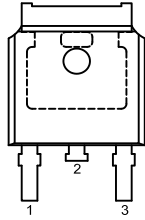
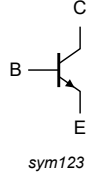
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{CM}	peak collector current	Fig. 1 ; Fig. 2 ; Fig. 3		-	-	8	A
P_{tot}	total power dissipation	$T_{mb} \leq 25\text{ °C}$; Fig. 4		-	-	80	W
V_{CESM}	collector-emitter peak voltage	$V_{BE} = 0\text{ V}$		-	-	1050	V
Static characteristics							
h_{FE}	DC current gain	$I_C = 0.1\text{ A}$; $V_{CE} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 11	[1]	48	66	100	
		$I_C = 0.8\text{ A}$; $V_{CE} = 3\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 12	[1]	25	42	50	

[1] Pulse test: pulse duration $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B	base	 <p>DPAK (SOT428)</p>	 <p>sym123</p>
2	C	collector ^[1]		
3	E	emitter		
mb	C	mounting base; connected to collector		

[1] it is not possible to make a connection to pin 2 of the SOT428 (DPAK) package

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUJ302AD	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CESM}	collector-emitter peak voltage	$V_{BE} = 0\text{ V}$	-	1050	V
V_{CEO}	collector-emitter voltage	$I_B = 0\text{ A}$	-	400	V
V_{EBO}	emitter-base voltage	$I_C = 0\text{ A}; I_E = 2\text{ A}; t_p < 10\text{ ms}$	-	24	V
I_C	collector current	Fig. 1 ; Fig. 2 ; Fig. 3	-	4	A
I_{CM}	peak collector current		-	8	A
I_B	base current		-	2	A
I_{BM}	peak base current		-	4	A
P_{tot}	total power dissipation	$T_{mb} \leq 25\text{ °C}$; Fig. 4	-	80	W
T_{stg}	storage temperature		-65	150	°C
T_j	junction temperature		-	150	°C

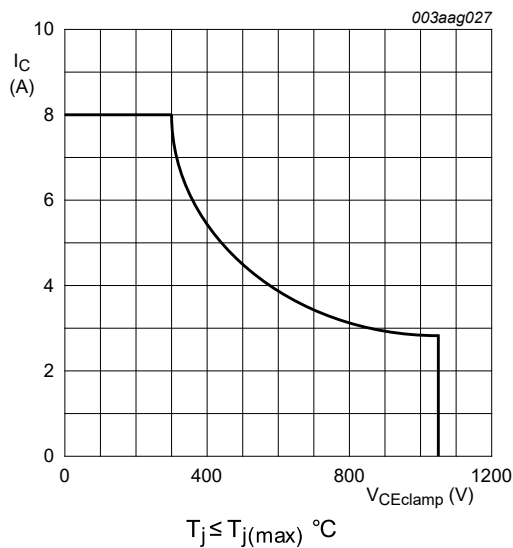


Fig. 1. Reverse bias safe operating area

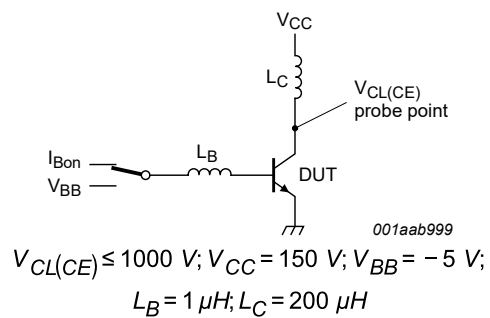
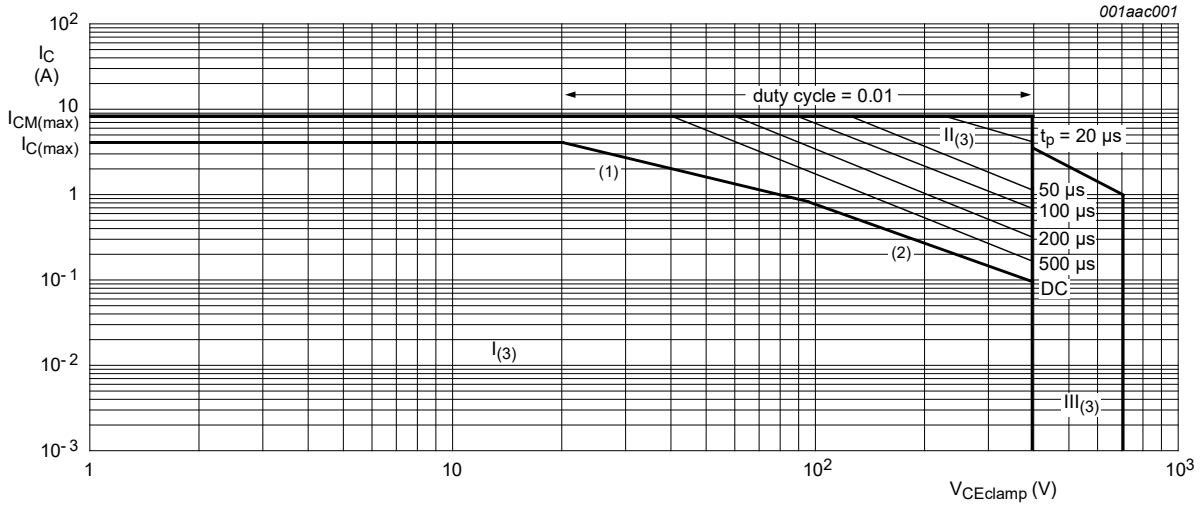
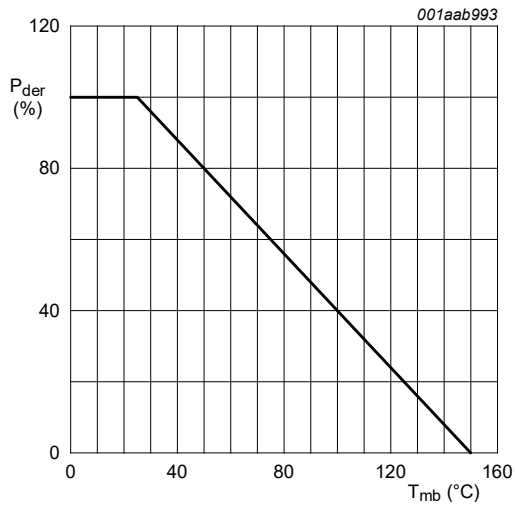


Fig. 2. Test circuit for reverse bias safe operating area



- 1) Ptot maximum and Ptot peak maximum lines
- 2) Second breakdown limits
- 3) I = Region of permissible DC operation
- II = Extension for repetitive pulse operation
- III = Extension during turn-on in single transistor converters provided that RBE ≤ 100 Ω and tp ≤ 0.6 μs

Fig. 3. Forward bias safe operating area for Tmb ≤ 25 °C



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig. 4. Normalized total power dissipation as a function of mounting base temperature

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	1.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board (FR4) mounted; minimum footprint	-	75	-	K/W

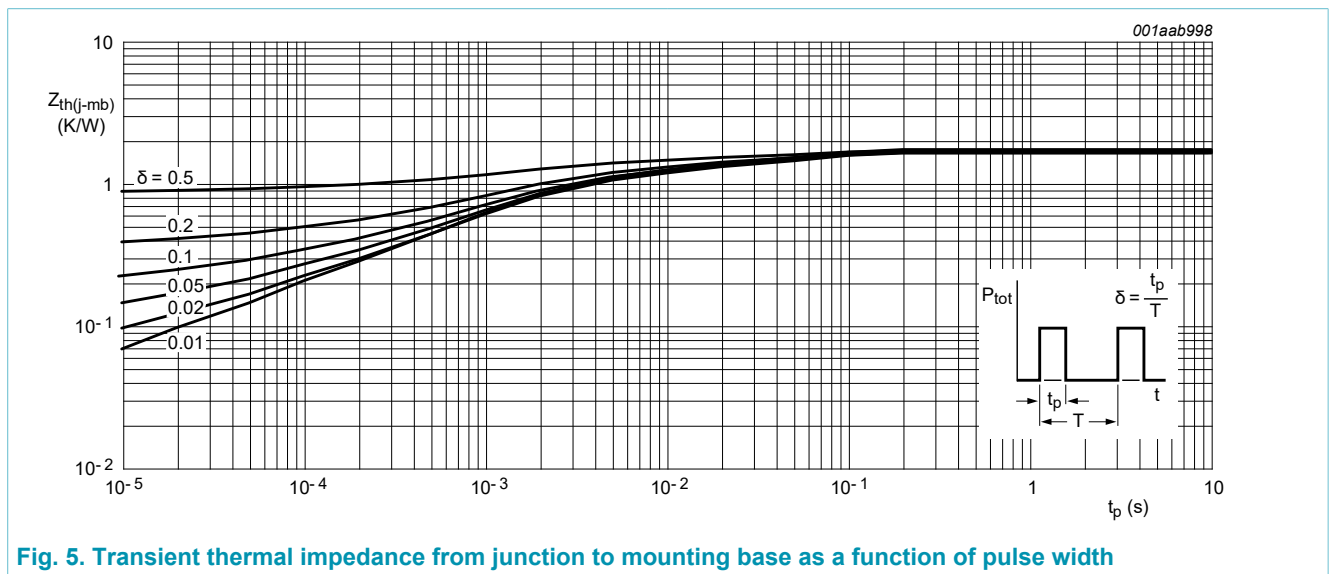


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse width

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Static characteristics							
I_{CES}	collector-emitter cut-off current (base shorted)	$V_{BE} = 0\text{ V}; V_{CE} = 1050\text{ V}$	-	0.2	10	μA	
I_{CEO}	collector-emitter cut-off current (base open)	$V_{CE} = 400\text{ V}; I_B = 0\text{ A}; T_{mb} = 25\text{ }^\circ\text{C}$	-	10	250	mA	
$V_{(BR)EBO}$	emitter-base breakdown voltage (collector open)	$I_B = 1\text{ mA}; I_C = 0\text{ A}; T_{mb} = 25\text{ }^\circ\text{C}$	15	19	-	V	
V_{CEOsus}	collector-emitter sustaining voltage (base open)	$I_B = 0\text{ A}; I_C = 10\text{ mA}; L_C = 25\text{ mH}; T_{mb} = 25\text{ }^\circ\text{C};$ Fig. 6 ; Fig. 7	[1]	400	470	-	V
V_{CEsat}	collector-emitter saturation voltage	$I_C = 1\text{ A}; I_B = 0.2\text{ A}; T_{mb} = 25\text{ }^\circ\text{C};$ Fig. 8 ; Fig. 9	[1]	-	0.15	0.5	V
		$I_C = 3.5\text{ A}; I_B = 1\text{ A}; T_{mb} = 25\text{ }^\circ\text{C};$ Fig. 8 ; Fig. 9	[1]	-	0.6	1.5	V
V_{BEsat}	base-emitter saturation voltage	$I_C = 3.5\text{ A}; I_B = 1\text{ A}; T_{mb} = 25\text{ }^\circ\text{C};$ Fig. 10	[1]	-	1.1	1.5	V
h_{FE}	DC current gain	$I_C = 0.1\text{ A}; V_{CE} = 5\text{ V}; T_{mb} = 25\text{ }^\circ\text{C};$ Fig. 11	[1]	48	66	100	
		$I_C = 0.8\text{ A}; V_{CE} = 3\text{ V}; T_{mb} = 25\text{ }^\circ\text{C};$ Fig. 12	[1]	25	42	50	
Dynamic characteristics							
t_s	storage time	$I_C = 2.5\text{ A}; I_{B(on)} = 0.5\text{ A}; I_{B(off)} = -0.5\text{ A}; R_L = 60\text{ }\Omega; V_{BB} = -5\text{ V}; T_{mb} = 25\text{ }^\circ\text{C};$ resistive load; $t_p = 300\text{ }\mu\text{s};$ Fig. 13 ; Fig. 14	-	-	3.5	μs	
t_f	fall time		-	-	500	ns	

[1] Pulse test: pulse duration $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

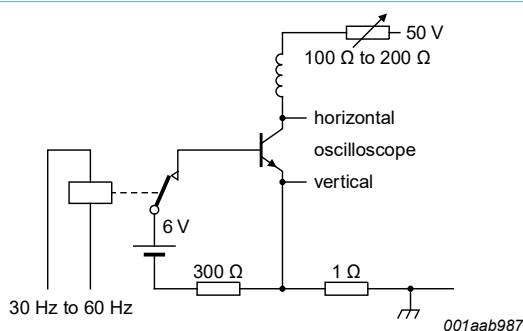


Fig. 6. Test circuit for collector-emitter sustaining voltage

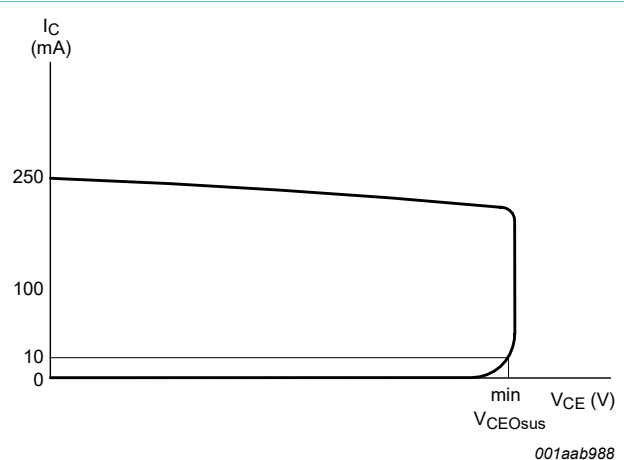


Fig. 7. Oscilloscope display for collector-emitter sustaining voltage test waveform

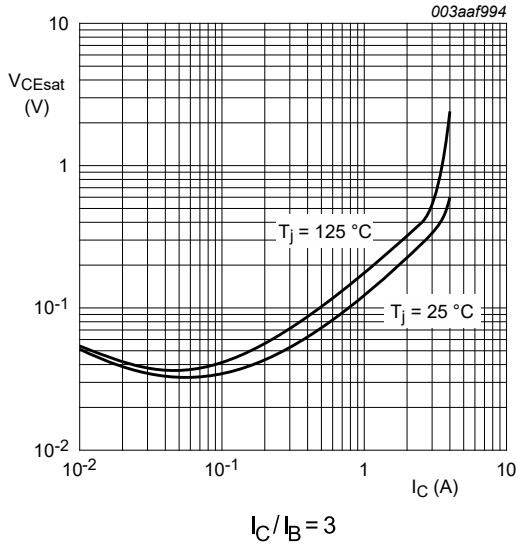


Fig. 8. Collector-emitter saturation voltage as a function of collector current; typical values

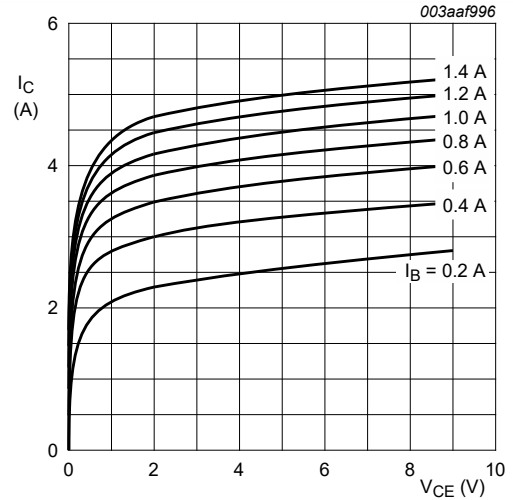


Fig. 9. Collector current as a function of collector-emitter voltage; typical values

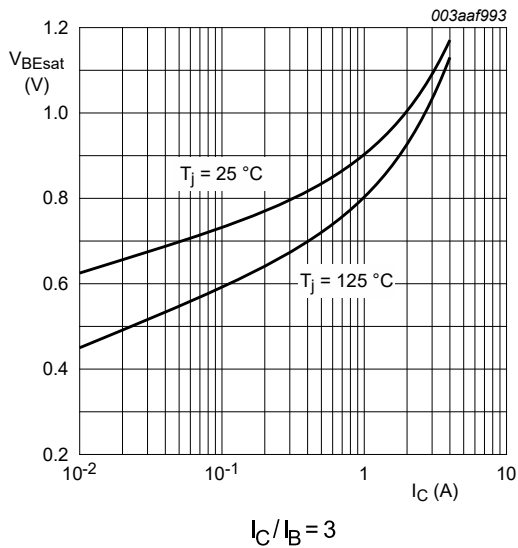


Fig. 10. Base-emitter saturation voltage as a function of collector current; typical values

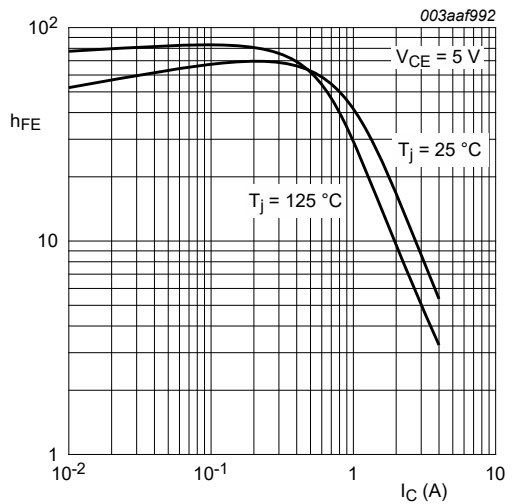


Fig. 11. DC current gain as a function of collector current; typical values

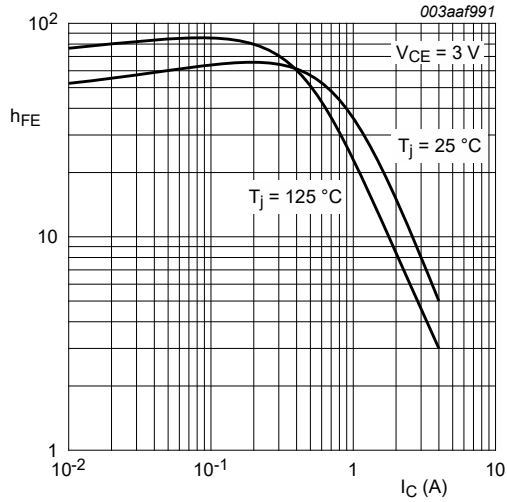
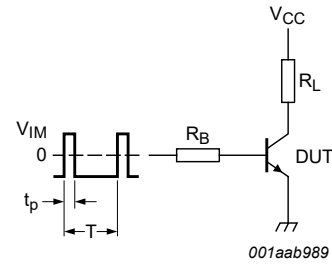


Fig. 12. DC current gain as a function of collector current; typical values



$V_{IM} = -6 \text{ to } +8 \text{ V}$; $V_{CC} = 250 \text{ V}$; $t_p = 20 \mu\text{s}$; $\delta = \frac{t_p}{T} = 0.01$
 R_B and R_L calculated from I_{Con} and I_{Boff} requirements.

Fig. 13. Test circuit for resistive load switching

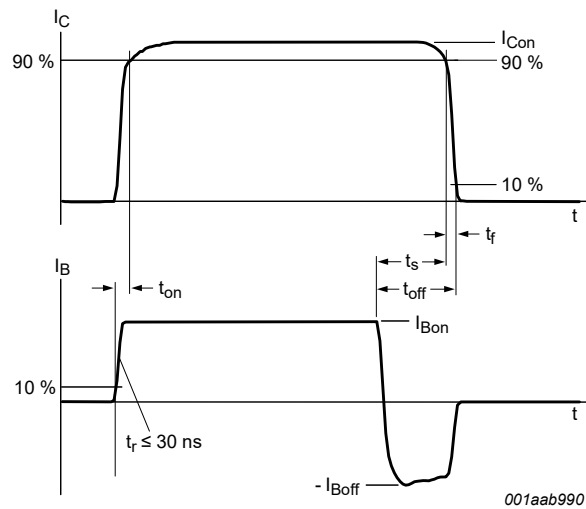


Fig. 14. Switching times waveforms for resistive load

10. Package outline

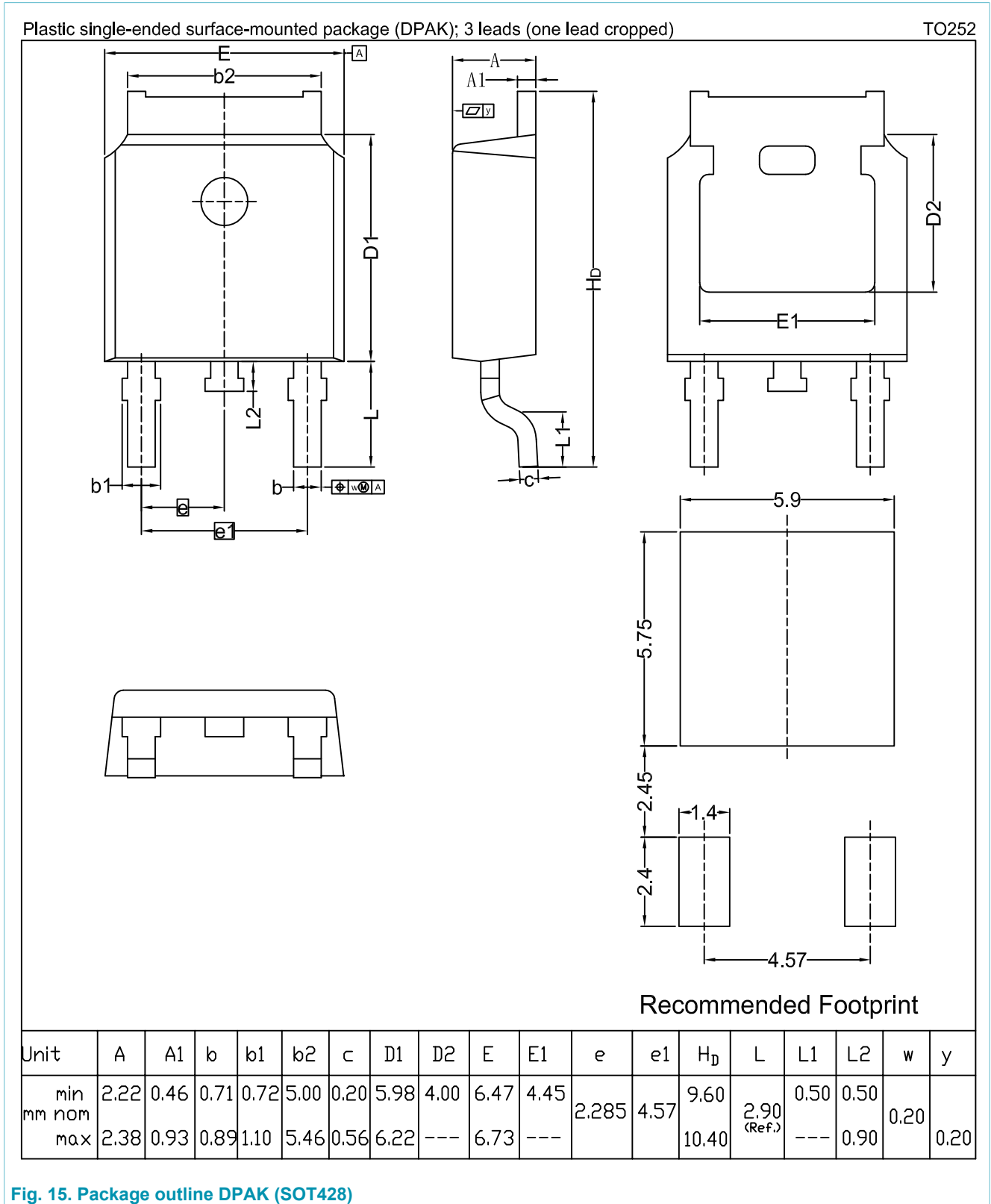
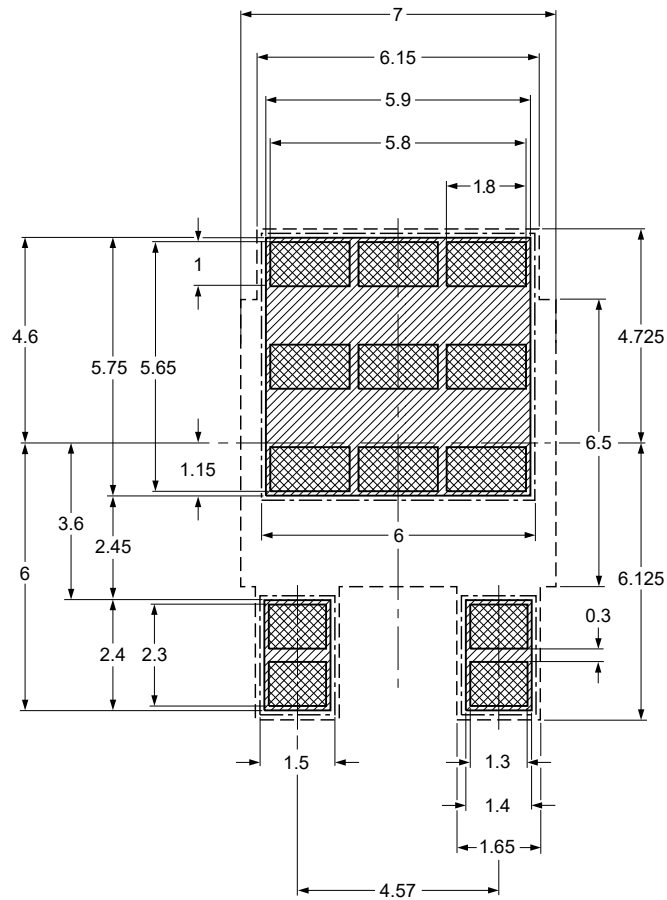


Fig. 15. Package outline DPAK (SOT428)

11. Soldering

Footprint information for reflow soldering of DPAK (SOT428) package

SOT428



Dimensions in mm

Issue date ~~14-03-12~~
14-03-17

sot428_fr

Fig. 16. Wave soldering footprint for DPAK (SOT428)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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