

NVMFS5826NL

Power MOSFET

60 V, 24 mΩ, 26 A, Single N-Channel

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS5826NLWF – Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- These are Pb-Free Devices and RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter | Symbol | Value | Unit | |
|---|--|------------------------------|------------------|---|
| Drain-to-Source Voltage | V_{DS} | 60 | V | |
| Gate-to-Source Voltage | V_{GS} | ± 20 | V | |
| Continuous Drain Current $R_{\Psi J-mb}$ (Notes 1, 2, 3, 4) | Steady State | $T_{mb} = 25^\circ\text{C}$ | I_D 26 | A |
| | | $T_{mb} = 100^\circ\text{C}$ | 19 | |
| Power Dissipation $R_{\Psi J-mb}$ (Notes 1, 2, 3) | Steady State | $T_{mb} = 25^\circ\text{C}$ | P_D 39 | W |
| | | $T_{mb} = 100^\circ\text{C}$ | 19 | |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3, 4) | Steady State | $T_A = 25^\circ\text{C}$ | I_D 8.0 | A |
| | | $T_A = 100^\circ\text{C}$ | 6.0 | |
| Power Dissipation $R_{\theta JA}$ (Notes 1 & 3) | Steady State | $T_A = 25^\circ\text{C}$ | P_D 3.6 | W |
| | | $T_A = 100^\circ\text{C}$ | 1.8 | |
| Pulsed Drain Current | $T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$ | I_{DM} 130 | A | |
| Operating Junction and Storage Temperature | T_J, T_{stg} | -55 to +175 | $^\circ\text{C}$ | |
| Source Current (Body Diode) | I_S | 32 | A | |
| Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}, V_{DD} = 24 \text{ V}, V_{GS} = 10 \text{ V}, I_{L(pk)} = 20 \text{ A}, L = 0.1 \text{ mH}, R_G = 25 \Omega$) | E_{AS} | 20 | mJ | |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | T_L | 260 | $^\circ\text{C}$ | |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|--|-----------------|-------|--------------------|
| Junction-to-Mounting Board (top) – Steady State (Notes 2, 3) | $R_{\Psi J-mb}$ | 3.9 | $^\circ\text{C/W}$ |
| Junction-to-Ambient – Steady State (Note 3) | $R_{\theta JA}$ | 42 | |

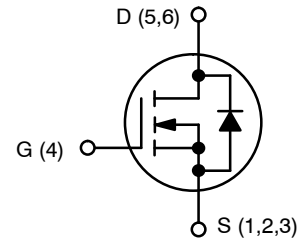
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



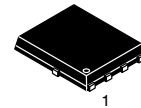
ON Semiconductor®

<http://onsemi.com>

| $V_{(BR)DSS}$ | $R_{DS(ON)} \text{ MAX}$ | $I_D \text{ MAX}$ |
|---------------|--------------------------|-------------------|
| 60 V | 24 mΩ @ 10 V | 26 A |
| | 32 mΩ @ 4.5 V | |

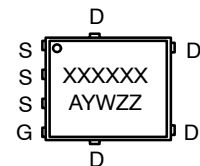


N-CHANNEL MOSFET



DFN5
(SO-8FL)
CASE 488AA
STYLE 1

MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVMFS5826NL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--------|----------------|-----|-----|-----|------|
|-----------|--------|----------------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|-----------------------------------|----------------------|--|------------------------|--|------|----|
| Drain-to-Source Breakdown Voltage | V _{(BR)DSS} | V _{GS} = 0 V, I _D = 250 μA | 60 | | | V |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{GS} = 0 V, V _{DS} = 60 V | T _J = 25°C | | 1.0 | μA |
| | | | T _J = 125°C | | 10 | |
| Gate-to-Source Leakage Current | I _{GSS} | V _{DS} = 0 V, V _{GS} = ± 20 V | | | ±100 | nA |

ON CHARACTERISTICS (Note 5)

| | | | | | | |
|-------------------------------|---------------------|---|-----|-----|-----|----|
| Gate Threshold Voltage | V _{GS(TH)} | V _{GS} = V _{DS} , I _D = 250 μA | 1.5 | | 2.5 | V |
| Drain-to-Source On Resistance | R _{DS(on)} | V _{GS} = 10 V, I _D = 10 A | | 18 | 24 | mΩ |
| | | V _{GS} = 4.5 V, I _D = 10 A | | 24 | 32 | |
| Forward Transconductance | g _{FS} | V _{DS} = 15 V, I _D = 5 A | | 8.0 | | S |

CHARGES AND CAPACITANCES

| | | | | | | |
|------------------------------|---------------------|--|--|-----|--|----|
| Input Capacitance | C _{iss} | V _{GS} = 0 V, f = 1 MHz, V _{DS} = 25 V | | 850 | | pF |
| Output Capacitance | C _{oss} | | | 85 | | |
| Reverse Transfer Capacitance | C _{rss} | | | 50 | | |
| Total Gate Charge | Q _{G(TOT)} | V _{GS} = 4.5 V, V _{DS} = 48 V, I _D = 10 A | | 9.1 | | nC |
| Threshold Gate Charge | Q _{G(TH)} | | | 1.0 | | |
| Gate-to-Source Charge | Q _{GS} | | | 3.0 | | |
| Gate-to-Drain Charge | Q _{GD} | | | 4.0 | | |
| Total Gate Charge | Q _{G(TOT)} | V _{GS} = 10 V, V _{DS} = 48 V, I _D = 10 A | | 17 | | nC |

SWITCHING CHARACTERISTICS (Note 6)

| | | | | | | |
|---------------------|---------------------|---|--|-----|--|----|
| Turn-On Delay Time | t _{d(ON)} | V _{GS} = 4.5 V, V _{DS} = 48 V, I _D = 10 A, R _G = 2.5 Ω | | 9.0 | | ns |
| Rise Time | t _r | | | 32 | | |
| Turn-Off Delay Time | t _{d(OFF)} | | | 15 | | |
| Fall Time | t _f | | | 24 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | | |
|-------------------------|-----------------|---|------------------------|-----|-----|-----|----|
| Forward Diode Voltage | V _{SD} | V _{GS} = 0 V, I _S = 10 A | T _J = 25°C | | 0.8 | 1.2 | V |
| | | | T _J = 125°C | | 0.7 | | |
| Reverse Recovery Time | t _{RR} | V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 10 A | | 15 | | ns | |
| Charge Time | t _a | | | 11 | | | |
| Discharge Time | t _b | | | 4.0 | | | |
| Reverse Recovery Charge | Q _{RR} | | | | 11 | | nC |

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

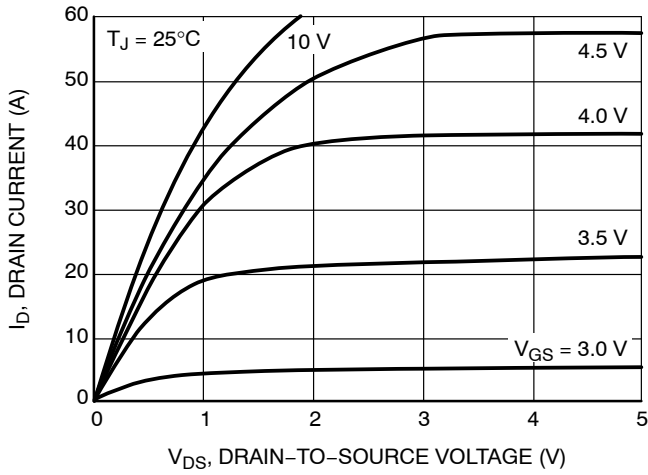


Figure 1. On-Region Characteristics

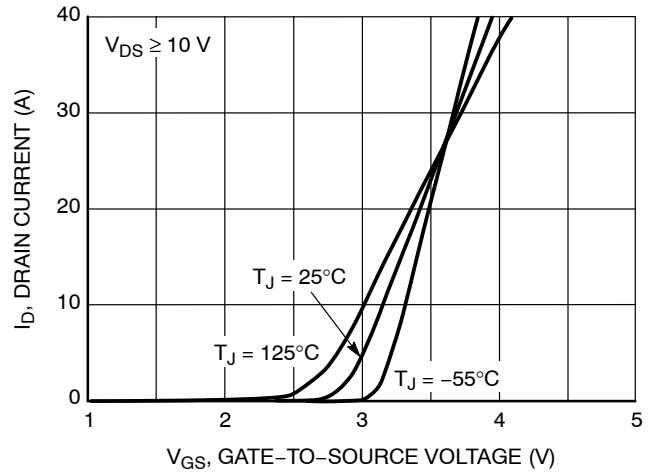


Figure 2. Transfer Characteristics

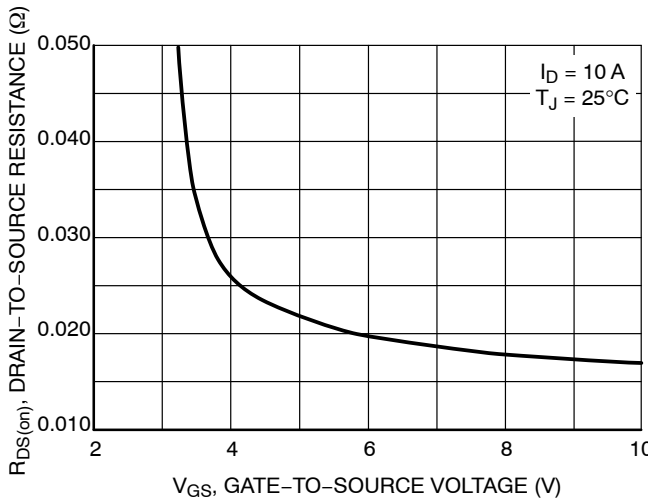


Figure 3. On-Resistance vs. Gate-to-Source Voltage

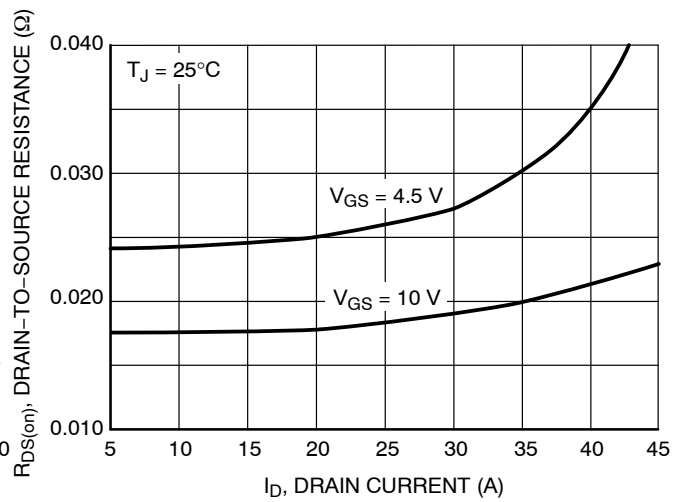


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

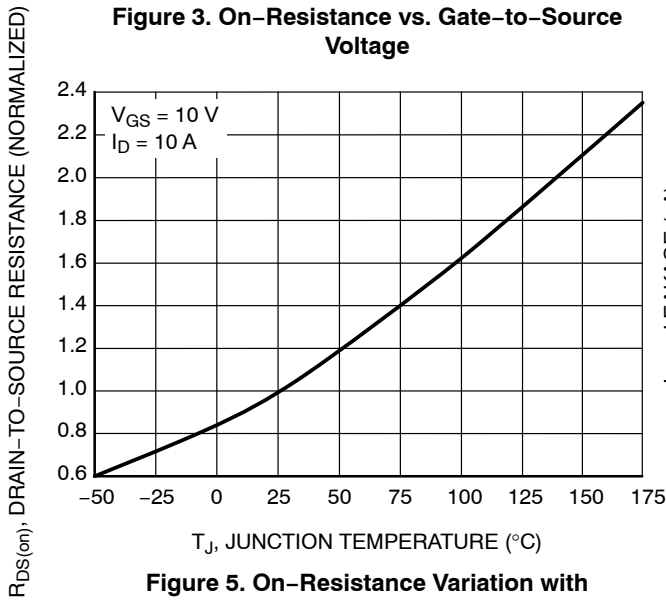


Figure 5. On-Resistance Variation with Temperature

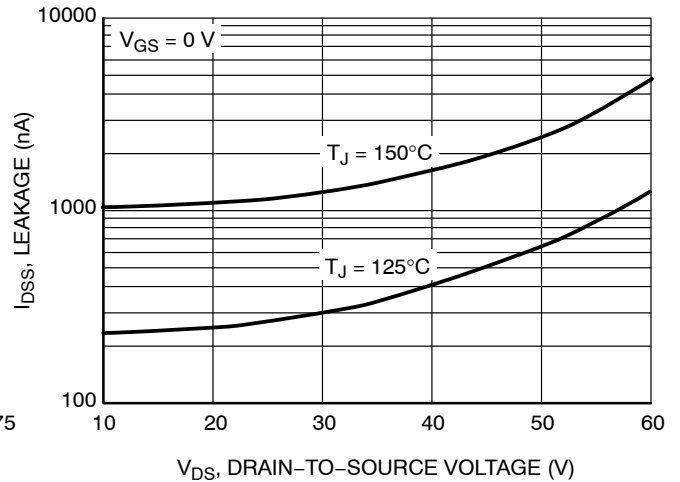


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

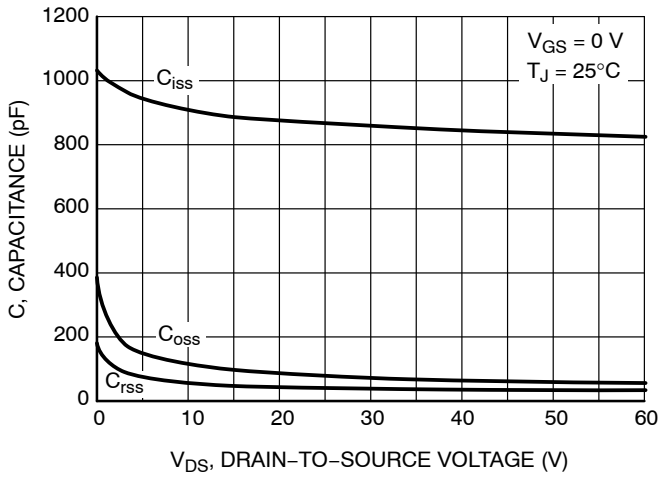


Figure 7. Capacitance Variation

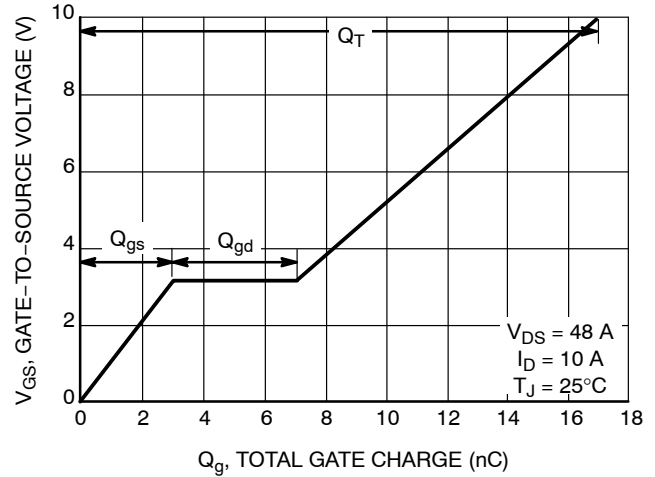


Figure 8. Gate-to-Source Voltage vs. Total Charge

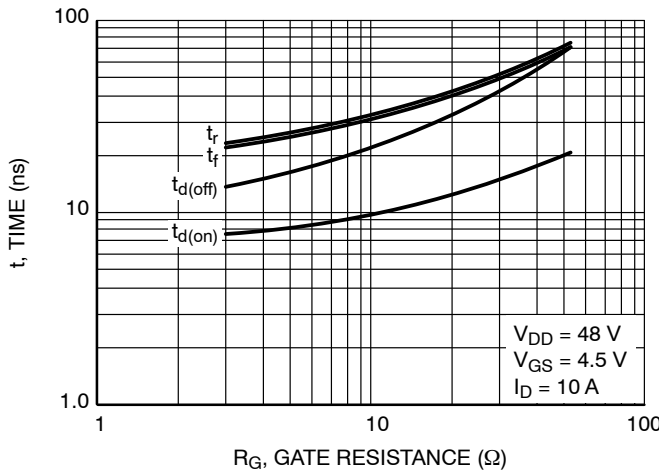


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

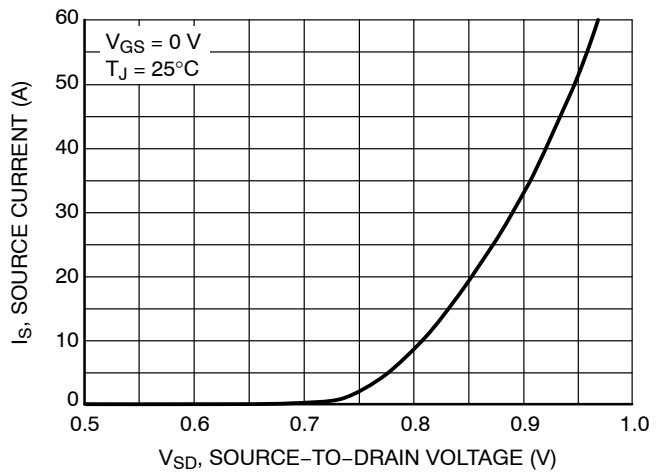


Figure 10. Diode Forward Voltage vs. Current

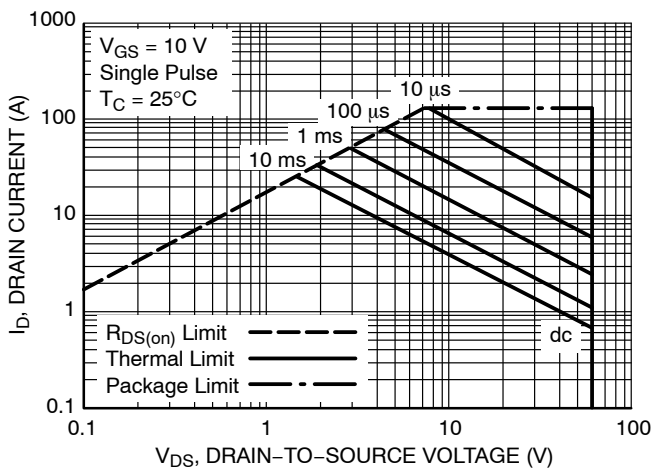


Figure 11. Maximum Rated Forward Biased Safe Operating Area

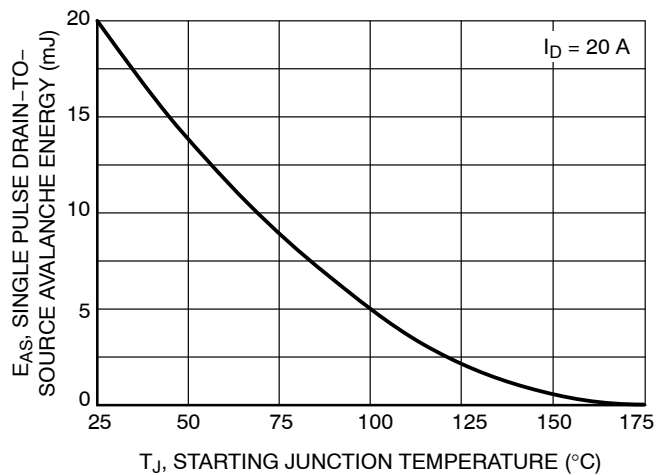


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

NVMFS5826NL

TYPICAL CHARACTERISTICS

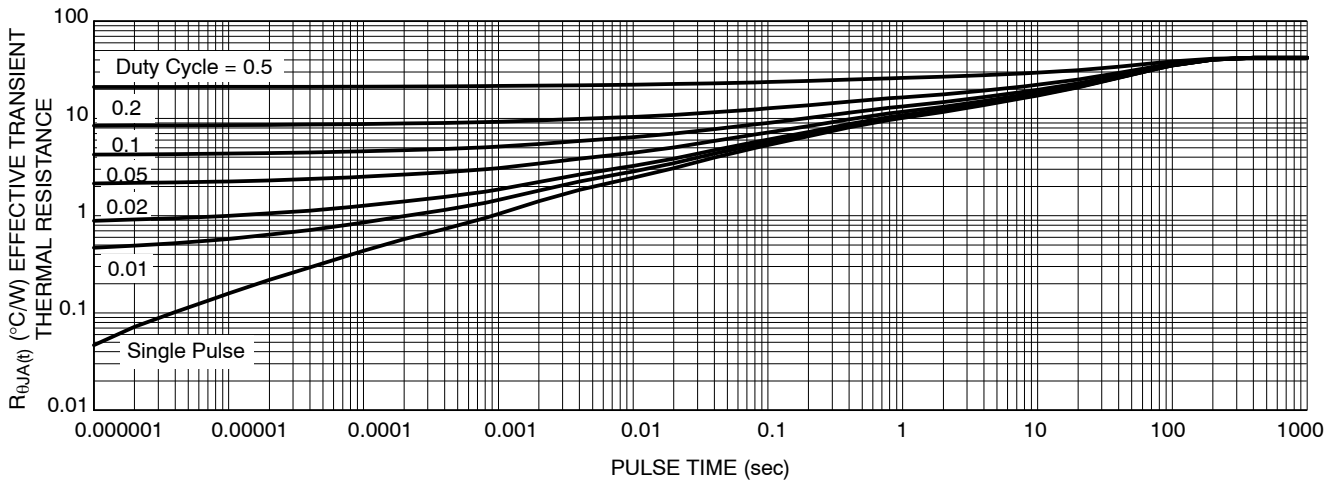


Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

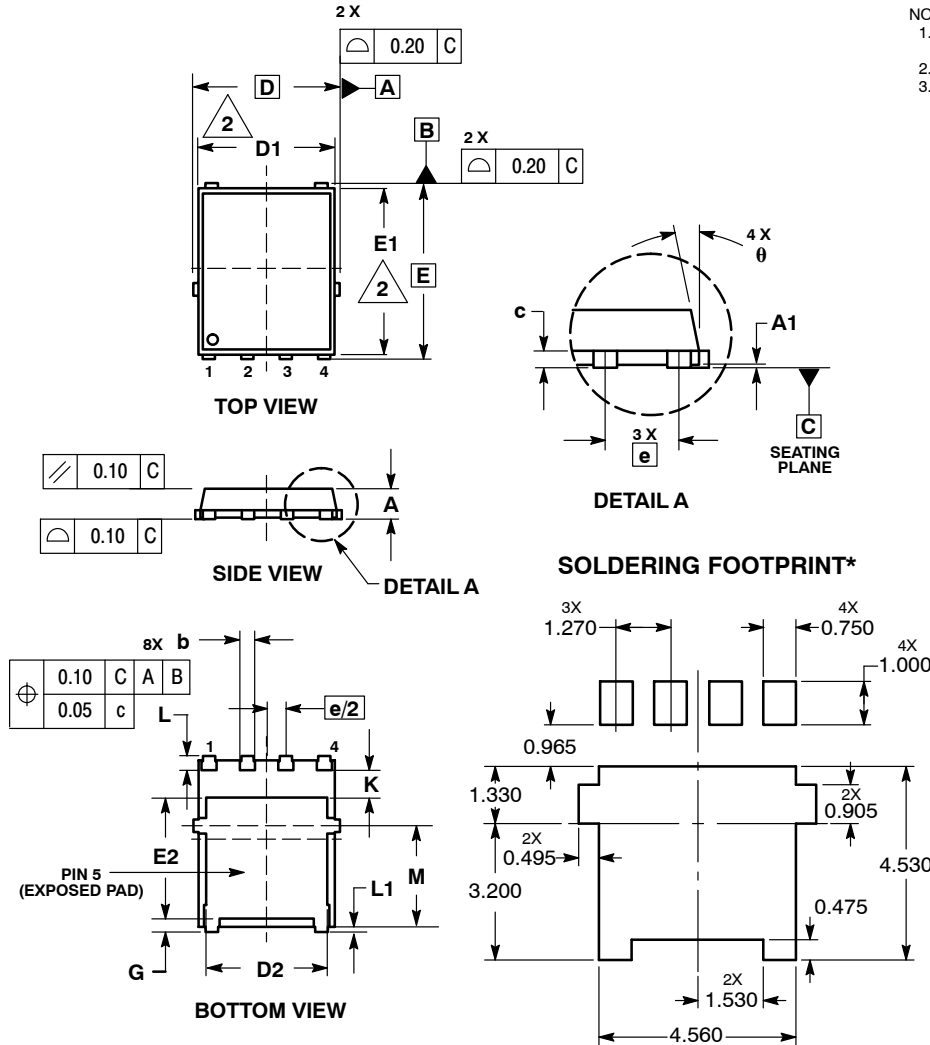
| Device | Marking | Package | Shipping† |
|------------------|---------|-------------------|--------------------|
| NVMFS5826NLT1G | V5826L | DFN5 (Pb-Free) | 1500 / Tape & Reel |
| NVMFS5826NLWFT1G | 5826LW | DFN5 (Pb-Free) | 1500 / Tape & Reel |
| NVMFS5826NLT3G | V5826L | DFN5 (Pb-Free) | 5000 / Tape & Reel |
| NVMFS5826NLWFT3G | 5826LW | DFN5 (Pb-Free) | 5000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NVMFS5826NL

PACKAGE DIMENSIONS

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE H



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.00 | --- | 0.05 |
| b | 0.33 | 0.41 | 0.51 |
| c | 0.23 | 0.28 | 0.33 |
| D | 5.15 BSC | | |
| D1 | 4.70 | 4.90 | 5.10 |
| D2 | 3.80 | 4.00 | 4.20 |
| E | 6.15 BSC | | |
| E1 | 5.70 | 5.90 | 6.10 |
| E2 | 3.45 | 3.65 | 3.85 |
| e | 1.27 BSC | | |
| G | 0.51 | 0.61 | 0.71 |
| K | 1.20 | 1.35 | 1.50 |
| L | 0.51 | 0.61 | 0.71 |
| L1 | 0.05 | 0.17 | 0.20 |
| M | 3.00 | 3.40 | 3.80 |
| θ | 0° | --- | 12° |

STYLE 1:

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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