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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

July 2013

FDMS3660AS

PowerTrench® Power Stage

Asymmetric Dual N-Channel MOSFET

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 8 mΩ at V_{GS} = 10 V, I_D = 13 A
- Max $r_{DS(on)}$ = 11 mΩ at V_{GS} = 4.5 V, I_D = 11 A

Q2: N-Channel

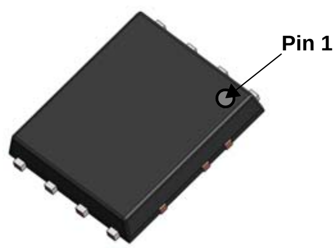
- Max $r_{DS(on)}$ = 1.8 mΩ at V_{GS} = 10 V, I_D = 30 A
- Max $r_{DS(on)}$ = 2.2 mΩ at V_{GS} = 4.5 V, I_D = 27 A
- Low inductance packaging shortens rise/fall times, resulting in lower switching losses
- MOSFET integration enables optimum layout for lower circuit inductance and reduced switch node ringing
- RoHS Compliant

General Description

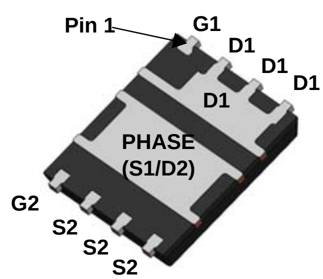
This device includes two specialized N-Channel MOSFETs in a dual PQFN package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET™ (Q2) have been designed to provide optimal power efficiency.

Applications

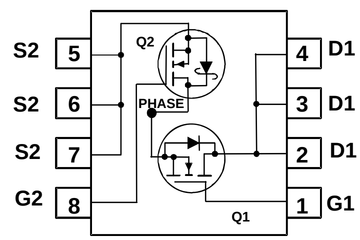
- Computing
- Communications
- General Purpose Point of Load
- Notebook VCORE



Top



Bottom



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DS}	Drain to Source Voltage		30	30	V
V_{GS}	Gate to Source Voltage	(Note 3)	±20	±12	V
I_D	Drain Current -Continuous	T_C = 25 °C	56	130	A
	-Continuous	T_A = 25 °C	13[1a]	30[1b]	
	-Pulsed	(Note 4)	70	140	
E_{AS}	Single Pulse Avalanche Energy		73[5]	150[6]	mJ
P_D	Power Dissipation for Single Operation	T_A = 25 °C	2.2[1a]	2.5[1b]	W
	Power Dissipation for Single Operation	T_A = 25 °C	1.0[1c]	1.0[1d]	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	57[1a]	50[1b]	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	125[1c]	120[1d]	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.5	2.2	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
27CF 32CD	FDMS3660AS	Power 56	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Off Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V I_D = 1 mA, V_{GS} = 0 V	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C I_D = 10 mA, referenced to 25 °C	Q1 Q2		16 29		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	Q1 Q2			1 500	μA μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = 20 V, V_{DS}= 0 V V_{GS} = 12 V, V_{DS}= 0 V	Q1 Q2			100 100	nA nA

On Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA V_{GS} = V_{DS}, I_D = 1 mA	Q1 Q2	1.1 1.2	2.0 1.5	2.7 2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C I_D = 10 mA, referenced to 25 °C	Q1 Q2		-6 -3		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10 V, I_D = 13 A V_{GS} = 4.5 V, I_D = 11 A V_{GS} = 10 V, I_D = 13 A , T_J = 125 °C	Q1		5.9 8.5 7.9	8 11 11	mΩ
		V_{GS} = 10 V, I_D = 30 A V_{GS} = 4.5 V, I_D = 27 A V_{GS} = 10 V, I_D = 30 A , T_J = 125 °C	Q2		1.2 1.5 1.8	1.8 2.2 2.7	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 13 A V_{DS} = 5 V, I_D = 30 A	Q1 Q2		173 240		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
C_{iss}	Input Capacitance	Q1: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ Q2: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2		1485 4150	2230 6225	pF
C_{oss}	Output Capacitance		Q1 Q2		397 1195	595 1795	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		37 117	70 245	pF
R_g	Gate Resistance		Q1 Q2	0.1 0.1	1.6 1.0	3.2 2.0	Ω

Switching Characteristics

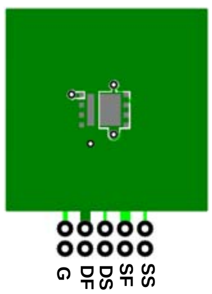
Symbol	Parameter	Test Conditions		Type	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	Q1: V_{DD} = 15 V, I_D = 13 A, R_{GEN} = 6 Ω Q2: V_{DD} = 15 V, I_D = 30 A, R_{GEN} = 6 Ω		Q1 Q2		9 12	17 22	ns
t_r	Rise Time			Q1 Q2		3 5	10 10	ns
$t_{d(off)}$	Turn-Off Delay Time			Q1 Q2		21 38	33 60	ns
t_f	Fall Time			Q1 Q2		3 5	10 10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V	Q1: V_{DD} = 15 V, I_D = 13 A Q2: V_{DD} = 15 V, I_D = 30 A	Q1 Q2		21 64	30 90	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V		Q1 Q2		10 30	13 43	nC
Q_{gs}	Gate to Source Gate Charge			Q1 Q2		4.5 9		nC
Q_{gd}	Gate to Drain “Miller” Charge			Q1 Q2		2.0 9		nC

Electrical Characteristics T_J = 25 °C unless otherwise noted

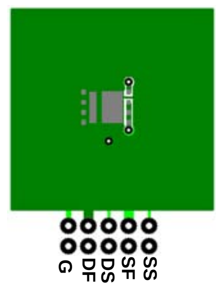
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 13 A (Note 2) V_{GS} = 0 V, I_S = 2 A (Note 2) V_{GS} = 0 V, I_S = 30 A (Note 2) V_{GS} = 0 V, I_S = 2 A (Note 2)	Q1 Q1 Q2 Q2		0.84 0.74 0.77 0.48	1.2 1.2 1.2 1.2	V
t_{rr}	Reverse Recovery Time	Q1: I_F = 13 A, di/dt = 100 A/μs	Q1 Q2		25 33	40 53	ns
Q_{rr}	Reverse Recovery Charge	Q2: I_F = 30 A, di/dt = 300 A/μs	Q1 Q2		9 41	18 66	nC

Notes:

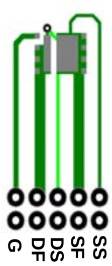
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 57 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 50 °C/W when mounted on a 1 in² pad of 2 oz copper



c. 125 °C/W when mounted on a minimum pad of 2 oz copper

d. 120 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. As an N-ch device, the negative Vgs rating is for low duty cycle pulse ocurrence only. No continuous rating is implied with the negative Vgs rating.
4. Pulsed Id limited by junction temperature, td<=100 μS, please refer to SOA curve for more details.
5. E_{AS} of 73 mJ is based on starting T_J = 25 °C; N-ch: L = 3 mH, I_{AS} = 7 A, V_{DD} = 30 V, V_{GS} = 10 V. 100% test at L= 0.1 mH, I_{AS} = 23 A.
6. E_{AS} of 150 mJ is based on starting T_J = 25 °C; N-ch: L = 3 mH, I_{AS} = 10 A, V_{DD} = 30 V, V_{GS} = 10 V. 100% test at L= 0.1 mH, I_{AS} = 31 A.

Typical Characteristics (Q1 N-Channel) T_J = 25 °C unless otherwise noted

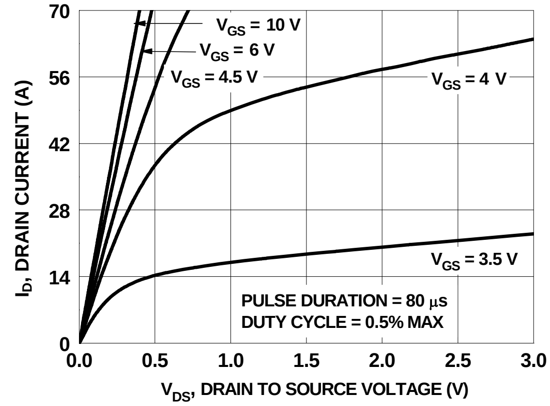


Figure 1. On Region Characteristics

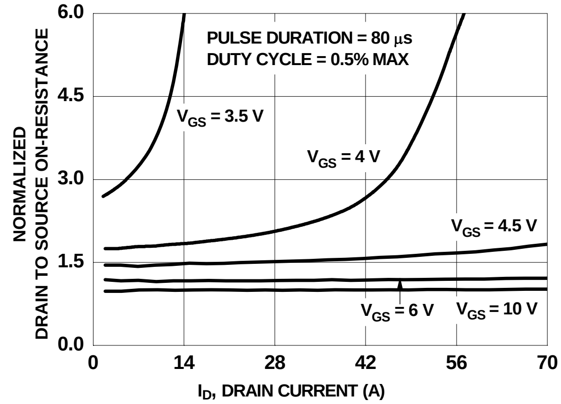


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

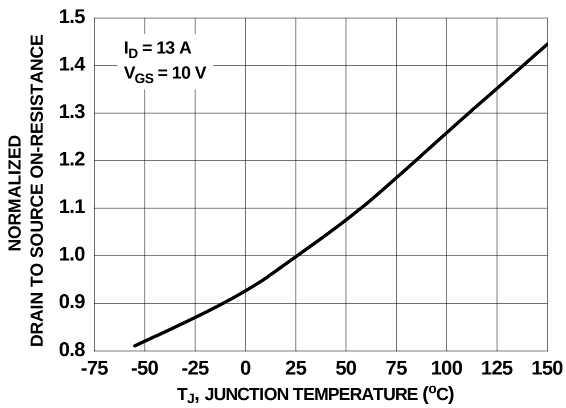


Figure 3. Normalized On Resistance vs Junction Temperature

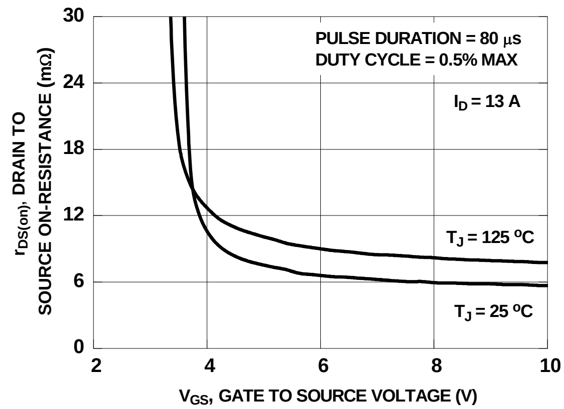


Figure 4. On-Resistance vs Gate to Source Voltage

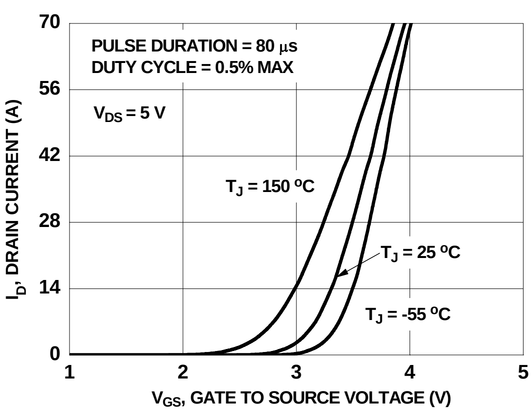


Figure 5. Transfer Characteristics

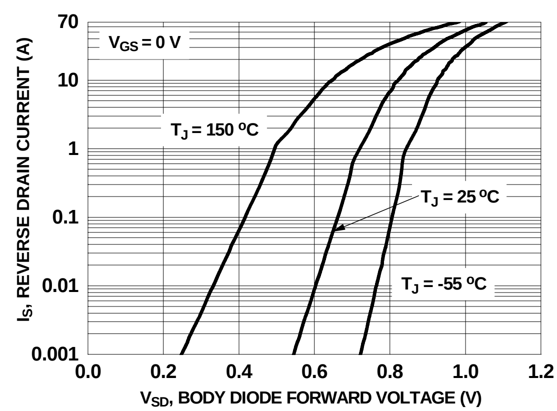


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) T_J = 25 °C unless otherwise noted

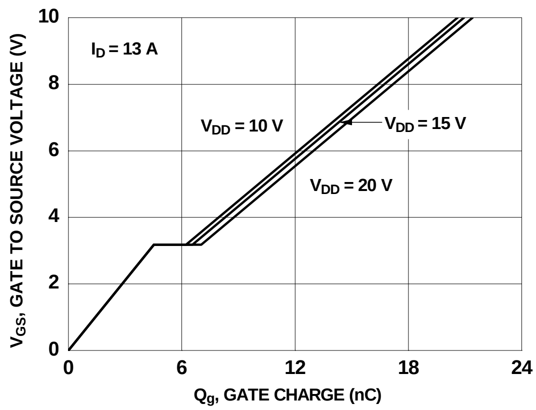


Figure 7. Gate Charge Characteristics

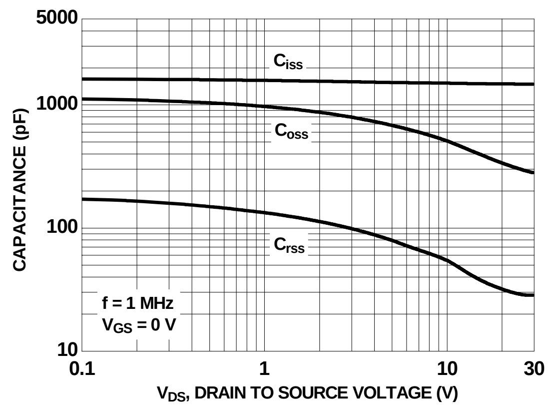


Figure 8. Capacitance vs Drain to Source Voltage

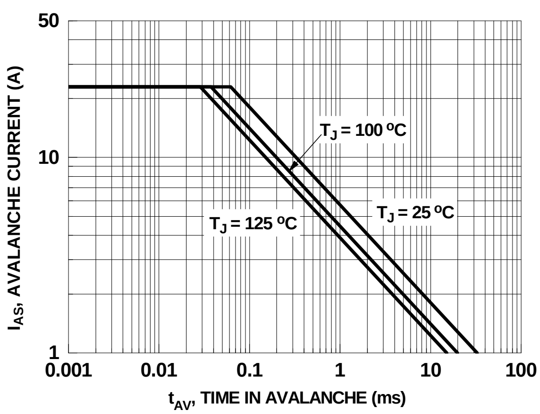


Figure 9. Unclamped Inductive Switching Capability

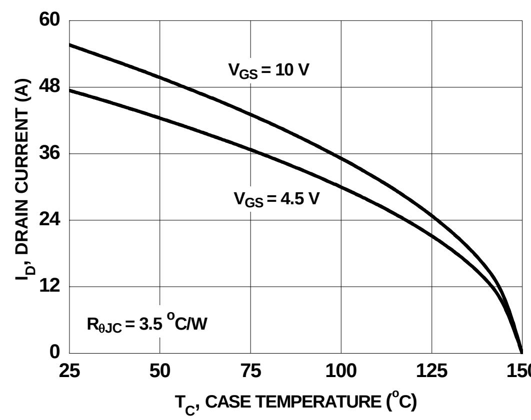


Figure 10. Maximum Continuous Drain Current vs Case Temperature

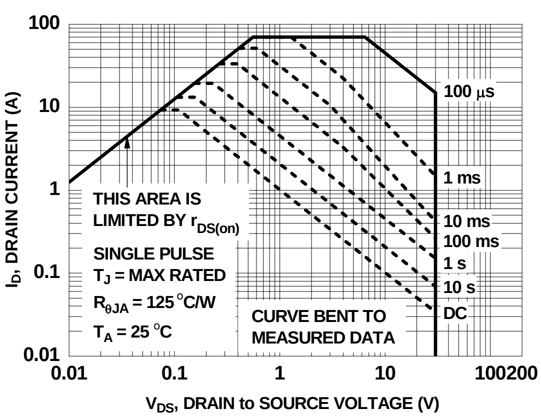


Figure 11. Forward Bias Safe Operating Area

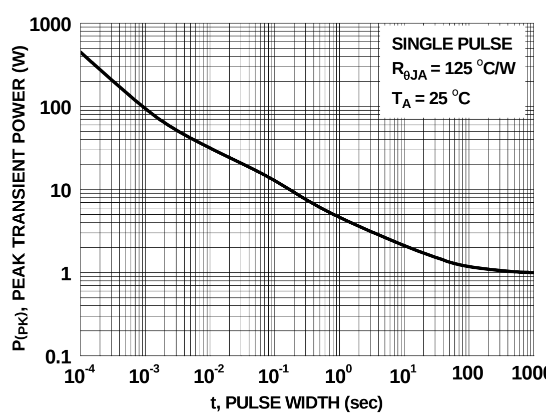


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) T_J = 25 °C unless otherwise noted

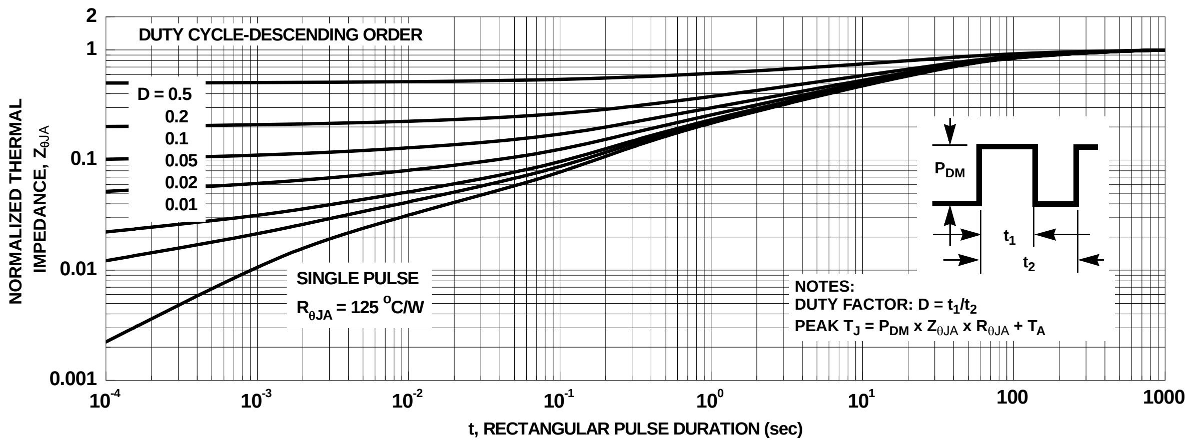


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unlenss otherwise noted

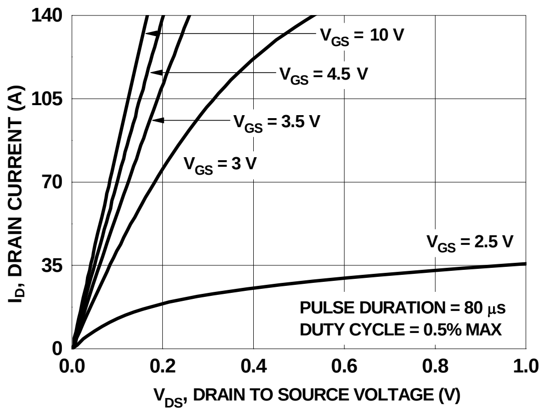


Figure 14. On-Region Characteristics

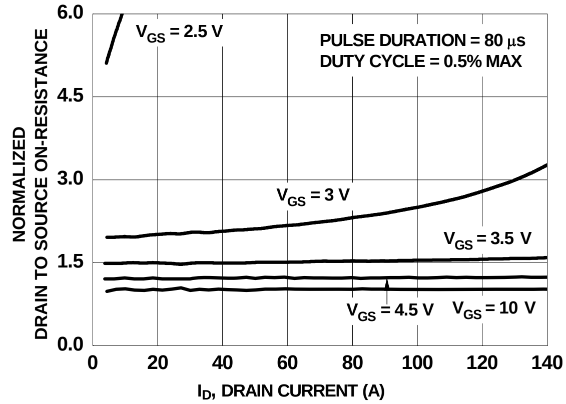


Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage

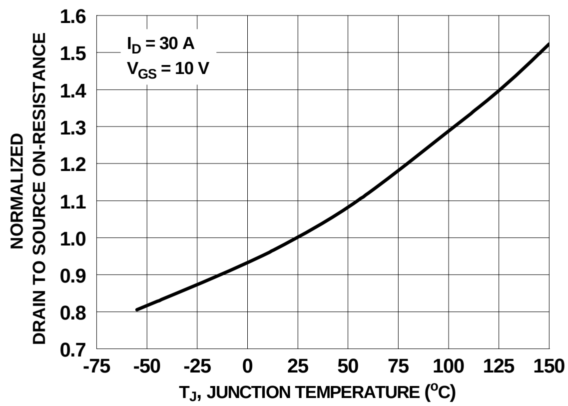


Figure 16. Normalized On-Resistance vs Junction Temperature

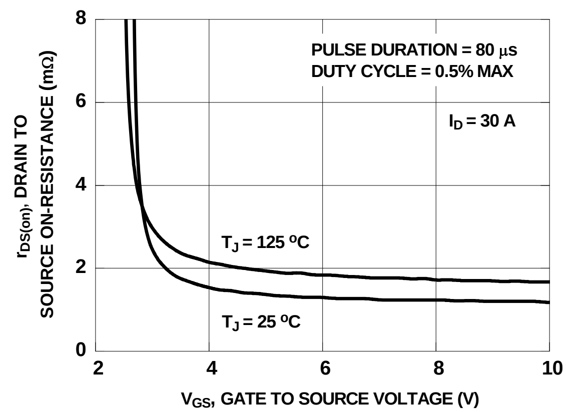


Figure 17. On-Resistance vs Gate to Source Voltage

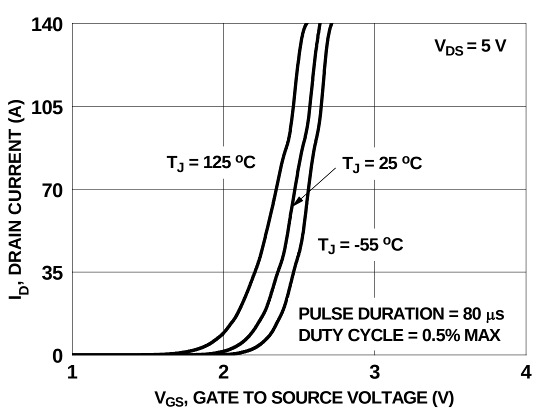


Figure 18. Transfer Characteristics

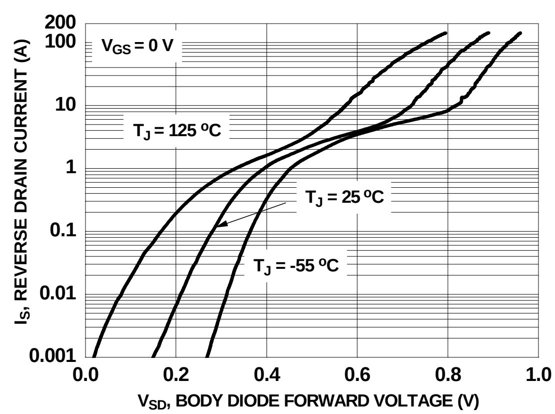


Figure 19. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted

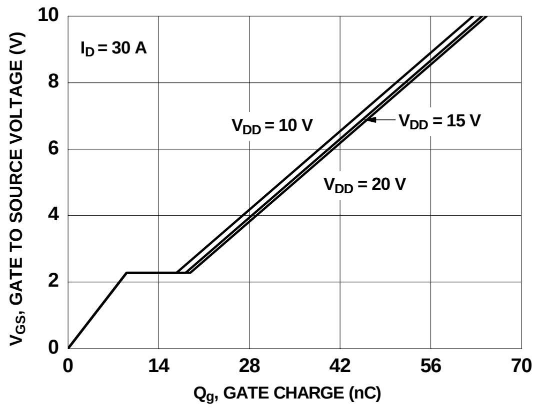


Figure 20. Gate Charge Characteristics

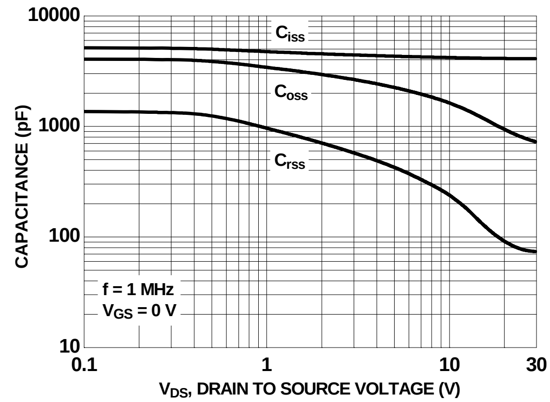


Figure 21. Capacitance vs Drain to Source Voltage

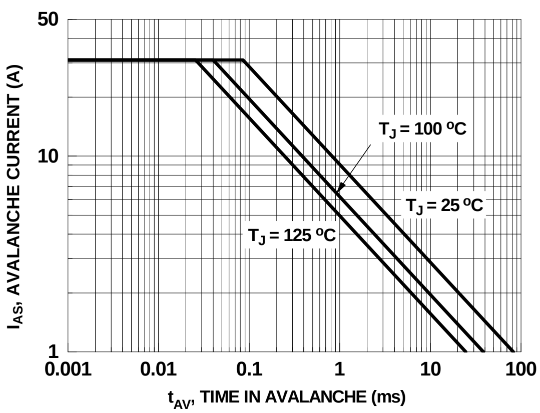


Figure 22. Unclamped Inductive Switching Capability

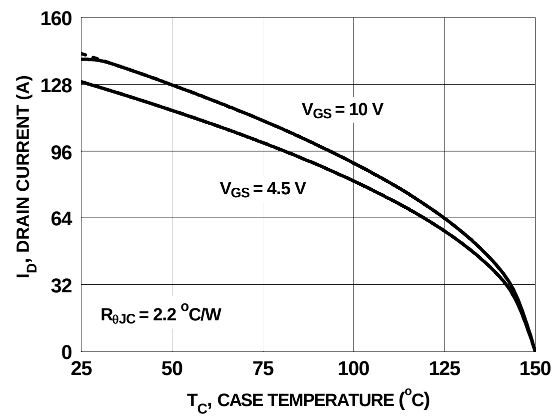


Figure 23. Maximun Continuous Drain Current vs Case Temperature

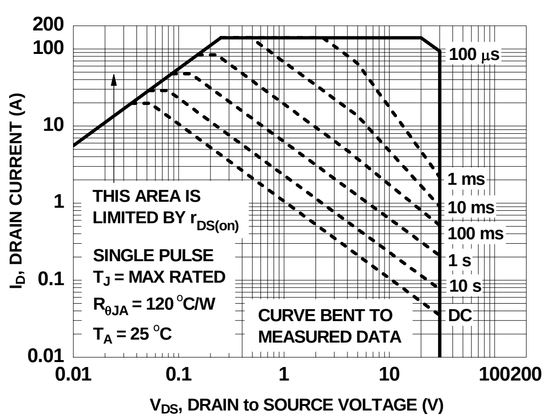


Figure 24. Forward Bias Safe Operating Area

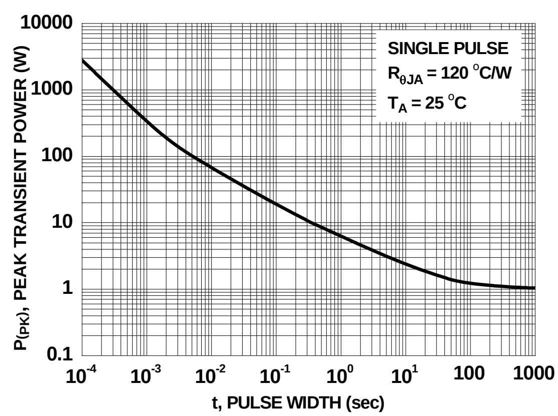


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted

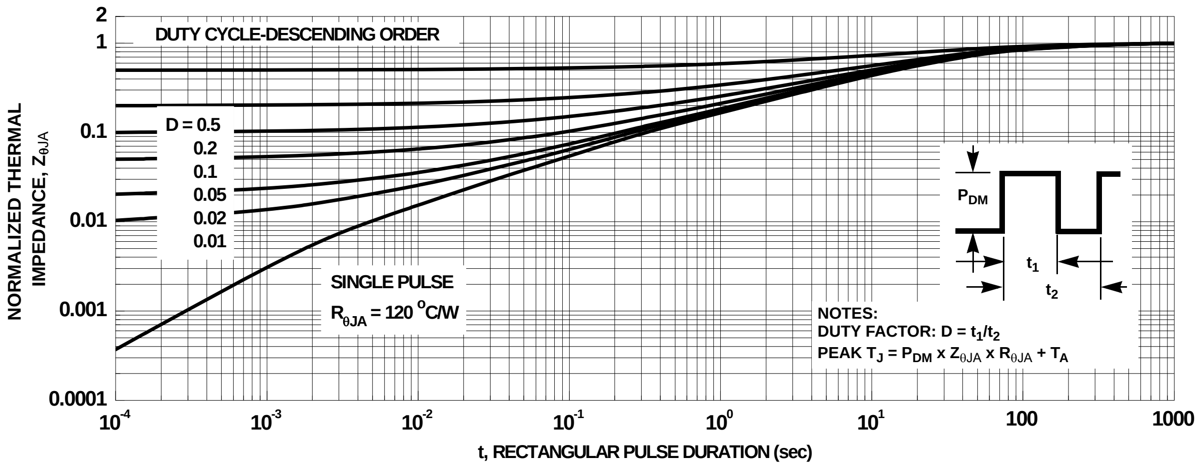


Figure 26. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET^{TM} Schottky body diode Characteristics

Fairchild's SyncFET^{TM} process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDMS3660AS.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

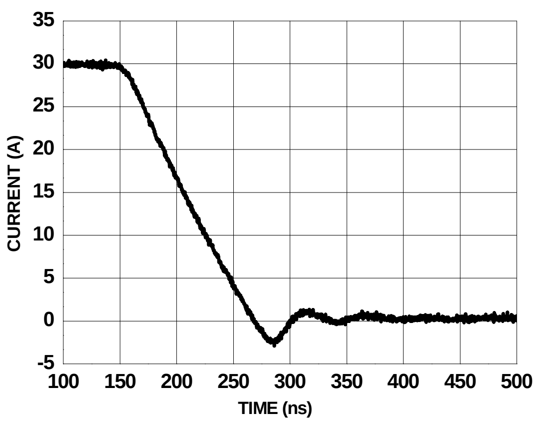


Figure 27. FDMS3660AS SyncFET^{TM} Body Diode Reverse Recovery Characteristic

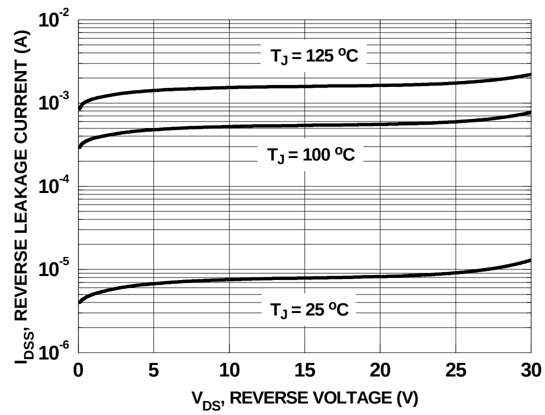
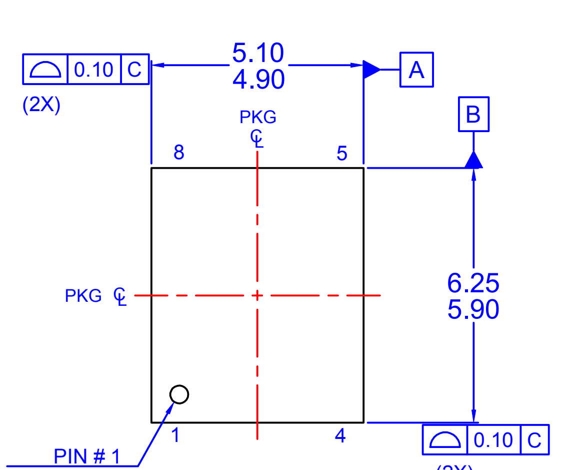
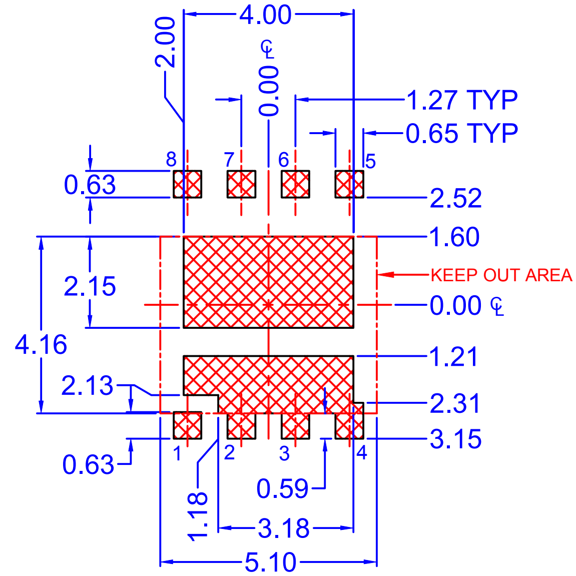


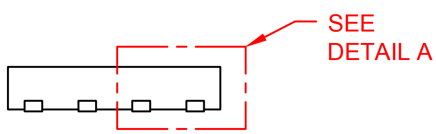
Figure 28. SyncFET^{TM} Body Diode Reverse Leakage Versus Drain-Source Voltage



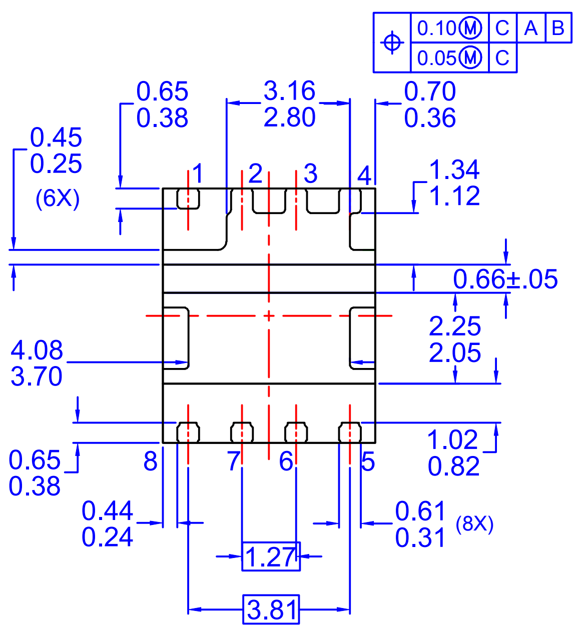
TOP VIEW



RECOMMENDED LAND PATTERN
FOR SAWN / PUNCHED TYPE

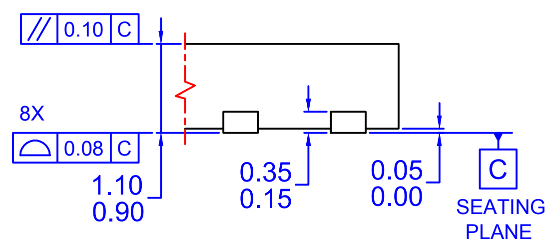


SIDE VIEW



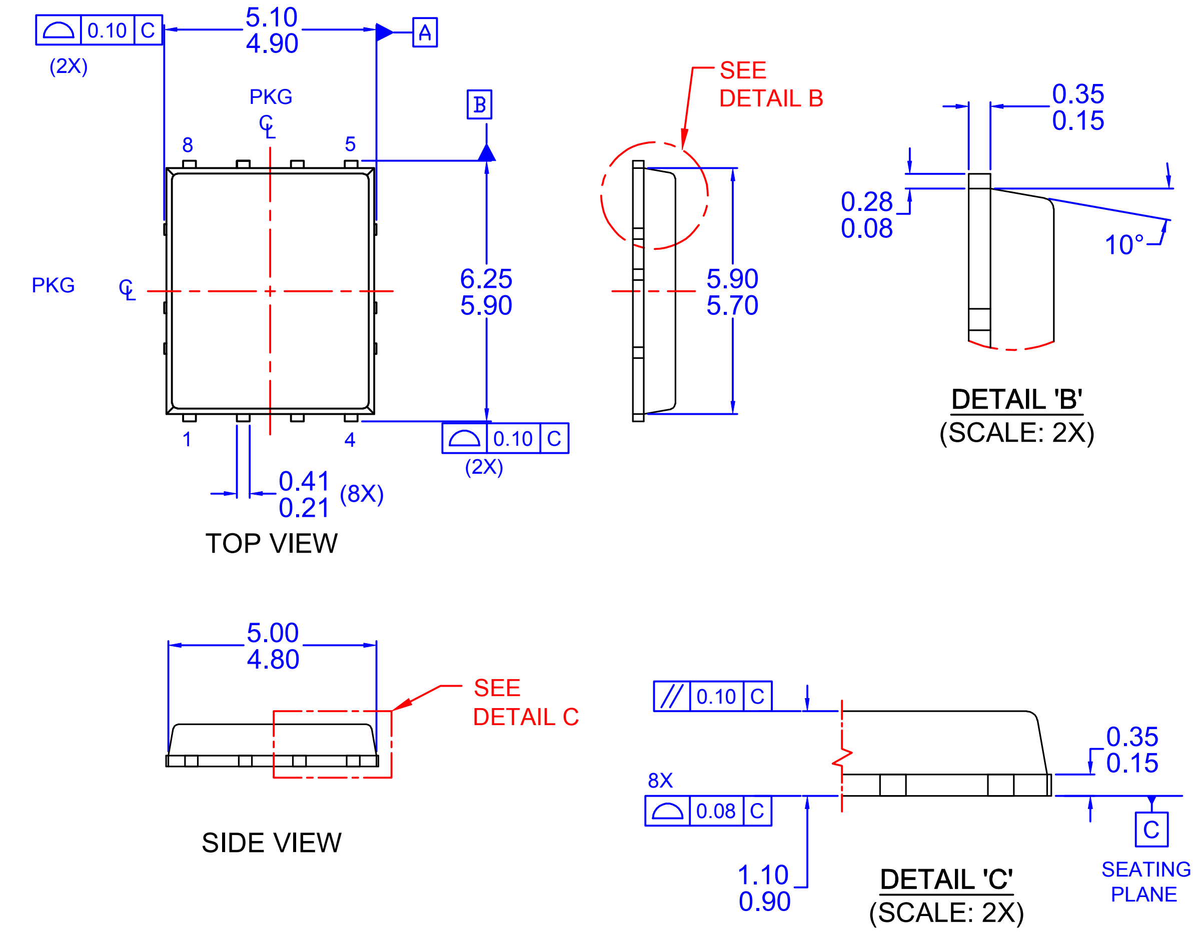
BOTTOM VIEW

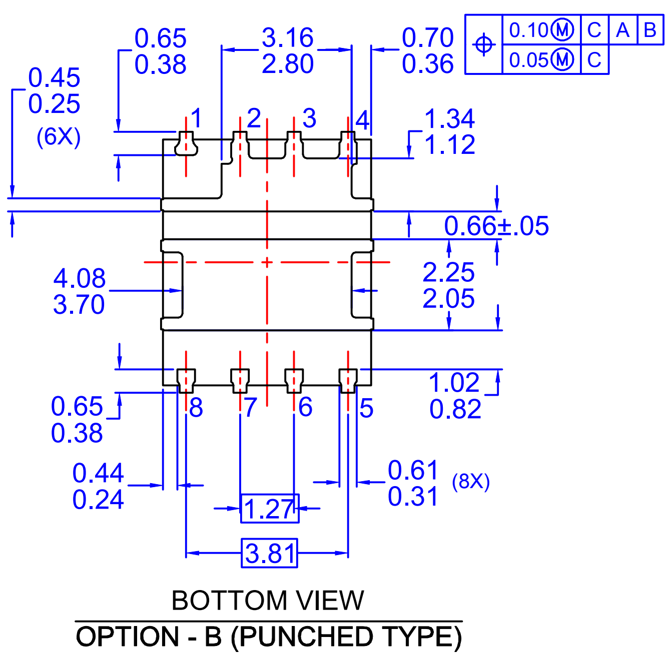
OPTION - A (SAWN TYPE)



DETAIL 'A'

(SCALE: 2X)





NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC REGISTRATION, MO-240, VARIATION AA.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

F) DRAWING FILE NAME: PQFN08EREV6.

G) FAIRCHILD SEMICONDUCTOR

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
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